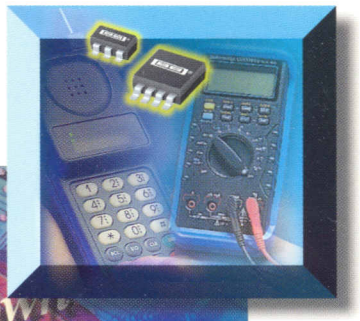
1998

# Burr-Brown IC Data Book

## Linear & Mixed Signal Products




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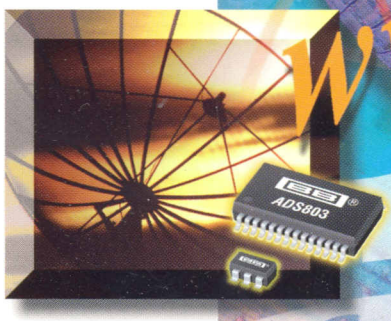
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# 1998
# Burr-Brown
# Integrated Circuits
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# Linear Products

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# 1 Burr-Brown Corporation



## About Burr-Brown

### Corporate Profile

Burr-Brown Corporation designs, manufactures, and markets a broad line of high-performance, standard analog and mixed signal integrated circuits used in the processing of electronic signals. Our products are used in a wide range of markets and applications, including industrial and process control, test and measurement, medical and scientific instrumentation, medical imaging, digital audio and video, communications, personal computers, and multimedia.

Our product strategy is to design proprietary circuits that yield maximum functional value in our customers' applications. Many of the products, although produced in standard configurations, are strategically designed, specified, and tested to position them for targeted applications such as audio signal processing or sensor-specific signal conditioning.

Burr-Brown's products include: operational amplifiers, instrumentation amplifiers, programmable gain amplifiers, isolation amplifiers, isolated DC/DC converters, voltage references and regulators, voltage-to-frequency converters, optoelectronic amplifiers, analog-to-digital converters, digital-to-analog converters, and "application specific" standard products. Our products are manufactured using a variety of wafer fabrication processes including bipolar, complementary bipolar, BiCMOS and CMOS with lithography requirements down to the 0.5 micron level.

We sell our products worldwide through our direct sales force, independent sales representatives, and third-party distributors. Burr-Brown has six direct sales offices in the United States and international sales subsidiaries in France, Germany, Italy, Japan, the Netherlands, Switzerland, and the United Kingdom. Through direct sales and distributors, our products reach over 30,000 OEM customers worldwide. Sales are divided evenly throughout the world, with approximately one-third from the United States market, one-third from Europe, and the remainder from Japan and the Southeast Asian region.

Burr-Brown employs over 1,900 people worldwide with manufacturing and technical facilities in Tucson, Arizona; Atsugi, Japan; and Livingston, Scotland. Located in Tucson, Arizona, corporate headquarters also includes an integrated circuit wafer fab, assembly and test operations. Burr-Brown was incorporated in Arizona in 1956; stock is traded on NASDAQ under the symbol, BBRC.

### Burr-Brown Receives ISO9001 Certification in U.S. and Europe

In September 1993, Burr-Brown Corporation received ISO9001 certification in the United States and Europe, simultaneously. In the United States, registration is recognized through the TUV Product Service Quality Registrar by the Registration Accreditation Board (RAB). Certification is accepted through the Electronics Industries Quality Registrar by the Dutch Registration Board (RCV) in Europe.

ISO9001 is the international standard for assessing the quality systems of companies that design, manufacture, and test products. Adopted by 91 member countries, it's the international quality standard for manufacturing, trade, and communications industries. Certification indicates that a formal quality system exists for all processes and that these processes are audited on a timely basis.



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# Sales and Service

## ABOUT THIS BOOK

With the publication of the *1998 IC Data Book*, Burr-Brown is taking a new path in the dissemination of product information. This book contains only abridged, 3-5 page versions of product data sheets; therefore, information on analog products can be found in the first half of the book, and mixed signal product information in the second half. The accompanying CD-ROM contains complete product data sheets, applications bulletins, selection guide, plus an updated interface and enhanced search capabilities. Complete product information is also available on our web site at: **http://www.burr-brown.com/**.

### How to Use This Book

Burr-Brown product numbers are listed in the Selection Trees and Tables at the beginning of each tabbed section. With these tools you can quickly compare specs among different products and choose the best part for your design.

Data sheets are arranged alphanumerically by product type, so if you know the name of the part you can find it quickly. Or, use the Product Index on the **inside front cover**.

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# Sales and Service

## Returns and Warranty Service

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# 2 Operational Amplifiers



The following selection guides include new products which combine exceptional performance with monolithic IC reliability and economy. Many of these products feature new package options for a maximum in design flexibility. The newest in package design, the SOT23, gives designers the same great Burr-Brown quality and precision in a size that economizes valuable board space.

The following highlights some of our newest developments:

**OPA130 Series**—Low-power FET-input op amps that combine precision dc performance with low quiescent current (530µA per amplifier). Available in single, dual, and quad configurations.

**OPA131 Series**—A family of single, dual and quad op amps that offer excellent overall performance for general purpose applications. Design features include 4MHz bandwidth and 10V/µs slew rate, yet quiescent current is only 1.5mA per amplifier.

**OPA132 Series**—High speed, precision, FET-input op amps that feature 8MHz GBW, and excellent dc performance at low cost. They are available in single, dual, and quad versions for maximum design flexibility.

**OPA134 Series**—Audio op amps provide high performance at low cost. Single, dual and quad versions available.

**OPA241 Series**—A new line of single supply micropower op amps that combine low offset voltage, high common-mode rejection, and wide supply range to provide excellent accuracy and versatility.

**OPA237 Series**—A family of Burr-Brown's ***MicroAmplifier***™ series of miniature products. In addition to small size, these devices feature low offset voltage, low quiescent current, low bias current, and a wide supply range.

**OPA277 Series**—A family of precision op amps which replace the industry standard OP177. They offer improved noise, wider output voltage swing, and are twice as fast with half the quiescent current.

**OPA336 Series**—A family of micropower CMOS operational amplifiers designed for battery powered applications. They operate on a single supply with operation as low as 2.1V. The output is rail-to-rail and swings to within 3mV of the supplies with a 100kΩ load.

**OPA2244**—A dual, single-supply micropower op amp with excellent speed/power performance (350kHz, 40µA).

**OPA2337**—A rail-to-rail output, dual CMOS operational amplifier designed for low cost and miniature applications. Packaged in the SOT23-8, the OPA2337EA is the world's smallest dual op-amp.

**OPA340 Series**—A family of rail-to-rail CMOS operational amplifiers optimized for low voltage, single supply operation. Rail-to-rail input/output and high speed operation make them ideal for driving sampling analog-to-digital converters.

**OPA642, OPA643 Series**—Unity gain and high gain stable, voltage feedback op amps with extremely low harmonic distortion. Both provide < –90dBc distortion at 5MHz 2Vp-p, Audio frequency distortion is < –125dBc. This exceptional linearity is complemented by very low input voltage and current noise. Now available in SOT23-5 packages.

**OPA655** is the industry's highest speed monolithic FET input op amp. Featuring unity gain stability and 220MHz Gain Bandwidth Product, this device also has the lowest input noise voltage at $6nV/\sqrt{Hz}$ for a high speed FET input op amp.

**OPA680, OPA681, OPA682 Series**—A family of wideband single channel op amps in voltage feedback, current feedback and fixed-gain versions, each includes an optional disable feature. All members of the family provide very high output power on low supply current (6mA trimmed). A new output stage architecture provides > 150mA drive current while requiring only 1V headroom to the power supply rails.

**OPA680 Series**—A very high slew rate, unity gain stable voltage feedback op amp. High output swing, Gain Bandwidth Product > 250MHz, and slew rate > 1500V/µs result in > 200MHz bandwidth for a 2Vp-p output on a single +5V supply. Future products include both dual and triple versions of the OPA680.

**OPA681 Series**—A low gain optimized, very wideband current feedback op amp providing even higher slew rate along with the gain bandwidth independence of current feedback. Bandwidth for a gain of +2 exceeds 250MHz with a slew rate > 2500V/µs. At a gain of +10, bandwidth exceeds 150MHz with the same slew rate. Future products include both dual and triple versions of the OPA681.

**OPA682 Series**—A wideband current feedback op amp with internal feedback and gain setting resistors. Precise gains of +1, +2, and –1 are easily achieved with no external gain setting resistors. Reduced feedback parasitics extend the bandwidth to > 300MHz at a gain of +2 with the same slew rate and output power as the OPA681. Future products include both dual and triple versions of the OPA682.

**OPA688 Series**—A wideband, unity gain stable, voltage feedback op amp with user-adjustable output limiting. An improved limiting architecture allows the limit voltages to be set within 100mV of the desired output swing with minimal impact on signal linearity. A very fast 1.7ns overdrive recovery provides nearly transparent overdrive protection for high speed digitizing channels.

**OPA689 Series**—A wideband, high gain stable, voltage feedback op amp with user-adjustable output limiting. As with the OPA688, reduced non-linearity near limiting yields a smaller required transition region between linear and voltage-limited operation. Unlike input limited designs, setting both the high and low limit levels directly at the output significantly improves performance for high gain operation.

# Operational Amplifiers

## OPERATIONAL AMPLIFIERS

### PRECISION

#### Low Drift ($V_{OS}$ Over Temp, max)

OPA177 (0.3µV/°C)
OPA627 (0.8µV/°C)
OPA637 (0.8µV/°C)
OPA111 (1µV/°C)
**OPA277 (1µV/°C)**
**OPA2277 (1µV/°C, Dual)**
**OPA4277 (1µV/°C, Quad)**
**OPA336 (1.5µV/°C, Dual)**
**OPA2336 (1.5µV/°C, Dual)**
**OPA4336 (1.5µV/°C, Quad)**
OPA27 (1.8µV/°C)
OPA37 (1.8µV/°C)
OPA602 (2µV/°C)
OPA1013 (2.5µV/°C, Dual)
OPA2111 (2.8µV/°C, Dual)
OPA234 (3µV/°C)
OPA2234 (3µV/°C, Dual)
OPA4234 (3µV/°C, Quad)
OPA124 (4µV/°C)

#### Low Bias Current $I_B$ (max)

OPA128 (75fA)
OPA129 (100fA)
OPA111 (1pA)
OPA602 (1pA)
OPA124 (2pA)
OPA2111 (4pA, Dual)
OPA404 (4pA, Quad)
OPA121 (5pA)
OPA627 (5pA)
OPA637 (5pA)
OPA2107 (5pA, Dual)
OPA606 (10pA)
**OPA336 (10pA)**
**OPA2336 (10pA, Dual)**
**OPA4336 (10pA, Quad)**
**OPA340 (10pA)**
**OPA2340 (10pA, Dual)**
**OPA4340 (10pA, Quad)**
OPA130 (20pA)
OPA2130 (20pA, Dual)
OPA4130 (20pA, Quad)
OPA131 (50pA)
OPA654 (50pA)
OPA671 (50pA)
OPA2131 (50pA, Dual)
OPA4131 (50pA, Quad)
OPA132 (50pA)
OPA2132 (50pA, Dual)
OPA4132 (50pA, Quad)
OPA655 (100pA)
**OPA134 (100pA)**
**OPA2134 (100pA, Dual)**
**OPA4134 (100pA, Quad)**

#### Low Noise (Voltage Noise at 10kHz, max)

**BIPOLAR INPUT**
OPA27 (4.5nV/√Hz)
OPA37 (4.5nV/√Hz)

**FET INPUT**
OPA627 (6nV/√Hz)
OPA637 (6nV/√Hz)
OPA655 (6nV/√Hz)
**OPA134 (8nV/√Hz)**
**OPA2134 (8nV/√Hz, Dual)**
OPA132 (8nV/√Hz)
OPA2132 (8nV/√Hz, Dual)
OPA4132 (8nV/√Hz, Quad)
OPA124 (8nV/√Hz)
OPA2111 (8nV/√Hz, Dual)
OPA111 (8nV/√Hz)
OPA2107 (8nV/√Hz, Dual)

VLA™ is a Voltage Limiting Amplifier.

### Single Supply ($V_S$, min)

**OPA2244 (2.2V, Dual)**
**OPA336 (2.3V)**
**OPA2336 (2.3V, Dual)**
**OPA4336 (2.3V, Quad)**
**OPA2337 (2.7V, Dual)**
**OPA241 (2.7V)**
**OPA251 (2.7V)**
**OPA340 (2.7V)**
**OPA2340 (2.7V, Dual)**
**OPA4340 (2.7V, Quad)**
**OPA237 (2.7V)**
**OPA2237 (2.7V, Dual)**
**OPA4237 (2.7V, Quad)**
OPA234 (2.7V)
OPA2234 (2.7V, Dual)
OPA4234 (2.7V, Quad)
OPA1013 (4V, Dual)

### GENERAL PURPOSE

OPA27 (Single)
OPA37 (Single)
OPA131 (Single)
OPA177 (Single)
OPA277 (Single)
OPA2277 (Dual)
OPA4277 (Quad)
OPA604 (Single)
OPA2131 (Dual)
OPA2604 (Dual)
OPA4131 (Quad)

### HIGH SPEED

#### Current Feedback

OPA603 ($V_S$ = ±15V
OPA644 (SR = 2500V/µs)
OPA658 (SR = 1700V/µs)
OPA2658 (Dual OPA658)
OPA4658 (Quad OPA658)
**OPA681 (SR = 2100V/µs)**
**OPA2681 (Dual OPA681)**

#### Voltage Feedback Unity Gain Stable

OPA620 (BW = 300MHz)
OPA640 (BW = 1.3GHz)
**OPA642 (92dB SFDR)**
OPA646 (BW = 650MHz)
OPA650 (BW = 560MHz)
OPA2650 (Dual OPA650)
OPA4650 Quad OPA650)
OPA655 FET Input, BW = 400MHz)
OPA671 (FET Input, $V_S$ = ±15V)
**OPA680 ($V_S$ = ±5V or +5V)**
**OPA2680 (Dual OPA680)**
**OPA688 (VLA™)**

#### Current Feedback Stable for G +2

OPA621 (BW = 500MHz, G +2)
**OPA643 (90dB SFDR, G +5)**
OPA651 (BW = 470MHz, G +2)
**OPA686 ($e_{ni}$ = 1.3nV/√Hz, G +7)**
**OPA689 (VLA™, G +4)**

### SPECIAL PURPOSE

**OPA134 (Audio)**
**OPA2134 (Audio, Dual)**
**OPA4134 (Audio, Quad)**
OPA660 (Transconductance)
OPA2662 (Transconductance, Dual)
OPA678 (Switched Input, G = +1 Stable)
VCA610 (Voltage Controlled Gain)

### MULTI-CHANNEL (refer to tables for details)

**DUAL**
OPA1013 (Precision, Low Drift, Single Supply)
OPA2107 (Precision, Low Bias Current)
OPA2111 (Precision, Low Noise)
OPA2130 (Precision, Low Bias Current)
OPA2131 (Precision, Low Bias Current)
OPA2132 (Single Supply)
**OPA2134 (Audio)**
OPA2234 (Single Supply)
**OPA2237 (Single Supply)**
**OPA2244 (Single Supply, Dual)**
**OPA2277 (Precision, Dual)**
**OPA2336 (MicroPower)**
***OPA2340 (Rail-Rail)***
OPA2541 (Power, High Current)
OPA2544 (Power, High Current)
OPA2604 (Precision, Low Bias Current)
OPA2650 (High Speed, VFB)
OPA2658 (High Speed, CFB)
OPA2662 (Transconductance)

**QUAD**
OPA404 (Precision, Low Bias Current)
OPA4130 (Precision, Low Bias Current)
OPA4131 (Precision, Low Bias Current)
OPA4132 (Precision, Low Bias Current)
**OPA4277 (Precision)**
OPA4234 **(Single Supply)**
**OPA4237 (Single Supply)**
**OPA4134 (Audio)**
**OPA4336 (MicroPower)**
***OPA4340 (Rail-Rail)***
OPA4650 (High Speed, VFB)
OPA4658 (High Speed, CFB)

**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

*For Immediate Assistance, Contact Your Local Salesperson*

| Product | Offset Voltage Drift max (±µV/°C) | Bias Current 25°C max (pA) | Noise Voltage at 10kHz max (nV/√Hz) | Offset Voltage 25°C max (±mV) | Open Loop Gain min (dB) | Rated Voltage Output[2] min (±V) | Rated Current Output min (±mA) | Description |
|---|---|---|---|---|---|---|---|---|
| AD515 | 15 | ±75fA | — | 1 | 88 | 10 | 10 | FET, Still Available |
| OPA27 | 1.8 | ±150nA | 4.5 | 0.10 | 100 | 12 | 16.7 | Bipolar |
| OPA37 | 1.8 | ±150nA | 4.5 | 0.10 | 100 | 12 | 16.7 | Bipolar |
| OPA103 | 2 | ±1 | 25* | 0.25 | 100 | 10 | 5 | FET, Still Available |
| OPA104 | 10 | ±75fA | 35* | 0.5 | 100 | 10 | 5 | FET, Still Available |
| OPA111 | 1 | ±1 | 8 | 0.25 | 120 | 11 | 5.5 | FET |
| OPA121 | 10 | ±5 | 6* | 2 | 110 | 11 | 5.5 | Low Cost |
| OPA124 | 4 | ±2 | 6* | 0.50 | 106 | 11 | 5.5 | FET |
| OPA128 | 5 | ±75fA | 15* | 0.5 | 110 | 10 | 5 | FET, Ultra-Low, Bias Current |
| OPA129 | 10 | ±100fA | 15* | 2 | 94 | 10 | 6 | FET, Ultra-Low, Bias Current |
| OPA130 | 10 | ±20 | 16 | 1 | 120 | 12 | 18* | FET, Low Power |
| OPA131 | 10 | ±50 | 15* | 1 | 94 | 12 | 25* | FET |
| OPA132 | 10 | 50 | 8 | 0.5 | 110 | 13.8 | 40* | FET, High Speed |
| **OPA134** | **2** | **100** | **8** | **2** | **104** | **13.8** | **40*** | **FET, Audio** |
| OPA177 | 0.1 | 1.5nA | 10* | 0.025 | 134 | 12 | 12 | Bipolar |
| OPA234 | 3 | –20nA | 25[1] | 0.1 | 110 | +14/–14.5 | 22* | Single Supply Amp |
| **OPA277** | **1** | **±2.8nA** | **8*** | **0.05** | **126** | **13.8** | **35*** | **Bipolar** |
| **OPA336** | **1.5*** | **10** | **40** | **0.125** | **100** | **5** | **1*** | **MicroPower, $I_Q$ = 20µA** |
| **OPA340** | **5** | **50** | **25** | **1** | **90** | **5** | **50*** | **Rail-Rail Input and Output** |
| OPA404 | 3* | ±4 | 12* | 0.75 | 92 | 11.5 | 5 | FET, Quad |
| OPA602 | 2 | ±1 | 12* | 0.25 | 92 | 11.5 | 15 | Wideband, (5MHz, min) |
| OPA606 | 5 | ±10 | 13 | 0.5 | 100 | 12 | 5 | Wideband, (9MHz, min) |
| OPA627 | 0.8 | ±5 | 6 | 0.1 | 112 | 11.5 | 45* | FET |
| OPA637 | 0.8 | ±5 | 6 | 0.1 | 112 | 11.5 | 45* | FET |
| OPA654 | 40* | ±50 | 14* | 3 | 94* | 11 | 200* | Wideband, (750V/µs, slew rate) |
| OPA655 | 10 | 100 | 6* | 2 | 53 | 2.5[3] | 25 | FET |
| OPA671 | 10* | ±50 | 12* | 5.0 | 74 | 10.5 | 50 | FET |
| OPA1013 | 2.5 | 30nA | — | 0.3 | 120 | 12 | 6.5 | Low Power, Dual Single Supply Operation |
| OPA2111 | 2.8 | ±3 | 8 | 0.5 | 114 | 10 | 5 | FET, Dual |
| OPA2107 | 10 | ±10 | 8* | 1 | 82 | 11 | 5.5 | FET, Dual |

* DENOTES TYPICAL
**BOLD DENOTES NEW PRODUCT**
***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

## PRECISION (CONT)

| Product | Offset Voltage Drift max (±µV/°C) | Bias Current 25°C max (pA) | Noise Voltage at 10kHz max (nV/√Hz) | Offset Voltage 25°C max (±mV) | Open Loop Gain min (dB) | Rated Voltage Output(2) min (±V) | Rated Current Output min (±mA) | Description |
|---|---|---|---|---|---|---|---|---|
| OPA2130 | 10 | ±20 | 16 | 1 | 120 | 12 | 18* | FET, Low Power, Dual |
| OPA2131 | 10 | ±50 | 15* | 1 | 94 | 12 | 25* | FET, Dual |
| OPA2132 | 10 | 50 | 8 | 0.5 | 110 | 13.8 | 40* | FET, High Speed, Dual |
| **OPA2134** | **2** | **100** | **8** | **2** | **104** | **13.8** | **40*** | **FET, Audio, Dual** |
| OPA2234 | 3 | –20nA | 25(1) | 0.1 | 110 | +14/–14.5 | 22* | Single Supply Amp, Dual |
| **OPA2277** | **1** | **±2.8nA** | **8*** | **0.05** | **126** | **13.8** | **35*** | **Bipolar, Dual** |
| **OPA2336** | **1.5*** | **10** | **40** | **0.125** | **100** | **5** | **1*** | **MicroPower, $I_Q$ = 20µA** |
| **OPA2340** | **5** | **50** | **25** | **1** | **90** | **5** | **50*** | **Rail-Rail Input and Output** |
| OPA4130 | 10 | ±20 | 16 | 1 | 120 | 12 | 18 | FET, Low Power, Quad |
| OPA4131 | 10 | ±50 | 15* | 1 | 94 | 12 | 25* | FET, Quad |
| OPA4132 | 10 | 50 | 8 | 0.5 | 110 | 13.8 | 40* | FET, High Speed, Quad |
| **OPA4134** | **2** | **100** | **8** | **2** | **104** | **13.8** | **40*** | **FET, Audio, Quad** |
| OPA4234 | 3 | –20nA | 25(1) | 0.1 | 110 | +14/–14.5 | 22* | Single Supply Amp, Quad |
| **OPA4277** | **1** | **±2.8nA** | **8*** | **0.05** | **126** | **13.8** | **35*** | **Bipolar, Quad** |
| **OPA4336** | **1.5*** | **10** | **40** | **0.5** | **100** | **5** | **1*** | **MicroPower, $I_Q$ = 20µA** |
| **OPA4340** | **5** | **50** | **25** | **1** | **90** | **5** | **50*** | **Rail-Rail Input and Output** |

NOTE: (1) Typical Noise Voltage at 1kHz (nV/√Hz). (2) For ±15V supplies. (3) For ±5V supplies.

## SINGLE SUPPLY

| Product | Single Supply Range min to max (V) | Quiescent Current max (mA, per amp) | Bias Current 25°C max (nA) | Small Signal Unity Gain typ (kHz) | Offset Voltage 25°C max (±µV) | Temp Range(1) | Pkg | Description |
|---|---|---|---|---|---|---|---|---|
| OPA234 | 2.7 to 36 | 0.3 | –20 | 350 | 100 | XInd | DIP, SO-8, MSOP-8 | Single, Bipolar |
| **OPA237** | **2.7 to 36** | **0.35** | **±40** | **1.5MHz** | **250** | **XInd** | **SOT-23-5, SO-8** | **Single, Bipolar** |
| **OPA241** | **2.7 to 36** | **0.34** | **–20** | **35** | **250** | **XInd** | **DIP, SO-8** | **Single, Bipolar** |
| **OPA251** | **2.7 to 36** | **0.34** | **–20** | **35** | **250** | **XInd** | **DIP, SO-8** | **Single, Bipolar** |
| **OPA336** | **2.3 to 5.5** | **0.032** | **10p** | **100** | **125** | **XInd** | **SOT-23-5, DIP, SO-8** | **Single, CMOS** |
| **OPA340** | **2.7 to 5** | **0.8** | **50p** | **5MHz** | **1mV** | **XInd** | **SOT-23-5, DIP, SO-8** | **Single, CMOS** |
| OPA1013 | 4 to 36 | 0.55 | –30 | 750 | 300 | Com/Ind | DIP | Dual, Bipolar |
| OPA2234 | 2.7 to 36 | 0.3 | –20 | 350 | 100 | XInd | DIP, SO-8 | Dual, Bipolar |

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Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

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## SINGLE SUPPLY (CONT)

| Product | Single Supply Range min to max (V) | Quiescent Current max (mA, per amp) | Bias Current 25°C max (nA) | Small Signal Unity Gain typ (kHz) | Offset Voltage 25°C max (±µV) | Temp Range[1] | Pkg | Description |
|---|---|---|---|---|---|---|---|---|
| **OPA2244** | **2.2 to 36** | **0.05** | **–25** | **350** | **1.5mV** | **XInd** | **DIP, SO-8, MSOP** | **Dual, Bipolar** |
| **OPA2237** | **2.7 to 36** | **0.35** | **±40** | **1.5MHz** | **250** | **XInd** | **MSOP-8, SO-8** | **Dual, Bipolar** |
| **OPA2336** | **2.3 to 5.5** | **0.032** | **10p** | **100** | **125** | **XInd** | **MSOP-8, DIP, SO-8** | **Dual, CMOS** |
| **OPA2337** | **2.7 to 5.5** | **0.525** | **10p** | **3MHz** | **3mV** | **XInd** | **DIP, SO-8, SOT-23-8** | **Dual, CMOS** |
| **OPA2340** | **2.7 to 5** | **0.8** | **50p** | **5MHz** | **1mV** | **XInd** | **MSOP-8, DIP, SO-8** | **Dual, CMOS** |
| OPA4234 | 2.7 to 36 | 0.3 | –20 | 350 | 100 | XInd | DIP, SO-14 | Quad, Bipolar |
| **OPA4237** | **2.7 to 36** | **0.35** | **±40** | **1.5MHz** | **250** | **XInd** | **SSOP-16** | **Quad, Bipolar** |
| **OPA4336** | **2.3 to 5.5** | **0.032** | **10p** | **100** | **125** | **XInd** | **SSOP-16, DIP** | **Quad, CMOS** |
| **OPA4340** | **2.7 to 5** | **0.8** | **50p** | **5MHz** | **1mV** | **XInd** | **SSOP-16, DIP** | **Quad, CMOS** |

NOTE: (1) Com = 0°C to 70°C, Ind = –25°C to 85°C, XInd = –40°C to 85°C.

## GENERAL PURPOSE

| Product | Offset Voltage 25°C max (±mV) | Offset Voltage Drift max (±µV/°C) | Bias Current 25°C max (nA) | Small Signal Unity Gain min (MHz) | Power Supply Range (V) | Quiescent Current, max (mA) | Description |
|---|---|---|---|---|---|---|---|
| OPA27 | 0.100 | 1.8 | 80 | 5 | ±4.0 to ±22 | 5.7 | Bipolar |
| OPA37 | 0.100 | 1.8 | 80 | 80[1] | ±4.0 to ±22 | 5.7 | Bipolar |
| OPA77 | 0.025 | 0.3 | 2 | 0.4 | ±3.0 to ±18 | 2.0 | Bipolar |
| OPA130 | 1.0 | 10 | 25pA | 1 | ±2.5 to ±18 | 0.65 | FET, Low Power |
| OPA131 | 1.0 | 10 | 50pA | 4* | ±4.5 to ±18 | 1.75 | FET |
| OPA177 | 0.025 | 0.1 | 1.5 | 0.4 | ±3.0 to ±18 | 2.0 | Bipolar |
| **OPA277** | **0.05** | **1** | **2.8** | **1** | **±20 to ±18** | **0.825** | **Bipolar** |
| OPA604 | 5.0 | 8* | 50pA | 20*[2] | ±4.5 to ±24 | 6.0 | FET, Low Distortion (0.0003%) |
| OPA2130 | 1.0 | 10 | 25pA | 1 | ±2.5 to ±18 | 0.65 | FET, Low Power, Dual |
| **OPA2277** | **0.05** | **1** | **2.8** | **1** | **±2.0 to ±18** | **1.65** | **Bipolar, Dual** |
| OPA2131 | 1.0 | 10 | 50pA | 4* | ±4.5 to ±18 | 3.5 | FET, Dual |
| OPA2604 | 5.0 | 8* | 0.1 | 20*[2] | ±4.5 to ±24 | 12 | FET, Dual, Low Distortion (0.0003%) |
| OPA4130 | 1.0 | 10 | 25pA | 1 | ±2.5 to ±18 | 0.65 | FET, Low Power, Quad |
| OPA4131 | 1.0 | 10.00 | 50pA | 4* | ±4.5 to ±18 | 7.0 | FET, Quad |
| **OPA4277** | **0.05** | **1** | **2.8** | **1** | **±2.0 to ±18** | **3.30** | **Bipolar, Quad** |

NOTE: (1) Gain Bandwidth at Gain = 5V/V. (2) Gain = 100.

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# HIGH SPEED - VOLTAGE FEEDBACK

| Product | Small Signal Bandwidth at Specified Gain typ (MHz) | Slew Rate min (V/µs) | Settling Time to ±0.1% (ns) | Rated Voltage Output[2] min (±V) | Rated Current Output min (±mA) | Description |
|---|---|---|---|---|---|---|
| OPA620 | 300, G = 1 | 175 | 13 | 3 | 50 | Low Noise 2.3nV/√Hz, Wideband |
| OPA621 | 500, G = 2 | 350 | 15 | 3 | 50 | Low Noise 2.3nV/√Hz, Wideband, G = 2 minimum |
| OPA622 | 250, G = 1 | 1600* | 17 | 3 | 70* | High Slew Rate |
| OPA640 | 1.3GHz, G = 1 | 350* | 18 | 2.25 | 25 | Voltage Feedback, Low Noise 2.9nV/√Hz |
| OPA641 | 800, G = 2 | 650* | 13 | 2.6 | 25 | Voltage Feedback, Low Noise 2.8nV/√Hz, G = 2 minimum |
| OPA642 | 450, G = 1 | 380* | 11.5 | 3.0 | 50 | Voltage Feedback, Low Distortion 95dB SFDR |
| OPA643 | 300, G = 5 | 1000* | 16.5 | 3.0 | 50 | Voltage Feedback, Low Distortion 90dB SFDR, G = 5 minimum |
| OPA650 | 560, G = 1 | 240 | 10.2 | 2.4 | +75/–65 | Voltage Feedback, Low Power, G = 1 minimum |
| OPA651 | 470, G = 2 | 300 | 11.5 | 2.4 | 45 | Voltage Feedback, Low Power, G = 2 minimum |
| OPA655 | 400, G = 1 | 210 | 8 | 2.8 | 35 | FET, Wideband, Low Distortion, Unity Gain Stable |
| OPA671 | 33, G = 1 | 107* | 150 | 10.5[1] | 50* | FET |
| OPA678 | 200, G = 1 | 250 | 22 | 2.5 | 44 | Very Fast Settling Switched Input |
| **OPA680** | **220, G = 2** | **1800** | **—** | **3.8** | **135** | **High Output Drive, Disable Pin** |
| **OPA686** | **250, G = 10** | **600** | **16** | **3.2** | **60** | **Low Noise, High GBWP** |
| **OPA688** | **260, G = 2** | **1000** | **7** | **3.9** | **85** | **Voltage Limiting Amplifier (VLA™)** |
| **OPA689** | **280, G = 6** | **1600** | **7** | **3.9** | **85** | **Voltage Limiting Amplifier (VLA™)** |
| OPA2650 | 360, G = 1 | 240 | 11 | 2.4 | +75/–65 | Dual, OPA650 |
| **OPA2680** | **220, G = 2** | **1800** | **—** | **3.8** | **135** | **Dual OPA680** |
| OPA4650 | 360, G = 1 | 240 | 10.3 | 2.2 | +75/–65 | Quad, OPA650 |

NOTE: (1) For ±15V supplies. (2) For ±5V supplies.

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*For Immediate Assistance, Contact Your Local Salesperson*

## HIGH SPEED - CURRENT FEEDBACK

| Product | Small Signal Bandwidth for G = +2V/V typ (MHz) | Slew Rate typ (V/μs) | Settling time, to ±0.1% (ns) | Rated Voltage Output[2] min (±V) | Rated Current Output min (±mA) | Description |
|---|---|---|---|---|---|---|
| OPA603 | 160 | 1000 | 50 | 10[1] | 15 | ±15V Supply |
| OPA644 | 300 | 2500 | 16.5 | 3.0 | 50 | High Slew Rate |
| OPA658 | 680 | 1700 | 11.5 | 2.5 | +80/–60 | Low Power, Wideband |
| **OPA681** | **220, G = 2** | **2100** | **8** | **3.8** | **135** | **High Output Drive, Disable Pin** |
| OPA2658 | 500 | 1700 | 12.6 | 2.5 | +80/–60 | Dual, OPA658 |
| **OPA2681** | **220, G = 2** | **2100** | **8** | **3.8** | **135** | **Dual, OPA681** |
| OPA4658 | 450 | 1700 | 15.1 | 2.5 | +80/–60 | Quad, OPA658 |

NOTE: (1) For ±15V supplies. (2) For ±5V supplies.

## SPECIAL PURPOSE

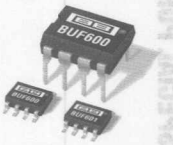
| Product | Offset Voltage 25°C max (±mV) | Offset Voltage Drift max (±μV/°C) | Bias Current 25°C max (μA) | Small Signal Bandwidth typ (MHz) | Rated Voltage Output min (±V) | Rated Current Output min (±mA) | Description |
|---|---|---|---|---|---|---|---|
| **OPA134** | **2** | **3** | **100p** | **8** | **14** | **35*** | **Audio** |
| OPA660 | +7* | 50* | NS | 850 | 3.7 | 10 | Transconductance Amp and Buffer |
| OPA678 | 1 | 10 | 50 | 200, G = 1 | 2.5 | 30 | Two-Channel, TTL & ECL Controlled |
| **OPA2134** | **2** | **3** | **100p** | **8** | **14** | **35*** | **Dual, Audio** |
| OPA2662 | 75 | 12* | NS | 370 | 3.4 | 75 | Transconductance Amp, Dual |
| **OPA4134** | **2** | **3** | **100p** | **8** | **14** | **35*** | **Quad, Audio** |
| VCA610 | — | — | 6* | 30, G = 40dB | 3.0* | 80* | Voltage Controlled Gain |

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BURR - BROWN®




# BUF600
# BUF601

www.burr-brown.com/databook/BUF600.html

# HIGH-SPEED BUFFER AMPLIFIER

## FEATURES

- OPEN-LOOP BUFFER
- HIGH-SLEW RATE: 3600V/µs, 5.0Vp-p
- BANDWIDTH: 320MHz, 5.0Vp-p
  900MHz, 0.2Vp-p
- LOW INPUT BIAS CURRENT: 0.7µA/1.5µA
- LOW QUIESCENT CURRENT: 3mA/6mA
- GAIN FLATNESS: 0.1dB, 0 to 300MHz

## APPLICATIONS

- VIDEO BUFFER/LINE DRIVER
- INPUT/OUTPUT AMPLIFIER FOR MEASUREMENT EQUIPMENT
- PORTABLE SYSTEMS
- TRANSMISSION SYSTEMS
- TELECOMMUNICATIONS
- HIGH-SPEED ANALOG SIGNAL PROCESSING
- ULTRASOUND

## DESCRIPTION

The BUF600 and BUF601 are monolithic open-loop unity-gain buffer amplifiers with a high symmetrical slew rate of up to 3600V/µs and a very wide bandwidth of 320MHz at 5Vp-p output swing. They use a complementary bipolar IC process, which incorporates pn-junction isolated high-frequency NPN and PNP transistors to achieve high-frequency performance previously unattainable with conventional integrated circuit technology.

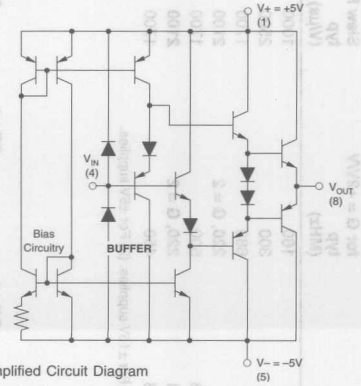
Their unique design offers a high-performance alternative to expensive discrete or hybrid solutions.

The BUF600 and BUF601 feature low quiescent current, low input bias current, small signal delay time and phase shift, and low differential gain and phase errors.

The BUF600 with 3mA quiescent current is well-suited for operation between high-frequency processing stages. It demonstrates outstanding performance even in feedback loops of wide-band amplifiers or phase-locked loop systems.

The BUF601, with 6mA quiescent current and therefore lower output impedance, can easily drive 50Ω inputs or 75Ω systems and cables.

The broad range of analog and digital applications extends from decoupling of signal processing stages, impedance transformation, and input amplifiers for RF equipment and ATE systems to video systems, distribution fields, IF/communications systems, and output drivers for graphic cards.




Simplified Circuit Diagram

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

## DC SPECIFICATION

At $V_{CC}$ = ±5V, $R_{LOAD}$ = 10kΩ, $R_{SOURCE}$ = 50Ω, and $T_{AMB}$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | BUF600AP, AU | | | BUF601AU | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT OFFSET VOLTAGE** | | | | | | | | |
| Initial | | | ±15 | ±30 | | ±15 | ±30 | mV |
| vs Temperature | | | 9 | | | 25 | | µV/°C |
| vs Supply (tracking) | $V_{CC}$ = ±4.5V to ±5.5V | –54 | –72 | | –54 | –77 | | dB |
| vs Supply (non-tracking) | $V_{CC}$ = +4.5V to +5.5V | | –55 | | | –55 | | dB |
| vs Supply (non-tracking) | $V_{CC}$ = –4.5V to –5.5V | | –54 | | | –54 | | dB |
| **INPUT BIAS CURRENT** | | | | | | | | |
| Initial | | | +3.5 | –2.5/+5 | | +3.5 | –5/+10 | µA |
| vs Temperature | | | 0.4 | | | 0.7 | | nA/°C |
| vs Supply (tracking) | $V_{CC}$ = ±4.5V to ±5.5V | | 0.15 | | | 0.3 | | µA/V |
| vs Supply (non-tracking) | $V_{CC}$ = +4.5V to +5.5V | | 0.5 | | | 0.5 | | µA/V |
| vs Supply (non-tracking) | $V_{CC}$ = –4.5V to –5.5V | | 20 | | | 20 | | nA/V |
| **INPUT IMPEDANCE** | | | 4.8 ‖ 1 | | | 2.5 ‖ 1 | | MΩ ‖ pF |
| **INPUT NOISE** | | | | | | | | |
| Voltage Noise Density | f = 100kHz to 100MHz | | 5.2 | | | 4.8 | | nV/√Hz |
| Signal-to-Noise Ratio | S/N = 20 Log (0.7/(Vn • √5MHz)) | | 95 | | | 96 | | dB |
| **TRANSFER CHARACTERISTICS** | Voltage Gain; $V_{IN}$ = ±2.5V | | | | | | | |
| | $R_{LOAD}$ = 100Ω | | | | | 0.95 | | V/V |
| | $R_{LOAD}$ = 200Ω | | 0.96 | | | | | V/V |
| | $R_{LOAD}$ = 10kΩ | | 0.99 | | | 0.99 | | V/V |
| **RATED OUTPUT** | | | | | | | | |
| Voltage Output | $V_{IN}$ = ±2.7V | | | | | | | |
| | $R_{LOAD}$ = 100Ω | | | | ±2.5 | ±2.6 | | V |
| | $R_{LOAD}$ = 200Ω | ±2.5 | ±2.6 | | | | | V |
| DC Current Output | DC, $R_{LOAD}$ = 100Ω | ±20 | | | ±20 | | | mA |
| Output Impedance | | | 6.2 | | | 3.6 | | Ω |
| **POWER SUPPLY** | | | | | | | | |
| Rated Voltage | | | ±5 | | | ±5 | | V |
| Derated Performance | | ±4.5 | | ±5.5 | ±4.5 | | ±5.5 | V |
| Quiescent Current | | ±2.6 | ±3 | ±3.4 | ±5.4 | ±6 | ±6.6 | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –40 | | 85 | –40 | | 85 | °C |
| Storage | | –40 | | 125 | –40 | | 125 | °C |

## AC SPECIFICATION

At $V_{CC}$ = ±5V, $R_{LOAD}$ = 200Ω (BUF600) and 100Ω (BUF601), $R_{SOURCE}$ = 50Ω, and $T_{AMB}$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | BUF600AP, AU | | | BUF601AU | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **FREQUENCY DOMAIN** | | | | | | | | |
| **LARGE SIGNAL BANDWIDTH** | $V_O$ = 5Vp-p, $C_{OUT}$ = 1pF | | 320 | | | 320 | | MHz |
| (–3dB) | $V_O$ = 2.8Vp-p, $C_{OUT}$ = 1pF | | 400 | | | 400 | | MHz |
| | $V_O$ = 1.4Vp-p, $C_{OUT}$ = 1pF | | 700 | | | 700 | | MHz |
| **SMALL SIGNAL BANDWIDTH** | $V_O$ = 0.2Vp-p, $C_{OUT}$ = 1pF | | 650 | | | 900 | | MHz |
| **GROUP DELAY TIME** | | | 250 | | | 200 | | ps |
| **DIFFERENTIAL GAIN** | $V_{IN}$ = 0.3Vp-p, f = 4.43MHz V = 0 to 0.7V | | | | | | | |
| | BUF600 $R_{LOAD}$ = 200Ω | | 0.5 | | | | | % |
| | $R_{LOAD}$ = 1kΩ | | 0.075 | | | | | % |
| | BUF601 $R_{LOAD}$ = 100Ω | | | | | 0.4 | | % |
| | $R_{LOAD}$ = 500Ω | | | | | 0.05 | | % |
| **DIFFERENTIAL PHASE** | $V_{IN}$ = 0.3Vp-p, f = 4.43MHz V = 0 to 0.7V | | | | | | | |
| | BUF600 $R_{LOAD}$ = 200Ω | | 0.02 | | | | | Degrees |
| | $R_{LOAD}$ = 1kΩ | | 0.04 | | | | | Degrees |
| | BUF601 $R_{LOAD}$ = 100Ω | | | | | 0.025 | | Degrees |
| | $R_{LOAD}$ = 500Ω | | | | | 0.03 | | Degrees |

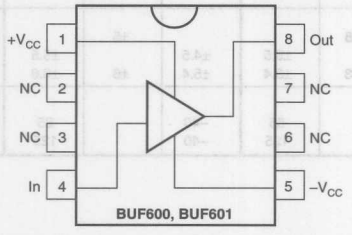
## AC-SPECIFICATIONS (CONT)

At $V_{CC}$ = ±5V, $R_{LOAD}$ = 200Ω (BUF600) and 100Ω (BUF601), $R_{SOURCE}$ = 50Ω, and $T_{AMB}$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | BUF600AP, AU | | | BUF601AU | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **HARMONIC DISTORTION** | | | | | | | | |
| Second Harmonic | f = 10MHz, $V_O$ = 1.4Vp-p | | –65 | | | –65 | | dBc |
| Third Harmonic | | | –64 | | | –67 | | dBc |
| Second Harmonic | f = 30MHz, $V_O$ = 1.4Vp-p | | –51 | | | –59 | | dBc |
| Third Harmonic | | | –56 | | | –62 | | dBc |
| Second Harmonic | f = 50MHz, $V_O$ = 1.4Vp-p | | –43 | | | –53 | | dBc |
| Third Harmonic | | | –48 | | | –54 | | dBc |
| **GAIN FLATNESS PEAKING** | | | | | | | | |
| | $V_O$ = 0.4Vp-p, DC to 30MHz | | 0.01 | | | 0.005 | | dB |
| | $V_O$ = 0.4Vp-p, 30MHz to 300MHz | | 0.3 | | | 0.1 | | dB |
| **LINEAR PHASE DEVIATION** | | | | | | | | |
| | $V_O$ = 0.4Vp-p, DC to 30MHz | | 5.5 | | | 3.8 | | Degrees |
| | $V_O$ = 0.4Vp-p, 30 to 300MHz | | 55 | | | 45 | | Degrees |
| **TIME DOMAIN** | | | | | | | | |
| **RISE TIME** | 10% to 90%, 700ps | | | | | | | |
| | 1.4Vp-p Step | | 0.82 | | | 0.87 | | ns |
| | 2.8Vp-p Step | | 0.97 | | | 0.95 | | ns |
| | 5.0Vp-p Step | | 1.18 | | | 1.13 | | ns |
| **SLEW RATE** | | | | | | | | |
| | $V_O$ = 1.4Vp-p | | 1500 | | | 1500 | | V/µs |
| | $V_O$ = 2.8Vp-p | | 2400 | | | 2400 | | V/µs |
| | $V_O$ = 5.0Vp-p | | 3400 | | | 3600 | | V/µs |

## PIN CONFIGURATION

Top View DIP/SO-8




BUF600, BUF601

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | ±6V |
| Input Voltage[1] | $\pm V_{CC}$ ±0.7V |
| Operating Temperature | –40°C to +85°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Inputs are internally diode-clamped to $\pm V_{CC}$.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| BUF600AP | Plastic 8-Pin DIP | 006 | –40°C to +85°C |
| BUF600AU | SO-8 Surface Mount | 182 | –40°C to +85°C |
| BUF601AU | SO-8 Surface Mount | 182 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## FUNCTIONAL DESCRIPTION

| FUNCTION | DESCRIPTION |
|---|---|
| In | Analog Input |
| Out | Analog Output |
| $+V_{CC}$ | Positive Supply Voltage; typical +5VDC |
| $-V_{CC}$ | Negative Supply Voltage; typical –5VDC |

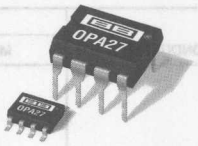
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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BURR-BROWN®



# OPA27
# OPA37

www.burr-brown.com/databook/OPA27.html



# Ultra-Low Noise Precision OPERATIONAL AMPLIFIERS

## FEATURES

- LOW NOISE: 4.5nV/√Hz max at 1kHz
- LOW OFFSET: 100µV max
- LOW DRIFT: 0.4µV/°C
- HIGH OPEN-LOOP GAIN: 117dB min
- HIGH COMMON-MODE REJECTION: 100dB min
- HIGH POWER SUPPLY REJECTION: 94dB min
- FITS OP-07, OP-05, AD510, AD517 SOCKETS

## APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- TRANSDUCER AMPLIFIER
- RADIATION HARD EQUIPMENT

## DESCRIPTION

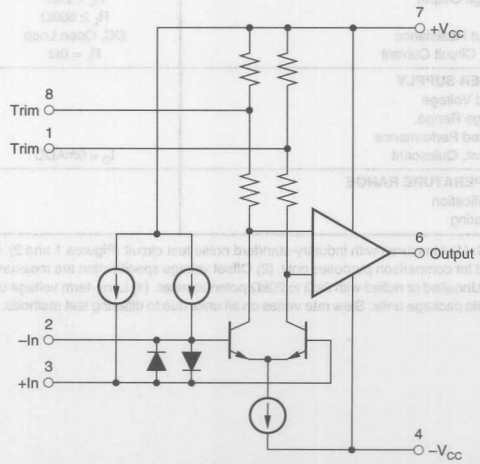
The OPA27/37 is an ultra-low noise, high precision monolithic operational amplifier.

Laser-trimmed thin-film resistors provide excellent long-term voltage offset stability and allow superior voltage offset compared to common zener-zap techniques.

A unique bias current cancellation circuit allows bias and offset current specifications to be met over the full –55°C to +125°C temperature range.

The OPA27 is internally compensated for unity-gain stability. The decompensated OPA37 requires a closed-loop gain ≥ 5.

The Burr-Brown OPA27/37 is an improved replacement for the industry-standard OP-27/OP-37.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

At $V_{CC}$ = ±15V and $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA27/37G MIN | OPA27/37G TYP | OPA27/37G MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT NOISE**[6] | | | | | |
| Voltage, $f_O$ = 10Hz | | | 3.8 | 8.0 | nV/√Hz |
| $f_O$ = 30Hz | | | 3.3 | 5.6 | nV/√Hz |
| $f_O$ = 1kHz | | | 3.2 | 4.5 | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 0.09 | 0.25 | µVp-p |
| Current,[1] $f_O$ = 10Hz | | | 1.7 | | pA/√Hz |
| $f_O$ = 30Hz | | | 1.0 | | pA/√Hz |
| $f_O$ = 1kHz | | | 0.4 | 0.6 | pA/√Hz |
| **OFFSET VOLTAGE**[2] | | | | | |
| Input Offset Voltage | | | ±25 | ±100 | µV |
| Average Drift[3] | $T_{A\,MIN}$ to $T_{A\,MAX}$ | | ±0.4 | ±1.8[6] | µV/°C |
| Long Term Stability[4] | | | 0.4 | 2.0 | µV/mo |
| Supply Rejection | $\pm V_{CC}$ = 4 to 18V | 94 | 120 | | dB |
| | $\pm V_{CC}$ = 4 to 18V | | ±1 | ±20 | µV/V |
| **BIAS CURRENT** | | | | | |
| Input Bias Current | | | ±15 | ±80 | nA |
| **OFFSET CURRENT** | | | | | |
| Input Offset Current | | | 10 | 75 | nA |
| **IMPEDANCE** | | | | | |
| Common-Mode | | | 2 ll 2.5 | | GΩ ll pF |
| **VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range | | ±11 | ±12.3 | | V |
| Common-Mode Rejection | $V_{IN}$ = ±11VDC | 100 | 122 | | dB |
| **OPEN-LOOP VOLTAGE GAIN, DC** | $R_L \geq 2k\Omega$ | 117 | 124 | | dB |
| | $R_L \geq 1k\Omega$ | | 124 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product[5] | OPA27 | 5[6] | 8 | | MHz |
| | OPA37 | 45[6] | 63 | | MHz |
| Slew Rate[5] | $V_O$ = ±10V, $R_L$ = 2kΩ | | | | |
| | OPA27, G = +1 | 1.7[6] | 1.9 | | V/µs |
| | OPA37, G = +5 | 11[6] | 11.9 | | V/µs |
| Settling Time, 0.01% | OPA27, G = +1 | | 25 | | µs |
| | OPA37, G = +5 | | 25 | | µs |
| **RATED OUTPUT** | | | | | |
| Voltage Output | $R_L \geq 2k\Omega$ | ±12 | ±13.8 | | V |
| | $R_L \geq 600\Omega$ | ±10 | ±12.8 | | V |
| Output Resistance | DC, Open Loop | | 70 | | Ω |
| Short Circuit Current | $R_L$ = 0Ω | | 25 | 60[6] | mA |
| **POWER SUPPLY** | | | | | |
| Rated Voltage | | | ±15 | | VDC |
| Voltage Range, Derated Performance | | ±4 | | ±22 | VDC |
| Current, Quiescent | $I_O$ = 0mADC | | 3.3 | 5.7 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –40 | | +85 | °C |
| Operating | | –40 | | +85 | °C |

NOTES: (1) Measured with industry-standard noise test circuit (Figures 1 and 2). Due to errors introduced by this method, these current noise specifications should be used for comparison purposes only. (2) Offset voltage specification are measured with automatic test equipment after approximately 0.5 seconds from power turn-on. (3) Unnulled or nulled with 8kΩ to 20kΩ potentiometer. (4) Long-term voltage offset vs time trend line does not include warm-up drift. (5) Typical specification only on plastic package units. Slew rate varies on all units due to differing test methods. Minimum specification applies to open-loop test. (6) This parameter guaranteed by design.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

# SPECIFICATIONS

At $V_{CC}$ = ±15V and $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA27/37G MIN | OPA27/37G TYP | OPA27/37G MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT VOLTAGE**[1] | | | | | |
| Input Offset Voltage | | | ±48 | ±220[3] | µV |
| Average Drift[2] | $T_{A\ MIN}$ to $T_{A\ MAX}$ | | ±0.4 | ±1.8[3] | µV/°C |
| Supply Rejection | ±$V_{CC}$ = 4.5 to 18V | | | | |
| | ±$V_{CC}$ = 4.5 to 18V | 90[3] | 122 | | dB |
| **BIAS CURRENT** | | | | | |
| Input Bias Current | | | ±21 | ±150[3] | nA |
| **OFFSET CURRENT** | | | | | |
| Input Offset Current | | | | | |
| E, F, G | | | 20 | 135[3] | nA |
| **VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range | | ±10.5[3] | ±11.8 | | V |
| Common-Mode Rejection | $V_{IN}$ = ±11VDC | 96[3] | 122 | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | |
| Open-Loop Voltage Gain | $R_L \geq 2k\Omega$ | 113[3] | 120 | | dB |
| **RATED OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 2kΩ | ±11.0[3] | ±13.4 | | V |
| Short Circuit Current | $V_O$ = 0VDC | | 25 | | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –40 | | +85 | °C |

NOTES: (1) Offset voltage specification are measured with automatic test equipment after approximately 0.5s from power turn-on. (2) Unnulled or nulled with 8kΩ to 20kΩ potentiometer. (3) This parameter guaranteed by design.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±22V |
| Internal Power Dissipation [1] | 500mW |
| Input Voltage | ±$V_{CC}$ |
| Output Short-Circuit Duration [2] | Indefinite |
| Differential Input Voltage [3] | ±0.7V |
| Differential Input Current [3] | ±25mA |
| Storage Temperature Range | –55°C to +125°C |
| Operating Temperature Range | –40°C to +85°C |
| Lead Temperature: | |
| P (soldering, 10s) | +300°C |
| U (soldering, 3s) | +260°C |

| PACKAGE TYPE | $\theta_{JA}$ | UNITS |
|---|---|---|
| 8-Pin Plastic DIP (P) | 100 | °C/W |
| 8-Pin SOIC (U) | 160 | °C/W |

NOTES: (1) Maximum package power dissipation vs ambient temperature. (2) To common with ±$V_{CC}$ = 15V. (3) The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

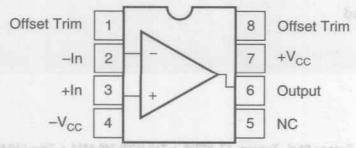
## PACKAGE/ORDERING INFORMATION

| PRODUCT[1] | PACKAGE | TEMPERATURE RANGE (°C) | OFFSET VOLTAGE MAX (µV), 25°C | PACKAGE DRAWING NUMBER[3] |
|---|---|---|---|---|
| OPA27GP | Plastic | –40 to +85 | ±100 | 006 |
| OPA27GU[2] | SOIC | –40 to +85 | ±100 | 182 |

NOTE: (1) Packages for OPA37 are same as for OPA27. (2) OPA27GU may be marked OPA27U. Likewise, OPA37GU may be marked OPA37U. (3) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## CONNECTION DIAGRAMS

**Top View** **P, U Packages**

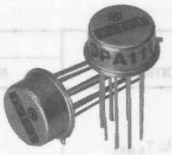



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®



# OPA111

www.burr-brown.com/databook/OPA111.html

# Low Noise Precision *Difet*® OPERATIONAL AMPLIFIER

## FEATURES

- LOW NOISE: 100% Tested, 8nV√Hz max (10kHz)
- LOW BIAS CURRENT: 1pA max
- LOW OFFSET: 250µV max
- LOW DRIFT: 1µV/°C max
- HIGH OPEN-LOOP GAIN: 120dB min
- HIGH COMMON-MODE REJECTION: 100dB min

## APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- OPTOELECTRONICS
- MEDICAL EQUIPMENT—CAT SCANNER
- RADIATION HARD EQUIPMENT

## DESCRIPTION

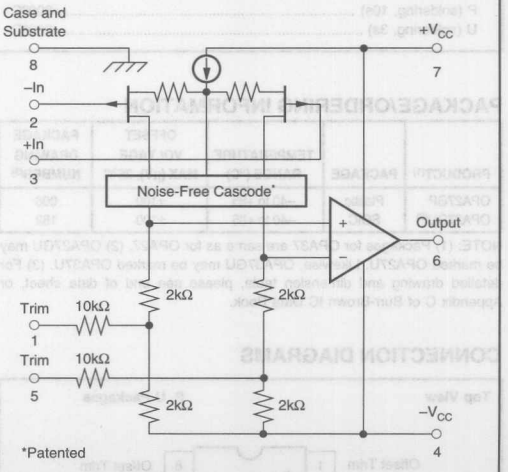
The OPA111 is a precision monolithic dielectrically isolated FET (***Difet***®) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with patented circuit design techniques. A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.




BIFET® National Semiconductor Corp., ***Difet***® Burr-Brown Corp.

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# SPECIFICATIONS

## ELECTRICAL

At $V_{CC}$ = ±15VDC and $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITION | OPA111AM | | | OPA111BM | | | OPA111SM | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT** | | | | | | | | | | | |
| **NOISE** | | | | | | | | | | | |
| Voltage, $f_O$ = 10Hz | 100% Tested | | 40 | 80 | | 30 | 60 | | 40 | 80 | nV/√Hz |
| $f_O$ = 100Hz | 100% Tested | | 15 | 40 | | 11 | 30 | | 15 | 40 | nV/√Hz |
| $f_O$ = 1kHz | 100% Tested | | 8 | 15 | | 7 | 12 | | 8 | 15 | nV/√Hz |
| $f_O$ = 10kHz | 100% Tested | | 6 | 8 | | 6 | 8 | | 6 | 8 | nV/√Hz |
| $f_B$ = 10Hz to 10kHz | 100% Tested | | 0.7 | 1.2 | | 0.6 | 1 | | 0.7 | 1.2 | µVrms |
| $f_B$ = 0.1Hz to 10Hz | (1) | | 1.6 | 3.3 | | 1.2 | 2.5 | | 1.6 | 3.3 | µVp-p |
| Current, $f_B$ = 0.1Hz to 10Hz | (1) | | 9.5 | 15 | | 7.5 | 12 | | 9.5 | 15 | fAp-p |
| $f_O$ = 0.1Hz thru 20kHz | (1) | | 0.5 | 0.8 | | 0.4 | 0.6 | | 0.5 | 0.8 | fA/√Hz |
| **OFFSET VOLTAGE**(2) | | | | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0VDC | | ±100 | ±500 | | ±50 | ±250 | | ±100 | ±500 | µV |
| Average Drift | $T_A = T_{MIN}$ to $T_{MAX}$ | | ±2 | ±5 | | ±0.5 | ±1 | | ±2 | ±5 | µV/°C |
| Supply Rejection | $V_{CC}$ = ±10V to ±18V | 90 | 110 | | 100 | 110 | | 90 | 110 | | dB |
| | | | ±3 | ±31 | | ±3 | ±10 | | ±3 | ±31 | µV/V |
| **BIAS CURRENT**(2) | | | | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC | | ±0.8 | ±2 | | ±0.5 | ±1 | | ±0.8 | ±2 | pA |
| **OFFSET CURRENT**(2) | | | | | | | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC | | ±0.5 | ±1.5 | | ±0.25 | ±0.75 | | ±0.5 | ±1.5 | pA |
| **IMPEDANCE** | | | | | | | | | | | |
| Differential | | | $10^{13}$ ‖ 1 | | | $10^{13}$ ‖ 1 | | | $10^{13}$ ‖ 1 | | Ω ‖ pF |
| Common-Mode | | | $10^{14}$ ‖ 3 | | | $10^{14}$ ‖ 3 | | | $10^{14}$ ‖ 3 | | Ω ‖ pF |
| **VOLTAGE RANGE** | | | | | | | | | | | |
| Common-Mode Input Range | | ±10 | ±11 | | ±10 | ±11 | | ±10 | ±11 | | V |
| Common-Mode Rejection | $V_{IN}$ = ±10VDC | 90 | 110 | | 100 | 110 | | 90 | 110 | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | | | | |
| Open-Loop Voltage Gain | $R_L \geq 2k\Omega$ | 114 | 125 | | 120 | 125 | | 114 | 125 | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | | | | |
| Unity Gain, Small Signal | | | 2 | | | 2 | | | 2 | | MHz |
| Full Power Response | 20Vp-p, $R_L$ = 2kΩ | 16 | 32 | | 16 | 32 | | 16 | 32 | | kHz |
| Slew Rate | $V_O$ = ±10V, $R_L$ = 2kΩ | 1 | 2 | | 1 | 2 | | 1 | 2 | | V/µs |
| Settling Time, 0.1% | Gain = –1, $R_L$ = 2kΩ | | 6 | | | 6 | | | 6 | | µs |
| 0.01% | 10V Step | | 10 | | | 10 | | | 10 | | µs |
| Overload Recovery, 50% Overdrive(3) | Gain = –1 | | 5 | | | 5 | | | 5 | | µs |
| **RATED OUTPUT** | | | | | | | | | | | |
| Voltage Output | $R_L$ = 2kΩ | ±11 | ±12 | | ±11 | ±12 | | ±11 | ±12 | | V |
| Current Output | $V_O$ = ±10VDC | ±5.5 | ±10 | | ±5.5 | ±10 | | ±5.5 | ±10 | | mA |
| Output Resistance | DC, Open Loop | | 100 | | | 100 | | | 100 | | Ω |
| Load Capacitance Stability | Gain = +1 | | 1000 | | | 1000 | | | 1000 | | pF |
| Short Circuit Current | | 10 | 40 | | 10 | 40 | | 10 | 40 | | mA |
| **POWER SUPPLY** | | | | | | | | | | | |
| Rated Voltage | | | ±15 | | | ±15 | | | ±15 | | VDC |
| Voltage Range, Derated Performance | | ±5 | | ±18 | ±5 | | ±18 | ±5 | | ±18 | VDC |
| Current, Quiescent | $I_O$ = 0mADC | | 2.5 | 3.5 | | 2.5 | 3.5 | | 2.5 | 3.5 | mA |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification | Ambient Temp. | –25 | | +85 | –25 | | +85 | –55 | | +125 | °C |
| Operating | Ambient Temp. | –55 | | +125 | –55 | | +125 | –55 | | +125 | °C |
| Storage | Ambient Temp. | –65 | | +150 | –65 | | +150 | –65 | | +150 | °C |
| θ Junction-Ambient | | | 200 | | | 200 | | | 200 | | °C/W |

NOTES: (1) Sample tested—this parameter is guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.

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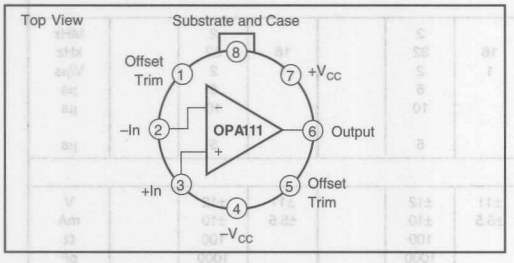
## ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC}$ = ±15VDC and $T_A = T_{MIN}$ to $T_{MAX}$ unless otherwise noted.

| PARAMETER | CONDITION | OPA111AM | | | OPA111BM | | | OPA111SM | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification Range | Ambient Temp. | –25 | | +85 | –25 | | +85 | –55 | | +125 | °C |
| **INPUT** | | | | | | | | | | | |
| **OFFSET VOLTAGE**(1) | | | | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0VDC | | ±220 | ±1000 | | ±110 | ±500 | | ±300 | ±1500 | µV |
| Average Drift | | | ±2 | ±5 | | ±0.5 | ±1 | | ±2 | ±5 | µV/°C |
| Supply Rejection | $V_{CC}$ = ±10V to ±18V | 86 | 100 | | 90 | 100 | | 86 | 100 | | dB |
| | | | ±10 | ±50 | | ±10 | ±32 | | ±10 | ±50 | µV/V |
| **BIAS CURRENT**(1) | | | | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC | | ±50 | ±250 | | ±30 | ±130 | | ±820 | ±4100 | pA |
| **OFFSET CURRENT**(1) | | | | | | | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC | | ±30 | ±200 | | ±15 | ±100 | | ±510 | ±3100 | pA |
| **VOLTAGE RANGE** | | | | | | | | | | | |
| Common-Mode Input Range | | ±10 | ±11 | | ±10 | ±11 | | ±10 | ±11 | | V |
| Common-Mode Rejection | $V_{IN}$ = ±10VDC | 86 | 100 | | 90 | 100 | | 86 | 100 | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | | | | |
| Open-Loop Voltage Gain | $R_L \geq 2k\Omega$ | 110 | 120 | | 114 | 120 | | 110 | 120 | | dB |
| **RATED OUTPUT** | | | | | | | | | | | |
| Voltage Output | $R_L$ = 2kΩ | ±10.5 | ±11 | | ±11 | ±11.5 | | ±11 | ±11.5 | | V |
| Current Output | $V_O$ = ±10VDC | ±5.25 | ±10 | | ±5.25 | ±10 | | ±5.25 | ±10 | | mA |
| Short Circuit Current | $V_O$ = 0VDC | 10 | 40 | | 10 | 40 | | 10 | 40 | | mA |
| **POWER SUPPLY** | | | | | | | | | | | |
| Current, Quiescent | $I_O$ = 0mADC | | 2.5 | 3.5 | | 2.5 | 3.5 | | 2.5 | 3.5 | mA |

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

## CONNECTION DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply | ±18VDC |
| Internal Power Dissipation(1) | 750mW |
| Differential Input Voltage(2) | ±36VDC |
| Input Voltage Range(2) | ±18VDC |
| Storage Temperature Range | –65°C to +150°C |
| Operating Temperature Range | –55°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short Circuit Duration(3) | Continuous |
| Junction Temperature | +175°C |

NOTES: (1) Packages must be derated based on $\theta_{JC}$ = 150°C/W or $\theta_{JA}$ = 300°C/W. (2) For supply voltages less than ±18VDC, the absolute maximum input voltage is equal to +18V > $V_{IN}$ > –$V_{CC}$ – 6V. See Figure 2. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and $T_J$.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| OPA111AM | TO-99 | 001 |
| OPA111BM | TO-99 | 001 |
| OPA111SM | TO-99 | 001 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

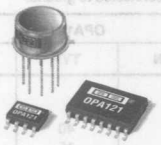
| PRODUCT | PACKAGE | TEMPERATURE RANGE | OFFSET VOLTAGE, MAX (µV) |
|---|---|---|---|
| OPA111AM | TO-99 | –25°C to +85°C | ±500 |
| OPA111BM | TO-99 | –25°C to +85°C | ±250 |
| OPA111SM | TO-99 | –55°C to +125°C | ±500 |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®



# OPA121

www.burr-brown.com/databook/OPA121.html

# Low Cost Precision *Difet*® OPERATIONAL AMPLIFIER

## FEATURES

- LOW NOISE: 6nV/√Hz typ at 10kHz
- LOW BIAS CURRENT: 5pA max
- LOW OFFSET: 2mV max
- LOW DRIFT: 3μV/°C typ
- HIGH OPEN-LOOP GAIN: 110dB min
- HIGH COMMON-MODE REJECTION: 86dB min

## APPLICATIONS

- OPTOELECTRONICS
- DATA ACQUISITION
- TEST EQUIPMENT
- MEDICAL EQUIPMENT
- RADIATION HARD EQUIPMENT

## DESCRIPTION

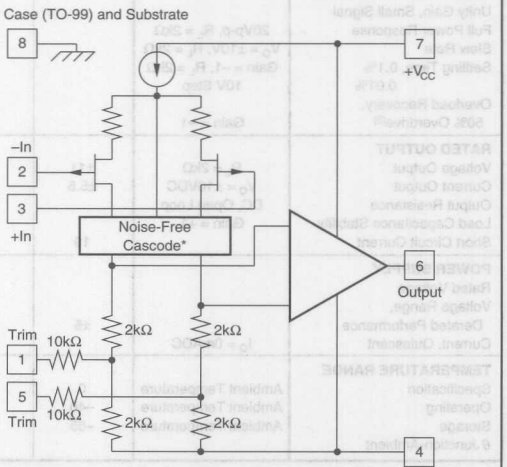
The OPA121 is a precision monolithic dielectrically-isolated FET (***Difet***®) operational amplifier. Outstanding performance characteristics are now available for low-cost applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very low bias current is obtained by dielectric isolation with on-chip guarding.

Laser-trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with new circuit design techniques (patented). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.




*Patented

OPA121 Simplified Circuit

*Difet*®, Burr-Brown Corp.
BIFET®, National Semiconductor Corp.

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# SPECIFICATIONS

## ELECTRICAL

At $V_{CC}$ = ±15VDC and $T_A$ = +25°C, unless otherwise noted. Pin 8 connected to ground.

| PARAMETER | CONDITIONS | OPA121KM | | | OPA121KP, KU | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT** | | | | | | | | |
| **NOISE** | | | | | | | | |
| Voltage, $f_O$ = 10Hz | (1) | | 40 | | | 50 | | nV/√Hz |
| $f_O$ = 100Hz | (1) | | 15 | | | 18 | | nV/√Hz |
| $f_O$ = 1kHz | (1) | | 8 | | | 10 | | nV/√Hz |
| $f_O$ = 10kHz | (1) | | 6 | | | 7 | | nV/√Hz |
| $f_B$ = 10Hz to 10kHz | (1) | | 0.7 | | | 0.8 | | µVrms |
| $f_B$ = 0.1Hz to 10 Hz | (1) | | 1.6 | | | 2 | | µVp-p |
| Current, $f_B$ = 0.1Hz to 10Hz | (1) | | 15 | | | 21 | | fA, p-p |
| $f_O$ = 0.1Hz thru 20kHz | (1) | | 0.8 | | | 1.1 | | fA/√Hz |
| **OFFSET VOLTAGE**[2] | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0VDC | | ±0.5 | ±2 | | ±0.5 | ±3 | mV |
| Average Drift | $T_A = T_{MIN}$ to $T_{MAX}$ | | ±3 | ±10 | | ±3 | ±10 | µV/°C |
| Supply Rejection | | 86 | 104 | | 86 | 104 | | dB |
| | | | ±6 | ±50 | | ±6 | ±50 | µV/V |
| **BIAS CURRENT**[2] | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC<br>Device Operating | | ±1 | ±5 | | ±1 | ±10 | pA |
| **OFFSET CURRENT**[2] | | | | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC<br>Device Operating | | ±0.7 | ±4 | | ±0.7 | ±8 | pA |
| **IMPEDANCE** | | | | | | | | |
| Differential | | | $10^{13}$ ‖ 1 | | | $10^{13}$ ‖ 1 | | Ω ‖ pF |
| Common-Mode | | | $10^{14}$ ‖ 3 | | | $10^{14}$ ‖ 3 | | Ω ‖ pF |
| **VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | ±10 | ±11 | | ±10 | ±11 | | V |
| Common-Mode Rejection | $V_{IN}$ = ±10VDC | 86 | 104 | | 82 | 100 | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | |
| Open-Loop Voltage Gain | $R_L \geq 2k\Omega$ | 110 | 120 | | 106 | 114 | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Unity Gain, Small Signal | | | 2 | | | 2 | | MHz |
| Full Power Response | 20Vp-p, $R_L$ = 2kΩ | | 32 | | | 32 | | kHz |
| Slew Rate | $V_O$ = ±10V, $R_L$ = 2kΩ | | 2 | | | 2 | | V/µs |
| Settling Time, 0.1% | Gain = –1, $R_L$ = 2kΩ | | 6 | | | 6 | | µs |
| 0.01% | 10V Step | | 10 | | | 10 | | µs |
| Overload Recovery, 50% Overdrive[3] | Gain = –1 | | 5 | | | 5 | | µs |
| **RATED OUTPUT** | | | | | | | | |
| Voltage Output | $R_L$ = 2kΩ | ±11 | ±12 | | ±11 | ±12 | | V |
| Current Output | $V_O$ = ±10VDC | ±5.5 | ±10 | | ±5.5 | ±10 | | mA |
| Output Resistance | DC, Open Loop | | 100 | | | 100 | | Ω |
| Load Capacitance Stability | Gain = +1 | | 1000 | | | 1000 | | pF |
| Short Circuit Current | | 10 | 40 | | 10 | 40 | | mA |
| **POWER SUPPLY** | | | | | | | | |
| Rated Voltage | | | ±15 | | | ±15 | | VDC |
| Voltage Range, Derated Performance | | ±5 | | ±18 | ±5 | | ±18 | VDC |
| Current, Quiescent | $I_O$ = 0mADC | | 2.5 | 4 | | 2.5 | 4.5 | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | Ambient Temperature | 0 | | +70 | 0 | | +70 | °C |
| Operating | Ambient Temperature | –40 | | +85 | –25 | | +85 | °C |
| Storage | Ambient Temperature | –65 | | +150 | –55 | | +125 | °C |
| θ Junction-Ambient | | | 200 | | | 150[4] | | °C/W |

NOTES: (1) Sample tested. (2) Offset voltage, offset current, and bias current are specified with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) 100°C/W for KU grade.

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## ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC}$ = ±15VDC and $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA121KM | | | OPA121KP, KU | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification Range | Ambient Temperature | 0 | | +70 | 0 | | +70 | °C |
| **INPUT** | | | | | | | | |
| **OFFSET VOLTAGE**[1] | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0VDC | | ±1 | ±3 | | ±1 | ±5 | mV |
| Average Drift | | | ±3 | ±10 | | ±3 | ±10 | µV/°C |
| Supply Rejection | | 82 | 94 | | 82 | 94 | | dB |
| | | | ±20 | ±80 | | ±20 | ±80 | µV/V |
| **BIAS CURRENT**[1] | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC Device Operating | | ±23 | ±115 | | ±23 | ±250 | pA |
| **OFFSET CURRENT**[1] | | | | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC Device Operating | | ±16 | ±100 | | ±16 | ±200 | pA |
| **VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | ±10 | ±11 | | ±10 | ±11 | | V |
| Common-Mode Rejection | $V_{IN}$ = ±10VDC | 82 | 98 | | 80 | 96 | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | |
| Open-Loop Voltage Gain | $R_L \geq 2k\Omega$ | 106 | 116 | | 100 | 110 | | dB |
| **RATED OUTPUT** | | | | | | | | |
| Voltage Output | $R_L$ = 2kΩ | ±10.5 | ±11 | | ±10.5 | ±11 | | V |
| Current Output | $V_O$ = ±10VDC | ±5.25 | ±10 | | ±5.25 | ±10 | | mA |
| Short Circuit Current | $V_O$ = 0VDC | 10 | 40 | | 10 | 40 | | mA |
| **POWER SUPPLY** | | | | | | | | |
| Current, Quiescent | $I_O$ = 0mADC | | 2.5 | 4.5 | | 2.5 | 5 | mA |

NOTE: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

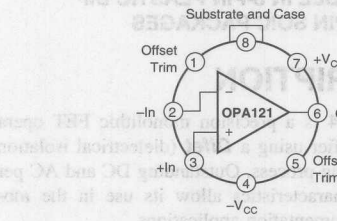
## ABSOLUTE MAXIMUM RATINGS

Supply ..... ±18VDC
Internal Power Dissipation[1] ..... 500mW
Differential Input Voltage ..... ±36VDC
Input Voltage Range ..... ±18VDC
Storage Temperature Range
M package ..... –65°C to +150°C
P, U packages ..... –55°C to +125°C
Operating Temperature Range
M package ..... –40°C to +85°C
P, U packages ..... –25°C to +85°C
Lead Temperature
M, P packages (soldering, 10s) ..... +300°C
U package (soldering, 3s) ..... +260°C
Output Short-Circuit Duration[2] ..... Continuous
Junction Temperature ..... +175°C

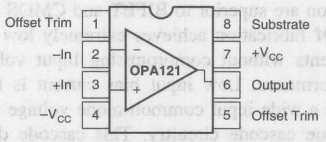
NOTES: (1) Packages must be derated based on $\theta_{JA}$ = 150°C/W (P package); $\theta_{JA}$ = 200°C/W (M package); $\theta_{JA}$ = 100°C/W (U package). (2) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and $T_J$.

## CONNECTION DIAGRAMS

**Top View** **M-Package** TO-99 (Hermetic)




**P-Package** Plastic Mini-DIP
**U-Package** Plastic SOIC




## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| OPA121KM | TO-99 | 001 | 0°C to +70°C |
| OPA121KP | 8-Pin Plastic DIP | 006 | 0°C to +70°C |
| OPA121KU | 8-Pin SOIC | 182 | 0°C to +70°C |

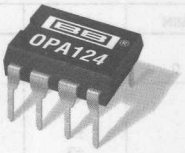
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# OPA124

www.burr-brown.com/databook/OPA124.html

# Low Noise Precision *Difet*® OPERATIONAL AMPLIFIER

## FEATURES

- LOW NOISE: 6nV/√Hz (10kHz)
- LOW BIAS CURRENT: 1pA max
- LOW OFFSET: 250µV max
- LOW DRIFT: 2µV/°C max
- HIGH OPEN-LOOP GAIN: 120dB min
- HIGH COMMON-MODE REJECTION: 100dB min
- AVAILABLE IN 8-PIN PLASTIC DIP AND 8-PIN SOIC PACKAGES

## APPLICATIONS

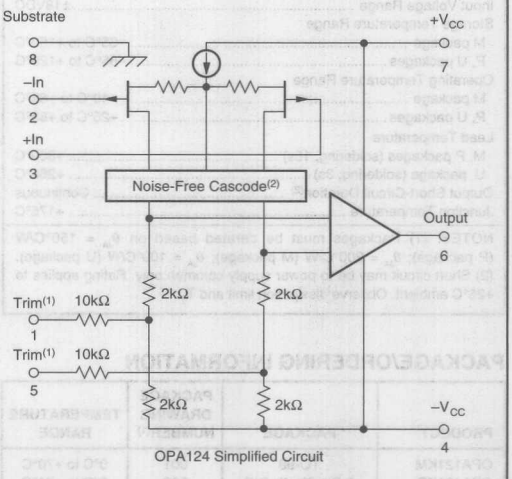
- PRECISION PHOTODIODE PREAMP
- MEDICAL EQUIPMENT
- OPTOELECTRONICS
- DATA ACQUISITION
- TEST EQUIPMENT

## DESCRIPTION

The OPA124 is a precision monolithic FET operational amplifier using a ***Difet*** (dielectrical isolation) manufacturing process. Outstanding DC and AC performance characteristics allow its use in the most critical instrumentation applications.

Bias current, noise, voltage offset, drift, open-loop gain, common-mode rejection and power supply rejection are superior to BIFET and CMOS amplifiers. ***Difet*** fabrication achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry. This cascode design also allows high precision input specifications and reduced susceptibility to flicker noise. Laser trimming of thin-film resistors gives very low offset and drift.

Compared to the popular OPA111, the OPA124 gives comparable performance and is available in an 8-pin PDIP and 8-pin SOIC package.




OPA124 Simplified Circuit

NOTES: (1) Omitted on SOIC. (2) Patented.

BIFET® National Semiconductor Corp.,
***Difet***® Burr-Brown Corp.

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# SPECIFICATIONS

## ELECTRICAL

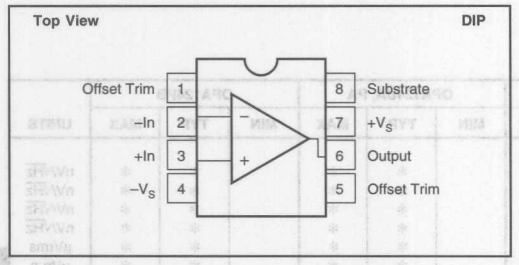
At $V_{CC}$ = ±15VDC and $T_A$ = +25°C, unless otherwise noted.

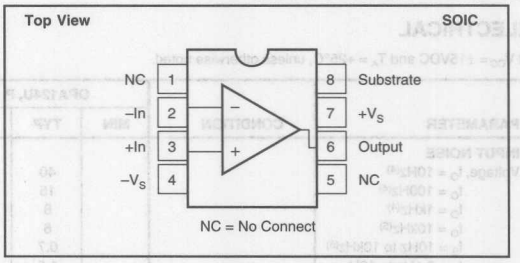
| PARAMETER | CONDITION | OPA124U, P | | | OPA124UA, PA | | | OPA124PB | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT NOISE** | | | | | | | | | | | |
| Voltage, $f_O$ = 10Hz[4] | | | 40 | 80 | | * | * | | * | * | nV/√Hz |
| $f_O$ = 100Hz[4] | | | 15 | 40 | | * | * | | * | * | nV/√Hz |
| $f_O$ = 1kHz[4] | | | 8 | 15 | | * | * | | * | * | nV/√Hz |
| $f_O$ = 10kHz[5] | | | 6 | 8 | | * | * | | * | * | nV/√Hz |
| $f_B$ = 10Hz to 10kHz[5] | | | 0.7 | 1.2 | | * | * | | * | * | µVrms |
| $f_B$ = 0.1Hz to 10Hz | | | 1.6 | 3.3 | | * | * | | * | * | µVp-p |
| Current, $f_B$ = 0.1Hz to 10Hz | | | 9.5 | 15 | | * | * | | * | * | fAp-p |
| $f_O$ = 0.1Hz thru 20kHz | | | 0.5 | 0.8 | | * | * | | * | * | fA/√Hz |
| **OFFSET VOLTAGE**[1] | | | | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0VDC | | ±200 | ±800 | | ±150 | ±500 | | ±100 | ±250 | µV |
| vs Temperature | $T_A = T_{MIN}$ to $T_{MAX}$ | | ±4 | ±7.5 | | ±2 | ±4 | | ±1 | ±2 | µV/°C |
| Supply Rejection | $V_{CC}$ = ±10V to ±18V | 88 | 110 | | 90 | * | | 100 | * | | dB |
| vs Temperature | $T_A = T_{MIN}$ to $T_{MAX}$ | 84 | 100 | | 86 | * | | 90 | * | | dB |
| **BIAS CURRENT**[1] | | | | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC | | ±1 | ±5 | | ±0.5 | ±2 | | ±0.35 | ±1 | pA |
| **OFFSET CURRENT**[1] | | | | | | | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC | | ±1 | ±5 | | ±0.5 | ±1 | | ±0.25 | ±0.5 | pA |
| **IMPEDANCE** | | | | | | | | | | | |
| Differential | | | $10^{13}$ \|\| 1 | | | * | | | * | | Ω \|\| pF |
| Common-Mode | | | $10^{14}$ \|\| 3 | | | * | | | * | | Ω \|\| pF |
| **VOLTAGE RANGE** | | | | | | | | | | | |
| Common-Mode Input Range | | ±10 | ±11 | | * | * | | * | * | | V |
| Common-Mode Rejection | $V_{IN}$ = ±10VDC | 92 | 110 | | 94 | * | | 100 | * | | dB |
| vs Temperature | $T_A = T_{MIN}$ to $T_{MAX}$ | 86 | 100 | | * | * | | 90 | * | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | | | | |
| Open-Loop Voltage Gain | $R_L$ ≥ 2kΩ | 106 | 125 | | * | * | | 120 | * | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | | | | |
| Unity Gain, Small Signal | | | 1.5 | | | * | | | * | | MHz |
| Full Power Response | 20Vp-p, $R_L$ = 2kΩ | 16 | 32 | | * | * | | * | * | | kHz |
| Slew Rate | $V_O$ = ±10V, $R_L$ = 2kΩ | 1 | 1.6 | | * | * | | * | * | | V/µs |
| THD | | | 0.0003 | | | * | | | * | | % |
| Settling Time, 0.1% | Gain = –1, $R_L$ = 2kΩ | | 6 | | | * | | | * | | µs |
| 0.01% | 10V Step | | 10 | | | * | | | * | | µs |
| Overload Recovery, 50% Overdrive[2] | Gain = –1 | | 5 | | | * | | | * | | µs |
| **RATED OUTPUT** | | | | | | | | | | | |
| Voltage Output | $R_L$ = 2kΩ | ±11 | ±12 | | * | * | | * | * | | V |
| Current Output | $V_O$ = ±10VDC | ±5.5 | ±10 | | * | * | | * | * | | mA |
| Output Resistance | DC, Open Loop | | 100 | | | * | | | * | | Ω |
| Load Capacitance Stability | Gain = +1 | | 1000 | | | * | | | * | | pF |
| Short Circuit Current | | 10 | 40 | | * | * | | * | * | | mA |
| **POWER SUPPLY** | | | | | | | | | | | |
| Rated Voltage | | | ±15 | | | * | | | * | | VDC |
| Voltage Range, Derated | | ±5 | | ±18 | * | | * | * | | * | VDC |
| Current, Quiescent | $I_O$ = 0mADC | | 2.5 | 3.5 | | * | * | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification | $T_{MIN}$ and $T_{MAX}$ | –25 | | +85 | * | | * | * | | * | °C |
| Storage | | –65 | | +125 | * | | * | * | | * | °C |
| θ Junction-Ambient: PDIP | | | 90 | | | * | | | * | | °C/W |
| SOIC | | | 100 | | | * | | | * | | °C/W |

* Specification same as OPA124U, P

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up. For performance at other temperatures see Typical Performance Curves. (2) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (3) For performance at other temperatures see Typical Performance Curves. (4) Sample tested, 98% confidence. (5) Guaranteed by design.

## CONNECTION DIAGRAMS




## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE | BIAS CURRENT pA, max | OFFSET DRIFT µV/°C, max |
|---|---|---|---|---|---|
| OPA124U | 8-Lead SOIC | 182 | –25°C to +85°C | 5 | 7.5 |
| OPA124P | 8-Pin Plastic DIP | 006 | –25°C to +85°C | 5 | 7.5 |
| OPA124UA | 8-Lead SOIC | 182 | –25°C to +85°C | 2 | 4 |
| OPA124PA | 8-Pin Plastic DIP | 006 | –25°C to +85°C | 2 | 4 |
| OPA124PB | 8-Pin Plastic DIP | 006 | –25°C to +85°C | 1 | 2 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Supply | ±18VDC |
| Internal Power Dissipation[2] | 750mW |
| Differential Input Voltage[3] | ±36VDC |
| Input Voltage Range[3] | ±18VDC |
| Storage Temperature Range | –65°C to +150°C |
| Operating Temperature Range | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short Circuit Duration[4] | Continuous |
| Junction Temperature | +175°C |

NOTES: (1) Stresses above these ratings may cause permanent damage. (2) Packages must be derated based on $\theta_{JA}$ = 90°C/W for PDIP and 100°C/W for SOIC. (3) For supply voltages less than ±18VDC, the absolute maximum input voltage is equal to +18V > $V_{IN}$ > $-V_{CC}$ – 6V. See Figure 2. (4) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and $T_J$.

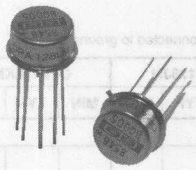
## ELECTROSTATIC DISCHARGE SENSITIVITY

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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BURR-BROWN®



# OPA128

www.burr-brown.com/databook/OPA128.html

# *Difet*® Electrometer-Grade OPERATIONAL AMPLIFIER

## FEATURES

- ULTRA-LOW BIAS CURRENT: 75fA max
- LOW OFFSET: 500μV max
- LOW DRIFT: 5μV/°C max
- HIGH OPEN-LOOP GAIN: 110dB min
- HIGH COMMON-MODE REJECTION: 90dB min
- IMPROVED REPLACEMENT FOR AD515 AND AD549

## APPLICATIONS

- ELECTROMETER
- MASS SPECTROMETER
- CHROMATOGRAPH
- ION GAUGE
- PHOTODETECTOR
- RADIATION-HARD EQUIPMENT

## DESCRIPTION

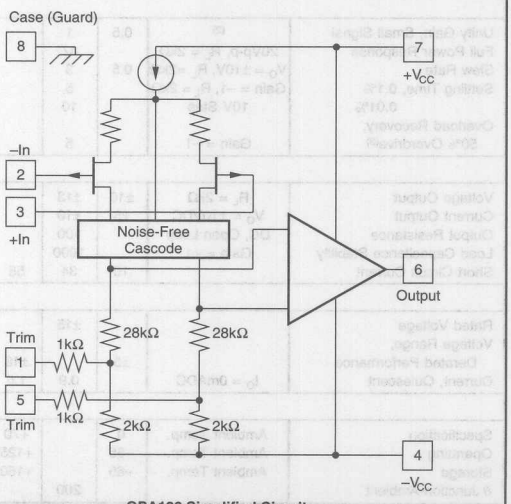
The OPA128 is an ultra-low bias current monolithic operational amplifier. Using advanced geometry dielectrically-isolated FET (***Difet***®) inputs, this monolithic amplifier achieves a performance level exceeding even the best hybrid electrometer amplifiers.

Laser-trimmed thin-film resistors give outstanding voltage offset and drift performance.

A noise-free cascode and low-noise processing give the OPA128 excellent low-level signal handling capabilities. Flicker noise is very low.

The OPA128 is an improved pin-for-pin replacement for the AD515.

***Difet***® Burr-Brown Corp.




OPA128 Simplified Circuit

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $V_{CC}$ = ±15VDC and $T_A$ = +25°C, unless otherwise noted. Pin 8 connected to ground.

| PARAMETER | CONDITIONS | OPA128JM | | | OPA128KM | | | OPA128LM | | | OPA128SM | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **BIAS CURRENT**[1] | | | | | | | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC, $R_L \geq 10k\Omega$ | | ±150 | ±300 | | ±75 | ±150 | | ±40 | ±75 | | ±75 | ±150 | fA |
| **OFFSET CURRENT**[1] | | | | | | | | | | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC, $R_L \geq 10k\Omega$ | | 65 | | | 30 | | | 30 | | | 30 | | fA |
| **OFFSET VOLTAGE**[1] | | | | | | | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0VDC | | ±260 | ±1000 | | ±140 | ±500 | | ±140 | ±500 | | ±140 | ±500 | µV |
| Average Drift | $T_A = T_{MIN}$ to $T_{MAX}$ | | | ±20 | | | ±10 | | | ±5 | | | ±10 | µV/°C |
| Supply Rejection | | 80 | 120 | | 90 | 120 | | 90 | 120 | | 90 | 120 | | dB |
| | | | ±1 | ±100 | | ±1 | ±32 | | ±1 | ±32 | | ±1 | ±32 | µV/V |
| **NOISE** | | | | | | | | | | | | | | |
| Voltage: $f_O$ = 10Hz | | | 92 | | | 92 | | | 92 | | | 92 | | nV/√Hz |
| $f_O$ = 100Hz | | | 78 | | | 78 | | | 78 | | | 78 | | nV/√Hz |
| $f_O$ = 1kHz | | | 27 | | | 27 | | | 27 | | | 27 | | nV/√Hz |
| $f_O$ = 10kHz | | | 15 | | | 15 | | | 15 | | | 15 | | nV/√Hz |
| $f_B$ = 10Hz to 10kHz | | | 2.4 | | | 2.4 | | | 2.4 | | | 2.4 | | µVrms |
| $f_B$ = 0.1Hz to 10Hz | | | 4 | | | 4 | | | 4 | | | 4 | | µVp-p |
| Current: $f_B$ = 0.1Hz to 10Hz | | | 4.2 | | | 3 | | | 2.3 | | | 3 | | fA, p-p |
| $f_O$ = 0.1Hz to 20kHz | | | 0.22 | | | 0.16 | | | 0.12 | | | 0.16 | | fA/√Hz |
| **IMPEDANCE** | | | | | | | | | | | | | | |
| Differential | | | $10^{13}$ \|\| 1 | | | $10^{13}$ \|\| 1 | | | $10^{13}$ \|\| 1 | | | $10^{13}$ \|\| 1 | | Ω \|\| pF |
| Common-Mode | | | $10^{15}$ \|\| 2 | | | $10^{15}$ \|\| 2 | | | $10^{15}$ \|\| 2 | | | $10^{15}$ \|\| 2 | | Ω \|\| pF |
| **VOLTAGE RANGE**[4] | | | | | | | | | | | | | | |
| Common-Mode Input Range | | ±10 | ±12 | | ±10 | ±12 | | ±10 | ±12 | | ±10 | ±12 | | V |
| Common-Mode Rejection | $V_{IN}$ = ±10VDC | 80 | 118 | | 90 | 118 | | 90 | 118 | | 90 | 118 | | dB |
| Open-Loop Voltage Gain | $R_L \geq 2k\Omega$ | 94 | 128 | | 110 | 128 | | 110 | 128 | | 110 | 128 | | dB |
| Unity Gain, Small Signal | [2] | 0.5 | 1 | | 0.5 | 1 | | 0.5 | 1 | | 0.5 | 1 | | MHz |
| Full Power Response | 20Vp-p, $R_L$ = 2kΩ | | 47 | | | 47 | | | 47 | | | 47 | | kHz |
| Slew Rate | $V_O$ = ±10V, $R_L$ = 2kΩ | 0.5 | 3 | | 1 | 3 | | 1 | 3 | | 1 | 3 | | V/µs |
| Settling Time, 0.1% | Gain = –1, $R_L$ = 2kΩ | | 5 | | | 5 | | | 5 | | | 5 | | µs |
| 0.01% | 10V Step | | 10 | | | 10 | | | 10 | | | 10 | | µs |
| Overload Recovery, 50% Overdrive[3] | Gain = –1 | | 5 | | | 5 | | | 5 | | | 5 | | µs |
| Voltage Output | $R_L$ = 2kΩ | ±10 | ±13 | | ±10 | ±13 | | ±10 | ±13 | | ±10 | ±13 | | V |
| Current Output | $V_O$ = ±10VDC | ±5 | ±10 | | ±5 | ±10 | | ±5 | ±10 | | ±5 | ±10 | | mA |
| Output Resistance | DC, Open Loop | | 100 | | | 100 | | | 100 | | | 100 | | Ω |
| Load Capacitance Stability | Gain = +1 | | 1000 | | | 1000 | | | 1000 | | | 1000 | | pF |
| Short Circuit Current | | 10 | 34 | 55 | 10 | 34 | 55 | 10 | 34 | 55 | 10 | 34 | 55 | mA |
| Rated Voltage | | | ±15 | | | ±15 | | | ±15 | | | ±15 | | VDC |
| Voltage Range, Derated Performance | | ±5 | | ±18 | ±5 | | ±18 | ±5 | | ±18 | ±5 | | ±18 | VDC |
| Current, Quiescent | $I_O$ = 0mADC | | 0.9 | 1.5 | | 0.9 | 1.5 | | 0.9 | 1.5 | | 0.9 | 1.5 | mA |
| Specification | Ambient Temp. | 0 | | +70 | 0 | | +70 | 0 | | +70 | –55 | | +125 | °C |
| Operating | Ambient Temp. | –55 | | +125 | –55 | | +125 | –55 | | +125 | –55 | | +125 | °C |
| Storage | Ambient Temp. | –65 | | +150 | –65 | | +150 | –65 | | +150 | –65 | | +150 | °C |
| θ Junction-Ambient | | | 200 | | | 200 | | | 200 | | | 200 | | °C/W |

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up. Bias current doubles approximately every 11°C. (2) Sample tested. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can withstand overload currents of 0.3mA indefinitely without damage.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

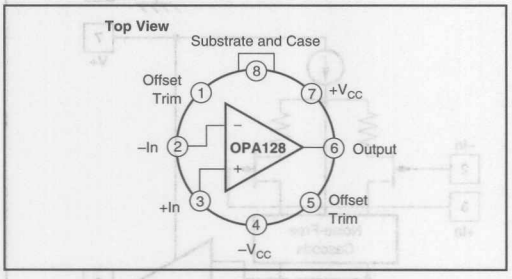
## ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC}$ = ±15VDC and $T_A = T_{MIN}$ and $T_{MAX}$, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA128JM | | | OPA128KM | | | OPA128LM | | | OPA128SM | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **TEMPERATURE RANGE** | | | | | | | | | | | | | | |
| Specification Range | Ambient Temp. | 0 | | +70 | 0 | | +70 | 0 | | +70 | –55 | | +125 | °C |
| **INPUT** | | | | | | | | | | | | | | |
| **BIAS CURRENT**[1] | | | | | | | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC | | ±2.5 | ±8 | | ±1.3 | ±4 | | ±0.7 | ±2 | | ±43 | ±170 | pA |
| **OFFSET CURRENT**[1] | | | | | | | | | | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC | | 1.1 | | | 0.6 | | | 0.6 | | | 18 | | pA |
| **OFFSET VOLTAGE**[1] | | | | | | | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0VDC | | | ±2.2mV | | | ±1mV | | | ±750 | | | ±1.5mV | µV |
| Average Drift | | | | ±20 | | | ±10 | | | ±5 | | | ±10 | µV/°C |
| Supply Rejection | | 74 | 114 | | 80 | 114 | | 80 | 114 | | 80 | 106 | | dB |
| | | | ±2 | ±200 | | ±2 | ±100 | | ±2 | ±100 | | ±5 | ±100 | µV/V |
| **VOLTAGE RANGE**[2] | | | | | | | | | | | | | | |
| Common-Mode Input Range | | ±10 | ±11 | | ±10 | ±11 | | ±10 | ±11 | | ±10 | ±11 | | V |
| Commmon-Mode Rejection | $V_{IN}$ = ±10VDC | 74 | 112 | | 80 | 112 | | 80 | 112 | | 74 | 104 | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | | | | | | | |
| Open-Loop Voltage Gain | $R_L \geq 2k\Omega$ | 90 | 125 | | 104 | 125 | | 104 | 125 | | 90 | 122 | | dB |
| **RATED OUTPUT** | | | | | | | | | | | | | | |
| Voltage Output | $R_L$ = 2k | ±10 | | | ±10 | | | ±10 | | | ±10 | | | V |
| Current Output | $V_O$ = ±10VDC | ±5 | | | ±5 | | | ±5 | | | ±5 | | | mA |
| Short Circuit Current | $V_O$ = 0VDC | 10 | 22 | | 10 | 22 | | 10 | 22 | | 10 | 18 | | mA |
| **POWER SUPPLY** | | | | | | | | | | | | | | |
| Current, Quiescent | I = 0mADC | | 0.9 | 1.8 | | 0.9 | 1.8 | | 0.9 | 1.8 | | 0.9 | 2 | mA |

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (2) If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can withstand overload currents of 0.3mA indefinitely without damage.

## CONNECTION DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply | ±18VDC |
| Internal Power Dissipation[1] | 500mW |
| Differential Input Voltage | ±36VDC |
| Input Voltage Range | ±18VDC |
| Storage Temperature Range | –65°C to +150°C |
| Operating Temperature Range | –55°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short Circuit Duration[2] | Continuous |
| Junction Temperature | +175°C |

NOTES: (1) Packages must be derated based on $\theta_{CA}$ = 150°C/W or $\theta_{JA}$ = 200°C/W. (2) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and $T_J$.

## ORDERING INFORMATION

| PRODUCT | PACKAGE | TEMPERATURE RANGE | BIAS CURRENT, max (fA) |
|---|---|---|---|
| OPA128JM | TO-99 | 0°C to +70°C | ±300 |
| OPA128KM | TO-99 | 0°C to +70°C | ±150 |
| OPA128LM | TO-99 | 0°C to +70°C | ±75 |
| OPA128SM | TO-99 | –55°C to +125°C | ±150 |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| OPA128JM | TO-99 | 001 |
| OPA128KM | TO-99 | 001 |
| OPA128LM | TO-99 | 001 |
| OPA128SM | TO-99 | 001 |

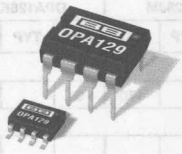
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®




# OPA129

www.burr-brown.com/databook/OPA129.html

# Ultra-Low Bias Current *Difet*® OPERATIONAL AMPLIFIER

## FEATURES

- ULTRA-LOW BIAS CURRENT: 100fA max
- LOW OFFSET: 2mV max
- LOW DRIFT: 10µV/°C max
- HIGH OPEN-LOOP GAIN: 94dB min
- LOW NOISE: 15nV/√Hz at 10kHz
- PLASTIC DIP and SOIC PACKAGE

## APPLICATIONS

- PHOTODETECTOR PREAMP
- CHROMATOGRAPHY
- ELECTROMETER AMPLIFIERS
- MASS SPECTROMETER
- pH PROBE AMPLIFIER
- ION GAGE MEASUREMENT

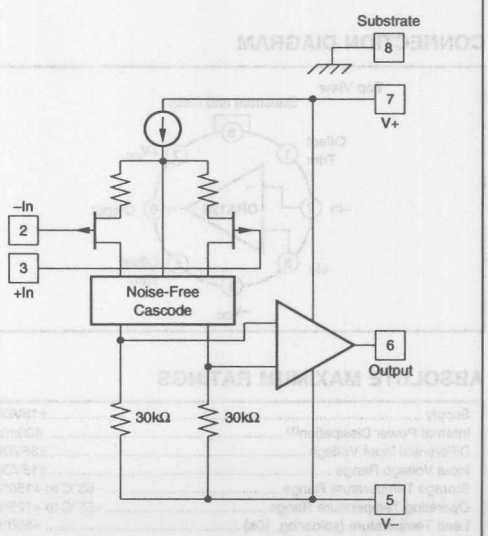
## DESCRIPTION

The OPA129 is an ultra-low bias current monolithic operational amplifier offered in an 8-pin PDIP and SO-8 package. Using advanced geometry dielectrically-isolated FET (***Difet***®) inputs, this monolithic amplifier achieves a high performance level.

***Difet*** fabrication eliminates isolation-junction leakage current—the main contributor to input bias current with conventional monolithic FETs. This reduces input bias current by a factor of 10 to 100. Very low input bias current can be achieved without resorting to small-geometry FETs or CMOS designs which can suffer from much larger offset voltage, voltage noise, drift, and poor power supply rejection.

The OPA129's special pinout eliminates leakage current that occurs with other op amps. Pins 1 and 4 have no internal connection, allowing circuit board guard traces—even with the surface-mount package version.

OPA129 is available in 8-pin DIP and SO-8 packages, specified for operation from –40°C to +85°C.




Simplified Circuit

*Difet*® Burr-Brown Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
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# SPECIFICATIONS

## ELECTRICAL

At $V_S$ = ±15V and $T_A$ = +25°C, unless otherwise noted. Pin 8 connected to ground.

| PARAMETER | CONDITION | OPA129PB, UB MIN | OPA129PB, UB TYP | OPA129PB, UB MAX | OPA129P, U MIN | OPA129P, U TYP | OPA129P, U MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **INPUT BIAS CURRENT**[1] | $V_{CM}$ = 0V | | ±30 | ±100 | | * | ±250 | fA |
| vs Temperature | Doubles every 10°C | | | | | * | | |
| **INPUT OFFSET CURRENT** | $V_{CM}$ = 0V | | ±30 | | | * | | fA |
| **OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0V | | ±0.5 | ±2 | | ±1 | ±5 | mV |
| vs Temperature | | | ±3 | ±10 | | ±5 | | µV/°C |
| Supply Rejection | $V_S$ = ±5V to ±18V | | ±3 | ±100 | | * | * | µV/V |
| **NOISE** | | | | | | | | |
| Voltage | f = 10Hz | | 85 | | | * | | nV/√Hz |
| | f = 100Hz | | 28 | | | * | | nV/√Hz |
| | f = 1kHz | | 17 | | | * | | nV/√Hz |
| | f = 10kHz | | 15 | | | * | | nV/√Hz |
| | $f_B$ = 0.1Hz to 10Hz | | 4 | | | * | | µVp-p |
| Current | f = 10kHz | | 0.1 | | | * | | fA/√Hz |
| **INPUT IMPEDANCE** | | | | | | | | |
| Differential | | | $10^{13}$ \|\| 1 | | | * | | Ω \|\| pF |
| Common-Mode | | | $10^{15}$ \|\| 2 | | | * | | Ω \|\| pF |
| **VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | ±10 | ±12 | | * | * | | V |
| Common-Mode Rejection | $V_{IN}$ = ±10V | 80 | 118 | | * | * | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | |
| Open-Loop Voltage Gain | $R_L$ ≥ 2kΩ | 94 | 120 | | * | * | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Unity Gain, Small Signal | | | 1 | | | * | | MHz |
| Full Power Response | 20Vp-p, $R_L$ = 2kΩ | | 47 | | | * | | kHz |
| Slew Rate | $V_O$ = ±10V, $R_L$ = 2kΩ | 1 | 2.5 | | * | * | | V/µs |
| Settling Time: | G = –1, $R_L$ = 2kΩ, 10V Step | | | | | | | |
| 0.1% | | | 5 | | | * | | µs |
| 0.01% | | | 10 | | | * | | µs |
| Overload Recovery, 50% Overdrive[2] | G = –1 | | 5 | | | * | | µs |
| **RATED OUTPUT** | | | | | | | | |
| Voltage Output | $R_L$ = 2kΩ | ±12 | ±13 | | * | * | | V |
| Current Output | $V_O$ = ±12V | ±6 | ±10 | | * | * | | mA |
| Load Capacitance Stability | Gain = +1 | | 1000 | | | * | | pF |
| Short-Circuit Current | | | ±35 | ±55 | | * | * | mA |
| **POWER SUPPLY** | | | | | | | | |
| Rated Voltage | | | ±15 | | | * | | V |
| Voltage Range, Derated Performance | | ±5 | | ±18 | * | | * | V |
| Current, Quiescent | $I_O$ = 0mA | | 1.2 | 1.8 | | * | * | mA |
| **TEMPERATURE** | | | | | | | | |
| Specification | Ambient Temperature | –40 | | +85 | * | | * | °C |
| Operating | Ambient Temperature | –40 | | +125 | * | | * | °C |
| Storage | | –40 | | +125 | * | | * | °C |
| Thermal Resistance | $\theta_{JA}$, Junction-to-Ambient | | | | | | | |
| PDIP—"P" | | | 90 | | | * | | °C/W |
| SOIC—"U" | | | 100 | | | * | | °C/W |

* Specification same as OPA129PB, UB.

NOTES: (1) High-speed automated test. (2) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.

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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | ±18V |
| Differential Input Voltage | V– to V+ |
| Input Voltage Range | V– to V+ |
| Storage Temperature Range | –40°C to +125°C |
| Operating Temperature Range | –40°C to +125°C |
| Lead Temperature (soldering, 10s; SOIC 3s) | +300°C |
| Output Short Circuit Duration[1] | Continuous |
| Junction Temperature ($T_J$) | +150°C |

NOTE: (1) Short circuit may be to power supply common at +25°C ambient.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

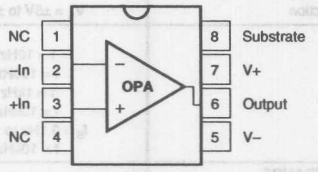
## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| OPA129P | 8-Pin Plastic DIP | 006 |
| OPA129PB | 8-Pin Plastic DIP | 006 |
| OPA129U | 8-Lead SOIC | 182 |
| OPA129UB | 8-Lead SOIC | 182 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

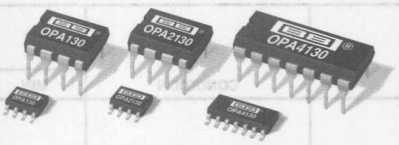
## CONNECTION DIAGRAM

Top View — DIP/SOIC




NC: No internal connection.

BURR-BROWN®




# OPA130
# OPA2130
# OPA4130

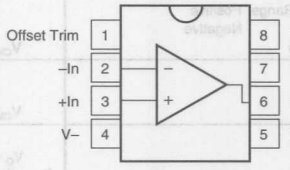
www.burr-brown.com/databook/OPA130.html

# Low Power, Precision FET-INPUT OPERATIONAL AMPLIFIERS

## FEATURES

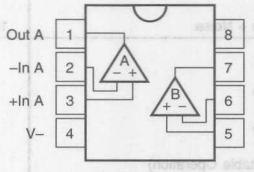
- LOW QUIESCENT CURRENT: 530μA/amp
- LOW OFFSET VOLTAGE: 1mV max
- HIGH OPEN-LOOP GAIN: 120dB min
- HIGH CMRR: 90dB min
- FET INPUT: $I_B$ = 20pA max
- EXCELLENT BANDWIDTH: 1MHz
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- SINGLE, DUAL, AND QUAD VERSIONS

OPA130



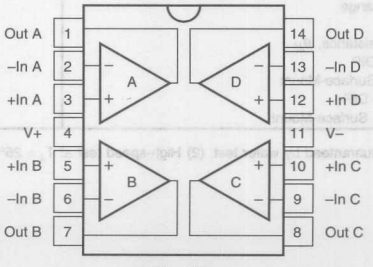

8-Pin DIP, SO-8

OPA2130




8-Pin DIP, SO-8

OPA4130




14-Pin DIP
SO-14

## DESCRIPTION

The OPA130 series of FET-input op amps combine precision dc performance with low quiescent current. Single, dual, and quad versions have identical specifications for maximum design flexibility. They are ideal for general-purpose, portable, and battery operated applications, especially with high source impedance.

OPA130 op amps are easy to use and free from phase inversion and overload problems often found in common FET-input op amps. Input cascode circuitry provides excellent common-mode rejection and maintains low input bias current over its wide input voltage range. OPA130 series op amps are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions, including high load capacitance. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Single and dual versions are available in 8-pin DIP and SO-8 surface-mount packages. Quad is available in 14-pin DIP and SO-14 surface-mount packages. All are specified for –40°C to +85°C operation.

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| PARAMETER | CONDITION | OPA130PA, UA OPA2130PA, UA OPA4130PA, UA MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | | | ±0.2 | ±1 | mV |
| vs Temperature[1] | Operating Temperature Range | | ±2 | ±10 | µV/°C |
| vs Power Supply | $V_S$ = ±2.25V to ±18V | | 2 | 20 | µV/V |
| Channel Separation (dual and quad) | | | 0.3 | | µV/V |
| **INPUT BIAS CURRENT**[2] | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | +5 | ±20 | pA |
| vs Temperature | | | See Typical Curve | | |
| Input Offset Current | $V_{CM}$ = 0V | | ±2 | ±20 | pA |
| **NOISE** | | | | | |
| Input Voltage Noise | | | | | |
| Noise Density, f = 10Hz | | | 30 | | nV/√Hz |
| f = 100Hz | | | 18 | | nV/√Hz |
| f = 1kHz | | | 16 | | nV/√Hz |
| f = 10kHz | | | 16 | | nV/√Hz |
| Current Noise Density, f = 1kHz | | | 4 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Voltage Range, Positive | | (V+)–2 | (V+)–1.5 | | V |
| Negative | | (V–)+2 | (V–)+1.2 | | V |
| Common-Mode Rejection | $V_{CM}$ = –13V to +13V | 90 | 105 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $10^{13}$ \|\| 1 | | Ω \|\| pF |
| Common-Mode | $V_{CM}$ = –13V to +13V | | $10^{13}$ \|\| 3 | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-loop Voltage Gain | $V_O$ = –13.8V to +13V | 120 | 135 | | dB |
| | $R_L$ = 2kΩ, $V_O$ = –13V to +12V | 120 | 135 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product | | | 1 | | MHz |
| Slew Rate | | | 2 | | V/µs |
| Settling Time: 0.1% | G = 1, 10V Step, $C_L$ = 100pF | | 5.5 | | µs |
| 0.01% | G = 1, 10V Step, $C_L$ = 100pF | | 7 | | µs |
| Overload Recovery Time | G = 1, $V_{IN}$ = ±15V | | 2 | | µs |
| Total Harmonic Distortion + Noise | 1kHz, G = 1, $V_O$ = 3.5Vrms | | 0.0003 | | % |
| **OUTPUT** | | | | | |
| Voltage Output, Positive | | (V+)–2 | (V+)–1.5 | | V |
| Negative | | (V–)+1.2 | (V–)+1 | | V |
| Positive | $R_L$ = 2kΩ | (V+)–3 | (V+)–2.5 | | V |
| Negative | $R_L$ = 2kΩ | (V–)+2 | (V–)+1.5 | | V |
| Short-Circuit Current | | | ±18 | | mA |
| Capacitive Load Drive (Stable Operation) | | | 10 | | nF |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±15 | | V |
| Operating Voltage Range | | ±2.25 | | ±18 | V |
| Quiescent Current (per amplifier) | $I_O$ = 0 | | ±530 | ±650 | µA |
| **TEMPERATURE RANGE** | | | | | |
| Operating Range | | –40 | | +85 | °C |
| Storage | | –40 | | +125 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| 8-Pin DIP | | | 100 | | °C/W |
| SO-8 Surface-Mount | | | 150 | | °C/W |
| 14-Pin DIP | | | 80 | | °C/W |
| SO-14 Surface-Mount | | | 110 | | °C/W |

NOTES: (1) Guaranteed by wafer test. (2) High-speed test at $T_J$ = 25°C.

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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, V+ to V– | 36V |
| Input Voltage | (V–) –0.7V to (V+) +0.7V |
| Output Short-Circuit[1] | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering, 10s) | 300°C |

NOTE: (1) Short-circuit to ground, one amplifier per package.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| **Single** | | |
| OPA130PA | 8-Pin Plastic DIP | 006 |
| OPA130UA | SO-8 Surface-Mount | 182 |
| **Dual** | | |
| OPA2130PA | 8-Pin Plastic DIP | 006 |
| OPA2130UA | SO-8 Surface-Mount | 182 |
| **Quad** | | |
| OPA4130PA | 14-Pin Plastic DIP | 010 |
| OPA4130UA | SO-14 Surface-Mount | 235 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

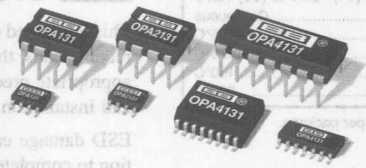
| PRODUCT | PACKAGE | TEMPERATURE RANGE |
|---|---|---|
| **Single** | | |
| OPA130PA | 8-Pin Plastic DIP | –40°C to +85°C |
| OPA130UA | SO-8 Surface-Mount | –40°C to +85°C |
| **Dual** | | |
| OPA2130PA | 8-Pin Plastic DIP | –40°C to +85°C |
| OPA2130UA | SO-8 Surface-Mount | –40°C to +85°C |
| **Quad** | | |
| OPA4130PA | 14-Pin Plastic DIP | –40°C to +85°C |
| OPA4130UA | SO-14 Surface-Mount | –40°C to +85°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# OPA131
# OPA2131
# OPA4131

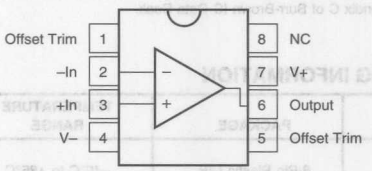
www.burr-brown.com/databook/OPA131.html

# General Purpose FET-INPUT OPERATIONAL AMPLIFIERS

## FEATURES

- FET INPUT: $I_B$ = 50pA max
- LOW OFFSET VOLTAGE: 750µV max
- WIDE SUPPLY RANGE: ±4.5V to ±18V
- SLEW RATE: 10V/µs
- WIDE BANDWIDTH: 4MHz
- EXCELLENT CAPACITIVE LOAD DRIVE
- SINGLE, DUAL, QUAD VERSIONS

OPA131




8-Pin DIP, SO-8

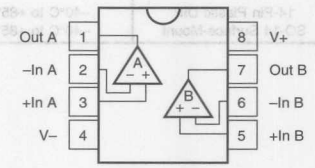
## DESCRIPTION

The OPA131 series of FET-input op amps provides high performance at low cost. Single, dual and quad versions in industry-standard pinouts allow cost-effective design options.

The OPA131 series offers excellent general purpose performance, including low offset voltage, drift, and good dynamic characteristics.

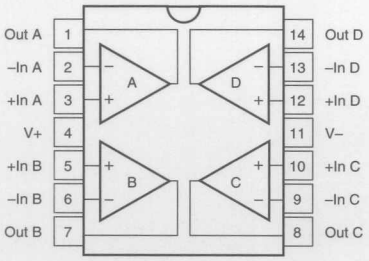
Single, dual and quad versions are available in DIP and SOIC packages. Performance grades include commercial and industrial temperature ranges.

OPA2131



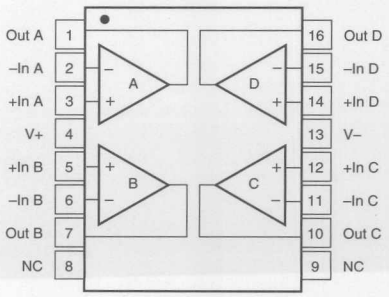

8-Pin DIP, SO-8

OPA4131




14-Pin DIP
SO-14

OPA4131




SOL-16

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# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = ±15V, and $R_L$ = 2kΩ, unless otherwise noted.

| PARAMETER | CONDITION | OPA131PA, UA OPA2131PA, UA OPA4131PA, UA, NA | | | OPA131PJ, UJ OPA2131PJ, UJ OPA4131PJ, NJ | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | | | ±0.2 | ±1 | | * | ±1.5 | mV |
| OPA131P, U models only | | | ±0.2 | 0.75 | | | | mV |
| vs Temperature[1] | Operating Temperature Range | | ±2 | ±10 | | * | * | µV/°C |
| vs Power Supply | $V_S$ = ±4.5V to ±18V | | 50 | 200 | | * | * | µV/V |
| OPA131P, U models only | | | 50 | 100 | | | | µV/V |
| **INPUT BIAS CURRENT[2]** | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | +5 | ±50 | | * | * | pA |
| vs Temperature | | | See Typical Curve | | | * | | |
| Input Offset Current | $V_{CM}$ = 0V | | ±1 | ±50 | | * | * | pA |
| **NOISE** | | | | | | | | |
| Input Voltage Noise | | | | | | | | |
| Noise Density, f = 10Hz | | | 21 | | | * | | nV/√Hz |
| f = 100Hz | | | 16 | | | * | | nV/√Hz |
| f = 1kHz | | | 15 | | | * | | nV/√Hz |
| f = 10kHz | | | 15 | | | * | | nV/√Hz |
| Current Noise Density, f = 1kHz | | | 3 | | | * | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Voltage Range | | (V–)+3 | | (V+)–1 | * | | * | V |
| Common-Mode Rejection | $V_{CM}$ = –12V to +14V | 70 | 80 | | * | * | | dB |
| OPA131P, U models only | | 80 | 86 | | | | | dB |
| **INPUT IMPEDANCE** | | | | | | | | |
| Differential | | | $10^{10}$ \|\| 1 | | | * | | Ω \|\| pF |
| Common-Mode | $V_{CM}$ = 0V | | $10^{12}$ \|\| 3 | | | * | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | | | | |
| Open-Loop Voltage Gain | $V_O$ = –12V to +12V | 94 | 110 | | * | * | | dB |
| OPA131P, U models only | | 100 | 110 | | | | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Gain-Bandwidth Product | | | 4 | | | * | | MHz |
| Slew Rate | | | 10 | | | * | | V/µs |
| Settling Time 0.1% | G = –1, 10V Step, $C_L$ = 100pF | | 1.5 | | | * | | µs |
| 0.01% | G = –1, 10V Step, $C_L$ = 100pF | | 2 | | | * | | µs |
| Total Harmonic Distortion + Noise | 1kHz, G = 1, $V_O$ = 3.5Vrms | | 0.0008 | | | * | | % |
| **OUTPUT** | | | | | | | | |
| Voltage Output, Positive | | (V+)–3 | (V+)–2.5 | | * | * | | V |
| Negative | | (V–)+3 | (V–)+2.5 | | * | * | | V |
| Short-Circuit Current | | | ±25 | | | * | | mA |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | | ±15 | | | * | | V |
| Operating Voltage Range | | ±4.5 | | ±18 | * | | * | V |
| Quiescent Current (per amplifier) | $I_O$ = 0 | | ±1.5 | ±1.75 | | * | ±2 | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Operating Range | | –40 | | +85 | 0 | | +70 | °C |
| Storage | | –40 | | +125 | * | | * | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| 8-Pin DIP | | | 100 | | | * | | °C/W |
| SO-8 Surface-Mount | | | 150 | | | * | | °C/W |
| 14-Pin DIP | | | 80 | | | * | | °C/W |
| SO-14, SOL-16 Surface-Mount | | | 110 | | | * | | °C/W |

* Specifications same as OPA131PA, OPA131UA.

NOTES: (1) Guaranteed by wafer test. (2) High-speed test at $T_J$ = 25°C.

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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, V+ to V– | 36V |
| Input Voltage | (V–) –0.7V to (V+) +0.7V |
| Output Short-Circuit[1] | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering, 10s) | 300°C |

NOTE: (1) Short-circuit to ground, one amplifier per package.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| **Single** | | | |
| OPA131PJ | 8-Pin Plastic DIP | 006 | 0 to +70°C |
| OPA131PA | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| OPA131P | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| OPA131UJ | SO-8 Surface-Mount | 182 | 0 to +70°C |
| OPA131UA | SO-8 Surface-Mount | 182 | –40°C to +85°C |
| OPA131U | SO-8 Surface-Mount | 182 | –40°C to +85°C |
| **Dual** | | | |
| OPA2131PJ | 8-Pin Plastic DIP | 006 | 0 to +70°C |
| OPA2131PA | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| OPA2131UJ | SO-8 Surface-Mount | 182 | 0 to +70°C |
| OPA2131UA | SO-8 Surface-Mount | 182 | –40°C to +85°C |
| **Quad** | | | |
| OPA4131PJ | 14-Pin Plastic DIP | 010 | 0 to +70°C |
| OPA4131PA | 14-Pin Plastic DIP | 010 | –40°C to +85°C |
| OPA4131UA | SOL-16 Surface-Mount | 211 | –40°C to +85°C |
| OPA4131NJ | SO-14 Surface-Mount | 235 | 0 to +70°C |
| OPA4131NA | SO-14 Surface-Mount | 235 | –40°C to +85°C |

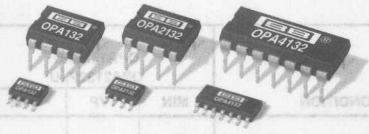
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# OPA132
# OPA2132
# OPA4132

www.burr-brown.com/databook/OPA132.html

# High Speed FET-INPUT OPERATIONAL AMPLIFIERS

## FEATURES

- FET INPUT: $I_B$ = 50pA max
- WIDE BANDWIDTH: 8MHz
- HIGH SLEW RATE: 20V/µs
- LOW NOISE: 8nV/√Hz (1kHz)
- LOW DISTORTION: 0.00008%
- HIGH OPEN-LOOP GAIN: 130dB (600Ω load)
- WIDE SUPPLY RANGE: ±2.5 to ±18V
- LOW OFFSET VOLTAGE: 500µV max
- SINGLE, DUAL, AND QUAD VERSIONS

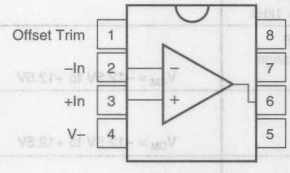
## DESCRIPTION

The OPA132 series of FET-input op amps provides high-speed and excellent dc performance. The combination of high slew rate and wide bandwidth provide fast settling time. Single, dual, and quad versions have identical specifications for maximum design flexibility. High performance grades are available in the single and dual versions. All are ideal for general-purpose, audio, data acquisition and communications applications, especially where high source impedance is encountered.

OPA132 op amps are easy to use and free from phase inversion and overload problems often found in common FET-input op amps. Input cascode circuitry provides excellent common-mode rejection and maintains low input bias current over its wide input voltage range. OPA132 series op amps are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions, including high load capacitance. Dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

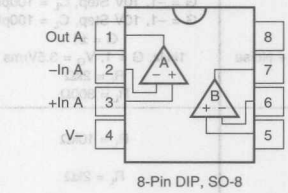
Single and dual versions are available in 8-pin DIP and SO-8 surface-mount packages. Quad is available in 14-pin DIP and SO-14 surface-mount packages. All are specified for –40°C to +85°C operation.

OPA132



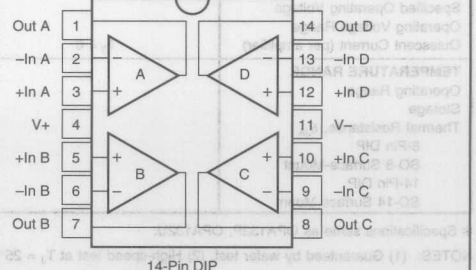

8-Pin DIP, SO-8

OPA2132




8-Pin DIP, SO-8

OPA4132




14-Pin DIP
SO-14

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At $T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

| PARAMETER | CONDITION | OPA132P, U OPA2132P, U MIN | OPA132P, U OPA2132P, U TYP | OPA132P, U OPA2132P, U MAX | OPA132PA, UA OPA2132PA, UA OPA4132PA, UA MIN | OPA132PA, UA OPA2132PA, UA OPA4132PA, UA TYP | OPA132PA, UA OPA2132PA, UA OPA4132PA, UA MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | | | ±0.25 | ±0.5 | | ±0.5 | ±2 | mV |
| vs Temperature[1] | Operating Temperature Range | | ±2 | ±10 | | * | * | µV/°C |
| vs Power Supply | $V_S$ = ±2.5V to ±18V | | 5 | 15 | | * | 30 | µV/V |
| Channel Separation (dual and quad) | $R_L$ = 2kΩ | | 0.2 | | | * | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | | |
| Input Bias Current[2] | $V_{CM}$ = 0V | | +5 | ±50 | | * | * | pA |
| vs Temperature | | | See Typical Curve | | | * | | |
| Input Offset Current[2] | $V_{CM}$ = 0V | | ±2 | ±50 | | * | * | pA |
| **NOISE** | | | | | | | | |
| Input Voltage Noise | | | | | | | | |
| Noise Density, f = 10Hz | | | 23 | | | * | | nV/√Hz |
| f = 100Hz | | | 10 | | | * | | nV/√Hz |
| f = 1kHz | | | 8 | | | * | | nV/√Hz |
| f = 10kHz | | | 8 | | | * | | nV/√Hz |
| Current Noise Density, f = 1kHz | | | 3 | | | * | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Voltage Range | | (V–)+2.5 | ±13 | (V+)–2.5 | * | * | * | V |
| Common-Mode Rejection | $V_{CM}$ = –12.5V to +12.5V | 96 | 100 | | 86 | 94 | | dB |
| **INPUT IMPEDANCE** | | | | | | | | |
| Differential | | | $10^{13}$ \|\| 2 | | | * | | Ω \|\| pF |
| Common-Mode | $V_{CM}$ = –12.5V to +12.5V | | $10^{13}$ \|\| 6 | | | * | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | | | | |
| Open-Loop Voltage Gain | $R_L$ = 10kΩ, $V_O$ = –14.5V to +13.8V | 110 | 120 | | 104 | * | | dB |
| | $R_L$ = 2kΩ, $V_O$ = –13.8V to +13.5V | 110 | 126 | | 104 | 120 | | dB |
| | $R_L$ = 600Ω, $V_O$ = –12.8V to +12.5V | 110 | 130 | | 104 | 120 | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Gain-Bandwidth Product | | | 8 | | | * | | MHz |
| Slew Rate | | | ±20 | | | * | | V/µs |
| Settling Time: 0.1% | G = –1, 10V Step, $C_L$ = 100pF | | 0.7 | | | * | | µs |
| 0.01% | G = –1, 10V Step, $C_L$ = 100pF | | 1 | | | * | | µs |
| Overload Recovery Time | G = ±1 | | 0.5 | | | * | | µs |
| Total Harmonic Distortion + Noise | 1kHz, G = 1, $V_O$ = 3.5Vrms | | | | | | | |
| | $R_L$ = 2kΩ | | 0.00008 | | | * | | % |
| | $R_L$ = 600Ω | | 0.00009 | | | * | | % |
| **OUTPUT** | | | | | | | | |
| Voltage Output, Positive | $R_L$ = 10kΩ | (V+)–1.2 | (V+)–0.9 | | * | * | | V |
| Negative | | (V–)+0.5 | (V–)+0.3 | | * | * | | V |
| Positive | $R_L$ = 2kΩ | (V+)–1.5 | (V+)–1.2 | | * | * | | V |
| Negative | | (V–)+1.2 | (V–)+0.9 | | * | * | | V |
| Positive | $R_L$ = 600Ω | (V+)–2.5 | (V+)–2.0 | | * | * | | V |
| Negative | | (V–)+2.2 | (V–)+1.9 | | * | * | | V |
| Short-Circuit Current | | | ±40 | | | * | | mA |
| Capacitive Load Drive (Stable Operation) | | | See Typical Curve | | | * | | |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | | ±15 | | | * | | V |
| Operating Voltage Range | | ±2.5 | | ±18 | * | | * | V |
| Quiescent Current (per amplifier) | $I_O$ = 0 | | ±4 | ±4.8 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Operating Range | | –40 | | +85 | * | | * | °C |
| Storage | | –40 | | +125 | * | | * | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| 8-Pin DIP | | | 100 | | | * | | °C/W |
| SO-8 Surface-Mount | | | 150 | | | * | | °C/W |
| 14-Pin DIP | | | 80 | | | * | | °C/W |
| SO-14 Surface-Mount | | | 110 | | | * | | °C/W |

* Specifications same as OPA132P, OPA132U.

NOTES: (1) Guaranteed by wafer test. (2) High-speed test at $T_J$ = 25°C.

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| | |
|---|---|
| Output Short-Circuit[1] | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering, 10s) | 300°C |

NOTE: (1) Short-circuit to ground, one amplifier per package.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| **Single** | | |
| OPA132PA | 8-Pin Plastic DIP | 006 |
| OPA132P | 8-Pin Plastic DIP | 006 |
| OPA132UA | SO-8 Surface-Mount | 182 |
| OPA132U | SO-8 Surface-Mount | 182 |
| **Dual** | | |
| OPA2132PA | 8-Pin Plastic DIP | 006 |
| OPA2132P | 8-Pin Plastic DIP | 006 |
| OPA2132UA | SO-8 Surface-Mount | 182 |
| OPA2132U | SO-8 Surface-Mount | 182 |
| **Quad** | | |
| OPA4132PA | 14-Pin Plastic DIP | 010 |
| OPA4132UA | SO-14 Surface-Mount | 235 |

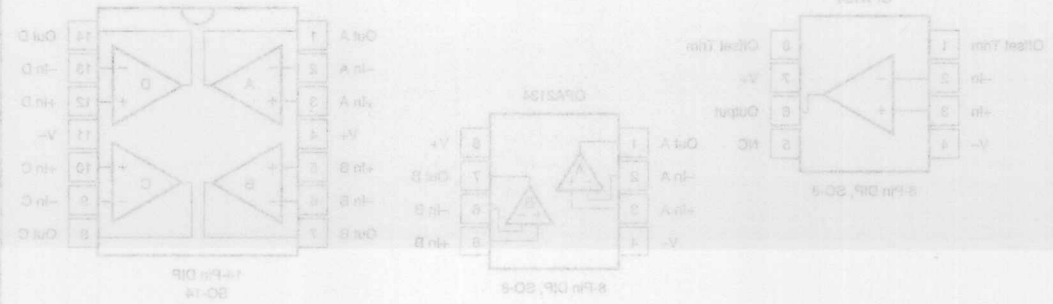
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

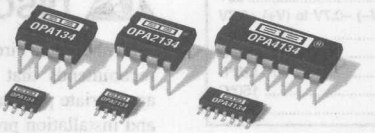
| PRODUCT | PACKAGE | TEMPERATURE RANGE |
|---|---|---|
| **Single** | | |
| OPA132PA | 8-Pin Plastic DIP | –40°C to +85°C |
| OPA132P | 8-Pin Plastic DIP | –40°C to +85°C |
| OPA132UA | SO-8 Surface-Mount | –40°C to +85°C |
| OPA132U | SO-8 Surface-Mount | –40°C to +85°C |
| **Dual** | | |
| OPA2132PA | 8-Pin Plastic DIP | –40°C to +85°C |
| OPA2132P | 8-Pin Plastic DIP | –40°C to +85°C |
| OPA2132UA | SO-8 Surface-Mount | –40°C to +85°C |
| OPA2132U | SO-8 Surface-Mount | –40°C to +85°C |
| **Quad** | | |
| OPA4132PA | 14-Pin Plastic DIP | –40°C to +85°C |
| OPA4132UA | SO-14 Surface-Mount | –40°C to +85°C |

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



BURR-BROWN®



# OPA134
# OPA2134
# OPA4134

www.burr-brown.com/databook/OPA134.html

## SoundPLUS™ High Performance AUDIO OPERATIONAL AMPLIFIERS

## FEATURES

- SUPERIOR SOUND QUALITY
- ULTRA LOW DISTORTION: 0.00008%
- LOW NOISE: 8nV/√Hz
- TRUE FET-INPUT: $I_B$ = 5pA
- HIGH SPEED:
  - SLEW RATE: 20V/µs
  - BANDWIDTH: 8MHz
- HIGH OPEN-LOOP GAIN: 120dB (600Ω)
- WIDE SUPPLY RANGE: ±2.5V to ±18V
- SINGLE, DUAL, AND QUAD VERSIONS

## APPLICATIONS

- PROFESSIONAL AUDIO AND MUSIC
- LINE DRIVERS
- LINE RECEIVERS
- MULTIMEDIA AUDIO
- ACTIVE FILTERS
- PREAMPLIFIERS
- INTEGRATORS
- CROSSOVER NETWORKS

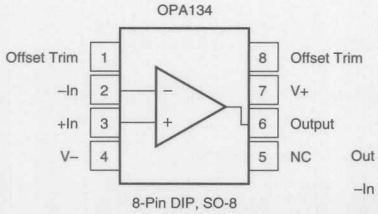
## DESCRIPTION

The OPA134 series are ultra-low distortion, low noise operational amplifiers fully specified for audio applications. A true FET input stage was incorporated to provide superior sound quality and speed for exceptional audio performance. This in combination with high output drive capability and excellent dc performance allows use in a wide variety of demanding applications. In addition, the OPA134's wide output swing, to within 1V of the rails, allows increased headroom making it ideal for use in any audio circuit.

OPA134 op amps are easy to use and free from phase inversion and overload problems often found in common FET-input op amps. They can be operated from ±2.5V to ±18V power supplies. Input cascode circuitry provides excellent common-mode rejection and maintains low input bias current over its wide input voltage range, minimizing distortion. OPA134 series op amps are unity-gain stable and provide excellent dynamic behavior over a wide range of load conditions, including high load capacitance. The dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

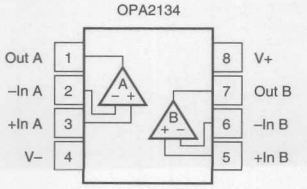
Single and dual versions are available in 8-pin DIP and SO-8 surface-mount packages in standard configurations. The quad is available in 14-pin DIP and SO-14 surface mount packages. All are specified for –40°C to +85°C operation. A SPICE macromodel is available for design analysis.

OPA134



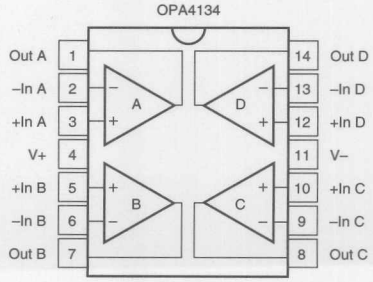

8-Pin DIP, SO-8

OPA2134




8-Pin DIP, SO-8

OPA4134




14-Pin DIP
SO-14

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

| PARAMETER | CONDITION | OPA134PA, UA OPA2134PA, UA OPA4134PA, UA MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **AUDIO PERFORMANCE** | | | | | |
| Total Harmonic Distortion + Noise | G = 1, f = 1kHz, $V_O$ = 3Vrms | | | | |
| | $R_L$ = 2kΩ | | 0.00008 | | % |
| | $R_L$ = 600Ω | | 0.00015 | | % |
| Intermodulation Distortion | G = 1, f = 1kHz, $V_O$ = 1Vp-p | | –98 | | dB |
| Headroom[1] | THD < 0.01%, $R_L$ = 2kΩ, $V_S$ = ±18V | | 23.6 | | dBu |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product | | | 8 | | MHz |
| Slew Rate[2] | | ±15 | ±20 | | V/µs |
| Full Power Bandwidth | | | 1.3 | | MHz |
| Settling Time 0.1% | G = 1, 10V Step, $C_L$ = 100pF | | 0.7 | | µs |
| 0.01% | G = 1, 10V Step, $C_L$ = 100pF | | 1 | | µs |
| Overload Recovery Time | $(V_{IN})$ • (Gain) = $V_S$ | | 0.5 | | µs |
| **NOISE** | | | | | |
| Input Voltage Noise | | | | | |
| Noise Voltage, f = 20Hz to 20kHz | | | 1.2 | | µVrms |
| Noise Density, f = 1kHz | | | 8 | | nV/√Hz |
| Current Noise Density, f = 1kHz | | | 3 | | fA/√Hz |
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | | | ±0.5 | ±2 | mV |
| | $T_A$ = –40°C to +85°C | | ±1 | ±3[3] | mV |
| vs Temperature | $T_A$ = –40°C to +85°C | | ±2 | | µV/°C |
| vs Power Supply (PSRR) | $V_S$ = ±2.5V to ±18V | 90 | 106 | | dB |
| Channel Separation (Dual, Quad) | dc, $R_L$ = 2kΩ | | 135 | | dB |
| | f = 20kHz, $R_L$ = 2kΩ | | 130 | | dB |
| **INPUT BIAS CURRENT** | | | | | |
| Input Bias Current[4] | $V_{CM}$ =0V | | +5 | ±100 | pA |
| vs Temperature[3] | | | See Typical Curve | ±5 | nA |
| Input Offset Current[4] | $V_{CM}$ =0V | | ±2 | ±50 | pA |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Voltage Range | | (V–)+2.5 | ±13 | (V+)–2.5 | V |
| Common-Mode Rejection | $V_{CM}$ = –12.5V to +12.5V | 86 | 100 | | dB |
| | $T_A$ = –40°C to +85°C | | 90 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $10^{13}$ ‖ 2 | | Ω ‖ pF |
| Common-Mode | $V_{CM}$ = –12.5V to +12.5V | | $10^{13}$ ‖ 5 | | Ω ‖ pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | $R_L$ = 10kΩ, $V_O$ = –14.5V to +13.8V | 104 | 120 | | dB |
| | $R_L$ = 2kΩ, $V_O$ = –13.8V to +13.5V | 104 | 120 | | dB |
| | $R_L$ = 600Ω, $V_O$ = –12.8V to +12.5V | 104 | 120 | | dB |
| **OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 10kΩ | (V–)+0.5 | | (V+)–1.2 | V |
| | $R_L$ = 2kΩ | (V–)+1.2 | | (V+)–1.5 | V |
| | $R_L$ = 600Ω | (V–)+2.2 | | (V+)–2.5 | V |
| Output Current | | | ±35 | | mA |
| Output Impedance, Closed-Loop[5] | f = 10kHz | | 0.01 | | Ω |
| Open-Loop | f = 10kHz | | 10 | | Ω |
| Short-Circuit Current | | | ±40 | | mA |
| Capacitive Load Drive (Stable Operation) | | | See Typical Curve | | |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±15 | | V |
| Operating Voltage Range | | ±2.5 | | ±18 | V |
| Quiescent Current (per amplifier) | $I_O$ = 0 | | 4 | 5 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specified Range | | –40 | | +85 | °C |
| Operating Range | | –55 | | +125 | °C |
| Storage | | –55 | | +125 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| 8-Pin DIP | | | 100 | | °C/W |
| SO-8 Surface-Mount | | | 150 | | °C/W |
| 14-Pin DIP | | | 80 | | °C/W |
| SO-14 Surface-Mount | | | 110 | | °C/W |

NOTES: (1) dBu = 20*log (Vrms/0.7746) where Vrms is the maximum output voltage for which THD+Noise is less than 0.01%. See THD+Noise text. (2) Guaranteed by design. (3) Guaranteed by wafer-level test to 95% confidence level. (4) High-speed test at $T_J$ = 25°C. (5) See "Closed-Loop Output Impedance vs Frequency" typical curve.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Supply Voltage, V+ to V– | 36V |
| Input Voltage | (V–) –0.7V to (V+) +0.7V |
| Output Short-Circuit[2] | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering, 10s) | 300°C |

NOTES: (1) Stresses above these ratings may cause permanent damage. (2) Short-circuit to ground, one amplifier per package.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| **Single** | | | |
| OPA134PA | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| OPA134UA | SO-8 Surface-Mount | 182 | –40°C to +85°C |
| **Dual** | | | |
| OPA2134PA | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| OPA2134UA | SO-8 Surface-Mount | 182 | –40°C to +85°C |
| **Quad** | | | |
| OPA4134PA | 14-Pin Plastic DIP | 010 | –40°C to +85°C |
| OPA4134UA | SO-14 Surface-Mount | 235 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

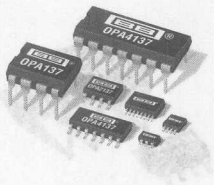
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# OPA137
# OPA2137
# OPA4137

PRELIMINARY INFORMATION
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www.burr-brown.com/databook/OPA137.html

# LOW COST FET-INPUT OPERATIONAL AMPLIFIERS
## *Micro*Amplifier™ Series

## FEATURES

- FET INPUT: $I_B$ = 20pA
- LOW OFFSET VOLTAGE: 1mV
- WIDE SUPPLY RANGE: ±2.25V to ±18V
- LOW QUIESCENT CURRENT: 200µA/channel
- HIGH SPEED: 1MHz, 3V/µs
- *Micro*SIZE PACKAGES
- SINGLE, DUAL, AND QUAD

## APPLICATIONS

- STRAIN GAGE AMPLIFIER
- PHOTODETECTOR AMPLIFIER
- PRECISION INTEGRATOR
- BATTERY-POWERED INSTRUMENTS
- TEST EQUIPMENT
- ACTIVE FILTERS

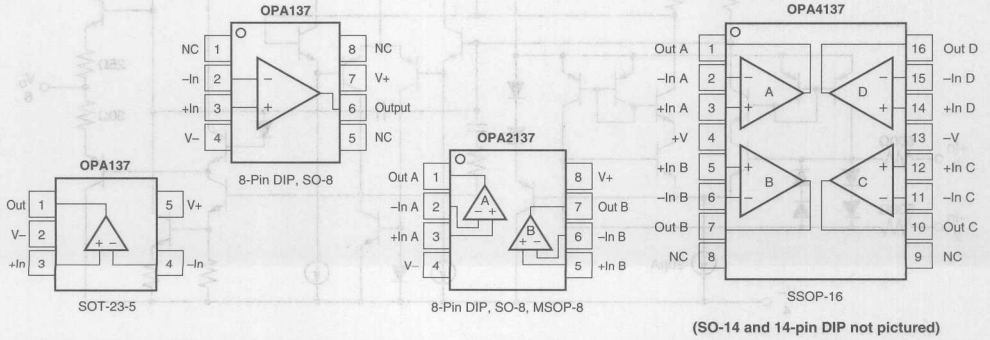
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## DESCRIPTION

OPA137 series of FET-input operational amplifiers provides high performance and low quiescent current at low cost. Features include low bias current, low offset voltage and offset drift, high common-mode rejection, and high power supply rejection. Either single (+4.5V to +36V) or dual (±2.25 to ±18V) supplies can be used. The input common-mode voltage range includes the positive supply—ideal for single supply applications. Single, dual, and quad versions have identical specifications for maximum design flexibility.

OPA137 op amps are easy to use and free from phase inversion and overload problems found in some FET-input amplifiers. High performance, including linearity, is maintained as the amplifiers swing to their specified limits. In addition, the combination of high slew rate (3V/µs) and wide bandwidth (1MHz) provide fast settling time assuring good dynamic response. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

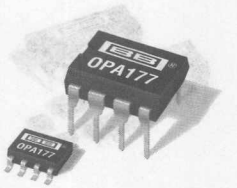
The single (OPA137) packages are the tiny 5-lead SOT-23-5 surface mount, SO-8 surface-mount, and 8-pin DIP. The dual (OPA2137) comes in the miniature MSOP-8 surface mount, SO-8 surface-mount, and 8-pin DIP packages. The quad (OPA4137) packages are the space-saving SSOP-16 surface mount, SO-14 surface-mount, and the 14-pin DIP. All are specified from –40°C to +85°C and operate from –55°C to +125°C.




(SO-14 and 14-pin DIP not pictured)

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# OPA177

www.burr-brown.com/databook/OPA177.html

# Precision OPERATIONAL AMPLIFIER

## FEATURES

- LOW OFFSET VOLTAGE: 25μV max
- LOW DRIFT: 0.3μV/°C
- HIGH OPEN-LOOP GAIN: 130dB min
- LOW QUIESCENT CURRENT: 1.5mA typ
- REPLACES INDUSTRY-STANDARD OP AMPS: OP-07, OP-77, OP-177, AD707, ETC.

## APPLICATIONS

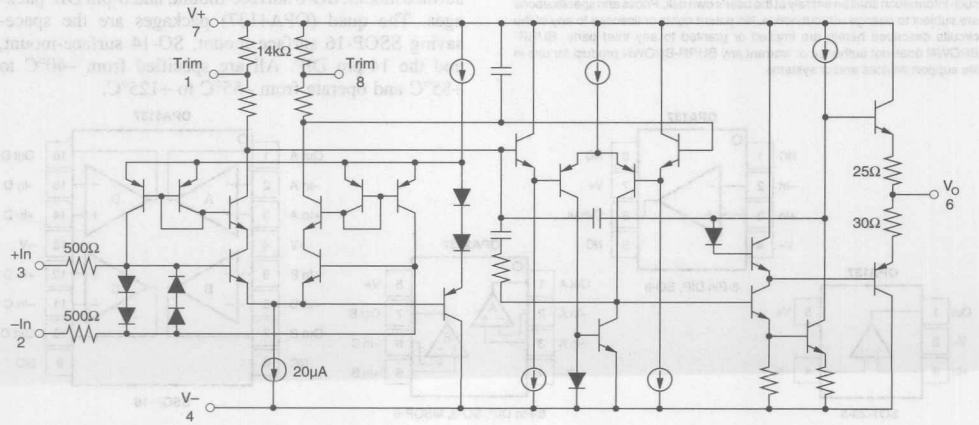
- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER

## DESCRIPTION

The OPA177 precision bipolar op amp feature very low offset voltage and drift. Laser-trimmed offset, drift and input bias current virtually eliminate the need for costly external trimming. The high performance and low cost make them ideally suited to a wide range of precision instrumentation.

The low quiescent current of the OPA177 dramatically reduce warm-up drift and errors due to thermoelectric effects in input interconnections. It provides an effective alternative to chopper-stabilized amplifiers. The low noise of the OPA177 maintains accuracy.

OPA177 performance gradeouts are available. Packaging options include 8-pin plastic DIP and SO-8 surface-mount packages.




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# OPA177 SPECIFICATIONS

At $V_S$ = ±15V, $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITION | OPA177F | | | OPA177G | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | | | 10 | 25 | | 20 | 60 | µV |
| Long-Term Input Offset(1) | | | 0.3 | | | 0.4 | | µV/Mo |
| Voltage Stability | | | | | | | | |
| Offset Adjustment Range | $R_P$ = 20kΩ | | ±3 | | | * | | mV |
| Power Supply Rejection Ratio | $V_S$ = ±3V to ±18V | 115 | 125 | | 110 | 120 | | dB |
| **INPUT BIAS CURRENT** | | | | | | | | |
| Input Offset Current | | | 0.3 | 1.5 | | * | 2.8 | nA |
| Input Bias Current | | | 0.5 | ±2 | | * | ±2.8 | nA |
| **NOISE** | | | | | | | | |
| Input Noise Voltage | 1Hz to 100Hz(2) | | 85 | 150 | | * | * | nVrms |
| Input Noise Current | 1Hz to 100Hz | | 4.5 | | | * | | pArms |
| **INPUT IMPEDANCE** | | | | | | | | |
| Input Resistance | Differential Mode(3) | 26 | 45 | | 18.5 | * | | MΩ |
| | Common-Mode | | 200 | | | * | | GΩ |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range(4) | | ±13 | ±14 | | * | * | | V |
| Common-Mode Rejection | $V_{CM}$ = ±13V | 130 | 140 | | 115 | * | | dB |
| **OPEN-LOOP GAIN** | $R_L$ ≥ 2kΩ | | | | | | | |
| Large Signal Voltage Gain | $V_O$ = ±10V(5) | 5110 | 12,000 | | 2000 | 6000 | | V/mV |
| **OUTPUT** | | | | | | | | |
| Output Voltage Swing | $R_L$ ≥ 10kΩ | ±13.5 | ±14 | | * | * | | V |
| | $R_L$ ≥ 2kΩ | ±12.5 | ±13 | | * | * | | V |
| | $R_L$ ≥ 1kΩ | ±12 | ±12.5 | | * | * | | V |
| Open-Loop Output Resistance | | | 60 | | | * | | Ω |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Slew Rate | $R_L$ ≥ 2kΩ | 0.1 | 0.3 | | * | * | | V/µs |
| Closed-Loop Bandwidth | G = +1 | 0.4 | 0.6 | | * | * | | MHz |
| **POWER SUPPLY** | | | | | | | | |
| Power Consumption | $V_S$ = ±15V, No Load | | 40 | 60 | | * | * | mW |
| | $V_S$ = ±3V, No Load | | 3.5 | 4.5 | | * | * | mW |
| Supply Current | $V_S$ = ±15V, No Load | | 1.3 | 2 | | * | * | mA |

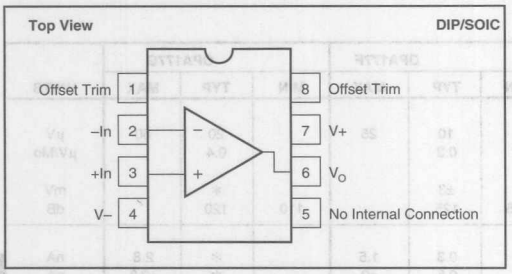
At $V_S$ = ±15V, –40°C ≤ $T_A$ ≤ +85°C, unless otherwise noted.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | | | 15 | 40 | | 20 | 100 | µV |
| Average Input Offset | | | 0.1 | 0.3 | | 0.7 | 1.2 | µV/°C |
| Voltage Drift | | | | | | | | |
| Power Supply Rejection Ratio | $V_S$ = ±3V to ±18V | 110 | 120 | | 106 | 115 | | dB |
| **INPUT BIAS CURRENT** | | | | | | | | |
| Input Offset Current | | | 0.5 | 2.2 | | * | 4.5 | nA |
| Average Input Offset Current | | | 1.5 | 40 | | * | 85 | pA/°C |
| Drift(6) | | | | | | | | |
| Input Bias Current | | | 0.5 | ±4 | | * | ±6 | nA |
| Average Input Bias Current | | | 8 | 40 | | 15 | 60 | pA/°C |
| Drift(6) | | | | | | | | |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | ±13 | ±13.5 | | * | * | | V |
| Common-Mode Rejection | $V_{CM}$ = ±13V | 120 | 140 | | 110 | * | | dB |
| **OPEN-LOOP GAIN** | | | | | | | | |
| Large Signal Voltage Gain | $R_L$ ≥ 2kΩ, $V_O$ = ±10V | 2000 | 6000 | | 1000 | 4000 | | V/mV |
| **OUTPUT** | | | | | | | | |
| Output Voltage Swing | $R_L$ ≥ 2kΩ | ±12 | ±13 | | * | * | | V |
| **POWER SUPPLY** | | | | | | | | |
| Power Consumption | $V_S$ = ±15V, No Load | | 60 | 75 | | * | * | mW |
| Supply Current | $V_S$ = ±15V, No Load | | 2 | 25 | | * | * | mA |

* Same as specification for product to left.

NOTES: (1) Long-Term Input Offset Voltage Stability refers to the averaged trend line of $V_{OS}$ vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in $V_{OS}$ during the first 30 operating days are typically less than 2µV. (2) Sample tested. (3) Guaranteed by design. (4) Guaranteed by CMRR test condition. (5) To insure high open-loop gain throughout the ±10V output range, $A_{OL}$ is tested at $-10V \le V_O \le 0V$, $0V \le V_O \le +10V$, and $-10V \le V_O \le +10V$. (6) Guaranteed by end-point limits.

## PIN CONFIGURATION




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | ±22V |
| Differential Input Voltage | ±30V |
| Input Voltage | $\pm V_S$ |
| Output Short Circuit | Continuous |
| Operating Temperature: | |
| Plastic DIP (P), SO-8 (S) | –40°C to +85°C |
| $\theta_{JA}$ (PDIP) | 100°C/W |
| $\theta_{JA}$ (SOIC) | 160°C/W |
| Storage Temperature: | |
| Plastic DIP (P), SO-8 (S) | –65°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) P packages | +300°C |
| (soldering, 3s) S package | +260°C |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| OPA177FP | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| OPA177GP | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| OPA177GS | SO-8 Surface-Mount | 182 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

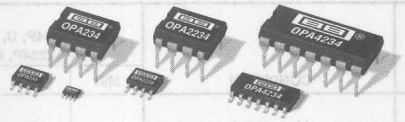
Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. ESD can cause damage ranging from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

Burr-Brown's standard ESD test method consists of five 1000V positive and negative discharges (100pF in series with 1.5kΩ) applied to each pin.

Failure to observe proper handling procedures could result in small changes to the OPA177's input bias current.

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BURR-BROWN®



# OPA234
# OPA2234
# OPA4234

www.burr-brown.com/databook/OPA234.html

# Low Power, Precision SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

## FEATURES

- WIDE SUPPLY RANGE:
  Single Supply: $V_S$ = +2.7V to +36V
  Dual Supply: $V_S$ = ±1.35V to ±18V
- GUARANTEED PERFORMANCE:
  +2.7V, +5V, and ±15V
- LOW QUIESCENT CURRENT: 250µA/amp
- LOW INPUT BIAS CURRENT: 25nA max
- LOW OFFSET VOLTAGE: 100µV max
- HIGH CMRR, PSRR, and $A_{OL}$
- SINGLE, DUAL, and QUAD VERSIONS

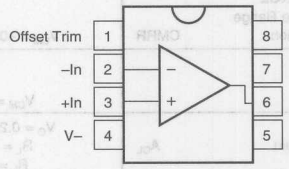
## DESCRIPTION

The OPA234 series low cost op amps are ideal for single supply, low voltage, low power applications. The series provides lower quiescent current than older "1013"-type products and comes in current industry-standard packages and pinouts. The combination of low offset voltage, high common-mode rejection, high power supply rejection, and a wide supply range provides excellent accuracy and versatility. Single, dual, and quad versions have identical specifications for maximum design flexibility. These general purpose op amps are ideal for portable and battery powered applications.

OPA234 series op amps operate from either single or dual supplies. In single supply operation, the input common-mode range extends below ground and the output can swing to within 50mV of ground. Excellent phase margin makes the OPA234 series ideal for demanding applications, including high load capacitance. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

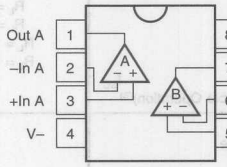
Single version packages are 8-Pin DIP, SO-8 surface-mount, and a space-saving MSOP-8 surface-mount. Dual packages are 8-Pin DIP and SO-8 surface-mount. Quad packages are 14-Pin DIP and SO-14 surface-mount. All are specified for –40°C to +85°C operation.

OPA234



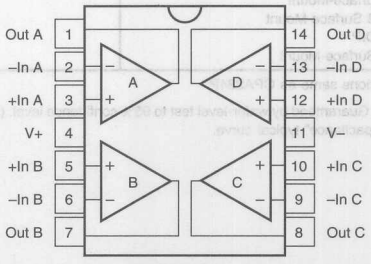

8-Pin DIP, SO-8, MSOP-8

OPA2234




8-Pin DIP, SO-8

OPA4234




14-Pin DIP
SO-14

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS: $V_S$ = +5V

At $T_A$ = 25°C, $V_S$ = +5V, $R_L$ = 10kΩ connected to $V_S/2$ and $V_{OUT}$ = $V_S/2$, unless otherwise noted.

| PARAMETER | | CONDITION | OPA234P, U, E OPA2234P, U MIN | OPA234P, U, E OPA2234P, U TYP | OPA234P, U, E OPA2234P, U MAX | OPA234PA, UA, EA OPA2234PA, UA OPA4234PA, UA, U MIN | OPA234PA, UA, EA OPA2234PA, UA OPA4234PA, UA, U TYP | OPA234PA, UA, EA OPA2234PA, UA OPA4234PA, UA, U MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | | | |
| Input Offset Voltage | $V_{OS}$ | $V_{CM}$ = 2.5V | | ±40 | ±100 | | * | ±250 | µV |
| OPA234E, EA | | | | ±100 | ±150 | | * | ±350 | µV |
| vs Temperature[1] | $dV_{OS}/dT$ | Operating Temperature Range | | ±0.5 | ±3 | | * | * | µV/°C |
| vs Power Supply | PSRR | $V_S$ = +2.7V to +30V, $V_{CM}$ = 1.7V | | 3 | 10 | | * | 20 | µV/V |
| vs Time | | | | 0.2 | | | * | | µV/mo |
| Channel Separation (Dual, Quad) | | | | 0.3 | | | * | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | | | |
| Input Bias Current[2] | $I_B$ | $V_{CM}$ = 2.5V | | –15 | –25 | | * | –50 | nA |
| Input Offset Current | $I_{OS}$ | $V_{CM}$ = 2.5V | | ±1 | ±5 | | * | * | nA |
| **NOISE** | | f = 1kHz | | | | | | | |
| Input Voltage Noise Density | $v_n$ | | | 25 | | | * | | nV/√Hz |
| Current Noise Density | $i_n$ | | | 80 | | | * | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | | | | |
| Common-Mode Voltage Range | | | –0.1 | | (V+) –1 | * | | * | V |
| Common-Mode Rejection | CMRR | $V_{CM}$ = –0.1V to 4V | 96 | 106 | | 86 | * | | dB |
| **INPUT IMPEDANCE** | | | | | | | | | |
| Differential | | | | $10^7$ ‖ 5 | | | * | | Ω ‖ pF |
| Common-Mode | | $V_{CM}$ = 2.5V | | $10^{10}$ ‖ 6 | | | * | | Ω ‖ pF |
| **OPEN-LOOP GAIN** | | $V_O$ = 0.25V to 4V | | | | | | | |
| Open-Loop Voltage Gain | $A_{OL}$ | $R_L$ = 10kΩ | 110 | 120 | | 100 | * | | dB |
| | | $R_L$ = 2kΩ | 90 | 96 | | 86 | * | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | | |
| Gain-Bandwidth Product | GBW | $C_L$ = 100pF | | 0.35 | | | * | | MHz |
| Slew Rate | SR | | | 0.2 | | | * | | V/µs |
| Settling Time: 0.1% | | G = 1, 3V Step, $C_L$ = 100pF | | 15 | | | * | | µs |
| 0.01% | | G = 1, 3V Step, $C_L$ = 100pF | | 25 | | | * | | µs |
| Overload Recovery Time | | ($V_{IN}$) (Gain) = $V_S$ | | 16 | | | * | | µs |
| **OUTPUT** | | | | | | | | | |
| Voltage Output: Positive | | $R_L$ = 10kΩ to $V_S/2$ | (V+) –1 | (V+) –0.65 | | * | * | | V |
| Negative | | $R_L$ = 10kΩ to $V_S/2$ | 0.25 | 0.05 | | * | * | | V |
| Positive | | $R_L$ = 10kΩ to Ground | (V+) –1 | (V+) –0.65 | | * | * | | V |
| Negative | | $R_L$ = 10kΩ to Ground | 0.1 | 0.05 | | * | * | | V |
| Short-Circuit Current | $I_{SC}$ | | | ±11 | | | * | | mA |
| Capacitive Load Drive (Stable Operation)[3] | | G = +1 | | 1000 | | | * | | pF |
| **POWER SUPPLY** | | | | | | | | | |
| Specified Operating Voltage | | | | +5 | | | * | | V |
| Operating Voltage Range | | | +2.7 | | +36 | * | | * | V |
| Quiescent Current (per amplifier) | $I_Q$ | $I_O$ = 0 | | 250 | 300 | | * | * | µA |
| **TEMPERATURE RANGE** | | | | | | | | | |
| Specified Range | | | –40 | | +85 | * | | * | °C |
| Operating Range | | | –40 | | +125 | * | | * | °C |
| Storage | | | –55 | | +125 | * | | * | °C |
| Thermal Resistance | $\theta_{JA}$ | | | | | | | | |
| 8-Pin DIP | | | | 100 | | | * | | °C/W |
| SO-8 Surface-Mount | | | | 150 | | | * | | °C/W |
| MSOP-8 Surface-Mount | | | | 220 | | | * | | °C/W |
| 14-Pin DIP | | | | 80 | | | * | | °C/W |
| SO-14 Surface-Mount | | | | 110 | | | * | | °C/W |

* Specifications same as OPA234P.

NOTES: (1) Guaranteed by wafer-level test to 95% confidence level. (2) Positive conventional current flows into the input terminals. (3) See "Small-Signal Overshoot vs Load Capacitance" typical curve.

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# SPECIFICATIONS: $V_S$ = +2.7V

At $T_A$ = 25°C, $V_S$ = +2.7V, $R_L$ = 10kΩ connected to $V_S/2$ and $V_{OUT} = V_S/2$, unless otherwise noted.

| PARAMETER | | CONDITION | OPA234P, U, E OPA2234P, U MIN | OPA234P, U, E OPA2234P, U TYP | OPA234P, U, E OPA2234P, U MAX | OPA234PA, UA, EA OPA2234PA, UA OPA4234PA, UA, U MIN | OPA234PA, UA, EA OPA2234PA, UA OPA4234PA, UA, U TYP | OPA234PA, UA, EA OPA2234PA, UA OPA4234PA, UA, U MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | | | |
| Input Offset Voltage | $V_{OS}$ | $V_{CM}$ = 1.35V | | ±40 | ±100 | | * | ±250 | µV |
| OPA234E, EA | | | | ±100 | ±150 | | * | ±350 | µV |
| vs Temperature[1] | $dV_{OS}/dT$ | Operating Temperature Range | | ±0.5 | ±3 | | * | * | µV/°C |
| vs Power Supply | PSRR | $V_S$ = +2.7V to +30V, $V_{CM}$ = 1.7V | | 3 | 10 | | * | 20 | µV/V |
| vs Time | | | | 0.2 | | | * | | µV/mo |
| Channel Separation (Dual, Quad) | | | | 0.3 | | | * | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | | | |
| Input Bias Current[2] | $I_B$ | $V_{CM}$ = 1.35V | | –15 | –25 | | * | –50 | nA |
| Input Offset Current | $I_{OS}$ | $V_{CM}$ = 1.35V | | ±1 | ±5 | | * | * | n |
| **NOISE** | | f = 1kHz | | | | | | | |
| Input Voltage Noise Density | $v_n$ | | | 25 | | | * | | nV/√Hz |
| Current Noise Density | $i_n$ | | | 80 | | | * | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | | | | |
| Common-Mode Voltage Range | | | –0.1 | | (V+) –1 | * | | * | V |
| Common-Mode Rejection | CMRR | $V_{CM}$ = –0.1V to 1.7V | 96 | 106 | | 86 | * | | dB |
| **INPUT IMPEDANCE** | | | | | | | | | |
| Differential | | | | $10^7$ ‖ 5 | | | * | | Ω ‖ pF |
| Common-Mode | | $V_{CM}$ = 1.35V | | $10^{10}$ ‖ 6 | | | * | | Ω ‖ pF |
| **OPEN-LOOP GAIN** | | $V_O$ = 0.25V to 1.7V | | | | | | | |
| Open-Loop Voltage Gain | $A_{OL}$ | $R_L$ = 10kΩ | 110 | 125 | | 100 | * | | dB |
| | | $R_L$ = 2kΩ | 90 | 96 | | 86 | * | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | | |
| Gain-Bandwidth Product | GBW | $C_L$ = 100pF | | 0.35 | | | * | | MHz |
| Slew Rate | SR | | | 0.2 | | | * | | V/µs |
| Settling Time: 0.1% | | G = 1, 1V Step, $C_L$ = 100pF | | 6 | | | * | | µs |
| 0.01% | | G = 1, 1V Step, $C_L$ = 100pF | | 16 | | | * | | µs |
| Overload Recovery Time | | ($V_{IN}$) (Gain) = $V_S$ | | 8 | | | * | | µs |
| **OUTPUT** | | | | | | | | | |
| Voltage Output: Positive | | $R_L$ = 10kΩ to $V_S/2$ | (V+) –1 | (V+) –0.6 | | * | * | | V |
| Negative | | $R_L$ = 10kΩ to $V_S/2$ | 0.25 | 0.05 | | * | * | | V |
| Positive | | $R_L$ = 10kΩ to Ground | (V+) –1 | (V+) –0.65 | | * | * | | V |
| Negative | | $R_L$ = 10kΩ to Ground | 0.1 | 0.05 | | * | * | | V |
| Short-Circuit Current | $I_{SC}$ | | | ±8 | | | * | | mA |
| Capacitive Load Drive (Stable Operation)[3] | | G = +1 | | 1000 | | | * | | pF |
| **POWER SUPPLY** | | | | | | | | | |
| Specified Operating Voltage | | | | +2.7 | | | * | | V |
| Operating Voltage Range | | | +2.7 | | +36 | * | | * | V |
| Quiescent Current (per amplifier) | $I_Q$ | $I_O$ = 0 | | 250 | 300 | | * | * | µA |
| **TEMPERATURE RANGE** | | | | | | | | | |
| Specified Range | | | –40 | | +85 | * | | * | °C |
| Operating Range | | | –40 | | +125 | * | | * | °C |
| Storage | | | –55 | | +125 | * | | * | °C |
| Thermal Resistance | $\theta_{JA}$ | | | | | | | | |
| 8-Pin DIP | | | | 100 | | | * | | °C/W |
| SO-8 Surface-Mount | | | | 150 | | | * | | °C/W |
| MSOP-8 Surface-Mount | | | | 220 | | | * | | °C/W |
| 14-Pin DIP | | | | 80 | | | * | | °C/W |
| SO-14 Surface-Mount | | | | 110 | | | * | | °C/W |

* Specifications same as OPA234P.

NOTES: (1) Guaranteed by wafer-level test to 95% confidence level. (2) Positive conventional current flows into the input terminals. (3) See "Small-Signal Overshoot vs Load Capacitance" typical curve.

## SPECIFICATIONS: $V_S = \pm 15V$

At $T_A = 25°C$, $V_S = \pm 15V$, $R_L = 10k\Omega$ connected to ground, unless otherwise noted.

| PARAMETER | | CONDITION | OPA234P, U, E OPA2234P, U MIN | OPA234P, U, E OPA2234P, U TYP | OPA234P, U, E OPA2234P, U MAX | OPA234PA, UA, EA OPA2234PA, UA OPA4234PA, UA, U MIN | OPA234PA, UA, EA OPA2234PA, UA OPA4234PA, UA, U TYP | OPA234PA, UA, EA OPA2234PA, UA OPA4234PA, UA, U MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | | | |
| Input Offset Voltage | $V_{OS}$ | $V_{CM} = 0V$ | | ±70 | ±250 | | * | ±500 | µV |
| OPA4234U Model | | | | | | | ±70 | ±250 | µV |
| vs Temperature[1] | $dV_{OS}/dT$ | Operating Temperature Range | | ±0.5 | ±5 | | * | * | µV/°C |
| vs Power Supply | PSRR | $V_S = \pm 1.35V$ to $\pm 18V$, $V_{CM} = 0V$ | | 3 | 10 | | * | 20 | µV/V |
| vs Time | | | | 0.2 | | | * | | µV/mo |
| Channel Separation (Dual, Quad) | | | | 0.3 | | | * | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | | | |
| Input Bias Current[2] | $I_B$ | $V_{CM} = 0V$ | | –12 | –25 | | * | –50 | nA |
| Input Offset Current | $I_{OS}$ | $V_{CM} = 0V$ | | ±1 | ±5 | | * | * | nA |
| **NOISE** | | f = 1kHz | | | | | | | |
| Input Voltage Noise Density | $v_n$ | | | 25 | | | * | | $nV/\sqrt{Hz}$ |
| Current Noise Density | $i_n$ | | | 80 | | | * | | $fA/\sqrt{Hz}$ |
| **INPUT VOLTAGE RANGE** | | | | | | | | | |
| Common-Mode Voltage Range | | | (V–) | | (V+) –1 | * | | * | V |
| Common-Mode Rejection | CMRR | $V_{CM} = -15V$ to 14V | 96 | 106 | | 86 | * | | dB |
| **INPUT IMPEDANCE** | | | | | | | | | |
| Differential | | | | $10^7$ ll 5 | | | * | | Ω ll pF |
| Common-Mode | | $V_{CM} = 0V$ | | $10^{10}$ ll 6 | | | * | | Ω ll pF |
| **OPEN-LOOP GAIN** | | | | | | | | | |
| Open-Loop Voltage Gain | $A_{OL}$ | $V_O = -14.5V$ to 14V | 110 | 120 | | 100 | * | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | | |
| Gain-Bandwidth Product | GBW | $C_L = 100pF$ | | 0.35 | | | * | | MHz |
| Slew Rate | SR | | | 0.2 | | | * | | V/µs |
| Settling Time: 0.1% | | G = 1, 10V Step, $C_L = 100pF$ | | 41 | | | * | | µs |
| 0.01% | | G = 1, 10V Step, $C_L = 100pF$ | | 47 | | | * | | µs |
| Overload Recovery Time | | $(V_{IN})$ (Gain) = $V_S$ | | 22 | | | * | | µs |
| **OUTPUT** | | | | | | | | | |
| Voltage Output: Positive | | | (V+) –1 | (V+) –0.7 | | * | * | | V |
| Negative | | | (V–) +0.5 | (V–) +0.15 | | * | * | | V |
| Short-Circuit Current | $I_{SC}$ | | | ±22 | | | * | | mA |
| Capacitive Load Drive (Stable Operation)[3] | | G = +1 | | 1000 | | | * | | pF |
| **POWER SUPPLY** | | | | | | | | | |
| Specified Operating Voltage | | | | ±15 | | | * | | V |
| Operating Voltage Range | | | ±1.35 | | ±18 | * | | * | V |
| Quiescent Current (per amplifier) | $I_Q$ | $I_O = 0$ | | ±275 | ±350 | | * | * | µA |
| **TEMPERATURE RANGE** | | | | | | | | | |
| Specified Range | | | –40 | | +85 | * | | * | °C |
| Operating Range | | | –40 | | +125 | * | | * | °C |
| Storage | | | –55 | | +125 | * | | * | °C |
| Thermal Resistance | $\theta_{JA}$ | | | | | | | | |
| 8-Pin DIP | | | | 100 | | | * | | °C/W |
| SO-8 Surface-Mount | | | | 150 | | | * | | °C/W |
| MSOP-8 Surface-Mount | | | | 220 | | | * | | °C/W |
| 14-Pin DIP | | | | 80 | | | * | | °C/W |
| SO-14 Surface-Mount | | | | 110 | | | * | | °C/W |

* Specifications same as OPA234P.

NOTES: (1) Guaranteed by wafer-level test to 95% confidence level. (2) Positive conventional current flows into the input terminals. (3) See "Small-Signal Overshoot vs Load Capacitance" typical curve.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

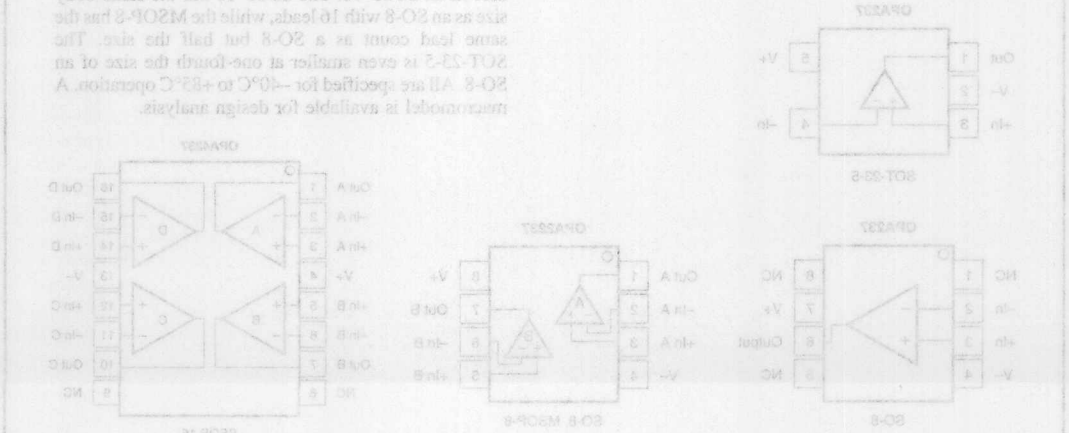
| | |
|---|---|
| Supply Voltage, V+ to V– | 36V |
| Input Voltage | (V–) –0.7V to (V+) +0.7V |
| Output Short-Circuit[1] | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering, 10s) | 300°C |

NOTE: (1) Short-circuit to ground, one amplifier per package.

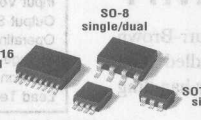
## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER[2] |
|---|---|---|---|---|---|
| **Single** | | | | | |
| OPA234EA | MSOP-8 Surface-Mount | 337 | –40°C to +85°C | A34[3] | OPA234EA-250<br>OPA234EA-2500 |
| OPA234E | MSOP-8 Surface-Mount | 337 | –40°C to +85°C | A34[3] | OPA234E-250<br>OPA234E-2500 |
| OPA234PA | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA234PA | OPA234PA |
| OPA234P | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA234P | OPA234P |
| OPA234UA | SO-8 Surface-Mount | 182 | –40°C to +85°C | OPA234UA | OPA234UA |
| OPA234U | SO-8 Surface-Mount | 182 | –40°C to +85°C | OPA234U | OPA234U |
| **Dual** | | | | | |
| OPA2234PA | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA2234PA | OPA2234PA |
| OPA2234P | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA2234P | OPA2234P |
| OPA2234UA | SO-8 Surface-Mount | 182 | –40°C to +85°C | OPA2234UA | OPA2234UA |
| OPA2234U | SO-8 Surface-Mount | 182 | –40°C to +85°C | OPA2234U | OPA2234U |
| **Quad** | | | | | |
| OPA4234PA | 14-Pin Plastic DIP | 010 | –40°C to +85°C | OPA4234PA | OPA4232PA |
| OPA4234UA | SO-14 Surface-Mount | 235 | –40°C to +85°C | OPA4234UA | OPA4234UA |
| OPA4234U | SO-14 Surface-Mount | 235 | –40°C to +85°C | OPA4234U | OPA4234U |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with -250 and -2500 are available only in Tape & Reel in the quantity indicated (e. g., -250 indicates 250 devices per reel). Ordering 2500 pieces of "OPA234EA-2500" will get a single 2500 piece Tape & Reel. For detailed Tape & Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book. (3) The grade will be marked on the Reel.



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# OPA237
# OPA2237
# OPA4237

www.burr-brown.com/databook/OPA237.html

# SINGLE-SUPPLY OPERATIONAL AMPLIFIERS
## *MicroAmplifier*™ Series

## FEATURES

- MICRO-SIZE, MINIATURE PACKAGES
  - Single: SOT-23-5, SO-8
  - Dual: MSOP-8, SO-8
  - Quad: SSOP-16
- LOW OFFSET VOLTAGE: 750µV max
- WIDE SUPPLY RANGE
  - Single Supply: +2.7V to +36V
  - Dual Supply: ±1.35V to ±18V
- LOW QUIESCENT CURRENT: 350µA max
- WIDE BANDWIDTH: 1.5MHz

## APPLICATIONS

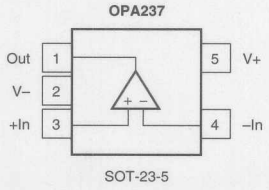
- BATTERY POWERED INSTRUMENTS
- PORTABLE DEVICES
- PCMCIA CARDS
- MEDICAL INSTRUMENTS
- TEST EQUIPMENT

## DESCRIPTION

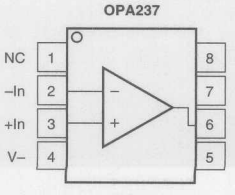
The OPA237 op amp family is one of Burr-Brown's *MicroAmplifier*™ series of miniature products. In addition to small size, these devices feature low offset voltage, low quiescent current, low bias current, and a wide supply range. Single, dual, and quad versions have identical specifications for maximum design flexibility. They are ideal for single supply, battery operated, and space-limited applications, such as PCMCIA cards and other portable instruments.

OPA237 series op amps can operate from either single or dual supplies. When operated from a single supply, the input common-mode range extends below ground and the output can swing to within 10mV of ground. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

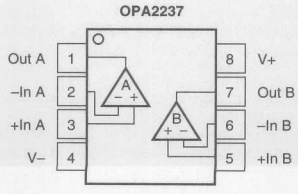
Single, dual, and quad are offered in space-saving surface-mount packages. The single version is available in the ultra-miniature 5-lead SOT-23-5 and SO-8 surface-mount. The dual version comes in a miniature MSOP-8 and SO-8 surface-mount. The quad is available in an SSOP-16. The SSOP-16 has the same body size as an SO-8 with 16 leads, while the MSOP-8 has the same lead count as a SO-8 but half the size. The SOT-23-5 is even smaller at one-fourth the size of an SO-8. All are specified for –40°C to +85°C operation. A macromodel is available for design analysis.



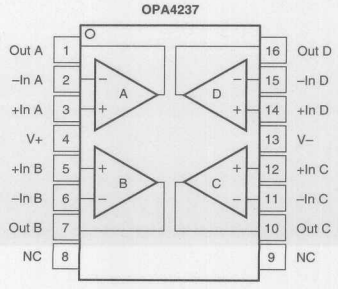

SOT-23-5




SO-8




SO-8, MSOP-8




SSOP-16

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132



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# SPECIFICATIONS: $V_S$ = +5V

At $T_A$ = +25°C, $V_S$ = +5V, $R_L$ = 10kΩ connected to $V_S$/2, unless otherwise noted.

| PARAMETER | CONDITION | OPA237UA, NA OPA2237UA, EA OPA4237UA MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | $V_{CM}$ = 2.5V | | ±250 | ±750 | µV |
| vs Temperature[1] | Specified Temperature Range | | ±2 | ±5 | µV/°C |
| vs Power Supply (PSRR) | $V_S$ = +2.7V to +36V | | 10 | 30 | µV/V |
| Channel Separation (dual and quad) | | | 0.5 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | |
| Input Bias Current[2] | $V_{CM}$ = 2.5V | | –10 | –40 | nA |
| Input Offset Current | $V_{CM}$ = 2.5V | | ±0.5 | ±10 | nA |
| **NOISE** | | | | | |
| Input Voltage Noise, f = 0.1 to 10Hz | | | 1 | | µVp-p |
| Input Voltage Noise Density, f = 1kHz | | | 28 | | $nV/\sqrt{Hz}$ |
| Current Noise Density, f = 1kHz | | | 60 | | $fA/\sqrt{Hz}$ |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Voltage Range | | –0.2 | | (V+) –1.5 | V |
| Common-Mode Rejection | $V_{CM}$ = –0.2V to 3.5V | 78 | 86 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $5 \cdot 10^6$ ‖ 4 | | Ω ‖ pF |
| Common-Mode | | | $5 \cdot 10^9$ ‖ 2 | | Ω ‖ pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | $V_O$ = 0.5V to 4V | 80 | 88 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product | | | 1.4 | | MHz |
| Slew Rate | G = 1 | | 0.5 | | V/µs |
| Settling Time: 0.1% | G = –1, 3V Step, $C_L$ = 100pF | | 11 | | µs |
| 0.01% | G = –1, 3V Step, $C_L$ = 100pF | | 16 | | µs |
| **OUTPUT** | | | | | |
| Voltage Output, Positive | $R_L$ = 100kΩ to Ground | (V+) –1 | (V+) –0.75 | | V |
| Negative | $R_L$ = 100kΩ to Ground | 0.01 | 0.001 | | V |
| Positive | $R_L$ = 100kΩ to 2.5V | (V+) –1 | (V+) –0.75 | | V |
| Negative | $R_L$ = 100kΩ to 2.5V | 0.12 | 0.04 | | V |
| Positive | $R_L$ = 10kΩ to 2.5V | (V+) –1 | (V+) –0.75 | | V |
| Negative | $R_L$ = 10kΩ to 2.5V | 0.5 | 0.35 | | V |
| Short-Circuit Current | | | –10/+4 | | mA |
| Capacitive Load Drive (stable operation) | | | See Typical Curves | | |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | +5 | | V |
| Operating Range | | +2.7 | | +36 | V |
| Quiescent Current (per amplifier) | | | 170 | 350 | µA |
| **TEMPERATURE RANGE** | | | | | |
| Specified Range | | –40 | | +85 | °C |
| Operating Range | | –55 | | +125 | °C |
| Storage | | –55 | | +125 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| 5-Lead SOT-23-5 | | | 200 | | °C/W |
| MSOP-8 Surface-Mount | | | 150 | | °C/W |
| SSOP-16 Surface-Mount | | | 150 | | °C/W |
| SO-8 Surface-Mount | | | 150 | | °C/W |

NOTES: (1) Guaranteed by wafer-level test to 95% confidence. (2) Positive conventional current flows into the input terminals.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

At $T_A$ = +25°C, $V_S$ = +2.7V, $R_L$ = 10kΩ connected to $V_S$/2, unless otherwise noted.

| PARAMETER | CONDITION | OPA237UA, NA OPA2237UA, EA OPA4237UA MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | $V_{CM}$ = 1V | | ±250 | ±750 | µV |
| vs Temperature[1] | Specified Temperature Range | | ±2 | ±5 | µV/°C |
| vs Power Supply (PSRR) | $V_S$ = +2.7V to +36V | | 10 | 30 | µV/V |
| Channel Separation (dual and quad) | | | 0.5 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | |
| Input Bias Current[2] | $V_{CM}$ = 1V | | –10 | –40 | nA |
| Input Offset Current | $V_{CM}$ = 1V | | ±0.5 | ±10 | nA |
| **NOISE** | | | | | |
| Input Voltage Noise, f = 0.1 to 10Hz | | | 1 | | µVp-p |
| Input Voltage Noise Density, f = 1kHz | | | 28 | | nV/√Hz |
| Current Noise Density, f = 1kHz | | | 60 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Voltage Range | | –0.2 | | (V+) –1.5 | V |
| Common-Mode Rejection | $V_{CM}$ = –0.2V to 1.2V | 75 | 85 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $5 \cdot 10^6$ \|\| 4 | | Ω \|\| pF |
| Common-Mode | | | $5 \cdot 10^9$ \|\| 2 | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | $V_O$ = 0.5V to 1.7V | 80 | 88 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product | | | 1.2 | | MHz |
| Slew Rate | G = 1 | | 0.5 | | V/µs |
| Settling Time: 0.1% | G = –1, 1V Step, $C_L$ = 100pF | | 5 | | µs |
| 0.01% | G = –1, 1V Step, $C_L$ = 100pF | | 8 | | µs |
| **OUTPUT** | | | | | |
| Voltage Output, Positive | $R_L$ = 100kΩ to Ground | (V+) –1 | (V+) –0.75 | | V |
| Negative | $R_L$ = 100kΩ to Ground | 0.01 | 0.001 | | V |
| Positive | $R_L$ = 100kΩ to 1.35V | (V+) –1 | (V+) –0.75 | | V |
| Negative | $R_L$ = 100kΩ to 1.35V | 0.06 | 0.02 | | V |
| Positive | $R_L$ = 10kΩ to 1.35V | (V+) –1 | (V+) –0.75 | | V |
| Negative | $R_L$ = 10kΩ to 1.35V | 0.3 | 0.2 | | V |
| Short-Circuit Current | | | –5/+3.5 | | mA |
| Capacitive Load Drive (stable operation) | | | See Typical Curves | | |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | +2.7 | | V |
| Operating Range | | +2.7 | | +36 | V |
| Quiescent Current (per amplifier) | | | 160 | 350 | µA |
| **TEMPERATURE RANGE** | | | | | |
| Specified Range | | –40 | | +85 | °C |
| Operating Range | | –55 | | +125 | °C |
| Storage | | –55 | | +125 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| 5-Lead SOT-23-5 | | | 200 | | °C/W |
| MSOP-8 Surface-Mount | | | 150 | | °C/W |
| SSOP-16 Surface-Mount | | | 150 | | °C/W |
| SO-8 Surface-Mount | | | 150 | | °C/W |

NOTES: (1) Guaranteed by wafer-level test to 95% confidence. (2) Positive conventional current flows into the input terminals.

## SPECIFICATIONS: $V_S$ = ±15V

At $T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 10kΩ connected to $V_S$/2, unless otherwise noted.

| PARAMETER | CONDITION | OPA237UA, NA<br>OPA2237UA, EA<br>OPA4237UA<br>MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0V | | ±350 | ±950 | µV |
| vs Temperature[1] | Specified Temperature Range | | ±2.5 | ±7 | µV/°C |
| vs Power Supply (PSRR) | $V_S$ = ±1.35V to ±18V | | 10 | 30 | µV/V |
| Channel Separation (dual and quad) | | | 0.5 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | |
| Input Bias Current[2] | $V_{CM}$ = 0V | | –8.5 | –40 | nA |
| Input Offset Current | $V_{CM}$ = 0V | | ±0.5 | ±10 | nA |
| **NOISE** | | | | | |
| Input Voltage Noise, f = 0.1 to 10Hz | | | 1 | | µVp-p |
| Input Voltage Noise Density, f = 1kHz | | | 28 | | nV/√Hz |
| Current Noise Density, f = 1kHz | | | 60 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Voltage Range | | (V–) –0.2 | | (V+) –1.5 | V |
| Common-Mode Rejection | $V_{CM}$ = –15V to 13.5V | 80 | 90 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $5 \cdot 10^6$ \|\| 4 | | Ω \|\| pF |
| Common-Mode | | | $5 \cdot 10^9$ \|\| 2 | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | $V_O$ = –14V to 13.8V | 80 | 88 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product | | | 1.5 | | MHz |
| Slew Rate | G = 1 | | 0.5 | | V/µs |
| Settling Time: 0.1% | G = –1, 10V Step, $C_L$ = 100pF | | 18 | | µs |
| 0.01% | G = –1, 10V Step, $C_L$ = 100pF | | 21 | | µs |
| **OUTPUT** | | | | | |
| Voltage Output, Positive | $R_L$ = 100kΩ | (V+) –1.2 | (V+) –0.9 | | V |
| Negative | $R_L$ = 100kΩ | (V–) +0.5 | (V–) +0.3 | | V |
| Positive | $R_L$ = 10kΩ | (V+) –1.2 | (V+) –0.9 | | V |
| Negative | $R_L$ = 10kΩ | (V–) +1 | (V–) +0.85 | | V |
| Short-Circuit Current | | | –8/+4.5 | | mA |
| Capacitive Load Drive (stable operation) | | | See Typical Curves | | |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±15 | | V |
| Operating Range | | ±1.35 | | ±18 | V |
| Quiescent Current (per amplifier) | | | ±200 | ±475 | µA |
| **TEMPERATURE RANGE** | | | | | |
| Specified Range | | –40 | | +85 | °C |
| Operating Range | | –55 | | +125 | °C |
| Storage | | –55 | | +125 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| 5-Lead SOT-23-5 | | | 200 | | °C/W |
| MSOP-8 Surface-Mount | | | 150 | | °C/W |
| SSOP-16 Surface-Mount | | | 150 | | °C/W |
| SO-8 Surface-Mount | | | 150 | | °C/W |

NOTES: (1) Guaranteed by wafer-level test to 95% confidence. (2) Positive conventional current flows into the input terminals.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER[2] |
|---|---|---|---|---|---|
| **Single** | | | | | |
| OPA237NA | 5-Lead SOT-23-5 | 331 | –40°C to +85°C | A37A | OPA237NA-250 |
| " | " | " | " | " | OPA237NA-3K |
| OPA237UA | SO-8 Surface-Mount | 182 | –40°C to +85°C | OPA237UA | OPA237UA |
| **Dual** | | | | | |
| OPA2237EA | MSOP-8 Surface-Mount | 337 | –40°C to +85°C | B37A | OPA2237EA-250 |
| " | " | " | " | " | OPA2237EA-2500 |
| OPA2237UA | SO-8 Surface-Mount | 182 | –40°C to +85°C | OPA2237UA | OPA2237UA |
| **Quad** | | | | | |
| OPA4237UA | SSOP-16 Surface-Mount | 322 | –40°C to +85°C | OPA4237UA | OPA4237UA-250 |
| " | " | " | " | " | OPA4237UA-2500 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with -250, -2500, and -3K are available only in Tape and Reel in the quantity indicated (e.g., -250 indicates 250 devices per reel). Ordering 3000 pieces of "OPA237NA-3K" will get a single 3000 piece Tape and Reel. SO-8 models are available in tubes or Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, V+ to V– | 36V |
| Input Voltage | (V–) –0.7V to (V+) +0.7V |
| Output Short-Circuit[1] | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | 300°C |

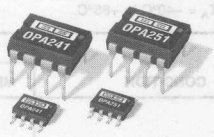
NOTE: (1) Short circuit to ground, one amplifier per package.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®




# OPA241
# OPA251

www.burr-brown.com/databook/OPA241.html

# Single-Supply, *Micro*POWER OPERATIONAL AMPLIFIERS

## FEATURES

- *Micro*POWER: $I_Q$ = 24μA
- SINGLE SUPPLY OPERATION
- RAIL-TO-RAIL OUTPUT SWING
- WIDE SUPPLY RANGE
  Single Supply: +2.7V to +36V
  Dual Supply: ±1.35V to ±18V
- LOW OFFSET VOLTAGE: ±250μV max
- HIGH COMMON-MODE REJECTION: 124dB
- HIGH OPEN-LOOP GAIN: 128dB
- 8-PIN DIP AND SO-8 PACKAGES

## APPLICATIONS

- BATTERY OPERATED INSTRUMENTS
- PORTABLE DEVICES
- MEDICAL INSTRUMENTS
- TEST EQUIPMENT

## DESCRIPTION

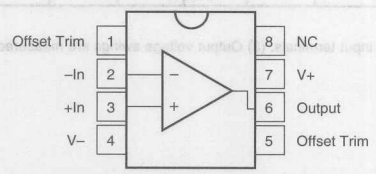
The OPA241 and OPA251 are specifically designed for battery powered, portable applications. In addition to very low power consumption (24μA), these amplifiers feature low offset voltage, rail-to-rail output swing, high common-mode rejection, and high open-loop gain.

The OPA241 is optimized for operation at low power supply voltage while the OPA251 is optimized for high power supplies. Both op amps can operate from either single (+2.7V to +36V) or dual supplies (±1.35V to ±18V). The input common-mode voltage range extends 200mV below the negative supply—ideal for single supply applications.

The OPA241 and OPA251 are unity-gain stable and can drive large capacitive loads. Special design considerations assure that these products are easy to use. High performance is maintained as the amplifiers swing to their specified limits. Because the initial offset voltage (±250μV max) is so low, user adjustment is usually not required. However, external trim pins are provided for special applications.

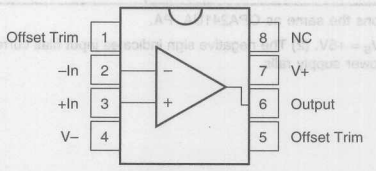
The OPA241 and OPA251 are available in standard 8-pin DIP and SO-8 surface-mount packages. Both are fully specified from –40°C to +85°C and operate from –55°C to +125°C.

OPA241




8-Pin DIP, SO-8

OPA251




8-Pin DIP, SO-8

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# SPECIFICATIONS: $V_S$ = 2.7V to 5V

At $T_A$ = +25°C, $R_L$ = 100kΩ connected to $V_S$/2, unless otherwise noted.
**Boldface** limits apply over the specified temperature range, $T_A$ = –40°C to +85°C.

| PARAMETER | | CONDITION | OPA241UA, PA MIN | OPA241UA, PA TYP[1] | OPA241UA, PA MAX | OPA251UA, PA MIN | OPA251UA, PA TYP[1] | OPA251UA, PA MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | | | |
| Input Offset Voltage | $V_{OS}$ | | | ±50 | ±250 | | ±100 | | µV |
| **$T_A$ = –40°C to +85°C** | | | | **±100** | **±400** | | **±130** | | µV |
| **vs Temperature** | $dV_{OS}/dT$ | $T_A$ = –40°C to +85°C | | **±0.4** | | | **±0.6** | | µV/°C |
| vs Power Supply | PSRR | $V_S$ = 2.7V to 36V | | 3 | 30 | | * | * | µV/V |
| **$T_A$ = –40°C to +85°C** | | $V_S$ = 2.7V to 36V | | | **30** | | | * | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | | | |
| Input Bias Current[2] | $I_B$ | | | –4 | –20 | | * | * | nA |
| **$T_A$ = –40°C to +85°C** | | | | | **–25** | | | * | nA |
| Input Offset Current | $I_{OS}$ | | | ±0.1 | ±2 | | * | * | nA |
| **$T_A$ = –40°C to +85°C** | | | | | **±2** | | | * | nA |
| **NOISE** | | | | | | | | | |
| Input Voltage Noise, f = 0.1 to 10kHz | | | | 1 | | | * | | µVp-p |
| Input Voltage Noise Density, f = 1kHz | $e_n$ | | | 45 | | | * | | $nV/\sqrt{Hz}$ |
| Current Noise Density, f = 1kHz | $i_n$ | | | 40 | | | * | | $fA/\sqrt{Hz}$ |
| **INPUT VOLTAGE RANGE** | | | | | | | | | |
| Common-Mode Voltage Range | $V_{CM}$ | | –0.2 | | (V+) –1 | | | | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = –0.2V to (V+) –1V | 80 | 106 | | | * | | dB |
| **$T_A$ = –40°C to +85°C** | | $V_{CM}$ = 0V to (V+) –1V | **80** | | | | | | dB |
| **INPUT IMPEDANCE** | | | | | | | | | |
| Differential | | | | $10^7$ II 2 | | | * | | Ω II pF |
| Common-Mode | | | | $10^9$ II 4 | | | * | | Ω II pF |
| **OPEN-LOOP GAIN** | | | | | | | | | |
| Open-Loop Voltage Gain | $A_{OL}$ | $R_L$ = 100kΩ, $V_O$ = (V–)+100mV to (V+)–100mV | 100 | 120 | | | * | | dB |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 100kΩ, $V_O$ = (V–)+100mV to (V+)–100mV | **100** | | | | | | dB |
| | | $R_L$ = 10kΩ, $V_O$ = (V–)+200mV to (V+)–200mV | 100 | 120 | | | * | | dB |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 10kΩ, $V_O$ = (V–)+200mV to (V+)–200mV | **100** | | | | | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | | |
| Gain-Bandwidth Product | GBW | | | 35 | | | * | | kHz |
| Slew Rate | SR | $V_S$ = 5V, G = 1 | | 0.01 | | | * | | V/µs |
| Overload Recovery Time | | $V_{IN}$ • G = $V_S$ | | 60 | | | * | | µs |
| **OUTPUT** | | | | | | | | | |
| Voltage Output Swing from Rail[3] | | $R_L$ = 100kΩ to $V_S$/2, $A_{OL}$ ≥ 70dB | | 50 | | | * | | mV |
| | | $R_L$ = 100kΩ to $V_S$/2, $A_{OL}$ ≥ 100dB | | 75 | 100 | | * | | mV |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 100kΩ to $V_S$/2, $A_{OL}$ ≥ 96dB | | | **100** | | | | mV |
| | | $R_L$ = 10kΩ to $V_S$/2, $A_{OL}$ ≥ 100dB | | 100 | 200 | | * | | mV |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 10kΩ to $V_S$/2, $A_{OL}$ ≥ 96dB | | | **200** | | | | mV |
| Short-Circuit Current | $I_{SC}$ | | | –24/+4 | | | * | | mA |
| Capacitive Load Drive | $C_{LOAD}$ | See Typical Curve | | | | | * | | |
| **POWER SUPPLY** | | | | | | | | | |
| Specified Voltage Range | $V_S$ | | | +2.7 to +5 | | | * | | V |
| Operating Voltage Range | | | +2.7 | | +36 | * | | * | V |
| Quiescent Current | $I_Q$ | $I_O$ = 0 | | ±24 | ±28 | | * | | µA |
| **$T_A$ = –40°C to +85°C** | | $I_O$ = 0 | | | **±34** | | | | µA |
| **TEMPERATURE RANGE** | | | | | | | | | |
| Specified Range | | | –40 | | +85 | * | | * | °C |
| Operating Range | | | –55 | | +125 | * | | * | °C |
| Storage Range | | | –55 | | +125 | * | | * | °C |
| Thermal Resistance | $\theta_{JA}$ | | | | | | | | |
| 8-Pin DIP | | | | 100 | | | * | | °C/W |
| SO-8 Surface Mount | | | | 150 | | | * | | °C/W |

* Specifications the same as OPA241UA, PA.

NOTES: (1) $V_S$ = +5V. (2) The negative sign indicates input bias current flows out of the input terminals. (3) Output voltage swings are measured between the output and power supply rails.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

# SPECIFICATIONS: $V_S$ = ±15V

At $T_A$ = +25°C, $R_L$ = 100kΩ connected to ground, unless otherwise noted.
**Boldface** limits apply over the specified temperature range, $T_A$ = –40°C to +85°C.

| PARAMETER | | CONDITION | OPA241UA, PA | | | OPA251UA, PA | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OFFSET VOLTAGE** | | | | | | | | | |
| Input Offset Voltage | $V_{OS}$ | | | ±100 | | | ±50 | ±250 | µV |
| **$T_A$ = –40°C to +85°C** | | | | **±150** | | | **±100** | **±300** | µV |
| **vs Temperature** | $dV_{OS}/dT$ | $T_A$ = –40°C to +85°C | | **±0.6** | | | **±0.5** | | µV/°C |
| vs Power Supply | PSRR | $V_S$ = ±1.35V to ±18V | | * | * | | 3 | 30 | µV/V |
| **$T_A$ = –40°C to +85°C** | | $V_S$ = ±1.35V to ±18V | | | * | | | **30** | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | | | |
| Input Bias Current[1] | $I_B$ | | | * | * | | –4 | –20 | nA |
| **$T_A$ = –40°C to +85°C** | | | | | * | | | **–25** | nA |
| Input Offset Current | $I_{OS}$ | | | * | * | | ±0.1 | ±2 | nA |
| **$T_A$ = –40°C to +85°C** | | | | | * | | | **±2** | nA |
| **NOISE** | | | | | | | | | |
| Input Voltage Noise, f = 0.1 to 10kHz | | | | * | | | 1 | | µVp-p |
| Input Voltage Noise Density, f = 1kHz | $e_n$ | | | * | | | 45 | | nV/√Hz |
| Current Noise Density, f = 1kHz | $i_n$ | | | * | | | 40 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | | | | |
| Common-Mode Voltage Range | $V_{CM}$ | | | | | (V–) –0.2 | | (V+) –1 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = –15.2V to 14V | | * | | 100 | 124 | | dB |
| **$T_A$ = –40°C to +85°C** | | $V_{CM}$ = –15V to 14V | | | | **100** | | | dB |
| **INPUT IMPEDANCE** | | | | | | | | | |
| Differential | | | | * | | | $10^6$ ‖ 2 | | Ω ‖ pF |
| Common-Mode | | | | * | | | $10^6$ ‖ 4 | | Ω ‖ pF |
| **OPEN-LOOP GAIN** | | | | | | | | | |
| Open-Loop Voltage Gain | $A_{OL}$ | $R_L$ = 100kΩ, $V_O$ = –14.75V to +14.75V | | * | | 100 | 128 | | dB |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 100kΩ, $V_O$ = –14.75V to +14.75V | | | | **100** | | | dB |
| | | $R_L$ = 20kΩ, $V_O$ = –14.7V to +14.7V | | * | | 100 | 128 | | dB |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 20kΩ, $V_O$ = –14.7V to +14.7V | | | | **100** | | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | | |
| Gain-Bandwidth Product | GBW | | | * | | | 35 | | kHz |
| Slew Rate | SR | G = 1 | | * | | | 0.01 | | V/µs |
| Overload Recovery Time | | $V_{IN}$ • G = $V_S$ | | * | | | 60 | | µs |
| **OUTPUT** | | | | | | | | | |
| Voltage Output Swing from Rail[2] | | $R_L$ = 100kΩ, $A_{OL}$ ≥ 70dB | | * | | | 50 | | mV |
| | | $R_L$ = 100kΩ, $A_{OL}$ ≥ 100dB | | * | | | 75 | 250 | mV |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 100kΩ, $A_{OL}$ ≥ 96dB | | | | | | **250** | mV |
| | | $R_L$ = 20kΩ, $A_{OL}$ ≥ 100dB | | * | | | 100 | 300 | mV |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 20kΩ, $A_{OL}$ ≥ 96dB | | | | | | **300** | mV |
| Short-Circuit Current | $I_{SC}$ | | | * | | | –21/+4 | | mA |
| Capacitive Load Drive | $C_{LOAD}$ | | | * | | | See Typical Curve | | |
| **POWER SUPPLY** | | | | | | | | | |
| Specified Voltage Range | $V_S$ | | | * | | | ±15 | | V |
| Operating Voltage Range | | | * | | * | ±1.35 | | ±18 | V |
| Quiescent Current | $I_Q$ | $I_O$ = 0 | | * | | | ±27 | ±38 | µA |
| **$T_A$ = –40°C to +85°C** | | $I_O$ = 0 | | | | | | **±45** | µA |
| **TEMPERATURE RANGE** | | | | | | | | | |
| Specified Range | | | * | | * | –40 | | +85 | °C |
| Operating Range | | | * | | * | –55 | | +125 | °C |
| Storage Range | | | * | | * | –55 | | +125 | °C |
| Thermal Resistance | $\theta_{JA}$ | | | | | | | | |
| 8-Pin DIP | | | | * | | | 100 | | °C/W |
| SO-8 Surface Mount | | | | * | | | 150 | | °C/W |

* Specifications the same as OPA251UA, PA.

NOTES: (1) The negative sign indicates input bias current flows out of the input terminals. (2) Output voltage swings are measured between the output and power supply rails.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Supply Voltage, V+ to V– | 36V |
| Input Voltage[2] | (V–) –0.5V to (V+) +0.5V |
| Output Short Circuit to Ground | Continuous |
| Operating Temperature | –55°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering, 10s) | 300°C |

NOTES: (1) Stresses above these ratings may cause permanent damage. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more that 0.5V beyond the supply rails should be current-limited to 5mA or less.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| OPA241PA | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| OPA241UA | SO-8 Surface Mount | 182 | –40°C to +85°C |
| OPA251PA | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| OPA251UA | SO-8 Surface Mount | 182 | –40°C to +85°C |

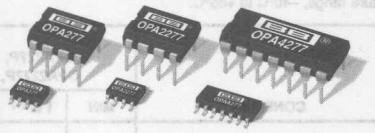
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®



# OPA277
# OPA2277
# OPA4277

## High Precision OPERATIONAL AMPLIFIERS

## FEATURES

- ULTRA LOW OFFSET VOLTAGE: 10µV
- ULTRA LOW DRIFT: ±0.1µV/°C
- HIGH OPEN-LOOP GAIN: 134dB
- HIGH COMMON-MODE REJECTION: 140dB
- HIGH POWER SUPPLY REJECTION: 130dB
- LOW BIAS CURRENT: 1nA max
- WIDE SUPPLY RANGE: ±2V to ±18V
- LOW QUIESCENT CURRENT: 800µA/amp
- SINGLE, DUAL, AND QUAD VERSIONS
- REPLACES OP-07, OP-77, OP-177

## APPLICATIONS

- TRANSDUCER AMPLIFIER
- BRIDGE AMPLIFIER
- TEMPERATURE MEASUREMENTS
- STRAIN GAGE AMPLIFIER
- PRECISION INTEGRATOR
- BATTERY POWERED INSTRUMENTS
- TEST EQUIPMENT

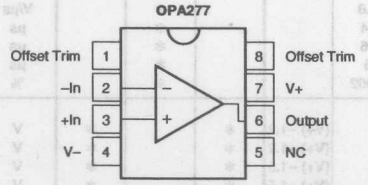
## DESCRIPTION

The OPA277 series precision op amps replace the industry standard OP-177. They offer improved noise, wider output voltage swing, and are twice as fast with half the quiescent current. Features include ultra low offset voltage and drift, low bias current, high common-mode rejection, and high power supply rejection. Single, dual, and quad versions have identical specifications for maximum design flexibility.

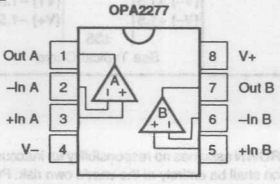
OPA277 series op amps operate from ±2V to ±18V supplies with excellent performance. Unlike most op amps which are specified at only one supply voltage, the OPA277 series is specified for real-world applications; a single limit applies over the ±5V to ±15V supply range. High performance is maintained as the amplifiers swing to their specified limits. Because the initial offset voltage (±20µV max) is so low, user adjustment is usually not required. However, the single version (OPA277) provides external trim pins for special applications.

OPA277 op amps are easy to use and free from phase inversion and overload problems found in some other op amps. They are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions. Dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

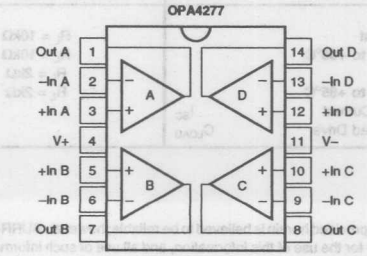
Single (OPA277) and dual (OPA2277) versions are available in 8-pin DIP and SO-8 surface-mount packages. The quad (OPA4277) comes in 14-pin DIP and SO-14 surface-mount packages. All are fully specified from –40°C to +85°C and operate from –55°C to +125°C.




8-Pin DIP, SO-8




8-Pin DIP, SO-8




14-Pin DIP, SO-14

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# SPECIFICATIONS: $V_S$ = ±5V to $V_S$ = ±15V

At $T_A$ = +25°C, and $R_L$ = 2kΩ, unless otherwise noted.
**Boldface** limits apply over the specified temperature range, –40°C to +85°C.

| PARAMETER | CONDITION | OPA277P, U OPA2277P, U | | | OPA277PA, UA OPA2277PA, UA OPA4277PA, UA | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP[1] | MAX | MIN | TYP[1] | MAX | |
| **OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage: $V_{OS}$ | | | | | | | | |
| OPA277P, U (high grade, single) | | | ±10 | ±20 | | | | µV |
| OPA2277P, U (high grade, dual) | | | ±10 | ±25 | | | | µV |
| All PA, UA Versions | | | | | | ±20 | ±50 | µV |
| **Input Offset Voltage Over Temperature** | | | | | | | | |
| OPA277P, U (high grade, single) | **$T_A$ = –40°C to +85°C** | | | **±30** | | | | µV |
| OPA2277P, U (high grade, dual) | **$T_A$ = –40°C to +85°C** | | | **±50** | | | | µV |
| All PA, UA Versions | **$T_A$ = –40°C to +85°C** | | | | | | **±100** | µV |
| **Input Offset Voltage Drift** $dV_{OS}/dT$ | | | | | | | | |
| OPA277P, U (high grade, single) | **$T_A$ = –40°C to +85°C** | | **±0.1** | **±0.15** | | | | µV/°C |
| OPA2277P, U (high grade, dual) | **$T_A$ = –40°C to +85°C** | | **±0.1** | **±0.25** | | | | µV/°C |
| All PA, UA Versions | **$T_A$ = –40°C to +85°C** | | | | | **±0.15** | **±1** | µV/°C |
| Input Offset Voltage: (all models) | | | | | | | | |
| vs Time | | | 0.2 | | | * | | µV/mo |
| vs Power Supply PSRR | $V_S$ = ±2V to ±18V | | ±0.3 | ±0.5 | | * | ±1 | µV/V |
| **$T_A$ = –40°C to +85°C** | $V_S$ = ±2V to ±18V | | | **±0.5** | | | **±1** | µV/V |
| Channel Separation (dual, quad) | dc | | 0.1 | | | * | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | | |
| Input Bias Current $I_B$ | | | ±0.5 | ±1 | | * | ±2.8 | nA |
| **$T_A$ = –40°C to +85°C** | | | | **±2** | | | **±4** | nA |
| Input Offset Current $I_{OS}$ | | | ±0.5 | ±1 | | * | ±2.8 | nA |
| **$T_A$ = –40°C to +85°C** | | | | **±2** | | | **±4** | nA |
| **NOISE** | | | | | | | | |
| Input Voltage Noise, f = 0.1 to 10Hz | | | 0.22 | | | * | | µVp-p |
| | | | 0.11 | | | * | | µVrms |
| Input Voltage Noise Density, f = 10Hz $e_n$ | | | 12 | | | * | | nV/√Hz |
| f = 100Hz | | | 8 | | | * | | nV/√Hz |
| f = 1kHz | | | 8 | | | * | | nV/√Hz |
| f = 10kHz | | | 8 | | | * | | nV/√Hz |
| Current Noise Density, f = 1kHz $i_n$ | | | 0.2 | | | * | | pA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Voltage Range $V_{CM}$ | | (V–) +2 | | (V+) –2 | * | | * | V |
| Common-Mode Rejection CMRR | $V_{CM}$ = (V–) +2V to (V+) –2V | 130 | 140 | | 115 | * | | dB |
| **$T_A$ = –40°C to +85°C** | $V_{CM}$ = (V–) +2V to (V+) –2V | **128** | | | **115** | | | dB |
| **INPUT IMPEDANCE** | | | | | | | | |
| Differential | | | 100 ll 3 | | | * | | MΩ ll pF |
| Common-Mode | $V_{CM}$ = (V–) +2V to (V+) –2V | | 250 ll 3 | | | * | | GΩ ll pF |
| **OPEN-LOOP GAIN** | | | | | | | | |
| Open-Loop Voltage Gain $A_{OL}$ | $V_O$ = (V–)+0.5V to (V+)–1.2V, $R_L$ = 10kΩ | | 140 | | | * | | dB |
| | $V_O$ = (V–)+0.5V to (V+)–1.5V, $R_L$ = 2kΩ | 126 | 134 | | * | * | | dB |
| **$T_A$ = –40°C to +85°C** | $V_O$ = (V–)+0.5V to (V+)–1.5V, $R_L$ = 2kΩ | **126** | | | * | | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Gain-Bandwidth Product GBW | | | 1 | | | * | | MHz |
| Slew Rate SR | | | 0.8 | | | * | | V/µs |
| Settling Time, 0.1% | $V_S$ = ±15V, G = 1, 10V Step | | 14 | | | * | | µs |
| 0.01% | $V_S$ = ±15V, G = 1, 10V Step | | 16 | | | * | | µs |
| Overload Recovery Time | $V_{IN}$ • G = $V_S$ | | 3 | | | * | | µs |
| Total Harmonic Distortion + Noise THD+N | 1kHz, G = 1, $V_O$ = 3.5Vrms | | 0.002 | | | * | | % |
| **OUTPUT** | | | | | | | | |
| Voltage Output | $R_L$ = 10kΩ | (V–) +0.5 | | (V+) –1.2 | * | | * | V |
| **$T_A$ = –40°C to +85°C** | $R_L$ = 10kΩ | **(V–) +0.5** | | **(V+) –1.2** | * | | * | V |
| | $R_L$ = 2kΩ | (V–) +1.5 | | (V+) –1.5 | * | | * | V |
| **$T_A$ = –40°C to +85°C** | $R_L$ = 2kΩ | **(V–) +1.5** | | **(V+) –1.5** | * | | * | V |
| Short-Circuit Current $I_{SC}$ | | | ±35 | | | * | | mA |
| Capacitive Load Drive $C_{LOAD}$ | | See Typical Curve | | | | * | | |

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## SPECIFICATIONS: $V_S$ = ±5V to $V_S$ = ±15V (CONT)

At $T_A$ = +25°C, and $R_L$ = 2kΩ, unless otherwise noted.
**Boldface** limits apply over the specified temperature range, –40°C to +85°C.

| PARAMETER | | CONDITION | OPA277P, U OPA2277P, U MIN | OPA277P, U OPA2277P, U TYP(1) | OPA277P, U OPA2277P, U MAX | OPA277PA, UA OPA2277PA, UA OPA4277PA, UA MIN | OPA277PA, UA OPA2277PA, UA OPA4277PA, UA TYP(1) | OPA277PA, UA OPA2277PA, UA OPA4277PA, UA MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | | | |
| Specified Voltage Range | $V_S$ | | ±5 | | ±15 | * | | * | V |
| Operating Voltage Range | | | ±2 | | ±18 | * | | * | V |
| Quiescent Current (per amplifier) | $I_Q$ | $I_O$ = 0 | | ±790 | ±825 | | * | * | µA |
| $T_A$ = –40°C to +85°C | | $I_O$ = 0 | | | **±900** | | | * | µA |
| **TEMPERATURE RANGE** | | | | | | | | | |
| Specified Range | | | –40 | | 85 | * | | * | °C |
| Operating Range | | | –55 | | 125 | * | | * | °C |
| Storage Range | | | –55 | | 125 | * | | * | °C |
| Thermal Resistance | $\theta_{JA}$ | | | | | | | | |
| SO-8 Surface-Mount | | | | 150 | | | * | | °C/W |
| 8-Pin DIP | | | | 100 | | | * | | °C/W |
| 14-Pin DIP | | | | 80 | | | * | | °C/W |
| SO-14 Surface-Mount | | | | 100 | | | * | | °C/W |

* Specifications same as OPA277P, U.

NOTE: (1) $V_S$ = ±15V.

### ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|---|
| Supply Voltage | 36V |
| Input Voltage | (V–) –0.7V to (V+) +0.7V |
| Output Short-Circuit(2) | Continuous |
| Operating Temperature | –55°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering, 10s) | 300°C |

NOTE: (1) Stresses above these rating may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Short-circuit to ground, one amplifier per package.

### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

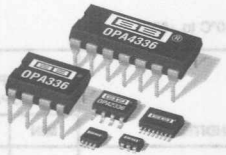
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGE/ORDERING INFORMATION

| PRODUCT | OFFSET VOLTAGE max, µV | OFFSET VOLTAGE DRIFT max, µV/°C | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE | ORDERING NUMBER(2) | TRANSPORT MEDIA |
|---|---|---|---|---|---|---|---|
| **Single** | | | | | | | |
| OPA277PA | ±50 | ±1 | 8-Pin DIP | 006 | –40°C to +85°C | OPA277PA | Rails |
| OPA277P | ±20 | ±0.15 | 8-Pin DIP | 006 | –40°C to +85°C | OPA277P | Rails |
| OPA277UA | ±50 | ±1 | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA277UA | Rails |
| " | " | " | " | " | " | OPA277UA/2K5 | Tape and Reel |
| OPA277U | ±20 | ±0.15 | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA277U | Rails |
| " | " | " | " | " | " | OPA277U/2K5 | Tape and Reel |
| **Dual** | | | | | | | |
| OPA2277PA | ±50 | ±0.25 | 8-Pin DIP | 006 | –40°C to +85°C | OPA2277PA | Rails |
| OPA2277P | ±25 | ±1 | 8-Pin DIP | 006 | –40°C to +85°C | OPA2277P | Rails |
| OPA2277UA | ±50 | ±0.25 | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA2277UA | Rails |
| " | " | " | " | " | " | OPA2277UA/2K5 | Tape and Reel |
| OPA2277U | ±25 | ±1 | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA2277U | Rails |
| " | " | " | " | " | " | OPA2277UA/2K5 | Tape and Reel |
| **Quad** | | | | | | | |
| OPA4277PA | ±50 | ±1 | 14-Pin DIP | 010 | –40°C to +85°C | OPA4277PA | Rails |
| OPA4277UA | ±50 | ±1 | SO-14 Surface Mount | 235 | –40°C to +85°C | OPA4277UA | Rails |
| " | " | " | " | " | " | OPA4277UA/2K5 | Tape and Reel |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Products followed by a slash (/) are only available in Tape and Reel in the quantities indicated (e.g. /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "OPA277UA/2K5" will get a single 2500 piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

BURR - BROWN®



# OPA336
# OPA2336
# OPA4336

www.burr-brown.com/databook/OPA336.html

# SINGLE-SUPPLY, *Micro*POWER CMOS OPERATIONAL AMPLIFIERS
## *MicroAmplifier*™ Series

## FEATURES

- SINGLE SUPPLY OPERATION
- RAIL-TO-RAIL OUTPUT (within 3mV)
- *Micro*POWER: $I_Q$ = 20μA/Amplifier
- *Micro*SIZE PACKAGES
- LOW OFFSET VOLTAGE: 125μV max
- SPECIFIED FROM $V_S$ = 2.3V to 5.5V
- SINGLE, DUAL, AND QUAD VERSIONS(1)

## APPLICATIONS

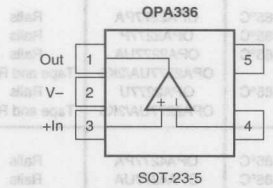
- BATTERY POWERED INSTRUMENTS
- PORTABLE DEVICES
- HIGH IMPEDANCE APPLICATIONS
- PHOTODIODE PRE-AMPS
- PRECISION INTEGRATORS
- MEDICAL INSTRUMENTS
- TEST EQUIPMENT

## DESCRIPTION

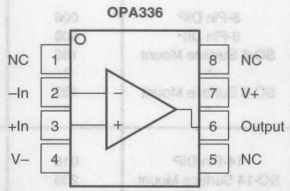
OPA336 series micropower CMOS operational amplifiers are designed for battery powered applications. They operate on a single supply with operation as low as 2.1V. The output is rail-to-rail and swings to within 3mV of the supplies with a 100kΩ load. The common-mode range extends to the negative supply—ideal for single-supply applications. Single, dual, and quad versions have identical specifications for maximum design flexibility.

In addition to small size and low quiescent current (20μA/amplifier), they feature low offset voltage (125μV max), low input bias current (1pA), and high open-loop gain (115dB). Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

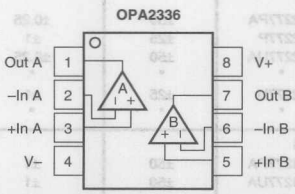
OPA336 packages are the tiny 5-lead SOT-23-5 surface mount, SO-8 surface-mount, and 8-pin DIP. OPA2336 comes in the miniature MSOP-8 surface-mount, SO-8 surface-mount, and 8-pin DIP packages. OPA4336 packages are the space-saving SSOP-16 surface-mount and the 14-pin DIP. All are specified from –40°C to +85°C and operate from –55°C to +125°C. A macromodel is available for design analysis.



SOT-23-5



8-Pin DIP, SO-8



8-Pin DIP, SO-8, MSOP-8

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS: $V_S$ = 2.3V to 5.5V

At $T_A$ = +25°C, and $R_L$ = 25kΩ connected to $V_S$/2, unless otherwise noted.
**Boldface** limits apply over the specified temperature range, –40°C to +85°C. $V_S$ = +5V.

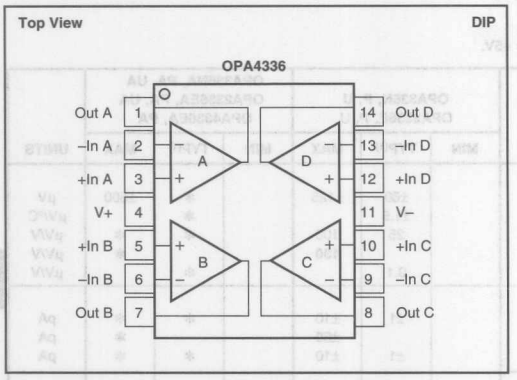
| PARAMETER | | CONDITION | OPA336N, P, U OPA2336E, P, U MIN | OPA336N, P, U OPA2336E, P, U TYP[1] | OPA336N, P, U OPA2336E, P, U MAX | OPA336NA, PA, UA OPA2336EA, PA, UA OPA4336EA, PA MIN | OPA336NA, PA, UA OPA2336EA, PA, UA OPA4336EA, PA TYP[1] | OPA336NA, PA, UA OPA2336EA, PA, UA OPA4336EA, PA MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | | | |
| Input Offset Voltage | $V_{OS}$ | | | ±60 | ±125 | | * | ±500 | µV |
| **vs Temperature** | $dV_{OS}/dT$ | | | **±1.5** | | | * | | µV/°C |
| vs Power Supply | PSRR | $V_S$ = 2.3V to 5.5V | | 25 | 100 | | * | * | µV/V |
| **$T_A$ = –40°C to +85°C** | | $V_S$ = 2.3V to 5.5V | | | **130** | | | * | µV/V |
| Channel Separation, dc | | | | 0.1 | | | * | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | | | |
| Input Bias Current | $I_B$ | | | ±1 | ±10 | | * | * | pA |
| **$T_A$ = –40°C to +85°C** | | | | | **±60** | | | * | pA |
| Input Offset Current | $I_{OS}$ | | | ±1 | ±10 | | * | * | pA |
| **NOISE** | | | | | | | | | |
| Input Voltage Noise, f = 0.1 to 10Hz | | | | 3 | | | * | | µVp-p |
| Input Voltage Noise Density, f = 1kHz | $e_n$ | | | 40 | | | * | | $nV/\sqrt{Hz}$ |
| Current Noise Density, f = 1kHz | $i_n$ | | | 30 | | | * | | $fA/\sqrt{Hz}$ |
| **INPUT VOLTAGE RANGE** | | | | | | | | | |
| Common-Mode Voltage Range | $V_{CM}$ | | –0.2 | | (V+) –1 | * | | * | V |
| Common-Mode Rejection Ratio | CMRR | –0.2V < $V_{CM}$ < (V+) –1V | 80 | 90 | | 76 | 86 | | dB |
| **$T_A$ = –40°C to +85°C** | | –0.2V < $V_{CM}$ < (V+) –1V | **76** | | | **74** | | | dB |
| **INPUT IMPEDANCE** | | | | | | | | | |
| Differential | | | | $10^{13}$ \|\| 2 | | | * | | Ω \|\| pF |
| Common-Mode | | | | $10^{13}$ \|\| 4 | | | * | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | | | | | |
| Open-Loop Voltage Gain | $A_{OL}$ | $R_L$ = 25kΩ, 100mV < $V_O$ < (V+) –100mV | 100 | 115 | | 90 | * | | dB |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 25kΩ, 100mV < $V_O$ < (V+) –100mV | **100** | | | **90** | | | dB |
| | | $R_L$ = 5kΩ, 500mV < $V_O$ < (V+) –500mV | 90 | 106 | | * | * | | dB |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 5kΩ, 500mV < $V_O$ < (V+) –500mV | **90** | | | * | | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | | |
| Gain-Bandwidth Product | GBW | $V_S$ = 5V, G = 1 | | 100 | | | * | | kHz |
| Slew Rate | SR | $V_S$ = 5V, G = 1 | | 0.03 | | | * | | V/µs |
| Overload Recovery Time | | $V_{IN}$ • G = $V_S$ | | 100 | | | * | | µs |
| **OUTPUT** | | | | | | | | | |
| Voltage Output Swing from Rail[2] | | $R_L$ = 100kΩ, $A_{OL}$ ≥ 70dB | | 3 | | | * | | mV |
| | | $R_L$ = 25kΩ, $A_{OL}$ ≥ 90dB | | 20 | 100 | | * | * | mV |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 25kΩ, $A_{OL}$ ≥ 90dB | | | **100** | | | * | mV |
| | | $R_L$ = 5kΩ, $A_{OL}$ ≥ 90dB | | 70 | 500 | | * | * | mV |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 5kΩ, $A_{OL}$ ≥ 90dB | | | **500** | | | * | mV |
| Short-Circuit Current | $I_{SC}$ | | | ±5 | | | * | | mA |
| Capacitive Load Drive | $C_{LOAD}$ | | | See Text | | | * | | pF |
| **POWER SUPPLY** | | | | | | | | | |
| Specified Voltage Range | $V_S$ | | 2.3 | | 5.5 | * | | * | V |
| Minimum Operating Voltage | | | | 2.1 | | | * | | V |
| Quiescent Current (per amplifier) | $I_Q$ | $I_O$ = 0 | | 20 | 32 | | * | * | µA |
| **$T_A$ = –40°C to +85°C** | | $I_O$ = 0 | | | **36** | | | * | µA |
| **TEMPERATURE RANGE** | | | | | | | | | |
| Specified Range | | | –40 | | +85 | * | | * | °C |
| Operating Range | | | –55 | | +125 | * | | * | °C |
| Storage Range | | | –55 | | +125 | * | | * | °C |
| Thermal Resistance | $\theta_{JA}$ | | | | | | | | |
| SOT-23-5 Surface-Mount | | | | 200 | | | * | | °C/W |
| MSOP-8 Surface-Mount | | | | 150 | | | * | | °C/W |
| SO-8 Surface-Mount | | | | 150 | | | * | | °C/W |
| 8-Pin DIP | | | | 100 | | | * | | °C/W |
| SSOP-16 Surface-Mount | | | | 100 | | | * | | °C/W |
| 14-Pin DIP | | | | 80 | | | * | | °C/W |

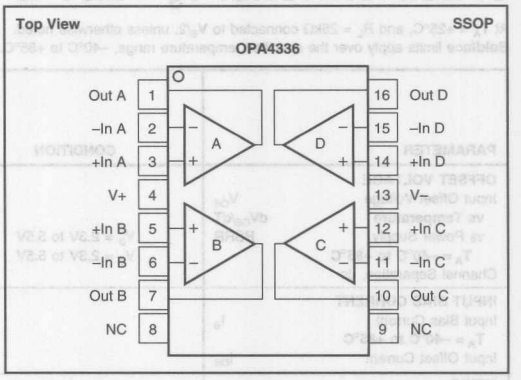
*Specifications same as OPA2336E, P, U.

NOTES: (1) $V_S$ = +5V. (2) Output voltage swings are measured between the output and positive and negative power supply rails.

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## PIN CONFIGURATIONS




## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Supply Voltage | 5.5V |
| Signal Input Terminals, Voltage[2] | (V–) –0.3V to (V+) +0.3V |
| Current[2] | 10mA |
| Output Short-Circuit[3] | Continuous |
| Operating Temperature | –55°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering, 10s) | 300°C |

NOTES: (1) Stresses above these ratings may cause permanent damage. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

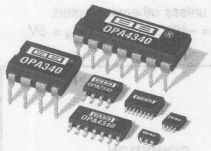
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER[2] | TRANSPORT MEDIA |
|---|---|---|---|---|---|---|
| **Single** | | | | | | |
| OPA336NA | 5-Lead SOT-23-5 | 331 | –40°C to +85°C | A36[3] | OPA336NA-250 | Tape and Reel |
| " | " | " | " | " | OPA336NA-3K | Tape and Reel |
| OPA336N | 5-Lead SOT-23-5 | 331 | –40°C to +85°C | A36[3] | OPA336N-250 | Tape and Reel |
| " | " | " | " | " | OPA336N-3K | Tape and Reel |
| OPA336PA | 8-Pin DIP | 006 | –40°C to +85°C | OPA336PA | OPA336PA | Rails |
| OPA336P | 8-Pin DIP | 006 | –40°C to +85°C | OPA336P | OPA336P | Rails |
| OPA336UA | SO-8 Surface-Mount | 182 | –40°C to +85°C | OPA336UA | OPA336UA | Rails[4] |
| OPA336U | SO-8 Surface-Mount | 182 | –40°C to +85°C | OPA336U | OPA336U | Rails[4] |
| **Dual** | | | | | | |
| OPA2336PA | 8-Pin DIP | 006 | –40°C to +85°C | OPA2336PA | OPA2336PA | Rails |
| OPA2336P | 8-Pin DIP | 006 | –40°C to +85°C | OPA2336P | OPA2336P | Rails |
| OPA2336UA | SO-8 Surface-Mount | 182 | –40°C to +85°C | OPA2336UA | OPA2336UA | Rails[4] |
| OPA2336U | SO-8 Surface-Mount | 182 | –40°C to +85°C | OPA2336U | OPA2336U | Rails[4] |
| OPA2336EA | MSOP-8 Surface-Mount | 337 | –40°C to +85°C | B36[3] | OPA2336EA-250 | Tape and Reel |
| " | " | " | " | " | OPA2336EA-2500 | Tape and Reel |
| OPA2336E | MSOP-8 Surface-Mount | 337 | –40°C to +85°C | B36[3] | OPA2336E-250 | Tape and Reel |
| " | " | " | " | " | OPA2336E-2500 | Tape and Reel |
| **Quad** | | | | | | |
| OPA4336EA | SSOP-16 Surface-Mount | 322 | –40°C to +85°C | OPA4336EA | OPA4336EA-250 | Tape and Reel |
| " | " | " | " | " | OPA4336EA-2500 | Tape and Reel |
| OPA4336PA | 14-Pin DIP | 010 | –40°C to +85°C | OPA4336PA | OPA4336PA | Rails |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with -250, -2500, and -3K are available only in Tape and Reel in the quantities indicated (e.g., -250 indicates 250 devices per reel). Ordering 3000 pieces of "OPA336NA-3K" will get a single 3000 piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book. (3) Grade will be marked on the Reel. (4) SO-8 models also available in Tape and Reel.

BURR-BROWN®



# OPA340
# OPA2340
# OPA4340

www.burr-brown.com/databook/OPA340.html

# SINGLE-SUPPLY, RAIL-TO-RAIL OPERATIONAL AMPLIFIERS
## *Micro*Amplifier™ Series

## FEATURES

- RAIL-TO-RAIL INPUT
- RAIL-TO-RAIL OUTPUT (within 1mV)
- *Micro*SIZE PACKAGES
- WIDE BANDWIDTH: 5.5MHz
- HIGH SLEW RATE: 6V/µs
- LOW THD+NOISE: 0.0007% (f = 1kHz)
- LOW QUIESCENT CURRENT: 750µA/channel
- SINGLE, DUAL, AND QUAD

## APPLICATIONS

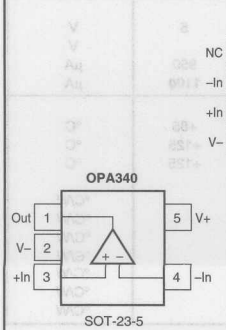
- DRIVING A/D CONVERTERS
- PCMCIA CARDS
- DATA ACQUISITION
- PROCESS CONTROL
- AUDIO PROCESSING
- COMMUNICATIONS
- ACTIVE FILTERS
- TEST EQUIPMENT

## DESCRIPTION

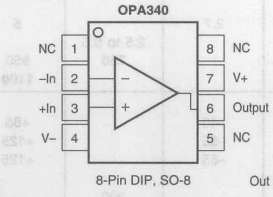
OPA340 series rail-to-rail CMOS operational amplifiers are optimized for low voltage, single supply operation. Rail-to-rail input/output and high speed operation make them ideal for driving sampling analog-to-digital converters. They are also well suited for general purpose and audio applications as well as providing I/V conversion at the output of D/A converters. Single, dual, and quad versions have identical specifications for design flexibility.

The OPA340 series operates on a single supply as low as 2.5V with an input common-mode voltage range that extends 500mV below ground and 500mV above the positive supply. Output voltage swing is to within 1mV of the supply rails with a 100kΩ load. They offer excellent dynamic response (BW = 5.5MHz, SR = 6V/µs), yet quiescent current is only 750µA. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

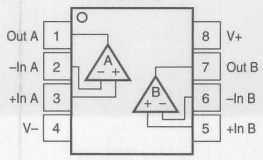
The single (OPA340) packages are the tiny 5-lead SOT-23-5 surface mount, SO-8 surface mount, and 8-pin DIP. The dual (OPA2340) comes in the miniature MSOP-8 surface mount, SO-8 surface mount, and 8-pin DIP packages. The quad (OPA4340) packages are the space-saving SSOP-16 surface mount, SO-14 surface mount, and the 14-pin DIP. All are specified from –40°C to +85°C and operate from –55°C to +125°C. A SPICE macromodel is available for design analysis.



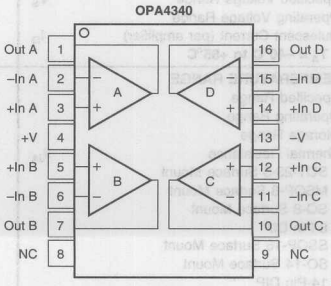

SOT-23-5




8-Pin DIP, SO-8




8-Pin DIP, SO-8, MSOP-8




SSOP-16

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

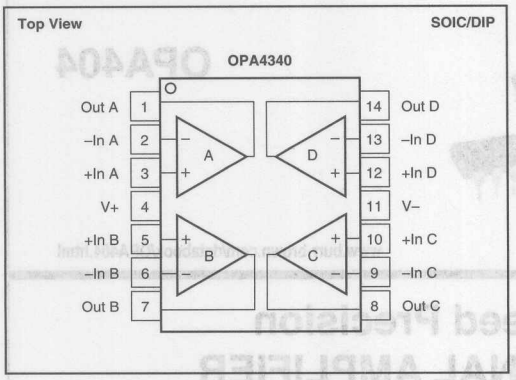
# SPECIFICATIONS: $V_S$ = 2.7V to 5V

At $T_A$ = +25°C, $R_L$ = 10kΩ connected to $V_S/2$ and $V_{OUT}$ = $V_S/2$, unless otherwise noted.
**Boldface** limits apply over the specified temperature range, $T_A$ = –40°C to +85°C. $V_S$ = 5V.

| PARAMETER | | CONDITION | OPA340NA, PA, UA OPA2340EA, PA, UA OPA4340EA, PA, UA MIN | TYP[1] | MAX | UNITS |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | $V_S$ = 5V | | ±150 | ±500 | µV |
| vs Temperature | $dV_{OS}/dT$ | | | **±2.5** | | µV/°C |
| vs Power Supply | PSRR | $V_S$ = 2.7V to 5.5V, $V_{CM}$ = 0V | | 30 | 120 | µV/V |
| **$T_A$ = –40°C to +85°C** | | $V_S$ = 2.7V to 5.5V, $V_{CM}$ = 0V | | | **120** | µV/V |
| Channel Separation, dc | | | | 0.2 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | |
| Input Bias Current | $I_B$ | | | ±0.2 | ±10 | pA |
| **$T_A$ = –40°C to +85°C** | | | | | **±60** | pA |
| Input Offset Current | $I_{OS}$ | | | ±0.2 | ±10 | pA |
| **NOISE** | | | | | | |
| Input Voltage Noise, f = 0.1 to 50kHz | | | | 8 | | µVrms |
| Input Voltage Noise Density, f = 1kHz | $e_n$ | | | 25 | | $nV/\sqrt{Hz}$ |
| Current Noise Density, f = 1kHz | $i_n$ | | | 3 | | $fA/\sqrt{Hz}$ |
| **INPUT VOLTAGE RANGE** | | | | | | |
| Common-Mode Voltage Range | $V_{CM}$ | | –0.3 | | (V+) +0.3 | V |
| Common-Mode Rejection Ratio | CMRR | –0.3V < $V_{CM}$ < (V+) –1.8V | 80 | 92 | | dB |
| | | $V_S$ = 5V, –0.3V < $V_{CM}$ < 5.3V | 70 | 84 | | dB |
| | | $V_S$ = 2.7V, –0.3V < $V_{CM}$ < 3V | 66 | 80 | | dB |
| **INPUT IMPEDANCE** | | | | | | |
| Differential | | | | $10^{13}$ \|\| 3 | | Ω \|\| pF |
| Common-Mode | | | | $10^{13}$ \|\| 6 | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | | |
| Open-Loop Voltage Gain | $A_{OL}$ | $R_L$ = 100kΩ, 5mV < $V_O$ < (V+) –5mV | 106 | 124 | | dB |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 100kΩ, 5mV < $V_O$ < (V+) –5mV | **106** | | | dB |
| | | $R_L$ = 10kΩ, 50mV < $V_O$ < (V+) –50mV | 100 | 120 | | dB |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 10kΩ, 50mV < $V_O$ < (V+) –50mV | **100** | | | dB |
| | | $R_L$ = 2kΩ, 200mV < $V_O$ < (V+) –200mV | 94 | 114 | | dB |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 2kΩ, 200mV < $V_O$ < (V+) –200mV | **94** | | | dB |
| **FREQUENCY RESPONSE** | | | | | | |
| Gain-Bandwidth Product | GBW | G = 1 | | 5.5 | | MHz |
| Slew Rate | SR | $V_S$ = 5V, G = 1, $C_L$ = 100pF | | 6 | | V/µs |
| Settling Time, 0.1% | | $V_S$ = 5V, 2V Step, $C_L$ = 100pF | | 1 | | µs |
| 0.01% | | $V_S$ = 5V, 2V Step, $C_L$ = 100pF | | 1.6 | | µs |
| Overload Recovery Time | | $V_{IN}$ • G = $V_S$ | | 0.2 | | µs |
| Total Harmonic Distortion + Noise | THD+N | $V_S$ = 5V, $V_O$ = 3Vp-p[2], G = 1, f = 1kHz | | 0.0007 | | % |
| **OUTPUT** | | | | | | |
| Voltage Output Swing from Rail[3] | | $R_L$ = 100kΩ, $A_{OL}$ ≥ 106dB | | 1 | 5 | mV |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 100kΩ, $A_{OL}$ ≥ 106dB | | | **5** | mV |
| | | $R_L$ = 10kΩ, $A_{OL}$ ≥ 100dB | | 10 | 50 | mV |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 10kΩ, $A_{OL}$ ≥ 100dB | | | **50** | mV |
| | | $R_L$ = 2kΩ, $A_{OL}$ ≥ 94dB | | 40 | 200 | mV |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 2kΩ, $A_{OL}$ ≥ 94dB | | | **200** | mV |
| Short-Circuit Current | $I_{SC}$ | | | ±50 | | mA |
| Capacitive Load Drive | $C_{LOAD}$ | | | See Typical Curve | | |
| **POWER SUPPLY** | | | | | | |
| Specified Voltage Range | $V_S$ | | 2.7 | | 5 | V |
| Operating Voltage Range | | | | 2.5 to 5.5 | | V |
| Quiescent Current (per amplifier) | $I_Q$ | $I_O$ = 0, $V_S$ = +5V | | 750 | 950 | µA |
| **$T_A$ = –40°C to +85°C** | | $I_O$ = 0, $V_S$ = +5V | | | **1100** | µA |
| **TEMPERATURE RANGE** | | | | | | |
| Specified Range | | | –40 | | +85 | °C |
| Operating Range | | | –55 | | +125 | °C |
| Storage Range | | | –55 | | +125 | °C |
| Thermal Resistance | $\theta_{JA}$ | | | | | |
| SOT-23-5 Surface Mount | | | | 200 | | °C/W |
| MSOP-8 Surface Mount | | | | 150 | | °C/W |
| SO-8 Surface Mount | | | | 150 | | °C/W |
| 8-Pin DIP | | | | 100 | | °C/W |
| SSOP-16 Surface Mount | | | | 100 | | °C/W |
| SO-14 Surface Mount | | | | 100 | | °C/W |
| 14-Pin DIP | | | | 80 | | °C/W |

NOTES: (1) $V_S$ = +5V. (2) $V_{OUT}$ = 0.25V to 3.25V. (3) Output voltage swings are measured between the output and power supply rails.

## PIN CONFIGURATIONS




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Supply Voltage | 5.5V |
| Signal Input Terminals, Voltage[2] | (V–) –0.5V to (V+) +0.5V |
| Current[2] | 10mA |
| Output Short-Circuit[3] | Continuous |
| Operating Temperature | –55°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering, 10s) | 300°C |

NOTES: (1) Stresses above these ratings may cause permanent damage. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.

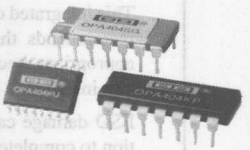
## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER[2] | TRANSPORT MEDIA |
|---|---|---|---|---|---|---|
| **Single** | | | | | | |
| OPA340NA | 5-Lead SOT-23-5 | 331 | –40°C to +85°C | A40 | OPA340NA-250 | Tape and Reel |
| " | " | " | " | " | OPA340NA-3K | Tape and Reel |
| OPA340PA | 8-Pin DIP | 006 | –40°C to +85°C | OPA340PA | OPA340PA | Rails |
| OPA340UA | SO-8 Surface-Mount | 182 | –40°C to +85°C | OPA340UA | OPA340UA | Rails[3] |
| **Dual** | | | | | | |
| OPA2340EA | MSOP-8 Surface-Mount | 337 | –40°C to +85°C | A40A | OPA2340EA-250 | Tape and Reel |
| " | " | " | " | " | OPA2340EA-2500 | Tape and Reel |
| OPA2340PA | 8-Pin DIP | 006 | –40°C to +85°C | OPA2340PA | OPA2340PA | Rails |
| OPA2340UA | SO-8 Surface-Mount | 182 | –40°C to +85°C | OPA2340UA | OPA2340UA | Rails[3] |
| **Quad** | | | | | | |
| OPA4340EA | SSOP-16 Surface-Mount | 322 | –40°C to +85°C | OPA4340EA | OPA4340EA-250 | Tape and Reel |
| " | " | " | " | " | OPA4340EA-2500 | Tape and Reel |
| OPA4340PA | 14-Pin DIP | 010 | –40°C to +85°C | OPA4340PA | OPA4340PA | Rails |
| OPA4340UA | SO-14 Surface Mount | 235 | –40°C to +85°C | OPA4340UA | OPA4340UA | Rails[3] |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with -250, -2500, and -3K are available only in Tape and Reel in the quantities indicated (e.g., -250 indicates 250 devices per reel). Ordering 3000 pieces of "OPA340NA-3K" will get a single 3000 piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book. (3) SO-8 and SO-14 models also available in Tape and Reel.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

BURR-BROWN®



# OPA404

www.burr-brown.com/databook/OPA404.html

# Quad High-Speed Precision *Difet*® OPERATIONAL AMPLIFIER

## FEATURES

- WIDE BANDWIDTH: 6.4MHz
- HIGH SLEW RATE: 35V/μs
- LOW OFFSET: ±750μV max
- LOW BIAS CURRENT: ±4pA max
- LOW SETTLING: 1.5μs to 0.01%
- STANDARD QUAD PINOUT

## APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DETECTOR ARRAYS

## DESCRIPTION

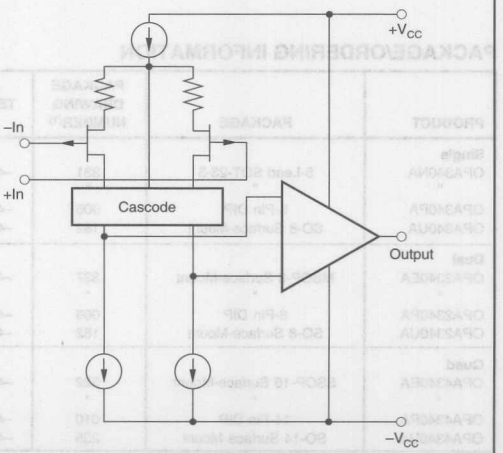
The OPA404 is a high performance monolithic ***Difet***®(dielectrically-isolated FET) quad operational amplifier. It offers an unusual combination of very-low bias current together with wide bandwidth and fast slew rate.

Noise, bias current, voltage offset, drift, and speed are superior to BIFET® amplifiers.

Laser-trimming of thin-film resistors gives very low offset and drift—the best available in a quad FET op amp.

The OPA404's input cascode design allows high precision input specifications and uncompromised high-speed performance.

Standard quad op amp pin configuration allows upgrading of existing designs to higher performance levels. The OPA404 is unity-gain stable.




OPA404 Simplified Circuit
(Each Amplifier)

*Difet*®, Burr-Brown Corp.
BIFET®, National Semiconductor Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $V_{CC}$ = ±15VDC and $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA404AG, KP, KU[1] MIN | OPA404AG, KP, KU[1] TYP | OPA404AG, KP, KU[1] MAX | OPA404BG MIN | OPA404BG TYP | OPA404BG MAX | OPA404SG MIN | OPA404SG TYP | OPA404SG MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | | | | | |
| **NOISE** | | | | | | | | | | | |
| Voltage: $f_O$ = 10Hz | | | 32 | | | * | | | * | | nV/√Hz |
| $f_O$ = 100Hz | | | 19 | | | * | | | * | | nV/√Hz |
| $f_O$ = 1kHz | | | 15 | | | * | | | * | | nV/√Hz |
| $f_O$ = 10kHz | | | 12 | | | * | | | * | | nV/√Hz |
| $f_B$ = 10Hz to 10kHz | | | 1.4 | | | * | | | * | | µVrms |
| $f_B$ = 0.1Hz to 10Hz | | | 0.95 | | | * | | | * | | µVp-p |
| Current: $f_B$ = 0.1Hz to 10Hz | | | 12 | | | * | | | * | | fA, p-p |
| $f_O$ = 0.1Hz thru 20kHz | | | 0.6 | | | * | | | * | | fA/√Hz |
| **OFFSET VOLTAGE** | | | | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0VDC | | ±260 | ±1mV | | * | ±750 | | * | * | µV |
| KP, KU | | | ±750 | ±2.5mV | | | | | | | µV |
| Average Drift | $T_A = T_{MIN}$ to $T_{MAX}$ | | ±3 | | | * | | | * | | µV/°C |
| KP, KU | | | ±5 | | | | | | | | µV/°C |
| Supply Rejection | $\pm V_{CC}$ = 12V to 18V | 80 | 100 | | 86 | * | | * | * | | dB |
| KP, KU | | 76 | 100 | | | | | | | | dB |
| Channel Separation | 100Hz, $R_L$ = 2kΩ | | 125 | | | * | | | * | | dB |
| **BIAS CURRENT** | | | | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC | | ±1 | ±8 | | * | ±4 | | * | * | pA |
| KP, KU | | | ±1 | ±12 | | | | | | | pA |
| **OFFSET CURRENT** | | | | | | | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC | | 0.5 | 8 | | * | 4 | | * | * | pA |
| KP, KU | | | 0.5 | 12 | | | | | | | pA |
| **IMPEDANCE** | | | | | | | | | | | |
| Differential | | | $10^{13}$ II 1 | | | * | | | * | | Ω II pF |
| Common-Mode | | | $10^{14}$ II 3 | | | * | | | * | | Ω II pF |
| **VOTAGE RANGE** | | | | | | | | | | | |
| Common-Mode Input Range | | ±10.5 | +13, –11 | | * | * | | * | * | | V |
| Common-Mode Rejection | $V_{IN}$ = ±10VDC | 88 | 100 | | 92 | * | | * | * | | dB |
| KP, KU | | 84 | 100 | | | | | | | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | | | | |
| Open-Loop Voltage Gain | $R_L \geq$ 2kΩ | 88 | 100 | | 92 | * | | * | * | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | | | | |
| Gain Bandwidth | Gain = 100 | 4 | 6.4 | | 5 | * | | * | * | | MHz |
| Full Power Response | 20Vp-p, $R_L$ = 2kΩ | | 570 | | | * | | | * | | kHz |
| Slew Rate | $V_O$ = ±10V, $R_L$ = 2kΩ | 24 | 35 | | 28 | * | | * | * | | V/µs |
| Settling Time: 0.1% | Gain = –1, $R_L$ = 2kΩ | | 0.6 | | | * | | | * | | µs |
| 0.01% | $C_L$ = 100 pF, 10V Step | | 1.5 | | | * | | | * | | µs |
| **RATED OUTPUT** | | | | | | | | | | | |
| Voltage Output | $R_L$ = 2kΩ | ±11.5 | +13.2, –13.8 | | * | * | | * | * | | V |
| Current Output | $V_O$ = ±10VDC | ±5 | ±10 | | * | * | | * | * | | mA |
| Output Resistance | 1MHz, Open-Loop | | 80 | | | * | | | * | | Ω |
| Load Capacitance Stability | Gain = +1 | | 1000 | | | * | | | * | | pF |
| Short Circuit Current | | ±10 | ±27 | ±40 | * | * | * | * | * | * | mA |
| **POWER SUPPLY** | | | | | | | | | | | |
| Rated Voltage | | | ±15 | | | * | | | * | | VDC |
| Voltage Range, | | | | | | | | | | | |
| Derated Performance | | ±5 | | ±18 | * | | * | * | | * | VDC |
| Current, Quiescent | $I_O$ = 0mADC | | 9 | 10 | | * | * | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification | Ambient Temperature | –25 | | +85 | * | | * | –55 | | +125 | °C |
| KP, KU | | 0 | | +70 | | | | | | | °C |
| Operating | Ambient Temperature | –55 | | +125 | * | | * | * | | * | °C |
| KP, KU | | –25 | | +85 | | | | | | | °C |
| Storage | Ambient Temperature | –65 | | +150 | * | | * | * | | * | °C |
| KP, KU | | –40 | | +125 | | | | | | | °C |
| θ Junction-Ambient | | | 100 | | | * | | | * | | °C/W |
| KP, KU | | | 120/100 | | | | | | | | °C/W |

* Specification same as OPA404AG.
NOTE: (1) OPA404KU may be marked OPA404U.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC}$ = ±15VDC and $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA404AG, KP, KU | | | OPA404BG | | | OPA404SG | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification Range | Ambient Temperature | –25 | | +85 | * | | * | –55 | | +125 | °C |
| KP, KU | | 0 | | +70 | | | | | | | °C |
| **INPUT OFFSET VOLTAGE** | | | | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0VDC | | ±450 | 2mV | | * | ±1.5mV | | ±550 | ±2.5mV | µV |
| KP KU | | | ±1 | ±3.5 | | | | | | | mV |
| Average Drift | | | ±3 | | | * | | | * | | µV/°C |
| KP, KU | | | ±5 | | | | | | | | µV/°C |
| Supply Rejection | | 75 | 96 | | 80 | * | | 70 | 93 | | dB |
| **BIAS CURRENT** | | | | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC | | ±32 | ±200 | | * | ±100 | | ±500 | ±5nA | pA |
| **OFFSET CURRENT** | | | | | | | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC | | 17 | 100 | | * | 50 | | 260 | 2.5nA | pA |
| **VOLTAGE RANGE** | | | | | | | | | | | |
| Common-Mode Input Range | | ±10 | ±12.7, –10.6 | | * | * | | ±10 | +12.6, –10.5 | | V |
| Common-Mode Rejection | $V_{IN}$ = ±10VDC | 82 | 99 | | 86 | * | | 80 | 88 | | dB |
| KP, KU | | 80 | 99 | | | | | | | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | | | | |
| Open-Loop Voltage Gain | $R_L \geq 2k\Omega$ | 82 | 94 | | 86 | * | | 80 | 88 | | dB |
| **RATED OUTPUT** | | | | | | | | | | | |
| Voltage Output | $R_L$ = 2kΩ | ±11.5 | ±12.9, –13.8 | | * | * | | ±11 | +12.7, –13.8 | | V |
| Current Output | $V_O$ = ±10VDC | ±5 | ±9 | | * | * | | * | ±8 | | mA |
| Short Circuit Current | $V_O$ = 0VDC | ±8 | ±20 | ±50 | * | * | * | * | * | * | mA |
| **POWER SUPPLY** | | | | | | | | | | | |
| Current, Quiescent | $I_O$ = 0mADC | | 9.3 | 10.5 | | * | * | | 9.4 | 11 | mA |

* Specification same as OPA404AG.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| OPA404KP | 14-Pin Plastic DIP | 010 | 0°C to +70°C |
| OPA404KU(2) | 16-Pin Plastic SOIC | 211 | 0°C to +70°C |
| OPA404AG | 14-Pin Ceramic DIP | 169 | –25°C to +85°C |
| OPA404BG | 14-Pin Ceramic DIP | 169 | –25°C to +85°C |
| OPA404SG | 14-Pin Ceramic DIP | 169 | –55°C to +125°C |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) OPA404KU may be marked OPA404U.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply | ±18VDC |
| Internal Power Dissipation(1) | 1000mW |
| Differential Input Voltage(2) | ±36VDC |
| Input Voltage Range(2) | ±18VDC |
| Storage Temperature Range ... P, U | –40°C/+125°C, G = –65°C/+150°C |
| Operating Temperature Range . P, U | –25°C/+85°C, G = –55°C/+125°C |
| Lead Temperature (soldering, 10s) | 300°C |
| SOIC (soldering, 3s) | +260°C |
| Output Short-Circuit Duration(3) | Continuous |
| Junction Temperature | +175°C |

NOTES: (1) Packages must be derated based on $\theta_{JC}$ = 30°C/W or $\theta_{JA}$ = 120°C/W. (2) For supply voltages less than ±18VDC the absolute maximum input voltage is equal to: 18V > $V_{IN}$ > –$V_{CC}$ – 8V. See Figure 2. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and $T_J$.

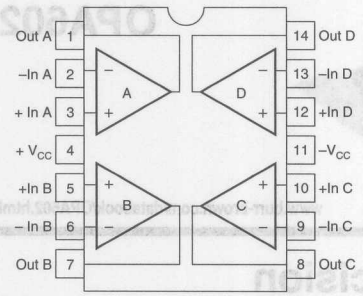
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

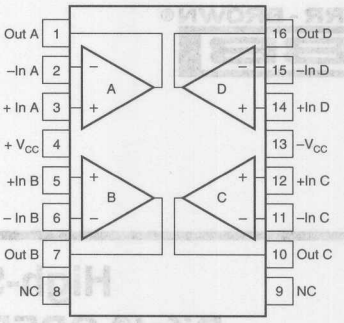
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

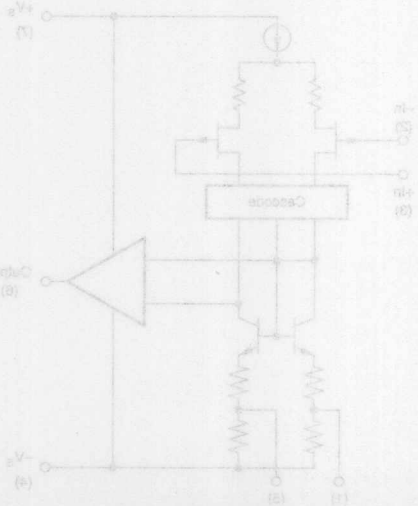
## PIN CONFIGURATIONS

Top View "G" or "P" (DIP) Package

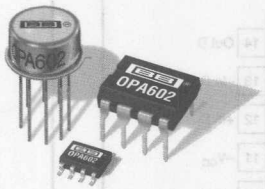



Top View "U" (SOIC) Package



BURR - BROWN®




# OPA602

www.burr-brown.com/databook/OPA602.html

# High-Speed Precision *Difet*® OPERATIONAL AMPLIFIER

## FEATURES

- WIDE BANDWIDTH: 6.5MHz
- HIGH SLEW RATE: 35V/μs
- LOW OFFSET: ±250μV max
- LOW BIAS CURRENT: ±1pA max
- FAST SETTLING TIME: 1μs to 0.01%
- UNITY-GAIN STABLE

## APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DATA CONVERSION

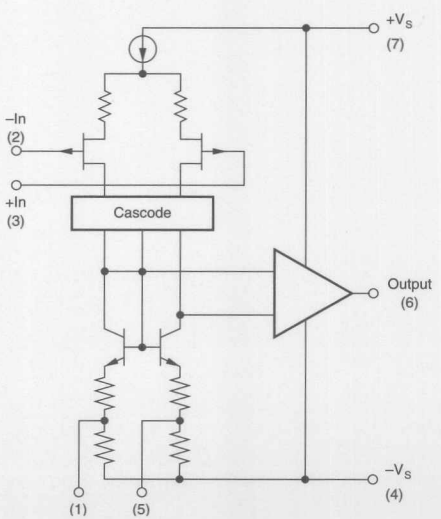
## DESCRIPTION

The OPA602 is a precision, wide bandwidth FET operational amplifier. Monolithic ***Difet*** (dielectrically isolated FET) construction provides an unusual combination of high speed and accuracy.

Its wide-bandwidth design minimizes dynamic errors. High slew rate and fast settling time allow accurate signal processing in pulse and data conversion applications. Wide bandwidth and low distortion minimize AC errors. All specifications are rated with a 1kΩ resistor in parallel with 500pF load. The OPA602 is unity-gain stable and easily drives capacitive loads up to 1500pF.

Laser-trimmed input circuitry provides offset voltage and drift performance normally associated with precision bipolar op amps. ***Difet*** construction achieves extremely low input bias currents (1pA max) without compromising input voltage noise.

The OPA602's unique input cascode circuitry maintains low input bias current and precise input characteristics over its full input common-mode voltage range.




*Difet*® Burr-Brown Corp.

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $V_S$ = ±15VDC and $T_A$ = +25°C, unless otherwise noted.

| | | OPA602AM, AP, AU | | | OPA602BM, SM, BP | | | OPA602CM | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **CONDITIONS** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **INPUT NOISE** | | | | | | | | | | | |
| Voltage: $f_O$= 10Hz | | | * | | | 23 | | | * | | nV/√Hz |
| $f_O$= 100Hz | | | * | | | 19 | | | * | | nV/√Hz |
| $f_O$= 1kHz | | | * | | | 13 | | | * | | nV/√Hz |
| $f_O$= 10kHz | | | * | | | 12 | | | * | | nV/√Hz |
| $f_B$= 10Hz to 10kHz | | | * | | | 1.4 | | | * | | µVrms |
| $f_B$= 0.1Hz to 10Hz | | | * | | | 0.95 | | | * | | µVp-p |
| Current: $f_B$= 0.1Hz to 10Hz | | | * | | | 12 | | | * | | fAp-p |
| $f_O$= 0.1Hz to 20kHz | | | * | | | 0.6 | | | * | | fA/√Hz |
| **OFFSET VOLTAGE** | | | | | | | | | | | |
| Input Offset Voltage: | | | | | | | | | | | |
| M Package | $V_{CM}$ = 0VDC | | ±300 | ±1000 | | ±150 | ±500 | | ±100 | ±250 | µV |
| P Package | | | 1 | 2 | | 0.5 | 1 | | | | mV |
| U Package | | | 1 | 3 | | | | | | | mV |
| Over Specified Temperature | | | | | | | | | | | |
| M Package | | | ±550 | | | ±250 | ±1000 | | ±200 | ±500 | µV |
| P, U Packages | | | ±1.5 | | | ±0.75 | ±1.5 | | | | mV |
| Average Drift | $T_A = T_{MIN}$ to $T_{MAX}$ | | * | ±15 | | ±3 | ±5 | | * | ±2 | µV/°C |
| Supply Rejection | $±V_S$ = 12V to 18V | 70 | * | | 80 | 100 | | 86 | * | | dB |
| **BIAS CURRENT** | | | | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC | | ±2 | ±10 | | ±1 | ±2 | | ±0.5 | ±1 | pA |
| Over Specified Temperature | | | ±20 | ±500 | | ±20 | ±200 | | ±10 | ±100 | pA |
| SM Grade | | | | | | ±200 | ±2000 | | | | pA |
| **OFFSET CURRENT** | | | | | | | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC | | 1 | 10 | | 0.5 | 2 | | 0.5 | 1 | pA |
| Over Specified Temperature | | | 20 | 500 | | 20 | 200 | | 10 | 100 | pA |
| SM Grade | | | | | | 200 | 1000 | | | | pA |
| **INPUT IMPEDANCE** | | | | | | | | | | | |
| Differential | | | * | | | $10^{13}$ ‖ 1 | | | * | | Ω ‖ pF |
| Common-Mode | | | * | | | $10^{14}$ ‖ 3 | | | * | | Ω ‖ pF |
| **INPUT VOLTAGE RANGE** | | | | | | | | | | | |
| Common-Mode Input Range | | * | * | | ±10.2 | +13, −11 | | * | * | | V |
| Common-Mode Rejection | $V_{IN}$ = ±10VDC | 75 | * | | 88 | 100 | | 92 | * | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | | | | |
| Open-Loop Voltage Gain | $R_L \geq 1k\Omega$ | 75 | * | | 88 | 100 | | 92 | * | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | | | | |
| Gain Bandwidth | Gain = 100 | 3.5 | * | | 4 | 6.5 | | 5 | * | | MHz |
| Full Power Response | 20Vp-p, $R_L$ = 1kΩ | | * | | | 570 | | | * | | kHz |
| Slew Rate | $V_O$ = ±10V, $R_L$ = 1kΩ | 20 | * | | 24 | 35 | | 28 | * | | V/µs |
| Settling Time: 0.1% | Gain = −1, $R_L$ = 1kΩ | | * | | | 0.6 | | | * | | µs |
| 0.01% | $C_L$ = 500pF, 10V Step | | * | | | 1.0 | | | * | | µs |
| **RATED OUTPUT** | | | | | | | | | | | |
| Voltage Output | $R_L$ = 1kΩ | ±11 | * | | ±11.5 | +12.9, −13.8 | | * | * | | V |
| Current Output | $V_O$ = ±10VDC | * | * | | ±15 | ±20 | | * | * | | mA |
| Output Resistance | 1MHz, Open Loop | | * | | | 80 | | | * | | Ω |
| Load Capacitance Stability | Gain = +1 | | * | | | 1500 | | | * | | pF |
| Short Circuit Current | | ±25 | * | | ±30 | ±50 | | * | * | | mA |
| **POWER SUPPLY** | | | | | | | | | | | |
| Rated Voltage | | | * | | | ±15 | | | * | | VDC |
| Voltage Range, | | | | | | | | | | | |
| Derated Performance | | * | | * | ±5 | | ±18 | * | | * | VDC |
| Current, Quiescent | $I_O$ = 0mADC | | * | * | | 3 | 4 | | * | * | mA |
| Over Specified Temperature | | | * | * | | 3.5 | 4.5 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification | Ambient Temperature | * | | * | −25 | | +85 | * | | * | °C |
| SM Grade | | | | | −55 | | +125 | | | | °C |
| Operating: M Package | Ambient Temperature | * | | * | −55 | | +125 | * | | * | °C |
| P, U Packages | | −25 | | +85 | −25 | | +85 | | | | °C |
| Storage: M Package | Ambient Temperature | * | | * | −65 | | +150 | * | | * | °C |
| P, U Packages | | −40 | | +125 | −40 | | +125 | | | | °C |
| $\theta_{JA}$ | | | * | | | 200 | | | * | | °C/W |

* Same specifications as OPA602BM.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18VDC |
| Internal Power Dissipation ($T_J \leq +175°C$) | 1000mW |
| Differential Input Voltage | Total $V_S$ |
| Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range | |
| M Package | –65°C to +150°C |
| P and U Packages | –40°C to +125°C |
| Operating Temperature Range | |
| M Package | –55°C to +125°C |
| P and U Packages | –25°C to + 85°C |
| Lead Temperature | |
| M and P Packages (soldering, 10s) | +300°C |
| U Package, SOIC (3s) | +260°C |
| Output Short Circuit to Ground (+25°C) | Continuous |
| Junction Temperature | +175°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

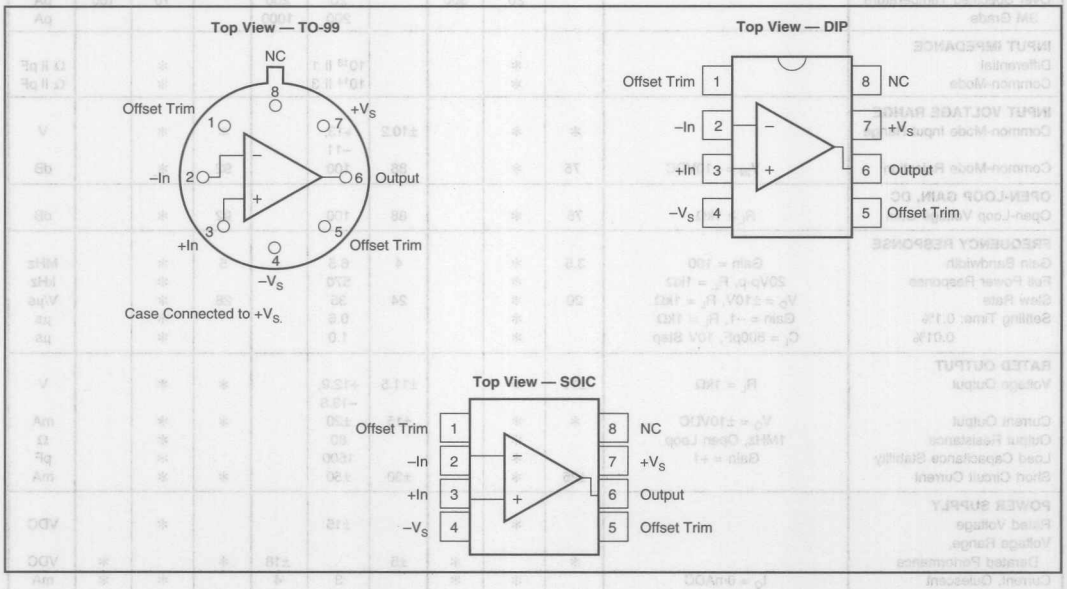
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE | OFFSET VOLTAGE MAX (µV) AT 25°C |
|---|---|---|---|---|
| OPA602AM | TO-99 | 001 | –25°C to +85°C | ±1000 |
| OPA602BM | TO-99 | 001 | –25°C to +85°C | ±500 |
| OPA602CM | TO-99 | 001 | –25°C to +85°C | ±250 |
| OPA602SM | TO-99 | 001 | –55°C to +125°C | ±500 |
| OPA602AP | Plastic DIP | 006 | –25°C to +85°C | ±2000 |
| OPA602BP | Plastic DIP | 006 | –25°C to +85°C | ±1000 |
| OPA602AU | Plastic SOIC | 182 | –25°C to +85°C | ±3000 |

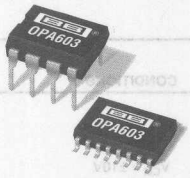
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN CONFIGURATIONS




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BURR-BROWN®




# OPA603

www.burr-brown.com/databook/OPA603.html

# High Speed, Current-Feedback, High Voltage OPERATIONAL AMPLIFIER

## FEATURES

- WIDE SUPPLY RANGE: ±4.5 to ±18V
- BANDWIDTH: 100MHz, G = 1 to 10
- SLEW RATE: 1000V/µs
- FAST SETTLING TIME: 50ns to 0.1%
- HIGH OUTPUT CURRENT: ±150mA peak
- HIGH OUTPUT VOLTAGE: ±12V

## APPLICATIONS

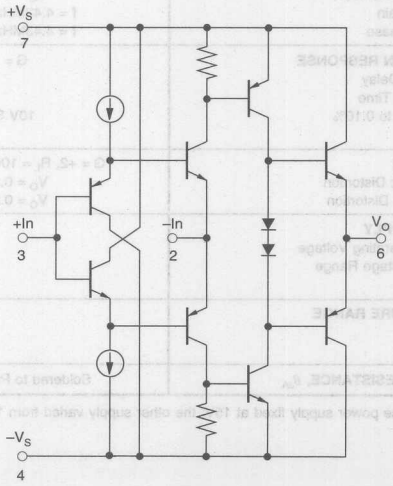
- VIDEO AMPLIFIER
- PULSE AMPLIFIER
- SONAR, ULTRASOUND BUFFERS
- ATE PIN DRIVERS
- xDSL LINE DRIVER
- FAST DATA ACQUISTION
- WAVEFORM GENERATORS

## DESCRIPTION

The OPA603 is a high-speed current-feedback op amp with guaranteed specifications at both ±5V and ±15V power supplies. It can deliver full ±10V signals into 150Ω loads with up to 1000V/µs slew rate. This allows it to drive terminated 75Ω cables. With 150mA peak output current capability it is suitable for driving load capacitance or long lines at high speed.

In contrast with conventional op amps, the current-feedback approach provides nearly constant bandwidth and settling time over a wide range of closed-loop voltage gains.

The OPA603 is available in a plastic 8-pin DIP and SO-16 surface-mount packages, specified over the industrial temperature range.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

## ELECTRICAL

At $T_A$ = +25°C, and $R_L$ = 150Ω, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA603AP, AU MIN | OPA603AP, AU TYP | OPA603AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT OFFSET VOLTAGE** | | | | | |
| Initial | | | | 5 | mV |
| vs Temperature | | | 8 | | µV/°C |
| vs Common-Mode Voltage | $V_{CM}$ = ±10V | 50 | 60 | | dB |
| vs Supply (tracking) Voltage | $V_S$ = ±12V to ±18V | 80 | 85 | | dB |
| vs Supply (non-tracking)[1] | $\|V_S\|$ = 12V to 18V | 55 | 60 | | dB |
| **+INPUT BIAS CURRENT** | | | | | |
| Initial | | | | 5 | µA |
| vs Temperature | | | 30 | | nA/°C |
| vs Common-Mode | $V_{CM}$ = ±10V | | 200 | 500 | nA/V |
| vs Supply (tracking) | $V_S$ = ±12V to ±18V | | 50 | 100 | nA/V |
| vs Supply (non-tracking)[1] | $\|V_S\|$ = 12V to 18V | | 150 | 300 | nA/V |
| **–INPUT BIAS CURRENT** | | | | | |
| Initial | | | | 25 | µA |
| vs Temperature | | | 300 | | nA/°C |
| vs Common-Mode | $V_{CM}$ = ±10V | | 200 | 600 | nA/V |
| vs Supply (tracking) | $V_S$ = ±12V to ±18V | | 300 | 500 | nA/V |
| vs Supply (non-tracking)[1] | $\|V_S\|$ = 12V to 18V | | 1500 | 2000 | nA/V |
| **INPUT IMPEDANCE** | | | | | |
| +Input | | | 5 ll 2 | | MΩ ll pF |
| –Input | | | 30 ll 2 | | Ω ll pF |
| **OPEN LOOP CHARACTERISTICS** | | | | | |
| Transresistance | $V_O$ = ±10V | 300 | 440 | | kΩ |
| Transcapacitance | | | 1.8 | | pF |
| **OUTPUT CHARACTERISTICS** | | | | | |
| Voltage | $R_L$ = 150Ω | ±10 | ±12 | | V |
| Peak Current | | | 150 | | mA |
| Short-Circuit Current[2] | $V_O$ = 0V | | 250 | | mA |
| Output Resistance, Open-Loop | | | 70 | | Ω |
| **FREQUENCY RESPONSE** | G = +2 | | | | |
| Small-Signal Bandwidth[3] | | 70 | 160 | | MHz |
| Gain Flatness, ±0.5dB | | 35 | 75 | | MHz |
| Full-Power Bandwidth | $V_O$ = 20Vp-p | | 10 | | MHz |
| Differential Gain | f = 4.43MHz, $V_O$ = 1V | | 0.03 | | % |
| Differential Phase | f = 4.43MHz, $V_O$ = 1V | | 0.025 | | Degrees |
| **TIME DOMAIN RESPONSE** | G = +2 | | | | |
| Propagation Delay | | | 10 | | ns |
| Rise and Fall Time | | | 10 | | ns |
| Settling Time to 0.10% | 10V Step | | 50 | | ns |
| Slew Rate | | | 1000 | | V/µs |
| **DISTORTION** | G = +2, $R_L$ = 100Ω, f = 10MHz | | | | |
| 2nd Harmonic Distortion | $V_O$ = 0.2Vp-p | | –60 | –65 | dBc |
| 3rd Harmonic Distortion | $V_O$ = 0.2Vp-p | | –70 | –90 | dBc |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±15 | | V |
| Operating Voltage Range | | ±4.5 | | ±18 | V |
| Current | | | ±21 | ±25 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –25 | | +85 | °C |
| Storage | | –40 | | +150 | °C |
| **THERMAL RESISTANCE, $\theta_{JA}$** | Soldered to Printed Circuit | | 90 | | °C/W |

NOTES: (1) One power supply fixed at 15V; the other supply varied from 12V to 18V. (2) Observe power derating curve. (3) See bandwidth versus gain curve, Figure 5.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

# SPECIFICATIONS: $V_S = \pm 5V$

## ELECTRICAL

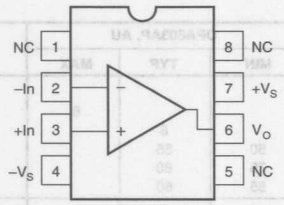
At $T_A$ = +25°C, and $R_L$ = 75Ω, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA603AP, AU MIN | OPA603AP, AU TYP | OPA603AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT OFFSET VOLTAGE** | | | | | |
| Initial | | | | 6 | mV |
| vs Temperature | | | 8 | | µV/°C |
| vs Common-Mode | $V_{CM}$ = ±3V | 50 | 55 | | dB |
| vs Supply (tracking) | $V_S$ = ±4V to ±6V | 75 | 80 | | dB |
| vs Supply (non-tracking)(1) | $\|V_S\|$ = 4V to 6V | 55 | 60 | | dB |
| **+INPUT BIAS CURRENT** | | | | | |
| Initial | | | | 5 | µA |
| vs Temperature | | | 30 | | nA/°C |
| vs Common-Mode | $V_{CM}$ = ±3V | | 350 | 600 | nA/V |
| vs Supply (tracking) | $V_S$ = ±4V to ±6V | | 100 | 200 | nA/V |
| vs Supply (non-tracking)(1) | $\|V_S\|$ = 4V to 6V | | 200 | 300 | nA/V |
| **–INPUT BIAS CURRENT** | | | | | |
| Initial | | | | 25 | µA |
| vs Temperature | | | 300 | | nA/°C |
| vs Common-Mode | $V_{CM}$ = ±3V | | 300 | 600 | nA/V |
| vs Supply (tracking) | $V_S$ = ±4V to ±6V | | 500 | 700 | nA/V |
| vs Supply (non-tracking)(1) | $\|V_S\|$ = 4V to 6V | | 2500 | 3000 | nA/V |
| **INPUT IMPEDANCE** | | | | | |
| +Input | | | 3.3 II 2 | | MΩ II pF |
| –Input | | | 30 II 2 | | Ω II pF |
| **OPEN LOOP CHARACTERISTICS** | | | | | |
| Transresistance | $V_O$ = ±2V | 225 | 330 | | kΩ |
| Transcapacitance | | | 2.4 | | pF |
| **OUTPUT CHARACTERISTICS** | | | | | |
| Voltage | $R_L$ = 75Ω | ±2 | ±2.75 | | V |
| Peak Current | | | 150 | | mA |
| Short-Circuit Current(2) | $V_O$ = 0V | | 250 | | mA |
| Output Resistance, Open-Loop | | | 80 | | Ω |
| **FREQUENCY RESPONSE** | G = +2 | | | | |
| Small-Signal Bandwidth(3) | | | 140 | | MHz |
| Gain Flatness, ±0.5dB | | | 65 | | MHz |
| Full-Power Bandwidth | | | 20 | | MHz |
| Differential Gain | f = 4.43MHz $V_O$ = 1V, $R_L$ = 150Ω | | 0.03 | | % |
| Differential Phase | f = 4.43MHz, $V_O$ = 1V, $R_L$ = 150Ω | | 0.025 | | Degrees |
| **TIME DOMAIN RESPONSE** | G = +2, $R_L$ = 100Ω | | | | |
| Propagation Delay | | | 15 | | ns |
| Rise and Fall Time | | | 20 | | ns |
| Settling Time to 0.10% | | | 60 | | ns |
| Slew Rate | | | 750 | | V/µs |
| **DISTORTION** | G = +2, $R_L$ = 100Ω, f = 10MHz | | | | |
| 2nd Harmonic Distortion | $V_O$ = 0.2Vp-p | | –67 | | dBc |
| 3rd Harmonic Distortion | $V_O$ = 0.2Vp-p | | –78 | | dBc |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±5 | | V |
| Operating Voltage Range | | ±4.5 | | ±18 | V |
| Current | | | ±21 | ±25 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –25 | | +85 | °C |
| Storage | | –40 | | +150 | °C |
| **THERMAL RESISTANCE,** $\theta_{JUNCTION\text{-}AMBIENT}$ | Soldered to Printed Circuit | | 90 | | °C/W |

NOTES: (1) One power supply fixed at 5V; the other supply varied from 4V to 6V. (2) Observe power derating curve. (3) See bandwidth versus gain curves, Figure 5.

## PIN CONFIGURATION

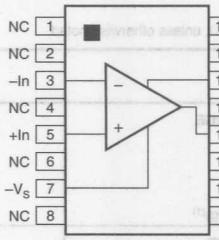
**Top View** **DIP**




NC: No Internal Connection.
Solder to ground plane for improved heat dissipation.

## PIN CONFIGURATION

**Top View** **SO-16**




NC: No Internal Connection.
Solder to ground plane for improved heat dissipation.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Input Voltage Range | ±$V_S$ |
| Differential Input Voltage | ±6V |
| Power Dissipation | See derating curve |
| Operating Temperature | +100°C |
| Storage Temperature | +150°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering SO-16 package, 3s) | +260°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

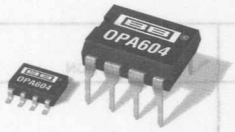
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | SPECIFIED TEMPERATURE RANGE |
|---|---|---|---|
| OPA603AP | Plastic DIP | 006 | –25°C to +85°C |
| OPA603AU | SO-16 | 211 | –25°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR - BROWN®



# OPA604

www.burr-brown.com/databook/OPA604.html

# FET-Input, Low Distortion OPERATIONAL AMPLIFIER

## FEATURES

- LOW DISTORTION: 0.0003% at 1kHz
- LOW NOISE: 10nV/√Hz
- HIGH SLEW RATE: 25V/µs
- WIDE GAIN-BANDWIDTH: 20MHz
- UNITY-GAIN STABLE
- WIDE SUPPLY RANGE: $V_S$ = ±4.5 to ±24V
- DRIVES 600Ω LOAD
- DUAL VERSION AVAILABLE (OPA2604)

## APPLICATIONS

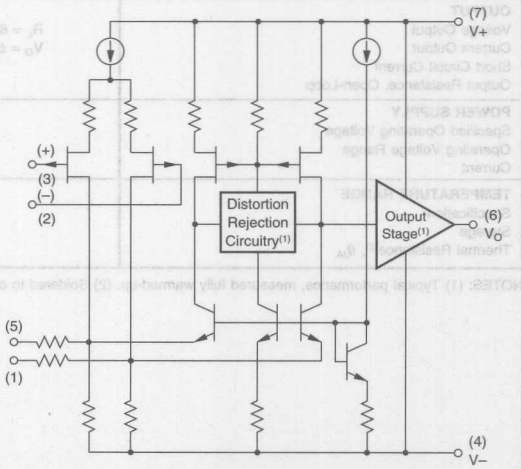
- PROFESSIONAL AUDIO EQUIPMENT
- PCM DAC I/V CONVERTER
- SPECTRAL ANALYSIS EQUIPMENT
- ACTIVE FILTERS
- TRANSDUCER AMPLIFIER
- DATA ACQUISITION

## DESCRIPTION

The OPA604 is a FET-input operational amplifier designed for enhanced AC performance. Very low distortion, low noise and wide bandwidth provide superior performance in high quality audio and other applications requiring excellent dynamic performance.

New circuit techniques and special laser trimming of dynamic circuit performance yield very low harmonic distortion. The result is an op amp with exceptional sound quality. The low-noise FET input of the OPA604 provides wide dynamic range, even with high source impedance. Offset voltage is laser-trimmed to minimize the need for interstage coupling capacitors.

The OPA604 is available in 8-pin plastic mini-DIP and SO-8 surface-mount packages, specified for the –25°C to +85°C temperature range.




NOTE: (1) Patents Granted: #5053718, 5019789

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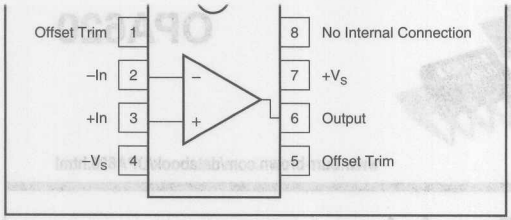
## ELECTRICAL

$T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

| PARAMETER | CONDITION | OPA604AP, AU MIN | OPA604AP, AU TYP | OPA604AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | | | ±1 | ±5 | mV |
| Average Drift | | | ±8 | | µV/°C |
| Power Supply Rejection | $V_S$ = ±5 to ±24V | 80 | 100 | | dB |
| **INPUT BIAS CURRENT**[1] | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | 50 | | pA |
| Input Offset Current | $V_{CM}$ = 0V | | ±3 | | pA |
| **NOISE** | | | | | |
| Input Voltage Noise | | | | | |
| Noise Density: f = 10Hz | | | 25 | | nV/√Hz |
| f = 100Hz | | | 15 | | nV/√Hz |
| f = 1kHz | | | 11 | | nV/√Hz |
| f = 10kHz | | | 10 | | nV/√Hz |
| Voltage Noise, BW = 20Hz to 20kHz | | | 1.5 | | µVp-p |
| Input Bias Current Noise | | | | | |
| Current Noise Density, f = 0.1Hz to 20kHz | | | 4 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range | | ±12 | ±13 | | V |
| Common-Mode Rejection | $V_{CM}$ = ±12V | 80 | 100 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $10^{12}$ ‖ 8 | | Ω ‖ pF |
| Common-Mode | | | $10^{12}$ ‖ 10 | | Ω ‖ pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±10V, $R_L$ = 1kΩ | 80 | 100 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product | G = 100 | | 20 | | MHz |
| Slew Rate | 20Vp-p, $R_L$ = 1kΩ | 15 | 25 | | V/µs |
| Settling Time: 0.01% | G = –1, 10V Step | | 1.5 | | µs |
| 0.1% | | | 1 | | µs |
| Total Harmonic Distortion + Noise (THD+N) | G = 1, f = 1kHz<br>$V_O$ = 3.5Vrms, $R_L$ = 1kΩ | | 0.0003 | | % |
| **OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 600Ω | ±11 | ±12 | | V |
| Current Output | $V_O$ = ±12V | | ±35 | | mA |
| Short Circuit Current | | | ±40 | | mA |
| Output Resistance, Open-Loop | | | 25 | | Ω |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±15 | | V |
| Operating Voltage Range | | ±4.5 | | ±24 | V |
| Current | | | ±5.3 | ±6 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –25 | | +85 | °C |
| Storage | | –40 | | +125 | °C |
| Thermal Resistance[2], $\theta_{JA}$ | | | 90 | | °C/W |

NOTES: (1) Typical performance, measured fully warmed-up. (2) Soldered to circuit board—see text.

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| | |
|---|---|
| Output Short Circuit to Ground | Continuous |
| Operating Temperature | –40°C to +100°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) AP | +300°C |
| Lead Temperature (soldering, 3s) AU | +260°C |

## ORDERING INFORMATION

| PRODUCT | PACKAGE | TEMP. RANGE |
|---|---|---|
| OPA604AP | 8-Pin Plastic DIP | –25°C to +85°C |
| OPA604AU | SO-8 Surface-Mount | –25°C to +85°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| OPA604AP | 8-Pin Plastic DIP | 006 |
| OPA604AU | SO-8 Surface-Mount | 182 |

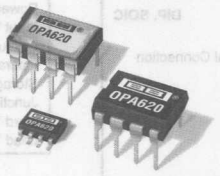
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

BURR - BROWN®



# OPA620

www.burr-brown.com/databook/OPA620.html

# Wideband Precision OPERATIONAL AMPLIFIER

## FEATURES

- LOW NOISE: 2.3nV/√Hz
- HIGH OUTPUT CURRENT: 100mA
- FAST SETTLING: 25ns (0.01%)
- GAIN-BANDWIDTH PRODUCT: 200MHz
- UNITY-GAIN STABLE
- LOW OFFSET VOLTAGE: ±200µV
- LOW DIFFERENTIAL GAIN/PHASE ERROR
- 8-PIN DIP, SO-8 PACKAGES

## APPLICATIONS

- LOW NOISE PREAMPLIFIER
- LOW NOISE DIFFERENTIAL AMPLIFIER
- HIGH-RESOLUTION VIDEO
- HIGH-SPEED SIGNAL PROCESSING
- LINE DRIVER
- ADC/DAC BUFFER
- ULTRASOUND
- PULSE/RF AMPLIFIERS
- ACTIVE FILTERS

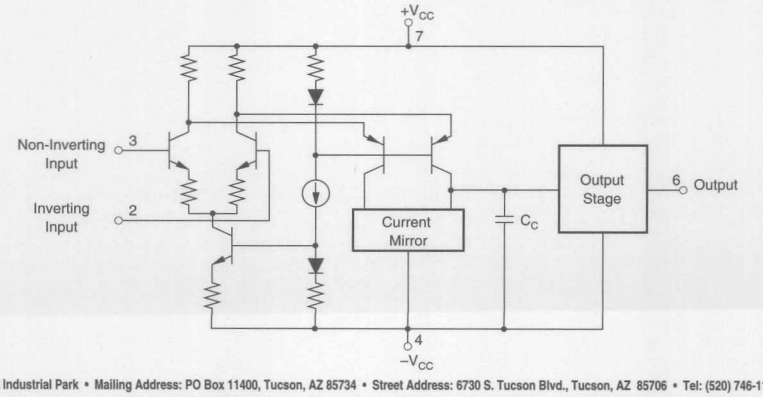
## DESCRIPTION

The OPA620 is a precision wideband monolithic operational amplifier featuring very fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA620 is internally compensated for unity-gain stability. This amplifier has a very low offset, fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA620 may be used in all op amp applications requiring high speed and precision.

Low noise and distortion, wide bandwidth, and high linearity make this amplifier suitable for RF and video applications. Short-circuit protection is provided by an internal current-limiting circuit.

The OPA620 is available in plastic and ceramic DIP and SO-8 packages. Two temperature ranges are offered: –40°C to +85°C and –55°C to +125°C.




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# SPECIFICATIONS

## ELECTRICAL

At $V_{CC}$ = ±5VDC, $R_L$ = 100Ω, and $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA620KP, KU | | | OPA620SG | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT NOISE** | | | | | | | | |
| Voltage: $f_O$ = 100Hz | $R_S$ = 0Ω | | 10 | | | * | | nV/√Hz |
| $f_O$ = 1kHz | | | 5.5 | | | * | | nV/√Hz |
| $f_O$ = 10kHz | | | 3.3 | | | * | | nV/√Hz |
| $f_O$ = 100kHz | | | 2.5 | | | * | | nV/√Hz |
| $f_O$ = 1MHz to 100MHz | | | 2.3 | | | * | | nV/√Hz |
| $f_B$ = 100Hz to 10MHz | | | 8.0 | | | * | | µVrms |
| Current: $f_O$ = 10kHz to 100MHz | | | 2.3 | | | * | | pA/√Hz |
| **OFFSET VOLTAGE**[1] | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0VDC | | ±200 | ±1000 | | * | * | µV |
| Average Drift | $T_A = T_{MIN}$ to $T_{MAX}$ | | ±8 | | | * | | µV/°C |
| Supply Rejection | $\pm V_{CC}$ = 4.5V to 5.5V | 50 | 60 | | * | * | | dB |
| **BIAS CURRENT** | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC | | 15 | 30 | | * | * | µA |
| **OFFSET CURRENT** | | | | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC | | 0.2 | 2 | | * | * | µA |
| **INPUT IMPEDANCE** | | | | | | | | |
| Differential | Open-Loop | | 15 ‖ 1 | | | * | | kΩ ‖ pF |
| Common-Mode | | | 1 ‖ 1 | | | * | | MΩ ‖ pF |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | ±3.0 | ±3.5 | | * | * | | V |
| Common-Mode Rejection | $V_{IN}$ = ±2.5VDC, $V_O$ = 0VDC | 65 | 75 | | * | * | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | |
| Open-Loop Voltage Gain | $R_L$ = 100Ω | 50 | 60 | | * | * | | dB |
| | $R_L$ = 50Ω | 48 | 58 | | * | * | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Closed-Loop Bandwidth | Gain = +1V/V | | 300 | | | * | | MHz |
| (–3dB) | Gain = +2V/V | | 100 | | | * | | MHz |
| | Gain = +5V/V | | 40 | | | * | | MHz |
| | Gain = +10V/V | | 20 | | | * | | MHz |
| Gain-Bandwidth Product | Gain ≥ +5V/V | | 200 | | | * | | MHz |
| Differential Gain | 3.58MHz, G = +1V/V | | 0.05 | | | * | | % |
| Differential Phase | 3.58MHz, G = +1V/V | | 0.05 | | | * | | Degrees |
| Harmonic Distortion[2] | G = +2V/V, f = 10MHz, $V_O$ = 2Vp-p | | | | | | | |
| | Second Harmonic | | –61 | –50 | | * | * | dBc[3] |
| | Third Harmonic | | –65 | –55 | | * | * | dBc |
| Full Power Bandwidth[2] | $V_O$ = 5Vp-p, Gain = +1V/V | 11 | 16 | | * | * | | MHz |
| | $V_O$ = 2Vp-p, Gain = +1V/V | 27 | 40 | | * | * | | MHz |
| Slew Rate[2] | 2V Step, Gain = –1V/V | 175 | 250 | | * | * | | V/µs |
| Overshoot | 2V Step, Gain = –1V/V | | 10 | | | * | | % |
| Settling Time: 0.1% | 2V Step, Gain = –1V/V | | 13 | | | * | | ns |
| 0.01% | | | 25 | | | * | | ns |
| Phase Margin | Gain = +1V/V | | 60 | | | * | | Degrees |
| Rise Time | Gain = +1V/V, 10% to 90% | | | | | | | |
| | $V_O$ = 100mVp-p; Small Signal | | 2 | | | * | | ns |
| | $V_O$ = 6Vp-p; Large Signal | | 22 | | | * | | ns |
| **RATED OUTPUT** | | | | | | | | |
| Voltage Output | $R_L$ = 100Ω | ±3.0 | ±3.5 | | * | * | | V |
| | $R_L$ = 50Ω | ±2.5 | ±3.0 | | * | * | | V |
| Output Resistance | 1MHz, Gain = +1V/V | | 0.015 | | | * | | Ω |
| Load Capacitance Stability | Gain = +1V/V | | 20 | | | * | | pF |
| Short Circuit Current | Continuous | | ±150 | | | * | | mA |
| **POWER SUPPLY** | | | | | | | | |
| Rated Voltage | $\pm V_{CC}$ | | 5 | | | * | | VDC |
| Derated Performance | $\pm V_{CC}$ | 4.0 | | 6.0 | * | | * | VDC |
| Current, Quiescent | $I_O$ = 0mA | | 21 | 23 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: KP, KU | Ambient Temperature | –40 | | +85 | * | | * | °C |
| SG | | | | | –55 | | +125 | °C |
| Operating: SG | Ambient Temperature | | | | –55 | | +125 | °C |
| KP, KU | | –40 | | +85 | | | | °C |
| $\theta_{JA}$: SG | | | | | | 125 | | °C/W |
| KP | | | 90 | | | | | °C/W |
| KU | | | 100 | | | | | °C/W |

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# SPECIFICATIONS (CONT)

## ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC}$ = ±5VDC, $R_L$ = 100Ω, and $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

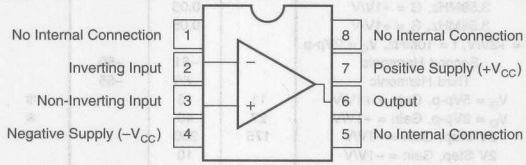
| PARAMETER | CONDITIONS | OPA620KP, KU MIN | OPA620KP, KU TYP | OPA620KP, KU MAX | OPA620SG MIN | OPA620SG TYP | OPA620SG MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: KP, KU | Ambient Temperature | –40 | | +85 | * | | * | °C |
| SG | | | | | –55 | | +125 | °C |
| **OFFSET VOLTAGE**(1) | | | | | | | | |
| Average Drift | Full Temp. | | ±8 | | | * | | µV/°C |
| Supply Rejection | 0°C to +70°C $\pm V_{CC}$ = 4.5V to 5.5V | 45 | 60 | | * | * | | dB |
| | Full Temp., $\pm V_{CC}$ = 4.5 to 5.5V | 40 | 55 | | * | * | | dB |
| **BIAS CURRENT** | | | | | | | | |
| Input Bias Current | Full Temp., $V_{CM}$ = 0VDC | | 15 | 40 | | * | * | µA |
| **OFFSET CURRENT** | | | | | | | | |
| Input Offset Current | Full Temp., $V_{CM}$ = 0VDC | | 0.2 | 5 | | * | * | µA |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | ±2.5 | ±3.0 | | * | * | | V |
| Common-Mode Rejection | $V_{IN}$ = ±2.5VDC, $V_O$ = 0VDC | 60 | 75 | | * | * | | dB |
| **OPEN LOOP GAIN, DC** | | | | | | | | |
| Open-Loop Voltage Gain | $R_L$ = 100Ω | 46 | 60 | | * | * | | dB |
| | $R_L$ = 50Ω | 44 | 58 | | * | * | | dB |
| **RATED OUTPUT** | | | | | | | | |
| Voltage Output | 0°C to +70°C, $R_L$ = 100Ω | ±3.0 | ±3.5 | | * | * | | V |
| | –40°C to +85°C, $R_L$ = 100Ω | ±2.75 | ±3.25 | | * | * | | V |
| | 0°C to +70°C, $R_L$ = 50Ω | ±2.5 | ±3.0 | | * | * | | V |
| | –40°C to +85°C, $R_L$ = 50Ω | ±2.25 | ±2.7 | | * | * | | V |
| **POWER SUPPLY** | | | | | | | | |
| Current, Quiescent | $I_O$ = 0mA | | 21 | 25 | | * | * | mA |

* Same specifications as for KP, KU.

NOTES: (1) Offset Voltage specifications are also guaranteed with units fully warmed up. (2) Parameter is guaranteed by characterization. (3) dBc = dB referred to carrier-input signal.

## PIN CONFIGURATION

Top View — DIP/SO-8




## ORDERING INFORMATION

OPA620 ( ) ( )

- Basic Model Number
- Performance Grade Code
  - K = –40°C to +85°C
  - S = –55°C to +125°C
- Package Code
  - G = 8-pin Ceramic DIP
  - P = 8-pin Plastic DIP
  - U = SO-8 Surface Mount

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| OPA620KP | 8-Pin Plastic DIP | 006 |
| OPA620KU | SO-8 Surface Mount | 182 |
| OPA620SG | 8-Pin Ceramic DIP | 157 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply | ±7VDC |
| Internal Power Dissipation(1) | See Applications Information |
| Differential Input Voltage | Total $V_{CC}$ |
| Input Voltage Range | See Applications Information |
| Storage Temperature Range: SG | –65°C to +150°C |
| KP, KU | –40°C to +125°C |
| *Lead Temperature (soldering, 10s)* | +300°C |
| (soldering, SO-8, 3s) | +260°C |
| Output Short Circuit to Ground (+25°C) | Continuous to Ground |
| Junction Temperature ($T_J$) | +175°C |

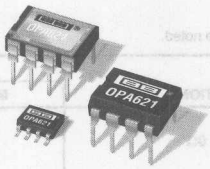
NOTE: (1) Packages must be derated based on specified $\theta_{JA}$. Maximum $T_J$ must be observed.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# OPA621

www.burr-brown.com/databook/OPA621.html



# Wideband Precision OPERATIONAL AMPLIFIER

## FEATURES

- LOW NOISE: 2.3nV/√Hz
- LOW DIFFERENTIAL GAIN/PHASE ERROR
- HIGH OUTPUT CURRENT: 150mA
- FAST SETTLING: 25ns (0.01%)
- GAIN-BANDWIDTH: 500MHz
- STABLE IN GAINS: ≥ 2V/V
- LOW OFFSET VOLTAGE: ±100μV
- SLEW RATE: 500V/μs
- 8-PIN DIP, SOIC PACKAGES

## APPLICATIONS

- LOW NOISE PREAMPLIFIER
- LOW NOISE DIFFERENTIAL AMPLIFIER
- HIGH-RESOLUTION VIDEO
- LINE DRIVER
- HIGH-SPEED SIGNAL PROCESSING
- ADC/DAC BUFFER
- ULTRASOUND
- PULSE/RF AMPLIFIERS
- ACTIVE FILTERS

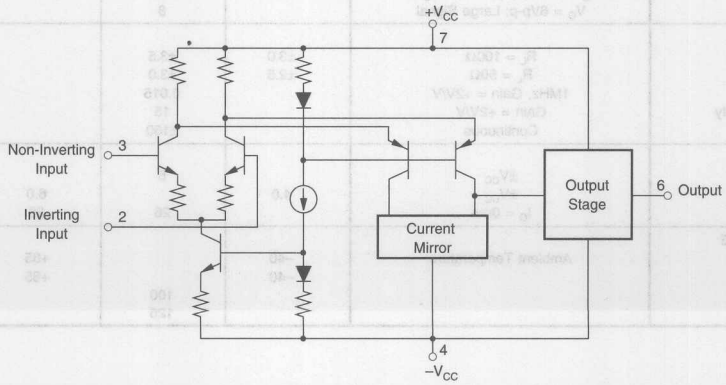
## DESCRIPTION

The OPA621 is a precision wideband monolithic operational amplifier featuring very fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA621 is stable in gains of ±2V/V or higher. This amplifier has a very low offset, fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA621 may be used in all op amp applications requiring high speed and precision.

Low noise and distortion, wide bandwidth, and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

The OPA621 is available in DIP and SO-8 packages.




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# SPECIFICATIONS

## ELECTRICAL

At $V_{CC}$ = ±5VDC, $R_L$ = 100Ω, and $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA621KP, KU MIN | OPA621KP, KU TYP | OPA621KP, KU MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT NOISE** | | | | | |
| Voltage: $f_O$ = 100Hz | $R_S$ = 0Ω | | 10 | | nV/√Hz |
| $f_O$ = 1kHz | | | 5.5 | | nV/√Hz |
| $f_O$ = 10kHz | | | 3.3 | | nV/√Hz |
| $f_O$ = 100kHz | | | 2.5 | | nV/√Hz |
| $f_O$ = 1MHz to 100MHz | | | 2.3 | | nV/√Hz |
| $f_B$ = 100Hz to 10MHz | | | 8.0 | | µV, rms |
| Current: $f_O$ = 10kHz to 100MHz | | | 2.3 | | pA/√Hz |
| **OFFSET VOLTAGE**[1] | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0VDC | | ±200 | ±1mV | µV |
| Average Drift | $T_A = T_{MIN}$ to $T_{MAX}$ | | ±12 | | µV/°C |
| Supply Rejection | $\pm V_{CC}$ = 4.5V to 5.5V | 50 | 60 | | dB |
| **BIAS CURRENT** | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC | | 18 | 30 | µA |
| **OFFSET CURRENT** | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC | | 0.2 | 2 | µA |
| **INPUT IMPEDANCE** | | | | | |
| Differential | Open-Loop | | 15 ‖ 1 | | kΩ ‖ pF |
| Common-Mode | | | 1 ‖ 1 | | MΩ ‖ pF |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range | | ±3.0 | ±3.5 | | V |
| Common-Mode Rejection | $V_{IN}$ = ±2.5VDC, $V_O$ = 0VDC | 65 | 75 | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | |
| Open-Loop Voltage Gain | $R_L$ = 100Ω | 50 | 60 | | dB |
| | $R_L$ = 50Ω | 48 | 58 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Closed-Loop Bandwidth | | | | | |
| (–3dB) | Gain = +2V/V | | 500 | | MHz |
| | Gain = +5V/V | | 100 | | MHz |
| | Gain = +10V/V | | 50 | | MHz |
| Gain-Bandwidth Product | Gain ≥ +10V/V | | 500 | | MHz |
| Differential Gain | 3.58MHz, G = +2V/V | | 0.05 | | % |
| Differential Phase | 3.58MHz, G = +2V/V | | 0.05 | | Degrees |
| Harmonic Distortion | G = +2V/V, f = 10MHz, $V_O$ = 2Vp-p | | | | |
| | f = 10MHz, Second Harmonic | | –62 | –50 | dBc[3] |
| | Third Harmonic | | –80 | –70 | dBc |
| Full Power Bandwidth | $V_O$ = 5Vp-p, Gain = +2V/V | 22 | 32 | | MHz |
| | $V_O$ = 2Vp-p, Gain = +2V/V | 55 | 80 | | MHz |
| Slew Rate | 2V Step, Gain = –2V/V | 350 | 500 | | V/µs |
| Overshoot | 2V Step, Gain = –2V/V | | 15 | | % |
| Settling Time: 0.1% | 2V Step, Gain = –2V/V | | 15 | | ns |
| 0.01% | | | 25 | | ns |
| Phase Margin | Gain = +2V/V | | 50 | | Degrees |
| Rise Time | Gain = +2V/V, 10% to 90% | | | | |
| | $V_O$ = 100mVp-p; Small Signal | | 1.8 | | ns |
| | $V_O$ = 6Vp-p; Large Signal | | 8 | | ns |
| **RATED OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 100Ω | ±3.0 | ±3.5 | | V |
| | $R_L$ = 50Ω | ±2.5 | ±3.0 | | V |
| Output Resistance | 1MHz, Gain = +2V/V | | 0.015 | | Ω |
| Load Capacitance Stability | Gain = +2V/V | | 15 | | pF |
| Short Circuit Current | Continuous | | ±150 | | mA |
| **POWER SUPPLY** | | | | | |
| Rated Voltage | $\pm V_{CC}$ | | 5 | | VDC |
| Derated Performance | $\pm V_{CC}$ | 4.0 | | 6.0 | VDC |
| Current, Quiescent | $I_O$ = 0mA | | 26 | 28 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification: KP, KU | Ambient Temperature | –40 | | +85 | °C |
| Operating: KP, KU | | –40 | | +85 | °C |
| $\theta_{JA}$ KP | | | 100 | | °C/W |
| KU | | | 125 | | °C/W |

# SPECIFICATIONS (CONT)

## ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC}$ = ±5VDC, $R_L$ = 100Ω, and $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA621KP, KU | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **TEMPERATURE RANGE** | | | | | |
| Specification: KP, KU | Ambient Temperature | –40 | | +85 | °C |
| **OFFSET VOLTAGE**(1) | | | | | |
| Average Drift | Full Temperature Range | | ±12 | | µV/°C |
| Supply Rejection | $\pm V_{CC}$ = 4.5V to 5.5V | 45 | 60 | | dB |
| **BIAS CURRENT** | | | | | |
| Input Bias Current | Full Temperature, $V_{CM}$ = 0VDC | | 18 | 40 | µA |
| **OFFSET CURRENT** | | | | | |
| Input Offset Current | Full Temperature, $V_{CM}$ = 0VDC | | 0.2 | 5 | µA |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range | | ±2.5 | ±3.0 | | V |
| Common-Mode Rejection | $V_{IN}$ = ±2.5VDC, $V_O$ = 0VDC | 60 | 75 | | dB |
| **OPEN LOOP GAIN, DC** | | | | | |
| Open-Loop Voltage Gain | $R_L$ = 100Ω | 46 | 60 | | dB |
| | $R_L$ = 50Ω | 44 | 58 | | dB |
| **RATED OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 100Ω | ±3.0 | ±3.5 | | V |
| | $R_L$ = 50Ω | ±2.5 | ±3.0 | | V |
| **POWER SUPPLY** | | | | | |
| Current, Quiescent | $I_O$ = 0mA | | 26 | 30 | mA |

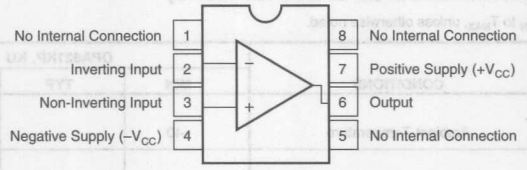
NOTES: (1) Offset Voltage specifications are also guaranteed with units fully warmed up. (2) Parameter is guaranteed by characterization. (3) dBc = dB referred to carrier-input signal.



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## PIN CONFIGURATION

Top View — DIP/SO-8




## ORDERING INFORMATION

OPA621 (_) (_)

- Basic Model Number
- Performance Grade Code
  - K = –40°C to +85°C
- Package Code
  - P = 8-pin Plastic DIP
  - U = 8-pin Plastic SO-8

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| OPA621KP | 8-Pin Plastic DIP | 006 |
| OPA621KU | 8-Pin SO-8 | 182 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply | ±7VDC |
| Internal Power Dissipation[1] | See Applications Information |
| Differential Input Voltage | Total $V_{CC}$ |
| Input Voltage Range | See Applications Information |
| Storage Temperature Range KP, KU: | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SO-8 3s) | +260°C |
| Output Short Circuit to Ground (+25°C) | Continuous to Ground |
| Junction Temperature ($T_J$) | +175°C |

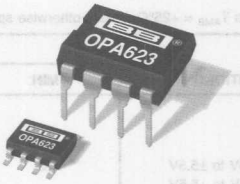
NOTE: (1) Packages must be derated based on specified $\theta_{JA}$. Maximum $T_J$ must be observed.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®




# OPA623

www.burr-brown.com/databook/OPA623.html

# Wide Bandwidth, Current-Feedback OPERATIONAL AMPLIFIER

## FEATURES

- BANDWIDTH: 350MHz, 2.8Vp-p
- HIGH OUTPUT CURRENT: ±70mA
- SLEW RATE: 2100V/μs, 5Vp-p
- DIFFERENTIAL GAIN/PHASE: 0.12%/0.05°
- LOW QUIESCENT CURRENT: ±4mA
- LOW INPUT BIAS CURRENT: 1.2μA
- RISE TIME: 1.9ns, 5Vp-p
- SETTLING TIME: 9ns, 0.1%

## APPLICATIONS

- BROADCAST/HDTV EQUIPMENT
- HIGH-SPEED DIGITAL COMMUNICATIONS
- PULSE/RF AMPLIFIERS
- HIGH-SPEED ANALOG SIGNAL PROCESSING
- LINE DRIVING (50Ω, 75Ω)
- DISTRIBUTION AMP
- CRT OUTPUT STAGE DRIVER
- ACTIVE FILTER

## DESCRIPTION

The OPA623 is a current-feedback operational amplifier designed for precision wide-bandwidth systems including high-resolution video, RF and IF circuitry, and communications equipment.

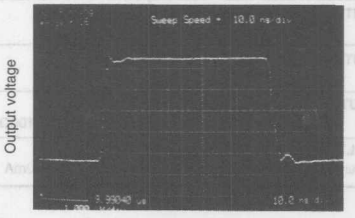
The new circuit design, together with the complementary bipolar process, achieves performance previously unattainable in monolithic integrated circuit technology.

The current-feedback op amp is optimized for wide bandwidth, excellent pulse response, gain flatness, low distortion, and operation at a low quiescent current of ±4mA.

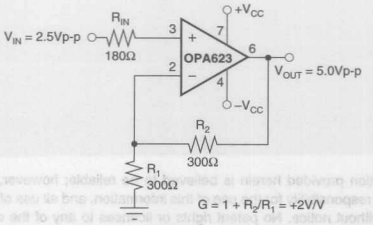
It provides a 350MHz large-signal bandwidth at 2.8Vp-p output voltage, as well as a 2100V/μs slew rate. The gain flatness of 0.05dB over a 30MHz bandwidth makes it suitable for HDTV designs. Another feature of the op amp is its high output current of ±70mA, enabling it to drive two back-terminated 75Ω cables when using the amplifier as a line driver in video routers, distribution amplifiers, and analog and digital communications equipment.

The OPA623 operates from a ±5V supply, is specified for the extended industrial temperature range (–40°C to +85°C), and is available in plastic SO-8 and 8-pin plastic DIP packages.

LARGE SIGNAL PULSE RESPONSE




Output Voltage - 5Vp-p, 5ns/DIV




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# SPECIFICATIONS

## DC-SPECIFICATION

At $V_{CC}$ = ±5VDC, $I_Q$ = ±4mA, $R_L$ = 100Ω, $R_{IN}$ = 210Ω, and $T_{AMB}$ = +25°C, unless otherwise specified.

| PARAMETER | CONDITIONS | OPA623AP, AU MIN | OPA623AP, AU TYP | OPA623AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT OFFSET VOLTAGE** | | | | | |
| Initial | | | –8 | ±25 | mV |
| vs Temperature | | | 125 | | µV/°C |
| vs Supply (tracking) | $V_{CC}$ = ±4.5V to ±5.5V | 45 | 50 | | dB |
| vs Supply (non-tracking) | $V_{CC}$ = +4.5V to +5.5V | | 47 | | dB |
| vs Supply (non-tracking) | $V_{CC}$ = –4.5V to –5.5V | | 39 | | dB |
| **+INPUT BIAS CURRENT** | | | | | |
| Initial | | | –1.2 | ±4 | µA |
| vs Temperature | | | 7 | | nA/°C |
| **–INPUT BIAS CURRENT** | | | | | |
| Initial | | | +4.5 | ±20 | µA |
| vs Temperature | | | 340 | | nA/°C |
| **INPUT IMPEDANCE** | | | | | |
| +Input | | | 2.74 ll 1 | | MΩ ll pF |
| **INPUT NOISE** | f = 100kHz to 100MHz | | | | |
| Voltage Noise Density | | | 10 | | $nV/\sqrt{Hz}$ |
| Signal-to-Noise Ratio | S/N = 0.7/(Vn • $\sqrt{5MHz}$) | | 89 | | dB |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range | | ±3 | ±3.2 | | V |
| Common-Mode Rejection | | 43 | 50 | | dB |
| **RATED OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 100Ω | ±3 | ±3.1 | | V |
| Output Current | | | ±70 | | mA |
| Closed-Loop Output Impedance | Gain = +2 | | 0.12 ll 1.5 | | Ω ll pF |
| **POWER SUPPLY** | | | | | |
| Rated Voltage | | ±4.5 | | ±5.5 | VDC |
| Derated Performance | | ±4 | | ±6 | VDC |
| Quiescent Current | $I_O$ = 0mA | ±3.5 | ±4 | ±4.5 | mA |
| Rejection Ratio | | 45 | 50 | | dB |

## ELECTRICAL (FULL TEMPERATURE RANGE, –40°C to +85°C)

At $V_{CC}$ = ±5VDC, $I_Q$ = ±4mA, $R_L$ = 100Ω, and $R_{IN}$ = 210Ω, unless otherwise specified.

| PARAMETER | CONDITIONS | OPA623AP, AU MIN | OPA623AP, AU TYP | OPA623AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT OFFSET VOLTAGE** | | | | ±30 | mV |
| **BIAS CURRENT** | | | | | |
| +Input | | | –1.5 | ±5 | µA |
| **BIAS CURRENT** | | | | | |
| –Input | | | 27 | ±50 | µA |
| **RATED OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 100Ω | ±3 | ±3.1 | | V |
| **POWER SUPPLY** | | | | | |
| Quiescent Current | $I_O$ = 0mA | ±2 | ±4 | ±7 | mA |

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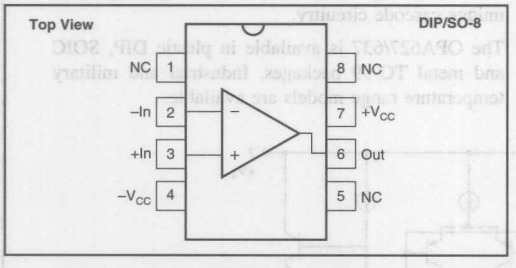
# SPECIFICATIONS

## AC-SPECIFICATION

At $V_{CC}$ = ±5VDC, $I_Q$ = ±4mA, $R_L$ = 100Ω, $R_{IN}$ = 210Ω, and $T_{AMB}$ = +25°C, unless otherwise specified.

| PARAMETER | CONDITIONS | OPA623AP, AU MIN | OPA623AP, AU TYP | OPA623AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **FREQUENCY DOMAIN** | | | | | |
| **Large Signal** Closed-Loop Bandwidth (–3dB) | $V_O$ = 2.8Vp-p, Gain = +1V/V | | 340 | | MHz |
| | $V_O$ = 2.8Vp-p, Gain = +2V/V | | 350 | | MHz |
| | $V_O$ = 2.8Vp-p, Gain = +5V/V | | 260 | | MHz |
| | $V_O$ = 2.8Vp-p, Gain = +10V/V | | 210 | | MHz |
| | $V_O$ = 2.8Vp-p, Gain = –1V/V | | 360 | | MHz |
| | $V_O$ = 2.8Vp-p, Gain = –2V/V | | 330 | | MHz |
| | $V_O$ = 5.0Vp-p, Gain = +2V/V | | 240 | | MHz |
| **SMALL SIGNAL BANDWIDTH** | $V_O$ = 0.2Vp-p, Gain = +2V/V | | 290 | | MHz |
| **GROUP DELAY TIME** | Pin 3 to Pin 6, Gain = +2V/V | | 1.2 | | ns |
| **DIFFERENTIAL GAIN** | G = +2V/V, f = 4.43MHz, $R_L$ = 150Ω, $V_O$ = +1.4V | | 0.12 | | % |
| **DIFFERENTIAL PHASE** | G = +2V/V, f = 4.43MHz, $R_L$ = 150Ω, $V_O$ = +1.4V | | 0.05 | | Degrees |
| **HARMONIC DISTORTION** | Gain = +2V/V | | | | |
| Second Harmonic | f = 10MHz, $V_O$ = 2.0Vp-p | | –56 | | dBc |
| Third Harmonic | | | –59 | | dBc |
| Second Harmonic | f = 30MHz, $V_O$ = 2.0Vp-p | | –30 | | dBc |
| Third Harmonic | | | –37 | | dBc |
| Second Harmonic | f = 50MHz, $V_O$ = 2.0Vp-p | | –30 | | dBc |
| Third Harmonic | | | –33 | | dBc |
| **GAIN FLATNESS PEAKING** | Gain = +2V/V | | | | |
| | $V_O$ = 2.0Vp-p, DC to 30MHz | | 0.05 | | dB |
| | $V_O$ = 2.0Vp-p, DC to 100MHz | | 0.20 | | dB |
| **TIME DOMAIN** | | | | | |
| **Rise Time** | Gain = +2V/V, 10% to 90% | | | | |
| | $V_O$ = 2.0Vp-p | | 1.4 | | ns |
| | $V_O$ = 5.0Vp-p | | 1.9 | | ns |
| **Fall Time** | Gain = +2V/V, 10% to 90% | | | | |
| | $V_O$ = 2.0Vp-p | | 1.4 | | ns |
| | $V_O$ = 5.0Vp-p | | 2.6 | | ns |
| **SLEW RATE** | Gain = +2V/V, Rise Time = 1ns | | | | |
| | $V_O$ = 0.2Vp-p | | 140 | | V/µs |
| | $V_O$ = 5.0Vp-p | | 2100 | | V/µs |
| **SETTLING TIME** | Gain = +2V/V, Rise Time = 2ns, $V_O$ = $2V_{p-p}$, 0.1% | | 9 | | ns |

## PIN CONFIGURATION




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | ±6V |
| Input Voltage[1] | $\pm V_{CC}$ ±0.7V |
| Operating Temperature | –40°C to +85°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

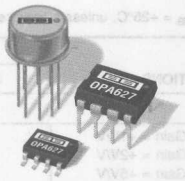
NOTE: (1) Inputs are internally diode-clamped to $\pm V_{CC}$.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| OPA623AP | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| OPA623AU | SO-8 Surface Mount | 182 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR-BROWN®



# OPA627
# OPA637

www.burr-brown.com/databook/OPA627.html

# Precision High-Speed *Difet*® OPERATIONAL AMPLIFIERS

## FEATURES

- VERY LOW NOISE: 4.5nV/√Hz at 10kHz
- FAST SETTLING TIME:
  OPA627—550ns to 0.01%
  OPA637—450ns to 0.01%
- LOW $V_{OS}$: 100µV max
- LOW DRIFT: 0.8µV/°C max
- LOW $I_B$: 5pA max
- OPA627: Unity-Gain Stable
- OPA637: Stable in Gain ≥ 5

## APPLICATIONS

- PRECISION INSTRUMENTATION
- FAST DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- ACTIVE FILTERS

## DESCRIPTION

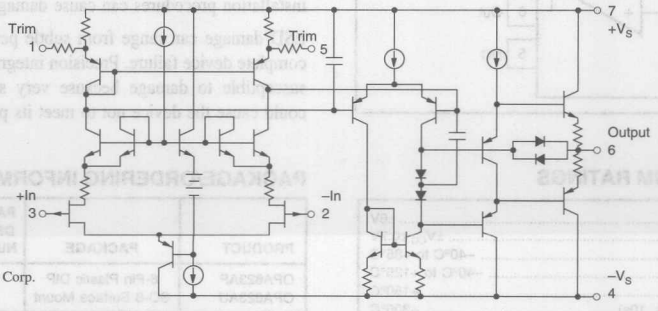
The OPA627 and OPA637 ***Difet*** operational amplifiers provide a new level of performance in a precision FET op amp. When compared to the popular OPA111 op amp, the OPA627/637 has lower noise, lower offset voltage, and much higher speed. It is useful in a broad range of precision and high speed analog circuitry.

The OPA627/637 is fabricated on a high-speed, dielectrically-isolated complementary NPN/PNP process. It operates over a wide range of power supply voltage—±4.5V to ±18V. Laser-trimmed ***Difet*** input circuitry provides high accuracy and low-noise performance comparable with the best bipolar-input op amps.

High frequency complementary transistors allow increased circuit bandwidth, attaining dynamic performance not possible with previous precision FET op amps. The OPA627 is unity-gain stable. The OPA637 is stable in gains equal to or greater than five.

***Difet*** fabrication achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry.

The OPA627/637 is available in plastic DIP, SOIC and metal TO-99 packages. Industrial and military temperature range models are available.




***Difet***®, Burr-Brown Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, and $V_S$ = ±15V, unless otherwise noted.

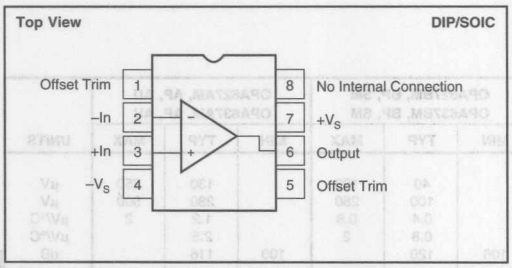
| PARAMETER | CONDITIONS | OPA627BM, BP, SM OPA637BM, BP, SM MIN | TYP | MAX | OPA627AM, AP, AU OPA637AM, AP, AU MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** (1) | | | | | | | | |
| Input Offset Voltage | | | 40 | 100 | | 130 | 250 | µV |
| AP, BP, AU Grades | | | 100 | 250 | | 280 | 500 | µV |
| Average Drift | | | 0.4 | 0.8 | | 1.2 | 2 | µV/°C |
| AP, BP, AU Grades | | | 0.8 | 2 | | 2.5 | | µV/°C |
| Power Supply Rejection | $V_S$ = ±4.5 to ±18V | 106 | 120 | | 100 | 116 | | dB |
| **INPUT BIAS CURRENT** (2) | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | 1 | 5 | | 2 | 10 | pA |
| Over Specified Temperature | $V_{CM}$ = 0V | | | 1 | | | 2 | nA |
| SM Grade | $V_{CM}$ = 0V | | | 50 | | | | nA |
| Over Common-Mode Voltage | $V_{CM}$ = ±10V | | 1 | | | 2 | | pA |
| Input Offset Current | $V_{CM}$ = 0V | | 0.5 | 5 | | 1 | 10 | pA |
| Over Specified Temperature | $V_{CM}$ = 0V | | | 1 | | | 2 | nA |
| SM Grade | | | | 50 | | | | nA |
| **NOISE** | | | | | | | | |
| Input Voltage Noise | | | | | | | | |
| Noise Density: f = 10Hz | | | 15 | 40 | | 20 | | nV/√Hz |
| f = 100Hz | | | 8 | 20 | | 10 | | nV/√Hz |
| f = 1kHz | | | 5.2 | 8 | | 5.6 | | nV/√Hz |
| f = 10kHz | | | 4.5 | 6 | | 4.8 | | nV/√Hz |
| Voltage Noise, BW = 0.1Hz to 10Hz | | | 0.6 | 1.6 | | 0.8 | | µVp-p |
| Input Bias Current Noise | | | | | | | | |
| Noise Density, f = 100Hz | | | 1.6 | 2.5 | | 2.5 | | fA/√Hz |
| Current Noise, BW = 0.1Hz to 10Hz | | | 30 | 60 | | 48 | | fAp-p |
| **INPUT IMPEDANCE** | | | | | | | | |
| Differential | | | $10^{13}$ \|\| 8 | | | * | | Ω \|\| pF |
| Common-Mode | | | $10^{13}$ \|\| 7 | | | * | | Ω \|\| pF |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | ±11 | ±11.5 | | * | * | | V |
| Over Specified Temperature | | ±10.5 | ±11 | | * | * | | V |
| Common-Mode Rejection | $V_{CM}$ = ±10.5V | 106 | 116 | | 100 | 110 | | dB |
| **OPEN-LOOP GAIN** | | | | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±10V, $R_L$ = 1kΩ | 112 | 120 | | 106 | 116 | | dB |
| Over Specified Temperature | $V_O$ = ±10V, $R_L$ = 1kΩ | 106 | 117 | | 100 | 110 | | dB |
| SM Grade | $V_O$ = ±10V, $R_L$ = 1kΩ | 100 | 114 | | | | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Slew Rate: OPA627 | G = –1, 10V Step | 40 | 55 | | * | * | | V/µs |
| OPA637 | G = –4, 10V Step | 100 | 135 | | * | * | | V/µs |
| Settling Time: OPA627 0.01% | G = –1, 10V Step | | 550 | | | * | | ns |
| 0.1% | G = –1, 10V Step | | 450 | | | * | | ns |
| OPA637 0.01% | G = –4, 10V Step | | 450 | | | * | | ns |
| 0.1% | G = –4, 10V Step | | 300 | | | * | | ns |
| Gain-Bandwidth Product: OPA627 | G = 1 | | 16 | | | * | | MHz |
| OPA637 | G = 10 | | 80 | | | * | | MHz |
| Total Harmonic Distortion + Noise | G = +1, f = 1kHz | | 0.00003 | | | * | | % |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | | ±15 | | | * | | V |
| Operating Voltage Range | | ±4.5 | | ±18 | * | | * | V |
| Current | | | ±7 | ±7.5 | | * | * | mA |
| **OUTPUT** | | | | | | | | |
| Voltage Output | $R_L$ = 1kΩ | ±11.5 | ±12.3 | | * | * | | |
| Over Specified Temperature | | ±11 | ±11.5 | | * | * | | V |
| Current Output | $V_O$ = ±10V | | ±45 | | | * | | mA |
| Short-Circuit Current | | ±35 | +70/–55 | ±100 | * | * | * | mA |
| Output Impedance, Open-Loop | 1MHz | | 55 | | | * | | Ω |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: AP, BP, AM, BM, AU | | –25 | | +85 | * | | * | °C |
| SM | | –55 | | +125 | | | | °C |
| Storage: AM, BM, SM | | –60 | | +150 | * | | * | °C |
| AP, BP, AU | | –40 | | +125 | * | | * | °C |
| $\theta_{J-A}$: AM, BM, SM | | | 200 | | | * | | °C/W |
| AP, BP | | | 100 | | | * | | °C/W |
| AU | | | 160 | | | | | °C/W |

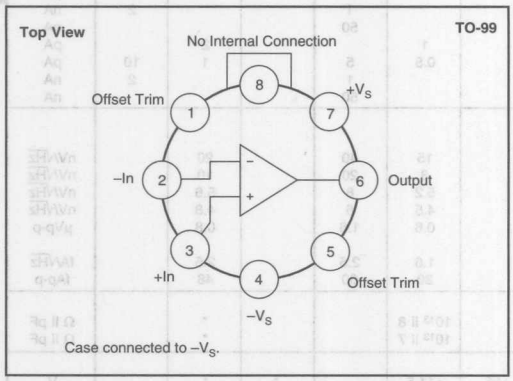
* Specifications same as "B" grade.

NOTES: (1) Offset voltage measured fully warmed-up. (2) High-speed test at $T_J$ = +25°C. See Typical Performance Curves for warmed-up performance.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN CONFIGURATIONS




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|---|
| Supply Voltage | ±18V |
| Input Voltage Range | $+V_S$ + 2V to $-V_S$ – 2V |
| Differential Input Range | Total $V_S$ + 4V |
| Power Dissipation | 1000mW |
| Operating Temperature | |
| M Package | –55°C to +125°C |
| P, U Package | –40°C to +125°C |
| Storage Temperature | |
| M Package | –65°C to +150°C |
| P, U Package | –40°C to +125°C |
| Junction Temperature | |
| M Package | +175°C |
| P, U Package | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| SOIC (soldering, 3s) | +260°C |

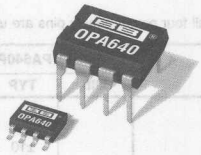
NOTE: (1) Stresses above these ratings may cause permanent damage.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| OPA627AP | Plastic DIP | 006 | –25°C to +85°C |
| OPA627BP | Plastic DIP | 006 | –25°C to +85°C |
| OPA627AU | SOIC | 182 | –25°C to +85°C |
| OPA627AM | TO-99 Metal | 001 | –25°C to +85°C |
| OPA627BM | TO-99 Metal | 001 | –25°C to +85°C |
| OPA627SM | TO-99 Metal | 001 | –55°C to +125°C |
| OPA637AP | Plastic DIP | 006 | –25°C to +85°C |
| OPA637BP | Plastic DIP | 006 | –25°C to +85°C |
| OPA637AU | SOIC | 182 | –25°C to +85°C |
| OPA637AM | TO-99 Metal | 001 | –25°C to +85°C |
| OPA637BM | TO-99 Metal | 001 | –25°C to +85°C |
| OPA637SM | TO-99 Metal | 001 | –55°C to +125°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR-BROWN®




# OPA640

www.burr-brown.com/databook/OPA640.html

# Wideband Voltage Feedback OPERATIONAL AMPLIFIER

## FEATURES

- UNITY-GAIN BANDWIDTH: 1.3GHz
- UNITY-GAIN STABLE
- LOW NOISE: 2.9nV/$\sqrt{Hz}$
- LOW HARMONICS: –75dBc at 10MHz
- HIGH COMMON MODE REJECTION: 85dB
- HIGH SLEW RATE: 350V/μs

## APPLICATIONS

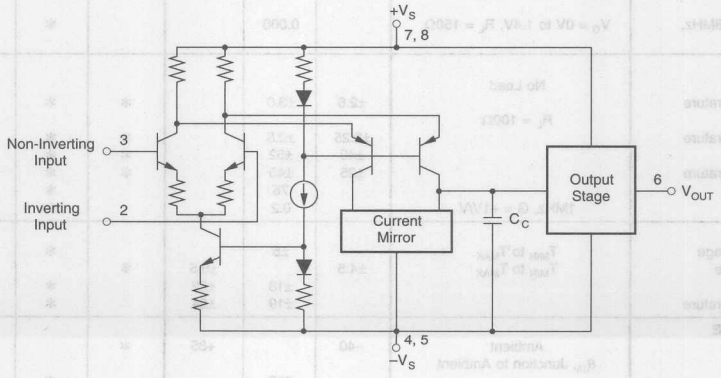
- COMMUNICATIONS
- MEDICAL IMAGING
- TEST EQUIPMENT
- CCD IMAGING
- ADC/DAC GAIN AMPLIFIER
- HIGH-RESOLUTION VIDEO
- LOW NOISE PREAMPLIFIER
- DIFFERENTIAL AMPLIFIER
- ACTIVE FILTERS

## DESCRIPTION

The OPA640 is an extremely wideband operational amplifier featuring low noise, high common-mode rejection and high spurious free dynamic range.

The OPA640 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. This allows the OPA640 to be used in all op amp applications requiring high speed and precision.

Low noise, wide bandwidth, and high linearity make this amplifier suitable for a variety of RF and video applications.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
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# SPECIFICATIONS

## ELECTRICAL

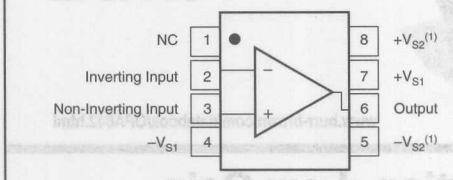
At $T_A$ = +25°C, $V_S$ = ±5V, $R_L$ = 100Ω, $C_L$ = 2pF, $R_{FB}$ = 402Ω and all four power supply pins are used, unless otherwise noted. $R_{FB}$ = 25Ω for a gain of +1.

| PARAMETER | CONDITIONS | OPA640P, U | | | OPA640UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | | | ±2.0 | ±5 | | 1.0 | ±2.0 | mV |
| Average Drift, | | | ±10 | | | ±6 | | µV/°C |
| Power Supply Rejection (+$V_S$) | $V_S$ = ±4.5 to ±5.5V | 60 | 75 | | * | * | | dB |
| (–$V_S$) | | 53 | 60 | | * | * | | dB |
| **INPUT BIAS CURRENT**(1) | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | 15 | 25 | | * | * | µA |
| Over Specified Temperature | | | 30 | 75 | | 18 | 55 | µA |
| Input Offset Current | $V_{CM}$ = 0V | | 0.3 | 2.0 | | * | 1.0 | µA |
| Over Specified Temperature | | | 0.5 | 2.5 | | * | 2.0 | µA |
| **NOISE** | | | | | | | | |
| Input Voltage Noise Density | | | | | | | | |
| f = 100Hz | | | 7.0 | | | * | | nV/√Hz |
| f = 10kHz | | | 2.8 | | | * | | nV/√Hz |
| f = 1MHz | | | 2.8 | | | * | | nV/√Hz |
| f = 1MHz to 500MHz | | | 2.9 | | | * | | nV/√Hz |
| Voltage Noise, BW = 100Hz to 500MHz | | | 65 | | | * | | µVrms |
| Input Bias Current Noise Density | | | | | | | | |
| f = 0.1Hz to 20kHz | | | 2.0 | | | * | | pA/√Hz |
| Noise Figure (NF) | | | | | | | | |
| $R_S$ = 1kΩ | | | 2.6 | | | * | | dB |
| $R_S$ = 50Ω | | | 10.9 | | | * | | dB |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | ±2.5 | ±2.85 | | * | * | | V |
| Over Temperature | | ±2.5 | ±2.75 | | * | * | | V |
| Common-Mode Rejection | $V_{CM}$ = ±0.5V | 70 | 85 | | 80 | 88 | | dB |
| **INPUT IMPEDANCE** | | | | | | | | |
| Differential | | | 15 ‖ 1 | | | * | | kΩ ‖ pF |
| Common-Mode | | | 2 ‖ 1 | | | * | | MΩ ‖ pF |
| **OPEN-LOOP GAIN, DC** | | | | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±2V, $R_L$ = 100Ω | 50 | 57 | | 53 | * | | dB |
| Over Specified Temperature | $V_O$ = ±2V, $R_L$ = 100Ω | 45 | 55 | | * | * | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Closed-Loop Bandwidth | Gain = +1V/V | | 1.3 | | | * | | GHz |
| | Gain = +2V/V | | 280 | | | * | | MHz |
| | Gain = +5V/V | | 65 | | | * | | MHz |
| | Gain = +10V/V | | 31 | | | * | | MHz |
| Slew Rate(2) | G = +1, 2V Step | | 350 | | | * | | V/µs |
| At Minimum Specified Temperature | G = +1, 2V Step | | 285 | | | * | | V/µs |
| Settling Time 0.01% | G = +1, 2V Step | | 22 | | | * | | ns |
| 0.1% | G = +1, 2V Step | | 18 | | | * | | ns |
| 1% | G = +1, 2V Step | | 4.5 | | | * | | ns |
| Spurious Free Dynamic Range | G = +1, f = 5MHz, $V_O$ = 2Vp-p | | 85 | | | * | | dBc |
| | G = +1, f = 10MHz, $V_O$ = 2Vp-p | | 75 | | | * | | dBc |
| | G = +1, f = 20MHz, $V_O$ = 2Vp-p | | 65 | | | * | | dBc |
| Gain Flatness to 0.1dB | G = +1 or +2 | | 120 | | | * | | MHz |
| Differential Gain at 3.58MHz, G = +2V/V | $V_O$ = 0V to 1.4V, $R_L$ = 150Ω | | 0.07 | | | * | | % |
| Differential Phase at 3.58MHz, G = +2V/V | $V_O$ = 0V to 1.4V, $R_L$ = 150Ω | | 0.008 | | | * | | Degrees |
| **OUTPUT** | | | | | | | | |
| Voltage Output | No Load | | | | | | | |
| Over Specified Temperature | | ±2.6 | ±3.0 | | * | * | | V |
| Voltage Output | $R_L$ = 100Ω | | | | | | | |
| Over Specified Temperature | | ±2.25 | ±2.5 | | * | * | | V |
| Current Output, +25°C | | ±40 | ±52 | | * | * | | mA |
| Over Specified Temperature | | ±25 | ±45 | | * | * | | mA |
| Short Circuit Current | | | 75 | | | * | | mA |
| Output Resistance | 1MHz, G = +1V/V | | 0.2 | | | * | | Ω |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | $T_{MIN}$ to $T_{MAX}$ | | ±5 | | | * | | V |
| Operating Voltage Range | $T_{MIN}$ to $T_{MAX}$ | ±4.5 | | ±5.5 | * | | * | V |
| Quiescent Current | | | ±18 | ±22 | | * | * | mA |
| Over Specified Temperature | | | ±19 | ±24 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: P, U, UB | Ambient | –40 | | +85 | * | | * | °C |
| Thermal Resistance | $\theta_{JA}$, Junction to Ambient | | | | | | | °C/W |
| P 8-Pin DIP | | | 100 | | | * | | °C/W |
| U, UB 8-Pin SO-8 | | | 125 | | | * | | °C/W |

NOTE: (1) Slew rate is rate of change from 10% to 90% of output voltage step.

## PIN CONFIGURATION

Top View DIP/SO-8




NOTE: (1) Making use of all four power supply pins is highly recommended, although not required. Using these four pins, instead of just pins 4 and 7, will lower the effective pin impedance and substantially lower distortion.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply | ±5.5VDC |
| Internal Power Dissipation | Thermal Considerations |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: P, U, UB | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SO-8 3s) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

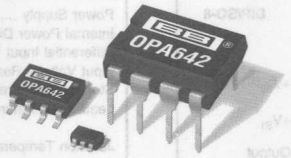
## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| OPA640P | 8-Pin Plastic DIP | 006 |
| OPA640U, UB | SO-8 Surface Mount | 182 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade of the SO-8 and package will be marked with a "B" by pin 8.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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# OPA642

www.burr-brown.com/databook/OPA642.html

# Wideband, Low Distortion, Low Gain OPERATIONAL AMPLIFIER

## FEATURES

- LOW DISTORTION: –95dBc at 5MHz
- GAIN OF +1 BANDWIDTH: 400MHz
- AVAILABLE IN SOT23-5 PACKAGE
- HIGH OPEN LOOP GAIN: 95dB
- HIGH COMMON-MODE REJECTION: 90dB
- FAST 12-BIT SETTLING: 13ns (0.01%)
- LOW NOISE: 2.7nV/√Hz
- HIGH OUTPUT CURRENT: ±60mA
- VERY LOW DIFF GAIN/PHASE ERROR: 0.007%/0.008°

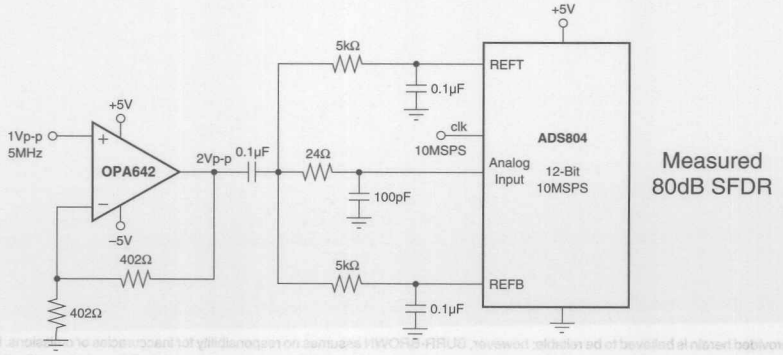
## APPLICATIONS

- ADC/DAC BUFFER AMPLIFIER
- LOW DISTORTION IF AMPLIFIER
- HIGH RESOLUTION IMAGING
- MEDICAL IMAGING
- LOW NOISE PREAMPLIFIER
- HIGH CMR DIFFERENCING AMPLIFIER
- TEST INSTRUMENTATION
- PROFESSIONAL AUDIO

## DESCRIPTION

The OPA642 provides a level of speed and dynamic range previously unattainable in a monolithic op amp. Using a unity gain stable voltage feedback architecture with two internal gain stages, the OPA642 achieves exceptionally low harmonic distortion over a wide frequency range. The "classic" differential input provides all the familiar benefits of precision op amps, such as bias current cancellation and very low inverting current noise compared with wideband current feedback op amps. Fast settling time, excellent differential gain/phase performance, low voltage noise and high output current drive make the OPA642 ideal for most high dynamic range applications.

Unity gain stability makes the OPA642 particularly suitable for low gain differential amplifiers, transimpedance amplifiers, gain of +2 video line drivers, wideband integrators and low distortion ADC buffers. Where higher gain or even lower harmonic distortion is required, consider the OPA643—a higher gain-bandwidth and lower noise version of the OPA642




Measured 80dB SFDR

High Dynamic Range 10MSPS Digitizer

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $V_S$ = ±5V, $R_L$ = 100Ω, $R_F$ = 402Ω, unless otherwise noted. $R_F$ = 25Ω for a gain of +1.

| PARAMETER | CONDITIONS | OPA642P, U, N | | | OPA642PB, UB, NB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | | | ±1.5 | ±4 | | ±0.5 | ±1.0 | mV |
| Average Drift | | | 4 | | | 2 | | µV/°C |
| Power Supply Rejection (PSR) | $V_S$ = ±4.5 to ±5.5V | 65 | 85 | | 73 | 95 | | dB |
| **INPUT BIAS CURRENT** | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | 25 | 45 | | * | * | µA |
| Over Specified Temperature | | | | 70 | | * | * | µA |
| Input Offset Current | $V_{CM}$ = 0V | | 0.1 | 2.0 | | * | * | µA |
| Over Specified Temperature | | | | 3.0 | | * | * | µA |
| **NOISE** | | | | | | | | |
| Input Voltage Noise | | | | | | | | |
| Noise Density: f ≥ 1MHz | | | 2.7 | | | * | | nV/√Hz |
| Integrated Voltage Noise, BW = 100Hz to 100MHz | | | 27 | | | * | | µVrms |
| Input Bias Current Noise Density | | | | | | | | |
| f ≥ 1MHz | | | 2.8 | | | * | | pA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | ±2.75 | ±3.0 | | * | * | | V |
| Over Temperature | | ±2.5 | | | * | | | V |
| Common-Mode Rejection (CMR) | $V_{CM}$ = ±0.5V | 65 | 90 | | 80 | * | | dB |
| **INPUT IMPEDANCE** | | | | | | | | |
| Differential | | | 11 ‖ 1 | | | * | | kΩ ‖ pF |
| Common-Mode | | | 650 ‖ 1 | | | * | | kΩ ‖ pF |
| **OPEN-LOOP GAIN** | | | | | | | | |
| Open-Loop Voltage Gain ($A_{OL}$) | $V_O$ = ±2V, $R_L$ = 100Ω | 80 | 95 | | 85 | 98 | | dB |
| Over Specified Temperature | | 80 | | | * | | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Closed-Loop Response | Gain = +1V/V | | 400 | | | * | | MHz |
| | Gain = +2V/V | | 150 | | | * | | MHz |
| | Gain = +5V/V | | 45 | | | * | | MHz |
| | Gain = +10V/V | | 21 | | | * | | MHz |
| Gain Bandwidth Product (GBP) | | | 210 | | | * | | MHz |
| Slew Rate[1] | G = +1, 2V Step | | 380 | | | * | | V/µs |
| At Minimum Specified Temperature | G = +1, 2V Step | | 340 | | | * | | V/µs |
| Settling Time: 0.01% | G = +1, 1V Step | | 13 | | | * | | ns |
| 0.1% | G = +1, 1V Step | | 11.5 | | | * | | ns |
| 1% | G = +1, 1V Step | | 3.5 | | | * | | ns |
| Spurious Free Dynamic Range (SFDR) | G = +1, f = 5MHz<br>$V_O$ = 2Vp-p, $R_L$ = 100Ω | | 92 | | | 95 | | dBc |
| Diff. Gain Error at 3.58MHz, G = +2V/V | $V_O$ = 0V to 1.4V, $R_L$ = 150Ω | | 0.007 | | | * | | % |
| Diff. Phase Error at 3.58MHz, G = +2V/V | $V_O$ = 0V to 1.4V, $R_L$ = 150Ω | | 0.008 | | | * | | degrees |
| **OUTPUT** | | | | | | | | |
| Voltage Output | No Load | | ±3.5 | | | * | | V |
| Over Specified Temperature | | ±3.0 | | | * | | | V |
| Voltage Output | $R_L$ = 100Ω | | ±2.75 | | | * | | V |
| Over Specified Temperature | | ±2.5 | | | * | * | | V |
| Current Output, +25°C | | ±40 | ±60 | | ±50 | ±65 | | mA |
| Over Specified Temperature | | ±35 | | | ±40 | | | mA |
| Closed-Loop Output Resistance | 0.1MHz, G = +1V/V | | 0.01 | | | * | | Ω |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | | ±5 | | | * | | V |
| Operating Voltage Range | $T_{MIN}$ to $T_{MAX}$ | ±4.5 | | ±5.5 | * | | * | V |
| Quiescent Current | | | ±20 | ±25 | ±16 | * | * | mA |
| Over Specified Temperature | | | | ±26 | | | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: P, U, N, PB, UB, NB | Ambient | –40 | | +85 | * | | * | °C |
| Thermal Resistance | $\theta_{JA}$, Junction-to-Ambient | | | | | | | °C/W |
| P, PB 8-Pin DIP | | | 100 | | | * | | °C/W |
| U, UB 8-Pin SO-8 | | | 125 | | | * | | °C/W |
| N, NB 5-Pin SOT23-5 | | | 150 | | | * | | °C/W |

* Indicates same specification as for OPA642P, U, N.

NOTE: (1) Slew rate is rate of change from 10% to 90% of output voltage step.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply | ±6.0VDC |
| Internal Power Dissipation[1] | See Thermal Analysis |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: P, PB, U, UB, N, NB | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SO-8 3s) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

NOTE: (1) Packages must be derated based on specified $\theta_{JA}$. Maximum $T_J$ must be observed.

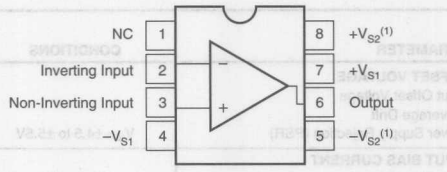
## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

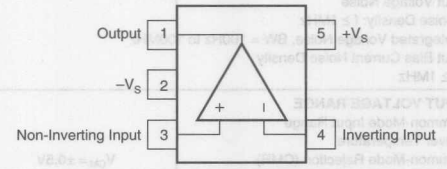
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION

Top View — DIP/SO-8




SOT23-5




NOTE: (1) Making use of all four power supply pins is recommended, although not required. Using these four pins, instead of just pins 4 and 7, will lower the power supply impedance improving distortion.

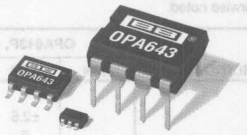
## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE | PACKAGE MARKING[2] | ORDERING NUMBER[3] |
|---|---|---|---|---|---|
| OPA642U | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA642U | OPA642U |
| OPA642UB | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA642UB | OPA642UB |
| OPA642N | 5-pin SOT23-5 | 331 | –40°C to +85°C | A42 | OPA642N-250<br>OPA642N-3k |
| OPA642NB | 5-pin SOT23-5 | 331 | –40°C to +85°C | A42B | OPA642NB-250<br>OPA642NB-3k |
| OPA642P | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA642P | OPA642P |
| OPA642PB | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA642PB | OPA642PB |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade of the SO-8 and DIP packages will be marked with a "B" by pin 8. The "B" grade of the SOT23-5 will be marked with a "B" near pins 3 and 4. (3) The SOT23-5 is only available on a 7" tape and reel (e.g. ordering 250 pieces of "OPA642N-250" will get a single 250 piece tape and reel. Ordering 3000 pieces of "OPA642N-3k" will get a single 3000 piece tape and reel). Please refer to Appendix B of Burr-Brown IC Data Book for detailed Tape and Reel Mechanical information.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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# OPA643

www.burr-brown.com/databook/OPA643.html

# Wideband Low Distortion, High Gain OPERATIONAL AMPLIFIER

## FEATURES

- LOW DISTORTION: –90dBc at 5MHz
- LOW NOISE: 2.3nV/√Hz
- GAIN-BANDWIDTH PRODUCT: 800MHz
- AVAILABLE IN SOT23-5 PACKAGE
- STABLE IN GAINS ≥ 3
- HIGH SLEW RATE: 1000V/µs
- HIGH OPEN-LOOP GAIN: 95dB
- HIGH OUTPUT CURRENT: ±60mA

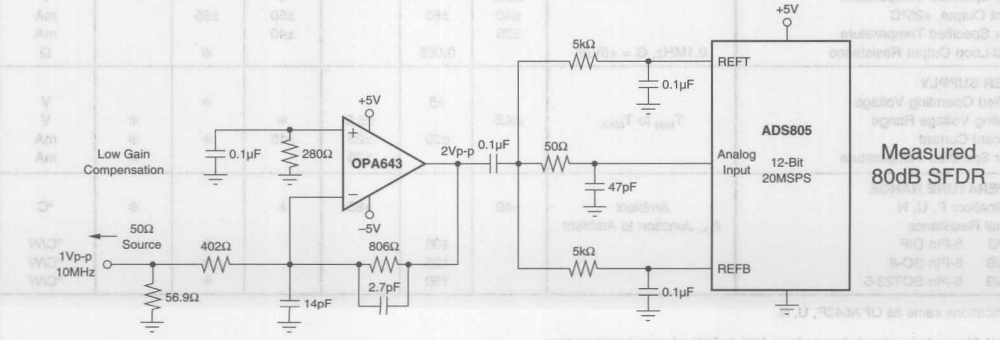
## APPLICATIONS

- BASE STATION ADC PREAMP
- ADC/DAC BUFFER AMPLIFIER
- LOW DISTORTION IF AMPLIFIER
- LOW NOISE, BROADBAND, TRANSIMPEDANCE AMPLIFIER
- LOW NOISE PREAMPLIFIER
- VIDEO AMPLIFICATION
- TEST INSTRUMENTATION

## DESCRIPTION

The OPA643 provides a level of speed and dynamic range previously unattainable in a monolithic op amp. Using a de-compensated voltage feedback architecture with two internal gain stages, the OPA643 achieves exceptionally low harmonic distortion over a wide frequency range. The "classic" differential input provides all the familiar benefits of precision op amps, such as bias current cancellation and very low inverting current noise compared with wideband current feedback op amps. High slew rate and open-loop gain, along with low input noise and high output current drive make the OPA643 ideal for very high dynamic range requirements.

The high gain bandwidth product for the gain ≥ 3 stable OPA643 makes it particularly suitable for wideband transimpedance amplifiers and moderate gain IF amplifier applications. External compensation techniques may be used to apply the OPA643 at low gains giving exceptionally low distortion and frequency response flatness. Where unity gain stability with comparable distortion performance is required, consider the OPA642.




High Dynamic Range 20MSPS Digitizer

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

## ELECTRICAL

At $T_A$ = +25°C, $V_S$ = ±5V, $R_L$ = 100Ω, $R_F$ = 402Ω, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA643P, U, N | | | OPA643PB, UB, NB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | | | ±2.5 | ±4 | | ±0.5 | ±1.5 | mV |
| Average Drift | | | 5 | | | 3 | | µV/°C |
| Power Supply Rejection (PSR) | $V_S$ = ±4.5 to ±5.5V | 65 | 90 | | 70 | * | | dB |
| **INPUT BIAS CURRENT** | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | 19 | 30 | | * | * | µA |
| Over Specified Temperature | | | | 40 | | | * | µA |
| Input Offset Current | $V_{CM}$ = 0V | | 0.1 | 2.0 | | * | * | µA |
| Over Specified Temperature | | | | 3.0 | | | * | µA |
| **NOISE** | | | | | | | | |
| Input Voltage Noise | | | | | | | | |
| Noise Density: f > 1MHz | | | 2.3 | | | * | | nV/√Hz |
| Integrated Voltage Noise, BW = 100Hz to 100MHz | | | 23 | | | * | | µVrms |
| Input Bias Current Noise | | | | | | | | |
| Current Noise Density, f > 1MHz | | | 2.5 | | | * | | pA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | ±2.75 | ±3.0 | | * | * | | V |
| Over Specified Temperature | | ±2.5 | | | * | | | V |
| Common-Mode Rejection (CMR) | $V_{CM}$ = ±0.5V | 65 | 85 | | 80 | 92 | | dB |
| **INPUT IMPEDANCE** | | | | | | | | |
| Differential | | | 7 ‖ 2.5 | | | * | | kΩ ‖ pF |
| Common-Mode | | | 630 ‖ 1.3 | | | * | | kΩ ‖ pF |
| **OPEN-LOOP GAIN** | | | | | | | | |
| Open-Loop Voltage Gain ($A_{OL}$) | $V_O$ = ±2V, $R_L$ = 100Ω | 82 | 95 | | 87 | * | | dB |
| Over Specified Temperature | $V_O$ = ±2V, $R_L$ = 100Ω | 80 | | | 80 | | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Closed-Loop Bandwidth | Gain = +5V/V | | 200 | | | * | | MHz |
| | Gain = +10V/V | | 85 | | | * | | MHz |
| | Gain = +20V/V | | 40 | | | * | | MHz |
| Gain Bandwidth Product (GBP) | | | 800 | | | * | | MHz |
| Slew Rate[1] | G = +5, 2V Step | | 1000 | | | * | | V/µs |
| At Minimum Specified Temperature | G = +5, 2V Step | | 920 | | | * | | V/µs |
| Settling Time: 0.01% | G = +5, 2V Step | | 21 | | | * | | ns |
| 0.1% | G = +5, 2V Step | | 16.5 | | | * | | ns |
| 1% | G = +5, 2V Step | | 7.5 | | | | | ns |
| Spurious Free Dynamic Range (SFDR) | G = +5, f = 5MHz | | 90 | | | 95 | | dBc |
| | $V_O$ = 2Vp-p, $R_L$ = 500Ω | | | | | | | |
| Differential Gain Error at 3.58MHz | G = +5V/V, $V_O$ = 0V to 1.4V, $R_L$ = 150Ω | | 0.005 | | | * | | % |
| Differential Phase Error at 3.58MHz | G = +5V/V, $V_O$ = 0V to 1.4V, $R_L$ = 150Ω | | 0.015 | | | * | | degrees |
| **OUTPUT** | | | | | | | | |
| Voltage Output | No Load | | ±3.25 | | | * | | V |
| Over Specified Temperature | | ±3.0 | | | * | | | V |
| Voltage Output, +25°C | $R_L$ = 100Ω | | ±2.75 | | | * | | V |
| Over Specified Temperature | | ±2.5 | | | * | | | V |
| Current Output, +25°C | | ±40 | ±60 | | ±50 | ±65 | | mA |
| Over Specified Temperature | | ±35 | | | ±40 | | | mA |
| Closed-Loop Output Resistance | 0.1MHz, G = +5V/V | | 0.055 | | | * | | Ω |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | | ±5 | | | * | | V |
| Operating Voltage Range | $T_{MIN}$ to $T_{MAX}$ | ±4.5 | | ±5.5 | * | | * | V |
| Quiescent Current | | | ±20 | ±25 | ±16 | * | * | mA |
| Over Specified Temperature | | | | ±26 | | | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: P, U, N | Ambient | –40 | | +85 | * | | * | °C |
| Thermal Resistance | $\theta_{JA}$, Junction to Ambient | | | | | | | |
| P, PB 8-Pin DIP | | | 100 | | | * | | °C/W |
| U, UB 8-Pin SO-8 | | | 125 | | | * | | °C/W |
| N, NB 5-Pin SOT23-5 | | | 150 | | | * | | °C/W |

* Specifications same as OPA643P, U, N.

NOTE: (1) Slew rate is rate of change from 10% to 90% of output voltage step.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply ($\pm V_S$) | ±6.0VDC |
| Internal Power Dissipation(1) | See Thermal Analysis |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: P, PB, U, UB, N, NB | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SO-8 3s) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

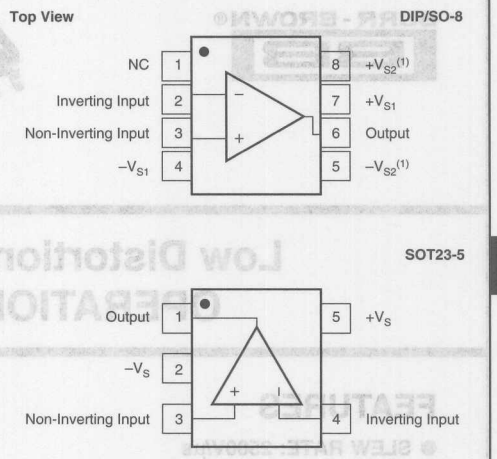
NOTE: (1) Packages must be derated based on specified $\theta_{JA}$. Maximum $T_J$ must be observed.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION




NOTE: (1) Making use of all four power supply pins is highly recommended, although not required. Using these four pins, instead of just pins 4 and 7, will lower the power supply impedance improving distortion.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE | PACKAGE MARKING(2) | ORDERING NUMBER(3) |
|---|---|---|---|---|---|
| OPA643U | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA643U | OPA643U |
| OPA643UB | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA643UB | OPA643UB |
| OPA643N | 5-pin SOT23-5 | 331 | –40°C to +85°C | A43 | OPA643N-250<br>OPA643N-3k |
| OPA643NB | 5-pin SOT23-5 | 331 | –40°C to +85°C | A43B | OPA643NB-250<br>OPA643NB-3k |
| OPA643P | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA643P | OPA643P |
| OPA643PB | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA643PB | OPA643PB |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade of the SO-8 and DIP packages will be marked with a "B" by pin 8. The "B" grade of the SOT23-5 will be marked with a "B" near pins 3 and 4. (3) The SOT23-5 is only available on a 7" tape and reel (e.g. ordering 250 pieces of "OPA643N-250" will get a single 250 piece tape and reel. Ordering 3000 pieces of "OPA643N-3k" will get a single 3000 piece tape and reel). Please refer to Appendix B of Burr-Brown IC Data Book for detailed Tape and Reel Mechanical information.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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# OPA644

www.burr-brown.com/databook/OPA644.html

# Low Distortion Current Feedback OPERATIONAL AMPLIFIER

## FEATURES

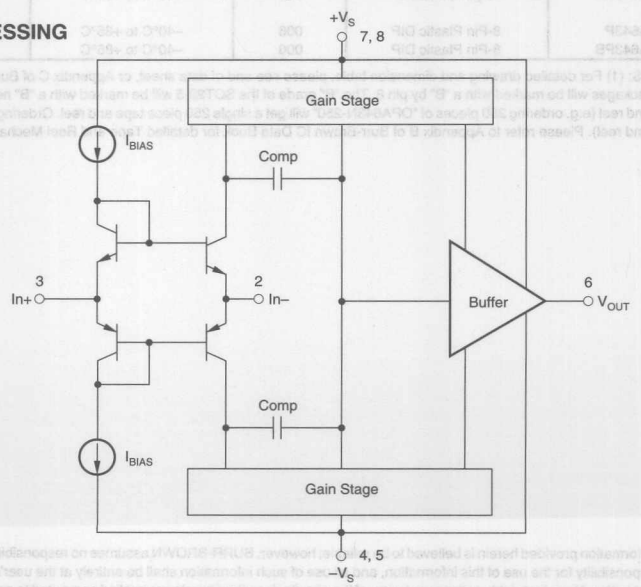
- SLEW RATE: 2500V/µs
- VERY LOW DIFFERENTIAL GAIN/PHASE ERROR: 0.008%/0.009°
- LOW DISTORTION AT 5MHz: –85dBc
- HIGH BANDWIDTH: 500MHz
- HIGH OPEN LOOP TRANSIMPEDANCE: 2.0MΩ
- HIGH LINEARITY
- FAST 12-BIT SETTLING: 21ns to 0.01%
- UNITY-GAIN STABLE

## APPLICATIONS

- HIGH-SPEED SIGNAL PROCESSING
- HIGH-RESOLUTION VIDEO
- PULSE AMPLIFICATION
- COMMUNICATIONS
- ADC/DAC GAIN AMPLIFIER
- RF AMPLIFICATION
- MEDICAL IMAGING
- AUDIO AMPLIFICATION

## DESCRIPTION

The OPA644 is a wideband precision current feedback operational amplifier featuring exceptionally high open loop transimpedance and high slew rate. The current feedback architecture allows for excellent large signal bandwidth, even at high gains. The high transimpedance allows this op amp to be used in applications requiring 16 bits or more of accuracy. This extra transimpedance at high bandwidths gives very low distortion and low differential gain and phase errors. The high slew rate and well-behaved pulse response allow for superior large signal amplification in a variety of RF, video and other signal processing applications. Fabricated on an advanced complementary bipolar process, the OPA644 offers exceptional performance in monolithic form.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132



PDS-1187D

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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $V_S$ = ±5V, $R_L$ = 100Ω, $C_L$ = 2pF, $R_{FB}$ = 402Ω and all four power supply pins are used, unless otherwise noted.

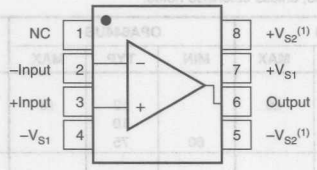
| PARAMETER | CONDITIONS | OPA644U MIN | OPA644U TYP | OPA644U MAX | OPA644UB MIN | OPA644UB TYP | OPA644UB MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | | | ±2.5 | ±6 | | ±2 | ±3 | mV |
| Average Drift | | | 20 | | | 10 | | µV/°C |
| Power Supply Rejection | $V_S$ = ±4.5 to ±5.5V | 40 | 65 | | 60 | 75 | | dB |
| **INPUT BIAS CURRENT**(1) | | | | | | | | |
| Non-Inverting | | | ±20 | ±40 | | ±15 | ±20 | µA |
| Over Specified Temperature | | | ±24 | ±90 | | ±20 | ±50 | µA |
| Inverting | | | ±2 | ±25 | | * | ±10 | µA |
| Over Specified Temperature | | | ±4 | ±35 | | ±3 | ±25 | µA |
| **NOISE** | | | | | | | | |
| Input Voltage Noise Density | | | | | | | | |
| f = 100Hz | | | 10.3 | | | * | | nV/√Hz |
| f = 1kHz | | | 2.9 | | | * | | nV/√Hz |
| f = 10kHz | | | 1.9 | | | * | | nV/√Hz |
| f = 1MHz | | | 1.9 | | | * | | nV/√Hz |
| $f_B$ = 100Hz to 200MHz | | | 33.6 | | | * | | µVrms |
| Inverting Input Bias Current | | | | | | | | |
| Noise Density: f = 10MHz | | | 15 | | | * | | pA/√Hz |
| Non-Inverting Input Current | | | | | | | | |
| Noise Density: f = 10MHz | | | 15 | | | * | | pA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | ±2.0 | ±2.25 | | * | * | | V |
| Over Specified Temperature | | ±1.8 | ±2.1 | | * | * | | V |
| Common-Mode Rejection | $V_{CM}$ = ±2V | 35 | 55 | | 45 | 65 | | dB |
| **INPUT IMPEDANCE** | | | | | | | | |
| Non-Inverting | | | 500 ‖ 1.0 | | | * | | kΩ ‖ pF |
| Inverting | | | 20 | | | 46 | | Ω |
| Open-Loop Transimpedance | $V_O$ = ±2V, $R_L$ = 1kΩ | 1.4 | 2.0 | | * | * | | MΩ |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Closed-Loop Bandwidth | G = +1V/V | | 500 | | | * | | MHz |
| | G = +2V/V | | 300 | | | * | | MHz |
| | G = +5V/V | | 180 | | | * | | MHz |
| | G = +10V/V | | 125 | | | * | | MHz |
| | G = +20V/V | | 80 | | | * | | MHz |
| Slew Rate(1) | G = +2, 2V Step | | 2500 | | | * | | V/µs |
| Settling Time: 0.01% | G = +2, 2V Step | | 21 | | | * | | ns |
| 0.1% | G = +2, 2V Step | | 16.5 | | | * | | ns |
| 1% | G = +2, 2V Step | | 5.5 | | | * | | ns |
| Overload Recovery Time(2) | | | 60 | | | * | | ns |
| Spurious Free Dynamic Range | G = –1, f = 5.0MHz, $V_O$ = 2Vp-p | | 84 | | | 86 | | dBc |
| | G = –1, f = 20MHz | | | | | | | dBc |
| Differential Gain Error at 3.58MHz | G = +2V/V, $V_O$ = 0V to 1.4V, $R_L$ = 150Ω | | 0.008 | | | * | | % |
| Differential Phase Error at 3.58MHz | G = +2V/V, $V_O$ = 0V to 1.4V, $R_L$ = 150Ω | | 0.009 | | | * | | Degrees |
| Gain Flatness to 1dB | G = +1 | | 250 | | | * | | MHz |
| **OUTPUT** | | | | | | | | |
| Current Output | | ±40 | ±60 | | ±50 | ±66 | | mA |
| Over Specified Temperature | | ±30 | ±45 | | ±40 | ±50 | | mA |
| Voltage Output | No Load | | | | | | | |
| Over Specified Temperature | | ±3.0 | ±3.5 | | * | * | | V |
| Voltage Output | $R_L$ = 100Ω | | | | | | | |
| Over Specified Temperature | | ±2.75 | ±3.25 | | * | * | | V |
| Short Circuit Current | | | 75 | | | | * | mA |
| Output Resistance | 1MHz, G = +2V/V | | 0.2 | | | | * | Ω |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | $T_{MIN}$ to $T_{MAX}$ | | ±5 | | | * | | V |
| Operating Voltage Range | $T_{MIN}$ to $T_{MAX}$ | ±4.5 | | ±5.5 | * | | * | V |
| Quiescent Current | $T_{MIN}$ to $T_{MAX}$ | | ±18 | ±26 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: U | | –40 | | +85 | * | | * | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| U, UB 8-Pin SO-8 | | | 125 | | | * | | °C/W |

* Specification same as OPA644U.

NOTES: (1) Slew rate is rate of change from 10% to 90% of the output voltage step. (2) Time for the output to resume linear operation after saturation.

## PIN CONFIGURATION (All Packages)

Top View SO-8




NOTE: (1) Making use of all four power supply pins is highly recommended, although not required. Using these four pins, instead of just pins 4 and 7, will lower the effective pin impedance and substantially lower distortion.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| OPA644U, UB | SO-8 Surface Mount | 182 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade of the SO-8 package will be marked with a "B" by pin 8.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply | ±5.5VDC |
| Internal Power Dissipation | See Thermal Considerations |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: U, UB | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SO-8 3s) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# OPA646

www.burr-brown.com/databook/OPA646.html

# Low Power, Wide Bandwidth OPERATIONAL AMPLIFIER

## FEATURES

- LOW POWER: 55mW
- UNITY-GAIN BANDWIDTH: 650MHz
- UNITY-GAIN STABLE
- FAST 12-BIT SETTLING: 15ns (0.01%)
- LOW INPUT BIAS CURRENT: 2μA
- LOW HARMONICS: –82dBc at 5MHz
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.025%/0.08°

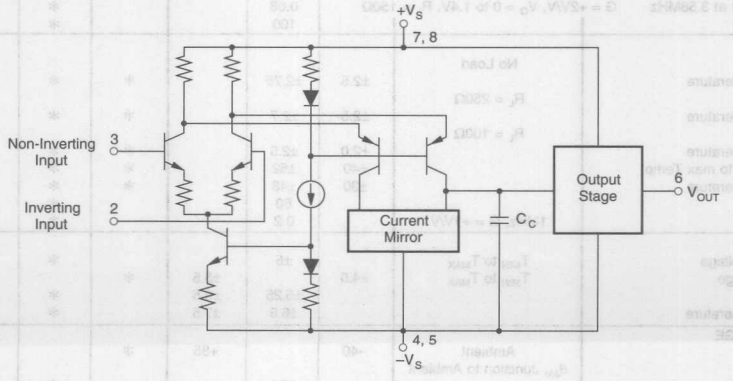
## APPLICATIONS

- TELECOMMUNICATIONS
- MEDICAL IMAGING
- CCD IMAGING
- PORTABLE EQUIPMENT
- ACTIVE FILTERS
- VIDEO AMPLIFICATION
- ADC/DAC GAIN AMPLIFIER
- HIGH SPEED INTEGRATORS

## DESCRIPTION

The OPA646 is a low power, wideband voltage feedback operational amplifier. It features a high bandwidth of 650MHz as well as a 12-bit settling time of only 15ns. Its low input bias current and wide bandwidth allows it to be used for high speed integrator and active filter designs. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA646 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Its unusual combination of speed, accuracy and low power make it an ideal choice for many portable, multichannel and other high speed applications where power is at a premium.




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# SPECIFICATIONS

## ELECTRICAL

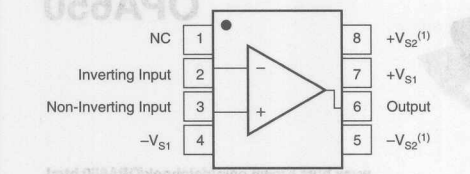
At $T_A$ = +25°C, $V_S$ = ±5V, $R_L$ = 100Ω, $C_L$ = 2pF, $R_{FB}$ = 402Ω and all four power supply pins are used, unless otherwise noted. $R_{FB}$ = 25Ω for a gain of +1.

| PARAMETER | CONDITIONS | OPA646U | | | OPA646UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | | | ±3 | ±8 | | ±1 | ±2.5 | mV |
| Average Drift | | | ±20 | | | ±12 | | µV/°C |
| Power Supply Rejection (+$V_S$) | $V_S$ = ±4.5 to ±5.5V | 50 | 70 | | 60 | * | | dB |
| (–$V_S$) | | 45 | 55 | | 48 | * | | dB |
| **INPUT BIAS CURRENT** | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | 2 | 5 | | * | 3.5 | µA |
| Over Specified Temperature | | | 3 | 7 | | * | * | µA |
| Input Offset Current | $V_{CM}$ = 0V | | 0.4 | 1.5 | | * | * | µA |
| Over Specified Temperature | | | 0.9 | 3.0 | | * | * | µA |
| **NOISE** | | | | | | | | |
| Input Voltage Noise | | | | | | | | |
| Noise Density: f = 100Hz | | | 23.2 | | | * | | nV/√Hz |
| f = 10kHz | | | 7.5 | | | * | | nV/√Hz |
| f = 1MHz | | | 7.1 | | | * | | nV/√Hz |
| f = 1MHz to 100MHz | | | 7.2 | | | * | | nV/√Hz |
| Voltage Noise, BW = 100Hz to 100MHz | | | 141 | | | * | | µVrms |
| Input Bias Current Noise | | | | | | | | |
| Current Noise Density, f = 0.1Hz to 20kHz | | | 1.1 | | | * | | pA/√Hz |
| Noise Figure (NF) | | | | | | | | |
| $R_S$ = 10kΩ | | | 3.0 | | | * | | dB |
| $R_S$ = 50Ω | | | 19.1 | | | * | | dB |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | ±2.5 | ±3.0 | | * | * | | V |
| Over Specified Temperature | | ±2.5 | ±3.0 | | * | * | | V |
| Common-Mode Rejection | $V_{CM}$ = ±0.5V | 60 | 80 | | 75 | 90 | | dB |
| **INPUT IMPEDANCE** | | | | | | | | |
| Differential | | | 15 ll 1 | | | * | | kΩ ll pF |
| Common-Mode | | | 1.6 ll 1 | | | * | | MΩ ll pF |
| **OPEN-LOOP GAIN** | | | | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±2V, $R_L$ = 100Ω | 45 | 51 | | 47 | 55 | | dB |
| Over Specified Temperature | | 43 | 49 | | 45 | 53 | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Closed-Loop Bandwidth | G = +1V/V | | 650 | | | * | | MHz |
| | G = +2V/V | | 160 | | | * | | MHz |
| | G = +5V/V | | 45 | | | * | | MHz |
| | G = +10V/V | | 22 | | | * | | MHz |
| Slew Rate[1] | G = +1, 2V Step | | 180 | | | * | | V/µs |
| At Minimum Specified Temperature | | | 155 | | | * | | V/µs |
| Rise Time | 1V Step | | 5.3 | | | * | | ns |
| Fall Time | 1V Step | | 5.9 | | | * | | ns |
| Settling Time: 0.01% | G = +1, 2V Step | | 15 | | | * | | ns |
| 0.1% | G = +1, 2V Step | | 11.5 | | | * | | ns |
| 1% | G = +1, 2V Step | | 6 | | | * | | ns |
| Over-Voltage Recovery[2] | | | 65 | | | | | ns |
| Spurious Free Dynamic Range | G = +1, f = 5.0MHz $V_O$ = 2Vp-p, $R_L$ = 402Ω | | 82 | | | * | | dBc |
| Differential Gain Error at 3.58MHz | G = +2V/V, $V_O$ = 0 to 1.4V, $R_L$ = 150Ω | | 0.025 | | | * | | % |
| Differential Phase Error at 3.58MHz | G = +2V/V, $V_O$ = 0 to 1.4V, $R_L$ = 150Ω | | 0.08 | | | * | | degrees |
| Gain Flatness to 0.1dB | | | 100 | | | * | | MHz |
| **OUTPUT** | | | | | | | | |
| Voltage Output | No Load | | | | | | | |
| Over Specified Temperature | | ±2.5 | ±2.75 | | * | * | | V |
| Voltage Output | $R_L$ = 250Ω | | | | | | | V |
| Over Specified Temperature | | ±2.5 | ±2.7 | | * | * | | V |
| Voltage Output | $R_L$ = 100Ω | | | | | | | |
| Over Specified Temperature | | ±2.0 | ±2.5 | | * | * | | V |
| Current Output, +25°C to max Temp | | ±40 | ±52 | | * | * | | mA |
| Over Specified Temperature | | ±30 | ±48 | | * | * | | mA |
| Short Circuit Current | | | 60 | | | * | | mA |
| Output Resistance | 1MHz, G = +1V/V | | 0.2 | | | * | | Ω |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | $T_{MIN}$ to $T_{MAX}$ | | ±5 | | | * | | V |
| Operating Voltage Range | $T_{MIN}$ to $T_{MAX}$ | ±4.5 | | ±5.5 | * | | * | V |
| Quiescent Current | | | ±5.25 | ±6.5 | | * | * | mA |
| Over Specified Temperature | | | ±6.5 | ±7.5 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: U, UB | Ambient | –40 | | +85 | * | | * | °C |
| Thermal Resistance | $\theta_{JA}$, Junction to Ambient | | | | | | | |
| U, UB 8-Pin SO-8 | | | 125 | | | * | | °C/W |

* Specification same as OPA646U.

NOTE: (1) Slew rate is rate of change from 10% to 90% of output voltage step. (2) Recovery time to linear operation from the input overdrive midpoint.

## PIN CONFIGURATION




NOTE: (1) Making use of all four power supply pins is highly recommended, although not required. Using these four pins, instead of just pins 4 and 7, will lower the effective pin impedance and substantially lower distortion.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply | ±5.5VDC |
| Internal Power Dissipation | See Thermal Considerations |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: U, UB | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SO-8 3s) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

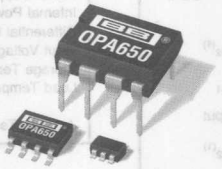
## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| OPA646U, UB | SO-8 Surface Mount | 182 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade of the SO-8 will be marked with a "B" by pin 8.

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# OPA650

www.burr-brown.com/databook/OPA650.html

# Wideband, Low Power Voltage Feedback OPERATIONAL AMPLIFIER

## FEATURES

- LOW POWER: 50mW
- UNITY GAIN STABLE BANDWIDTH: 560MHz
- LOW HARMONICS: –77dBc at 5MHz
- FAST SETTLING TIME: 20ns to 0.01%
- LOW INPUT BIAS CURRENT: 5μA
- DIFFERENTIAL GAIN/PHASE ERROR: 0.01%/0.03°
- HIGH OUTPUT CURRENT: 85mA

## APPLICATIONS

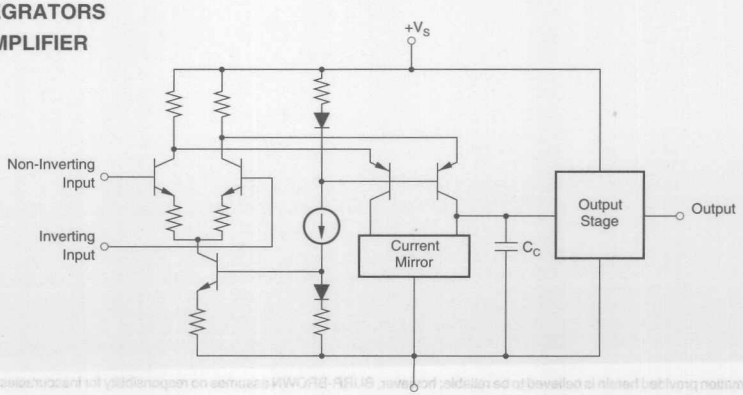
- HIGH RESOLUTION VIDEO
- BASEBAND AMPLIFIER
- CCD IMAGING AMPLIFIER
- ULTRASOUND SIGNAL PROCESSING
- ADC/DAC GAIN AMPLIFIER
- ACTIVE FILTERS
- HIGH SPEED INTEGRATORS
- DIFFERENTIAL AMPLIFIER

## DESCRIPTION

The OPA650 is a low power, wideband voltage feedback operational amplifier. It features a high bandwidth of 560MHz as well as a 12-bit settling time of only 20ns. The low distortion allows its use in communications applications, while the wide bandwidth and true differential input stage make it suitable for use in a variety of active filter applications. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA650 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Its unusual combination of speed, accuracy and low power make it an outstanding choice for many portable, multi-channel and other high speed applications, where power is at a premium.

The OPA650 is also available in dual (OPA2650) and quad (OPA4650) configurations.




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PDS-1264F

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# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = ±5V, $R_L$ = 100Ω, and $R_{FB}$ = 402Ω, unless otherwise noted. $R_{FB}$ = 25Ω for a gain of +1.

| PARAMETER | CONDITIONS | OPA650P, U, N MIN | OPA650P, U, N TYP | OPA650P, U, N MAX | OPA650UB, NB MIN | OPA650UB, NB TYP | OPA650UB, NB MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **FREQUENCY RESPONSE** | | | | | | | | |
| Closed-Loop Bandwidth[2] | G = +1 | | 560 | | | *[1] | | MHz |
| | G = +2 | | 140 | | | * | | MHz |
| | G = +5 | | 37 | | | * | | MHz |
| | G = +10 | | 18 | | | * | | MHz |
| Gain Bandwidth Product | | | 180 | | | * | | MHz |
| Slew Rate | G = +1, 2V Step | | 240 | | | * | | V/µs |
| Over Specified Temperature | | | 220 | | | * | | V/µs |
| Rise Time | 0.2V Step | | 1 | | | * | | ns |
| Fall Time | 0.2V Step | | 1 | | | * | | ns |
| Settling Time 0.01% | G = +1, 2V Step | | 19.6 | | | * | | ns |
| 0.1% | G = +1, 2V Step | | 10.2 | | | * | | ns |
| 1% | G = +1, 2V Step | | 6.3 | | | * | | ns |
| Spurious Free Dynamic Range | G = +1, f = 5.0 MHz, $V_O$ = 2Vp-p | | | | | | | |
| | $R_L$ = 100Ω | | 73 | | | * | | dBc |
| | $R_L$ = 200Ω | | 77 | | | * | | dBc |
| Differential Gain | G = +1, NTSC, $V_O$ = 1.4Vp, $R_L$ = 150Ω | | 0.01 | | | * | | % |
| Differential Phase | G = +1, NTSC, $V_O$ = 1.4Vp, $R_L$ = 150Ω | | 0.03 | | | * | | Degrees |
| Bandwidth for 0.1dB Gain Flatness | G = +2 | | 25 | | | * | | MHz |
| **INPUT OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | | | ±1 | ±5 | | 0.6 | ±2.5 | mV |
| Average Drift | | | ±3 | | | * | | µV/°C |
| Power Supply Rejection (+$V_S$) | $\|V_S\|$ = 4.5V to 5.5V | 60 | 76 | | 70 | * | | dB |
| (–$V_S$) | | 47 | 53 | | 50 | * | | dB |
| **INPUT BIAS CURRENT** | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | 5 | 20 | | * | 10 | µA |
| Over Temperature | | | | 30 | | | 20 | µA |
| Input Offset Current | $V_{CM}$ = 0V | | 0.5 | 1 | | 0.2 | 0.5 | µA |
| Over Temperature | | | | 3 | | | 2 | µA |
| **NOISE** | | | | | | | | |
| Input Voltage Noise | | | | | | | | |
| Noise Density, f = 100Hz | | | 43 | | | * | | nV/√Hz |
| f = 10kHz | | | 9.4 | | | * | | nV/√Hz |
| f = 1MHz | | | 8.4 | | | * | | nV/√Hz |
| f = 1MHz to 100MHz | | | 8.4 | | | * | | nV/√Hz |
| Integrated Noise, BW = 10Hz to 100MHz | | | 84 | | | * | | µVrms |
| Input Bias Current Noise | | | | | | | | |
| Current Noise Density, f = 0.1MHz to 100MHz | | | 1.2 | | | * | | pA/√Hz |
| Noise Figure (NF) | | | | | | | | |
| | $R_S$ = 10kΩ | | 4 | | | * | | dB |
| | $R_S$ = 50Ω | | 19.5 | | | * | | dB |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | | ±2.8 | | | * | | V |
| Over Specified Temperature | | ±2.2 | | | * | | | V |
| Common-Mode Rejection | $V_{CM}$ = ±0.5V | 65 | 90 | | 70 | * | | dB |
| **INPUT IMPEDANCE** | | | | | | | | |
| Differential | | | 15 ‖ 1 | | | * | | kΩ ‖ pF |
| Common-Mode | | | 16 ‖ 1 | | | * | | MΩ ‖ pF |
| **OPEN-LOOP GAIN** | | | | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±2V, $R_L$ = 100Ω | 45 | 51 | | 46 | * | | dB |
| Over Specified Temperature | $V_O$ = ±2V, $R_L$ = 100Ω | 43 | | | 44 | | | dB |
| **OUTPUT** | | | | | | | | |
| Voltage Output | | | | | | | | |
| Over Specified Temperature | No Load | ±2.2 | ±3.0 | | ±2.4 | * | | V |
| | $R_L$ = 250Ω | ±2.2 | ±2.5 | | ±2.4 | * | | V |
| | $R_L$ = 100Ω | ±2.0 | ±2.3 | | ±2.2 | * | | V |
| Current Output, Sourcing | | 75 | 110 | | * | * | | mA |
| Over Specified Temperature | | 65 | | | * | | | mA |
| Current Output, Sinking | | 65 | 85 | | * | * | | mA |
| Over Specified Temperature | | 35 | | | * | | | mA |
| Short Circuit Current | | | 150 | | | * | | mA |
| Output Resistance | 0.1MHz, G = +1 | | 0.08 | | | * | | Ω |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | | ±5 | | | * | | V |
| Derated Voltage Range | | ±4.5 | | ±5.5 | * | | * | V |
| Quiescent Current | | | ±5.1 | ±7.75 | | ±5.1 | ±6.5 | mA |
| Over Specified Temperature | | | | ±8.75 | | | ±7.5 | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: P, U, N, UB, NB | | –40 | | +85 | * | | * | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| P 8-Pin DIP | | | 100 | | | * | | °C/W |
| U SO-8 | | | 125 | | | * | | °C/W |
| N SOT23-5 | | | 150 | | | * | | °C/W |

NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Frequency response can be strongly influenced by PC board parasitics. The OPA650 is nominally compensated assuming 2pF parasitic load. The demonstration boards show low parasitic layouts for the different package styles.

## ABSOLUTE MAXIMUM RATINGS

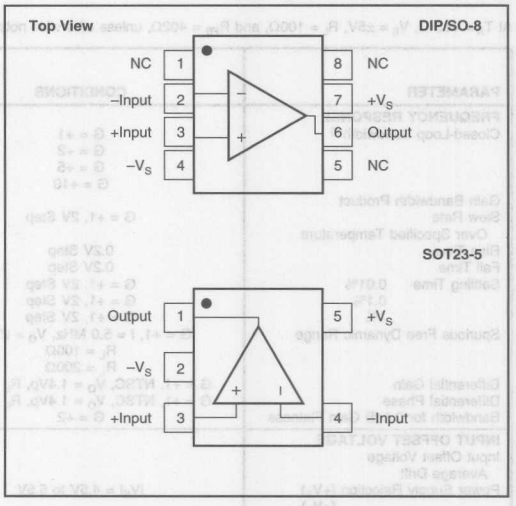
| | |
|---|---|
| Supply | ±5.5V |
| Internal Power Dissipation | See Thermal Conditions |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: P, U, UB, N, NB | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SOIC 3s) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION



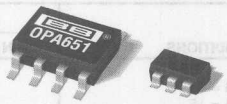

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE | PACKAGE MARKING(2) | ORDERING NUMBER(3) |
|---|---|---|---|---|---|
| OPA650U | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA650U | OPA650U |
| OPA650UB | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA650UB | OPA650UB |
| OPA650N | 5-pin SOT23-5 | 331 | –40°C to +85°C | A50 | OPA650N-250<br>OPA650N-3k |
| OPA650NB | 5-pin SOT23-5 | 331 | –40°C to +85°C | A50B | OPA650NB-250<br>OPA650NB-3k |
| OPA650P | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA650P | OPA650P |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade of the SO-8 package will be marked with a "B" by pin 8. The "B" grade of the SOT23-5 will be marked with a "B" near pins 3 and 4. (3) The SOT23-5 is only available on a 7" tape and reel (e.g. ordering 250 pieces of "OPA650N-250" will get a single 250 piece tape and reel. Ordering 3000 pieces of "OPA650N-3k" will get a single 3000 piece tape and reel). Please refer to Appendix B of Burr-Brown IC Data Book for detailed Tape and Reel Mechanical information.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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# OPA651

www.burr-brown.com/databook/OPA651.html

# Wideband, Low Power Voltage Feedback OPERATIONAL AMPLIFIER

## FEATURES

- STABLE IN GAINS: ≥ 2V/V
- LOW POWER: 50mW
- BANDWIDTH: 470MHz at G = 2
- FAST SETTLING TIME: 16ns to 0.01%
- LOW HARMONICS: –78dB at 5MHz
- LOW INPUT BIAS CURRENT: 4μA
- DIFFERENTIAL GAIN/PHASE ERROR: 0.01%/0.025°
- LOW VOLTAGE NOISE: 4.6nV/√Hz

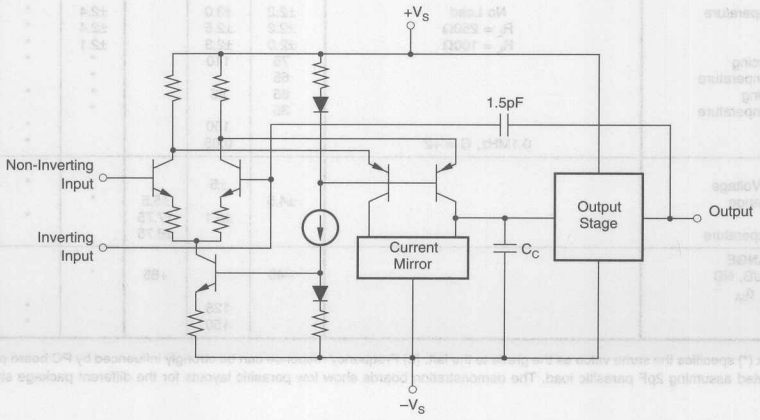
## APPLICATIONS

- HIGH RESOLUTION VIDEO
- MONITOR PREAMPLIFIER
- CCD IMAGING AMPLIFIER
- ULTRASOUND SIGNAL PROCESSING
- ADC/DAC GAIN AMPLIFIER
- BASEBAND SIGNAL PROCESSING

## DESCRIPTION

The OPA651 is a low power, wideband voltage feedback operational amplifier. It features a bandwidth at G = +2 of 470MHz as well as a 12-bit settling time of only 16ns. The wide bandwidth and true differential input stage make it suitable for use in a variety of applications. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA651 is compensated for stability in gains of two or more, differentiating it from the unity gain stable OPA650. Its unusual combination of speed, accuracy and low power make it an outstanding choice for many portable, multi-channel and other high speed applications, where power is at a premium.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = ±5V, $R_L$ = 100Ω, $R_{FB}$ = 402Ω, G = +2, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA651U, N | | | OPA651UB, NB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Closed-Loop Bandwidth[2] | G = +2 | | 470 | | | *[1] | | MHz |
| | G = +5 | | 70 | | | * | | MHz |
| | G = +10 | | 34 | | | * | | MHz |
| Gain Bandwidth Product | | | 340 | | | * | | MHz |
| Slew Rate | G = +2, $V_O$ = 2V step | | 300 | | | * | | V/µs |
| Over Specified Temperature | | | 275 | | | * | | V/µs |
| Rise Time | 0.2V Step | | 0.8 | | | * | | ns |
| Fall Time | 0.2V Step | | 0.8 | | | * | | ns |
| Settling Time 0.01% | G = +2, $V_O$ = 2V step | | 16.2 | | | * | | ns |
| 0.1% | G = +2, $V_O$ = 2V step | | 11.5 | | | * | | ns |
| 1% | G = +2, $V_O$ = 2V step | | 7.2 | | | * | | ns |
| Spurious Free Dynamic Range | G = +2, f = 5.0 MHz, $V_O$ = 2Vp-p, | | | | | | | |
| | $R_L$ = 100Ω | | 67 | | | * | | dBc |
| | $R_L$ = 400Ω | | 78 | | | * | | dBc |
| Differential Gain | G = +2, NTSC, $V_O$ = 1.4Vp, $R_L$ = 150Ω | | 0.01 | | | * | | % |
| Differential Phase | G = +2, NTSC, $V_O$ = 1.4Vp, $R_L$ = 150Ω | | 0.025 | | | * | | Degrees |
| Bandwidth For 0.1dB Flatness | G = +2 | | 43 | | | * | | MHz |
| **INPUT OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | | | ±1 | ±5.0 | | * | ±2.0 | mV |
| Average Drift | | | ±3 | | | * | | µV/°C |
| Power Supply Rejection (+$V_S$) | $V_S$ = ±4.5V to ±5.5V | 65 | 85 | | 70 | * | | dB |
| (–$V_S$) | | 52 | 60 | | 55 | * | | dB |
| **INPUT BIAS CURRENT** | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | 4 | 20 | | * | 10 | µA |
| Over Temperature | | | 6 | 30 | | * | 20 | µA |
| Input Offset Current | $V_{CM}$ = 0V | | 0.4 | 1.5 | | * | * | µA |
| Over Temperature | | | 0.9 | 3.0 | | * | * | µA |
| **INPUT NOISE** | | | | | | | | |
| Input Voltage Noise | | | | | | | | |
| Noise Density, f = 100Hz | | | 13 | | | * | | nV/√Hz |
| f = 10kHz | | | 4.6 | | | * | | nV/√Hz |
| f = 1MHz | | | 4.6 | | | * | | nV/√Hz |
| Voltage Noise, BW = 10Hz to 100MHz | | | 46 | | | * | | µVrms |
| Input Bias Current Noise | | | | | | | | |
| Current Noise Density, f = 0.1Hz to 20kHz | | | 1.1 | | | * | | pA/√Hz |
| Noise Figure (NF) | $R_S$ = 10kΩ | | 3.2 | | | * | | dB |
| | $R_S$ = 50Ω | | 14 | | | * | | dB |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | | ±3.5 | | | * | | V |
| Over Specified Temperature | | ±3.0 | | | * | | | V |
| Common-Mode Rejection | $V_{CM}$ = ±0.5V | 75 | 90 | | 80 | * | | dB |
| **INPUT IMPEDANCE** | | | | | | | | |
| Differential | | | 60 ll 1 | | | * | | kΩ ll pF |
| Common-Mode | | | 2.6 ll 1 | | | * | | MΩ ll pF |
| **OPEN-LOOP GAIN** | | | | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±2V, $R_L$ = 100Ω | 42 | 50 | | 45 | * | | dB |
| Over Specified Temperature | $V_O$ = ±2V, $R_L$ = 100Ω | 40 | | | 42 | | | dB |
| **OUTPUT** | | | | | | | | |
| Voltage Output | | | | | | | | |
| Over Specified Temperature | No Load | ±2.2 | ±3.0 | | ±2.4 | * | | V |
| | $R_L$ = 250Ω | ±2.2 | ±2.5 | | ±2.4 | * | | V |
| | $R_L$ = 100Ω | ±2.0 | ±2.3 | | ±2.1 | * | | V |
| Current Output, Sourcing | | 75 | 110 | | * | * | | mA |
| Over Specified Temperature | | 65 | | | * | | | mA |
| Current Output, Sinking | | 65 | 85 | | * | * | | mA |
| Over Specified Temperature | | 35 | | | * | | | mA |
| Short Circuit Current | | | 150 | | | * | | mA |
| Output Resistance | 0.1MHz, G = +2 | | 0.05 | | | * | | Ω |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | | ±5 | | | * | | V |
| Operating Voltage Range | | ±4.5 | | ±5.5 | * | | * | V |
| Quiescent Current | | | ±5.1 | ±7.75 | | * | ±6.5 | mA |
| Over Specified Temperature | | | | ±8.75 | | | ±7.5 | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: U, N, UB, NB | | –40 | | +85 | * | | * | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| U SO-8 | | | 125 | | | * | | °C/W |
| N SOT23-5 | | | 150 | | | * | | °C/W |

NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Frequency response can be strongly influenced by PC board parasitics. The OPA651 is nominally compensated assuming 2pF parasitic load. The demonstration boards show low parasitic layouts for the different package styles.

## ABSOLUTE MAXIMUM RATINGS

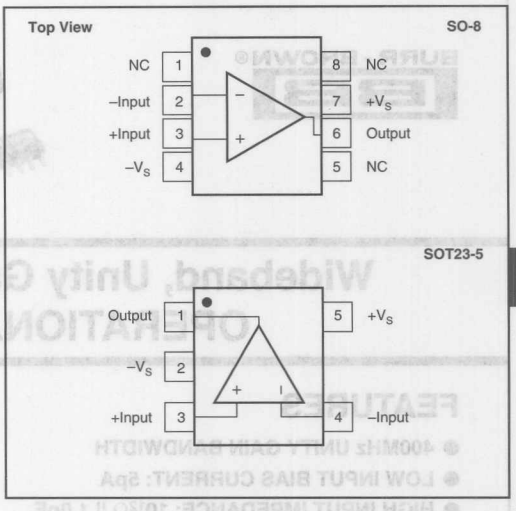
| | |
|---|---|
| Supply | ±5.5V |
| Internal Power Dissipation[1] | See Thermal Conditions |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: U, UB, N, NB | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SO-8 3s) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION



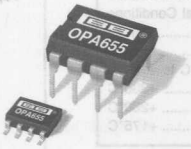

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE | PACKAGE MARKING[2] | ORDERING NUMBER[3] |
|---|---|---|---|---|---|
| OPA651U | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA651U | OPA651U |
| OPA651UB | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA651UB | OPA651UB |
| OPA651N | 5-pin SOT23-5 | 331 | –40°C to +85°C | A51 | OPA651N-250<br>OPA651N-3k |
| OPA651NB | 5-pin SOT23-5 | 331 | –40°C to +85°C | A51B | OPA651NB-250<br>OPA651NB-3k |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade of the SO-8 package will be marked with a "B" by pin 8. The "B" grade of the SOT23-5 will be marked with a "B" near pins 3 and 4. (3) The SOT23-5 is only available on a 7" tape and reel (e.g. ordering 250 pieces of "OPA651N-250" will get a single 250 piece tape and reel. Ordering 3000 pieces of "OPA651N-3k" will get a single 3000 piece tape and reel). Please refer to Appendix B of Burr-Brown IC Data Book for detailed Tape and Reel Mechanical information.

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# OPA655

www.burr-brown.com/databook/OPA655.html

# Wideband, Unity Gain Stable, FET-Input OPERATIONAL AMPLIFIER

## FEATURES

- 400MHz UNITY GAIN BANDWIDTH
- LOW INPUT BIAS CURRENT: 5pA
- HIGH INPUT IMPEDANCE: $10^{12}\Omega$ || 1.0pF
- ULTRA-LOW dG/dP: 0.006%/0.009°
- LOW DISTORTION: 90dB SFDR at 5MHz
- FAST SETTLING: 17ns (0.01%)
- HIGH OUTPUT CURRENT: 60mA
- FAST OVERDRIVE RECOVERY

## APPLICATIONS

- WIDEBAND PHOTODIODE AMPLIFIER
- PEAK DETECTOR
- CCD OUTPUT BUFFER
- ADC INPUT BUFFER
- HIGH SPEED INTEGRATOR
- TEST AND MEASUREMENT FRONT END

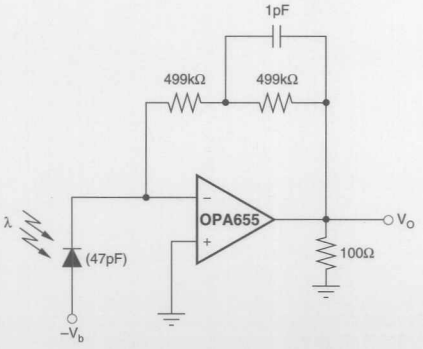
## DESCRIPTION

The OPA655 combines a very wideband, unity gain stable, voltage feedback op amp with a FET input stage to offer an ultra high dynamic range amplifier for ADC buffering and transimpedance applications. Extremely low harmonic distortion along with excellent pulse settling characteristics will support even the most demanding ADC input buffer requirements.

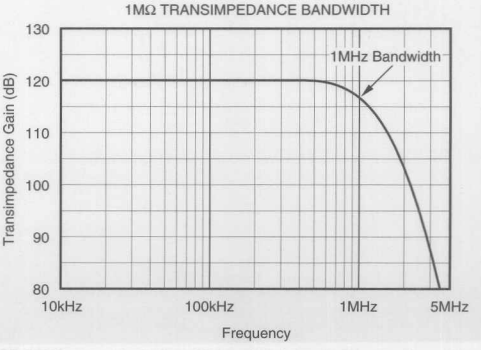
The broad unity gain stable bandwidth and FET input allows exceptional performance in high speed, low noise integrators.

The high input impedance and low bias current provided by the FET input is further supported by the ultra-low $6nV/\sqrt{Hz}$ input voltage noise to achieve a very low integrated noise in wideband photodiode transimpedance applications.

Broad transimpedance bandwidths are achievable given the OPA655's high 240MHz gain bandwidth product. As shown below, a –3dB bandwidth of 1MHz is provided even for a high 1MΩ transimpedance gain from a 47pF source capacitance.




Wideband Photodiode Transimpedance Amplifier




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = ±5V, $R_{FB}$ = 100Ω, and $R_L$ = 100Ω, unless otherwise noted. $R_{FB}$ = 0 for G = +1.

| PARAMETER | CONDITIONS | OPA655P, U MIN | OPA655P, U TYP | OPA655P, U MAX | UNITS |
|---|---|---|---|---|---|
| **FREQUENCY RESPONSE** | | | | | |
| Closed-Loop Response | Gain = +1V/V, $V_O$ = 200mVp-p | | 400 | | MHz |
| | Gain = +2V/V, $V_O$ = 200mVp-p | | 185 | | MHz |
| | Gain = +5V/V, $V_O$ = 200mVp-p | | 57 | | MHz |
| | Gain = +10V/V, $V_O$ = 200mVp-p | | 24 | | MHz |
| Gain-Bandwidth Product | | | 240 | | MHz |
| Slew Rate | G = +1, 1V Step | 210 | 290 | | V/µs |
| Over Temperature | | 200 | | | V/µs |
| Rise Time | 0.2V Step | | 1 | | ns |
| Fall Time | 0.2V Step | | 1 | | ns |
| Settling Time: 0.01% | G = +1, 1V Step | | 17 | | ns |
| 0.1% | G = +1, 1V Step | | 8 | | ns |
| 1% | G = +1, 1V Step | | 6 | | ns |
| Spurious-Free Dynamic Range | G = +1, f = 5MHz, $V_O$ = ±1V, $R_L$ = 100Ω | 75 | 90 | | dBc |
| Differential Gain | 3.58MHz, 0 to 1.4V, $R_L$ = 150Ω | | 0.006 | | % |
| Differential Phase | 3.58MHz, 0 to 1.4V, $R_L$ = 150Ω | | 0.009 | | degrees |
| Bandwidth for 0.1dB flatness | G = +2, 2Vp-p | | 30 | | MHz |
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | | | ±1 | ±2 | mV |
| Over Temperature | | | ±10 | | µV/°C |
| Power Supply Rejection (+$V_S$) | $\|V_S\|$ = 4.50V to 5.50V | 55 | 70 | | dB |
| (–$V_S$) | | 50 | 65 | | dB |
| **INPUT BIAS CURRENT**[1] | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | –5 | –125 | pA |
| Over Temperature | $V_{CM}$ = 0V | | | –8.0 | nA |
| Input Offset Current | $V_{CM}$ = 0V | | ±2 | ±125 | pA |
| Over Temperature | $V_{CM}$ = 0V | | | ±8 | nA |
| **NOISE** | | | | | |
| Input Voltage Noise | | | | | |
| Noise Density: f = 100Hz | | | 20 | | nV/√Hz |
| f = 1kHz | | | 8 | | nV/√Hz |
| f = 10kHz | | | 6 | | nV/√Hz |
| f = 0.1MHz to 100MHz | | | 6 | | nV/√Hz |
| Integrated Voltage Noise, BW = 1MHz to 100MHz | | | 60 | | µVrms |
| Input Bias Current Noise | | | | | |
| Current Noise Density, f = 10Hz to 10kHz | | | 1.3 | 4 | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range | | | ±2.75 | | V |
| Over Temperature | | ±2.5 | | | V |
| Common-Mode Rejection | $V_{CM}$ = ±0.5V | 55 | 70 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $10^{12}$ ‖ 1.2 | | Ω ‖ pF |
| Common-Mode | | | $10^{12}$ ‖ 1.0 | | Ω ‖ pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±2V, $R_L$ = 100Ω | 53 | 58 | | dB |
| Over Temperature | $V_O$ = ±2V, $R_L$ = 100Ω | 50 | | | dB |
| **OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 100Ω, G = +1 | ±3.0 | ±3.4 | | V |
| Over Temperature | | ±2.8 | | | V |
| Current Output | | ±35 | ±60 | | mA |
| Over Temperature | | ±28 | | | mA |
| Short-Circuit Output Current | | | ±140 | | mA |
| Output Resistance | 0.1MHz, G = +1 | | 0.04 | | Ω |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±5 | | V |
| Operating Voltage Range | $T_{MIN}$ to $T_{MAX}$ | ±4.75 | | ±5.25 | V |
| Quiescent Current | $T_{MIN}$ to $T_{MAX}$ | ±21 | ±25 | ±29 | mA |
| Over Temperature | | | | ±31 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification: P, U | | –40 | | +85 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| P | | | 100 | | °C/W |
| U | | | 125 | | °C/W |

NOTE: (1) Junction temperature = +25°C for room temperature tested input bias and offset current.

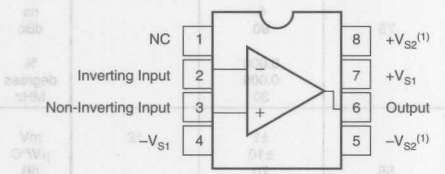
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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Total Supply Voltage Across Device ($V_{S\ (TOTAL)}$) | 11V |
| Internal Power Dissipation | See Thermal Considerations |
| Differential Input Voltage | $V_{S\ (TOTAL)}$ |
| Common-Mode Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: P, U | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SO-8, 3s) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

## PIN CONFIGURATION

**Top View** **DIP/SO-8**




NOTE: (1) Making use of all four power supply pins is highly recommended, although not required. Using these four pins, instead of pins 4 and 7 only, will reduce the effective pin impedance and substantially improve distortion.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| OPA655P | 8-Pin Plastic DIP | 006 |
| OPA655U | SO-8 | 182 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

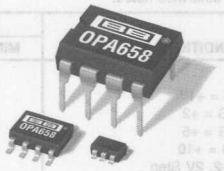
| PRODUCT | PACKAGE | TEMPERATURE RANGE |
|---|---|---|
| OPA655P | 8-Pin Plastic DIP | –40°C to +85°C |
| OPA655U | SO-8 | –40°C to +85°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

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# OPA658

www.burr-brown.com/databook/OPA658.html

# Wideband, Low Power Current Feedback OPERATIONAL AMPLIFIER

## FEATURES

- UNITY GAIN STABLE BANDWIDTH: 900MHz
- LOW POWER: 50mW
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.025%/0.02°
- HIGH SLEW RATE: 1700V/µs
- GAIN FLATNESS: 0.1dB to 135MHz
- HIGH OUTPUT CURRENT (80mA)

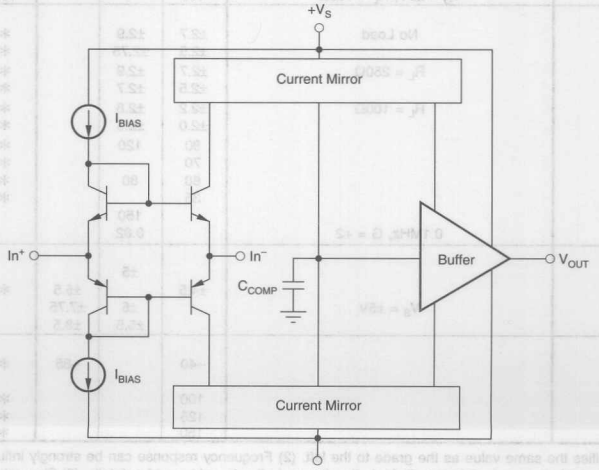
## APPLICATIONS

- MEDICAL IMAGING
- HIGH-RESOLUTION VIDEO
- HIGH-SPEED SIGNAL PROCESSING
- COMMUNICATIONS
- PULSE AMPLIFIERS
- ADC/DAC GAIN AMPLIFIER
- MONITOR PREAMPLIFIER
- CCD IMAGING AMPLIFIER

## DESCRIPTION

The OPA658 is an ultra-wideband, low power current feedback video operational amplifier featuring high slew rate and low differential gain/phase error. The current feedback design allows for superior large signal bandwidth, even at high gains. The low differential gain/phase errors, wide bandwidth and low quiescent current make the OPA658 a perfect choice for numerous video, imaging and communications applications.

The OPA658 is optimized for low gain operation and is also available in dual (OPA2658) and quad (OPA4658) configurations.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = ±5V, $R_L$ = 100Ω, and $R_{FB}$ = 402Ω, unless otherwise noted.

| PARAMETER | CONDITION | OPA658P, U, N | | | OPA658UB, NB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Closed-Loop Bandwidth[2] | G = +1[4] | | 900 | | | *[1] | | MHz |
| | G = +2 | | 680 | | 400 | * | | MHz |
| | G = +5 | | 370 | | | * | | MHz |
| | G = +10 | | 200 | | | * | | MHz |
| Slew Rate[3] | G = +2, 2V Step | | 1700 | | 1000 | * | | V/µs |
| At Minimum Specified Temperature | | | 1500 | | 900 | * | | V/µs |
| Settling Time: 0.01% | G = +2, 2V Step | | 15 | | | * | | ns |
| 0.1% | G = +2, 2V Step | | 11.5 | | | * | | ns |
| 1% | G = +2, 2V Step | | 6 | | | * | | ns |
| Spurious Free Dynamic Range | f = 5MHz, G = +2, $V_O$ = 2Vp-p | | 68 | | | * | | dBc |
| | f = 20MHz, G= +2, $V_O$ = 2Vp-p | | 56 | | | * | | dBc |
| Third Order Intercept Point | f = 10MHz, 4dBm Each Tone | | 40 | | | * | | dBm |
| Differential Gain | G = +2, NTSC, $V_O$ = 1.4Vp-p, $R_L$ = 150Ω | | 0.025 | | | * | | % |
| Differential Phase | G = +2, NTSC, $V_O$ = 1.4Vp-p, $R_L$ = 150Ω | | 0.02 | | | * | | degrees |
| Bandwidth for 0.1dB Flatness | G = +2 | | 135[5] | | | * | | MHz |
| **OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0V | | ±3 | ±5.5 | | ±2 | ±4.5 | mV |
| Over Temperature Range | | | ±5 | ±8 | | ±4 | ±7 | mV |
| Power Supply Rejection Ratio | $V_S$ = ±4.7 to ±5.5V | 55 | 64 | | 58 | 67 | | dB |
| **INPUT BIAS CURRENT** | | | | | | | | |
| Non-Inverting | $V_{CM}$ = 0V | | ±5.7 | ±30 | | * | ±18 | µA |
| Over Temperature Range | | | ±10 | ±80 | | * | ±35 | µA |
| Inverting | $V_{CM}$ = 0V | | ±1.1 | ±35 | | * | * | µA |
| Over Temperature Range | | | ±30 | ±75 | | * | * | µA |
| **NOISE** | | | | | | | | |
| Input Voltage Noise Density | | | | | | | | |
| f = 100Hz | | | 16 | | | * | | nV/√Hz |
| f = 2kHz | | | 4.9 | | | * | | nV/√Hz |
| f = 10kHz | | | 3.2 | | | * | | nV/√Hz |
| f = 1MHz | | | 3.2 | | | * | | nV/√Hz |
| $f_B$ = 100Hz to 200MHz | | | 45.3 | | | * | | µVrms |
| Input Bias Current Noise Density | | | | | | | | |
| Inverting: f = 1MHz | | | 32 | | | * | | pA/√Hz |
| Non-Inverting: f = 1MHz | | | 11.9 | | | * | | pA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | | | | | | | |
| Over Temperature Range | | ±2.5 | ±2.9 | | * | * | | V |
| Common-Mode Rejection | $V_{CM}$ = ±1V | 45 | 50 | | * | * | | dB |
| **INPUT IMPEDANCE** | | | | | | | | |
| Non-Inverting | | | 500 ll 1 | | | * | | kΩ ll pF |
| Inverting | | | 50 | | | * | | Ω |
| **OPEN-LOOP TRANSRESISTANCE** | | | | | | | | |
| Open-Loop Transresistance | $V_O$ = ±2V, $R_L$ = 100Ω | 150 | 190 | | 200 | 250 | | kΩ |
| Over Temperature Range | $V_O$ = ±2V, $R_L$ = 100Ω | 100 | | | 150 | | | kΩ |
| **OUTPUT** | | | | | | | | |
| Voltage Output | No Load | ±2.7 | ±2.9 | | * | * | | V |
| Over Temperature Range | | ±2.5 | ±2.75 | | * | * | | V |
| Voltage Output | $R_L$ = 250Ω | ±2.7 | ±2.9 | | * | * | | V |
| Over Temperature Range | | ±2.5 | ±2.7 | | * | * | | V |
| Voltage Output | $R_L$ = 100Ω | ±2.2 | ±2.8 | | * | * | | V |
| Over Temperature Range | | ±2.0 | ±2.5 | | * | * | | V |
| Output Current, Sourcing | | 80 | 120 | | * | * | | mA |
| Over Temperature | | 70 | | | * | | | mA |
| Output Current, Sinking | | 60 | 80 | | * | * | | mA |
| Over Temperature | | 35 | | | * | | | mA |
| Short Circuit Current | | | 150 | | | * | | mA |
| Output Resistance | 0.1MHz, G = +2 | | 0.02 | | | * | | Ω |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | | ±5 | | | * | | V |
| Operating Voltage Range | | ±4.5 | | ±5.5 | * | | * | V |
| Quiescent Current | $V_S$ = ±5V | | ±5 | ±7.75 | | ±4.5 | ±5.75 | mA |
| Over Temperature Range | | | ±5.5 | ±8.5 | | ±4.7 | ±6.5 | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: P, U, N, UB, NB | | –40 | | +85 | * | | * | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| P 8-Pin DIP | | 100 | | | * | | °C/W | |
| U SO-8 | | 125 | | | * | | °C/W | |
| N SOT23-5 | | 150 | | | * | | °C/W | |

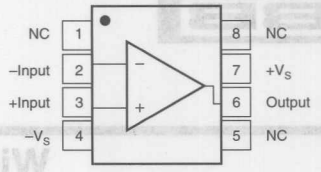
NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Frequency response can be strongly influenced by PC board parasitics. The demonstration boards show low parasitic layouts for this part. Refer to the demonstration board layout for details. (3) Slew rate is rate of change from 10% to 90% of output voltage step. (4) At G = +1, $R_{FB}$ = 560Ω for PDIP and 402Ω for SO-8. (5) This specification is PC board layout dependent.

## ABSOLUTE MAXIMUM RATINGS

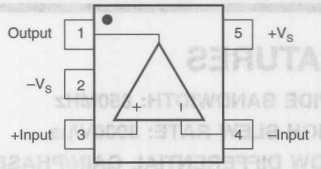
| | |
|---|---|
| Supply | ±5.5V |
| Internal Power Dissipation | See Thermal Considerations |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: P, U, UB, N, NB | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SOIC 3s) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

## PIN CONFIGURATION

Top View DIP/SO-8




SOT23-5




## ELECTROSTATIC DISCHARGE SENSITIVITY

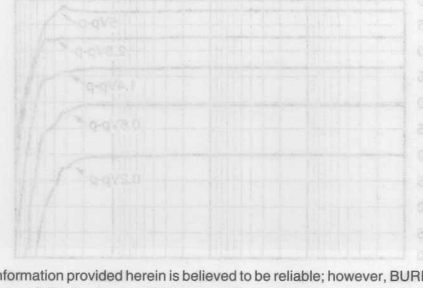
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## PACKAGE/ORDERING INFORMATION

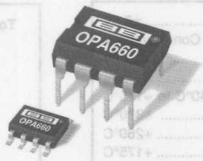
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE | PACKAGE MARKING(2) | ORDERING NUMBER(3) |
|---|---|---|---|---|---|
| OPA658U | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA658U | OPA658U |
| OPA658UB | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA658UB | OPA658UB |
| OPA658N | 5-pin SOT23-5 | 331 | –40°C to +85°C | A58 | OPA658N-250<br>OPA658N-3k |
| OPA658NB | 5-pin SOT23-5 | 331 | –40°C to +85°C | A58B | OPA658NB-250<br>OPA658NB-3k |
| OPA658P | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA658P | OPA658P |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade of the SO-8 will be marked with a "B" by pin 8. The "B" grade of the SOT23-5 will be marked with a "B" near pins 3 and 4. (3) The SOT23-5 is only available on a 7" tape and reel (e.g. ordering 250 pieces of "OPA658N-250" will get a single 250 piece tape and reel. Ordering 3000 pieces of "OPA658N-3k" will get a single 3000 piece tape and reel). Please refer to Appendix B of Burr-Brown IC Data Book for detailed Tape and Reel Mechanical information.



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# OPA660

www.burr-brown.com/databook/OPA660.html

# Wide Bandwidth OPERATIONAL TRANSCONDUCTANCE AMPLIFIER AND BUFFER

## FEATURES

- WIDE BANDWIDTH: 850MHz
- HIGH SLEW RATE: 3000V/µs
- LOW DIFFERENTIAL GAIN/PHASE ERROR: 0.06%/0.02°
- VERSATILE CIRCUIT FUNCTION
- EXTERNAL $I_Q$-CONTROL

## APPLICATIONS

- BASE LINE RESTORE CIRCUITS
- VIDEO/BROADCAST EQUIPMENT
- COMMUNICATIONS EQUIPMENT
- HIGH-SPEED DATA ACQUISITION
- WIDEBAND LED DRIVER
- AGC-MULTIPLIER
- NS-PULSE INTEGRATOR
- CONTROL LOOP AMPLIFIER
- 400MHz DIFFERENTIAL INPUT AMPLIFIER

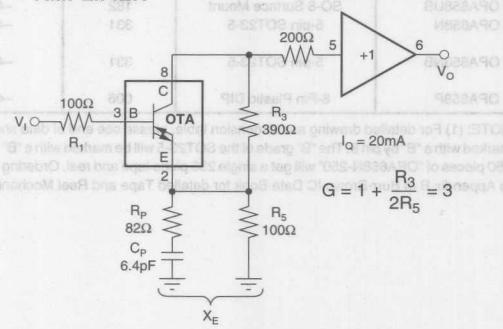
## DESCRIPTION

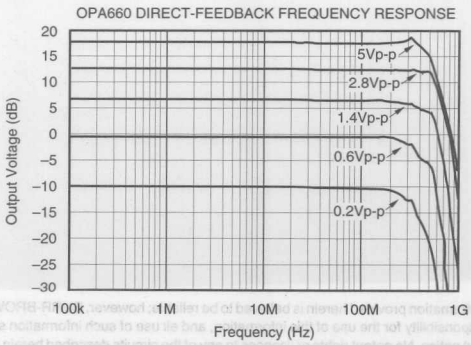
The OPA660 is a versatile monolithic component designed for wide-bandwidth systems including high performance video, RF and IF circuitry. It includes a wideband, bipolar integrated voltage-controlled current source and voltage buffer amplifier.

The voltage-controlled current source or Operational Transconductance Amplifier (OTA) can be viewed as an "ideal transistor." Like a transistor, it has three terminals—a high-impedance input (base), a low-impedance input/output (emitter), and the current output (collector). The OTA, however, is self-biased and bipolar. The output current is zero-for-zero differential input voltage. AC inputs centered about zero produce an output current which is bipolar and centered about zero. The transconductance of the OTA can be adjusted with an external resistor, allowing bandwidth, quiescent current and gain trade-offs to be optimized.

The open-loop buffer amplifier provides 850MHz bandwidth and 3000V/µs slew rate. Used as a basic building block, the OPA660 simplifies the design of AGC amplifiers, LED driver circuits for Fiber Optic Transmission, integrators for fast pulses, fast control loop amplifiers, and control amplifiers for capacitive sensors and active filters.

The OPA660 is packaged in SO-8 surface-mount, and 8-pin plastic DIP, specified from –40°C to +85°C.



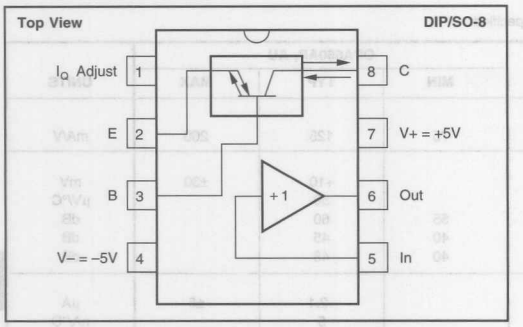

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# SPECIFICATIONS

Typical at $I_O$ = 20mA, $V_S$ = ±5V, $T_A$ = +25°C, and $R_L$ = 500Ω, unless otherwise specified.

| PARAMETER | CONDITIONS | OPA660AP, AU | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **OTA TRANSCONDUCTANCE** | | | | | |
| Transconductance | $V_C$ = 0V | 75 | 125 | 200 | mA/V |
| **OTA INPUT OFFSET VOLTAGE** | $V_B$ = 0 | | | | |
| Initial | | | +10 | ±30 | mV |
| vs Temperature | | | 50 | | µV/°C |
| vs Supply (tracking) | $V_S$ = ±4.5V to ±5.5V | 55 | 60 | | dB |
| vs Supply (non-tracking) | V+ = 4.5V to 5.5V | 40 | 45 | | dB |
| vs Supply (non-tracking) | V– = –4.5V to –5.5V | 40 | 48 | | dB |
| **OTA B-INPUT BIAS CURRENT** | | | | | |
| Initial | | | –2.1 | ±5 | µA |
| vs Temperature | | | 5 | | nA/°C |
| vs Supply (tracking) | $V_S$ = ±4.5V to ±5.5V | | | ±750 | nA/V |
| vs Supply (non-tracking) | V+ = 4.5V to 5.5V | | | ±1500 | nA/V |
| vs Supply (non-tracking) | V– = –4.5V to –5.5V | | | ±500 | nA/V |
| **OTA OUTPUT BIAS CURRENT** | | | | | |
| Output Bias Current | $V_B$ = 0, $V_C$ = 0V | | ±10 | ±20 | µA |
| vs Temperature | | | 500 | | nA/°C |
| vs Supply (tracking) | $V_S$ = ±4.5V to ±5.5V | | ±10 | ±25 | µA/V |
| vs Supply (non-tracking) | V+ = 4.5V to 5.5V | | ±10 | ±25 | µA/V |
| vs Supply (non-tracking) | V– = –4.5V to –5.5V | | ±10 | ±25 | µA/V |
| **OTA OUTPUT** | | | | | |
| Output Current | | ±10 | ±15 | | mA |
| Output Voltage Compliance | $I_C$ = ±1mA | ±4.0 | ±4.7 | | V |
| Output Impedance | | | 25k ‖ 4.2 | | Ω ‖ pF |
| Open-Loop Gain | f = 1kHz | | 70 | | dB |
| **BUFFER OFFSET VOLTAGE** | | | | | |
| Initial | | | +7 | ±30 | mV |
| vs Temperature | | | 50 | | µV/°C |
| vs Supply (tracking) | $V_S$ = ±4.5V to ±5.5V | 55 | 60 | | dB |
| vs Supply (non-tracking) | V+ = 4.5V to 5.5V | 40 | 45 | | dB |
| vs Supply (non-tracking) | V– = –4.5V to –5.5V | 40 | 48 | | dB |
| **BUFFER INPUT BIAS CURRENT** | | | | | |
| Initial | | | –2.1 | ±5 | µA |
| vs Temperature | | | 5 | | nA/°C |
| vs Supply (tracking) | $V_S$ = ±4.5V to ±5.5V | | | ±750 | nA/V |
| vs Supply (non-tracking) | V+ = 4.5V to 5.5V | | | ±1500 | nA/V |
| vs Supply (non-tracking) | V– = –4.5V to –5.5V | | | ±500 | nA/V |
| **BUFFER and OTA INPUT IMPEDANCE** | | | | | |
| Input Impedance | | | 1.0 ‖ 2.1 | | MΩ ‖ pF |
| **BUFFER INPUT NOISE** | | | | | |
| Voltage Noise Density, f = 100kHz | | | 4 | | nV/√Hz |
| **BUFFER DYNAMIC RESPONSE** | | | | | |
| Small Signal Bandwidth | $V_O$ = ±100mV | | 850 | | MHz |
| Full Power Bandwidth | $V_O$ = ±1.4V | | 800 | | MHz |
| | $V_O$ = ±2.5V | | 570 | | MHz |
| Differential Gain Error | 3.58MHz, at 0.7V | | 0.06 | | % |
| Differential Phase Error | 3.58MHz, at 0.7V | | 0.02 | | Degrees |
| Harmonic Distortion, 2nd Harmonic | f = 10MHz, $V_O$ = 0.5Vp-p | | –68 | | dBc |
| Slew Rate | 5V Step | | 3000 | | V/µs |
| Settling Time 0.1% | 2V Step | | 25 | | ns |
| Rise Time (10% to 90%) | $V_O$ = 100mVp-p | | 1 | | ns |
| | 5V Step | | 1.5 | | ns |
| Group Delay Time | | | 250 | | ps |
| **BUFFER RATED OUTPUT** | | | | | |
| Voltage Output | $I_O$ = ±1mA | ±3.7 | ±4.2 | | V |
| Current Output | | ±10 | ±15 | | mA |
| Gain | $R_L$ = 500Ω | 0.96 | 0.975 | | V/V |
| | $R_L$ = 5kΩ | | 0.99 | | V/V |
| Output Impedance | | | 7 ‖ 2 | | Ω ‖ pF |
| **POWER SUPPLY** | | | | | |
| Voltage, Rated | | | ±5 | | V |
| Derated Performance | | ±4.5 | | ±5.5 | V |
| Quiescent Current (Programmable, Useful Range) | | | ±3 to ±26 | | mA |

## PIN CONFIGURATION




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | ±6V |
| Input Voltage[1] | $\pm V_S$ ±0.7V |
| Operating Temperature | –40°C to +85°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +175°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Inputs are internally diode-clamped to $\pm V_S$.

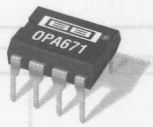
## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| OPA660AP | 8-Pin Plastic DIP | 006 | –25°C to +85°C |
| OPA660AU | SO-8 Surface-Mount | 182 | –25°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

BURR-BROWN®




# OPA671

www.burr-brown.com/databook/OPA671.html

# Wide Bandwidth, Fast Settling *Difet*® OPERATIONAL AMPLIFIER

## FEATURES

- HIGH GAIN-BANDWIDTH: 35MHz
- LOW INPUT NOISE: 10nV/√Hz
- HIGH SLEW RATE: 100V/µs
- FAST SETTLING: 240ns to 0.01%
- FET INPUT: $I_B$ = 50pA max
- HIGH OUTPUT CURRENT: 50mA
- WIDE SUPPLY RANGE: $V_S$ = ±4.5 to ±18V

## APPLICATIONS

- HIGH-SPEED DATA ACQUISITION
- OPTOELECTRONICS
- TRANSIMPEDANCE AMPLIFIER
- LINE DRIVER
- CCD BUFFER AMPLIFIER

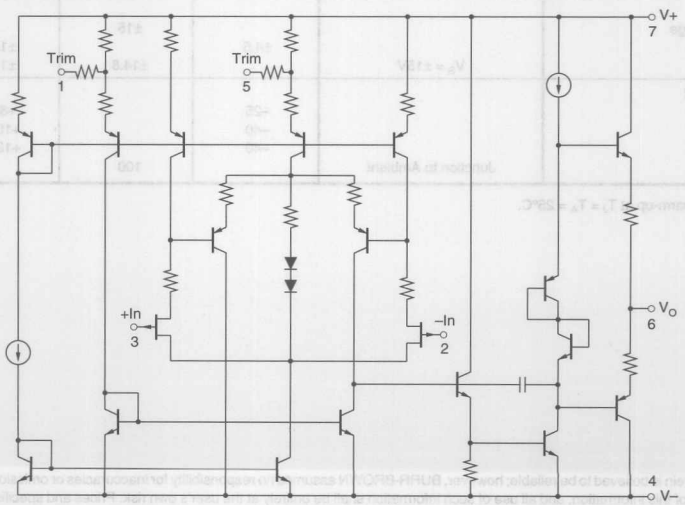
## DESCRIPTION

The OPA671 is a FET-input monolithic operational amplifier featuring wide bandwidth and fast settling time. Fabricated using Burr-Brown's ***Difet***, complementary bipolar process, it provides an excellent combination of high speed, accuracy, and high output current.

The OPA671 is versatile, operating from ±4.5V to ±18V power supplies. It can deliver ±10V signals into a 200Ω load at slew rates of 100V/µs. OPA671's ***Difet*** input provides input bias current thousands of times lower than bipolar-input wideband op amps.

The OPA671 is internally compensated to be unity-gain stable, allowing use in the widest range of applications.

The OPA671 is available in an 8-pin plastic DIP, rated for the industrial temperature range.




*Difet*® Burr-Brown Corporation

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# SPECIFICATIONS

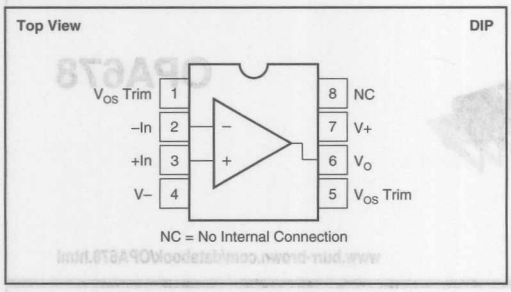
At $T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

| PARAMETER | CONDITION | OPA671AP MIN | OPA671AP TYP | OPA671AP MAX | UNITS |
|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | | | ±0.5 | ±5 | mV |
| Average Drift | | | ±10 | | µV/°C |
| Power Supply Rejection | $V_S$ = ±4.5 to ±16.5V | 72 | 94 | | dB |
| **INPUT BIAS CURRENT**(1) | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | 5 | 50 | pA |
| Input Offset Current | $V_{CM}$ = 0V | | 2 | | pA |
| **NOISE** | | | | | |
| Input Voltage Noise | | | | | |
| Noise Density, f = 100Hz | | | 24 | | nV/√Hz |
| f = 1kHz | | | 15 | | nV/√Hz |
| f = 10kHz | | | 12 | | nV/√Hz |
| f = 100kHz | | | 10 | | nV/√Hz |
| Voltage Noise, BW = 10Hz to 1MHz | | | 60 | | µVp-p |
| Input Bias Current Noise | | | | | |
| Current Noise Density, f = 10Hz to 1MHz | | | 2 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range | | ±12 | ±13 | | V |
| Common-Mode Rejection | $V_{CM}$ = ±10V | 74 | 92 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $10^{12}$ ‖ 4.5 | | Ω ‖ pF |
| Common-Mode | | | $10^{12}$ ‖ 6 | | Ω ‖ pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±10V, $R_L$ = 1kΩ | | 80 | | dB |
| | $V_O$ = ±10V, $R_L$ = 200Ω | 74 | 78 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product | | | 35 | | MHz |
| Slew Rate | G = –1, 10V Step | | 107 | | V/µs |
| Settling Time 0.01% | G = –1, 10V Step | | 240 | | ns |
| 0.1% | G = –1, 10V Step | | 150 | | ns |
| 1% | G = –1, 10V Step | | 85 | | ns |
| Total Harmonic Distortion | G = 1, f = 100kHz<br>$V_O$ = 3V, $R_L$ = 200Ω | | 0.0006 | | % |
| **OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 200Ω | ±10.5 | ±11.5 | | V |
| Current Output | $V_O$ = ±10V | | 50 | | mA |
| Short Circuit Current | | | –90/+105 | | mA |
| Output Resistance, Open-Loop | DC | | 20 | | Ω |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±15 | | V |
| Operating Voltage Range | | ±4.5 | | ±18 | V |
| Quiescent Current | $V_S$ = ±15V | | ±14.8 | ±17 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –25 | | +85 | °C |
| Operating | | –40 | | +100 | °C |
| Storage | | –40 | | +125 | °C |
| Thermal Resistance, $\theta_{JA}$ | Junction to Ambient | | 100 | | °C/W |

NOTE: (1) Tested without warm-up at $T_J = T_A$ = 25°C.

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## PIN CONFIGURATION




## ELECTROSTATIC DISCHARGE SENSITIVITY

An integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## ABSOLUTE MAXIMUM RATINGS

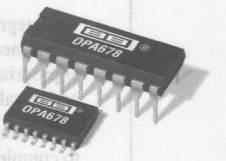
| | |
|---|---|
| Power Supply Voltage | ±18V |
| Input Voltage | (V+) +1V to (V–) –1V |
| Operating Temperature | –40°C to +100°C |
| Storage Temperature | –40°C to +125°C |
| Output Short-Circuit to Ground | 15s |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

## PACKAGE/ORDERING INFORMATION

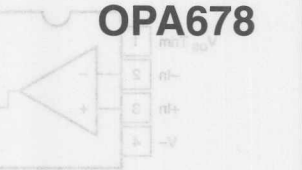
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| OPA671AP | 8-Pin Plastic DIP | 006 | –25°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR - BROWN®



# OPA678



www.burr-brown.com/databook/OPA678.html

# Wideband Switched-Input OPERATIONAL AMPLIFIER

## FEATURES

- FAST SETTLING: 11ns (1%)
- WIDE BANDWIDTH: 200MHz
- TWO LOGIC SELECTABLE INPUTS
- LOW OFFSET VOLTAGE: ±380µV
- FAST INPUT SWITCHING: 4ns
- ACCEPTS TTL/ECL SWITCHING SIGNALS
- UNITY GAIN STABLE
- 16-PIN DIP AND SO-16 PACKAGES

## APPLICATIONS

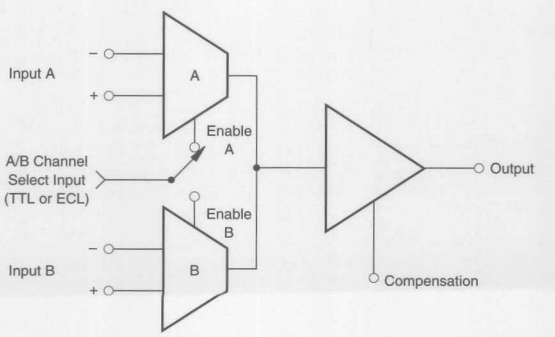
- VIDEO AMPLIFICATION AND SWITCHING
- FAST 2-INPUT MULTIPLEXER
- PULSE/RF AMPLIFIERS
- PROGRAMMABLE-GAIN AMPLIFIER
- ACTIVE FILTERS
- SYNCHRONOUS DEMODULATOR
- LOW COST REPLACEMENT FOR OPA675/676

## DESCRIPTION

The OPA678 is a wideband monolithic operational amplifier with two independent differential inputs. Either input can be selected by an external TTL or ECL logic signal. The amplifier is externally compensated and features a very fast input selection speed, 4ns for either ECL or TTL. This amplifier features fully symmetrical differential inputs due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA678 may be used in all op amp applications requiring high speed and precision.

Low distortion and crosstalk make this amplifier suitable for RF and video applications.

The OPA678 is available in plastic DIP and SO-16 packages.




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PDS-1136E

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# SPECIFICATIONS

## ELECTRICAL

At $V_{CC}$ = ±5VDC, $R_L$ = 150Ω, $C_{COMP}$ = 5pF, and $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA678AP, AU MIN | OPA678AP, AU TYP | OPA678AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT NOISE**[1] | | | | | |
| Voltage: $f_O$ = 100Hz | $R_S$ = 0Ω | | 55 | | nV/√Hz |
| $f_O$ = 1kHz | | | 21 | | nV/√Hz |
| $f_O$ = 10kHz | | | 7.8 | | nV/√Hz |
| $f_O$ = 100kHz | | | 4.9 | | nV/√Hz |
| $f_B$ = 10Hz to 10MHz | | | 18 | | µVrms |
| Current: $f_O$ = 10Hz to 1MHz | | | 2.1 | | pA/√Hz |
| **OFFSET VOLTAGE**[1] | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0VDC | | ±380 | ±1.5mV | µV |
| Offset Voltage Drift | $T_A = T_{MIN}$ to $T_{MAX}$ | | ±3 | ±15 | µV/°C |
| Supply Rejection | $±V_{CC}$ = 4.5V to 5.5V | 65 | 71 | | dB |
| **BIAS CURRENT**[1] | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC | | 14 | 50 | µA |
| **OFFSET CURRENT**[1] | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC | | 0.2 | 2 | µA |
| **INPUT IMPEDANCE**[1] | | | | | |
| Differential | | | 25k \|\| 2 | | Ω \|\| pF |
| Common-Mode | | | $10^6$ \|\| 5 | | Ω \|\| pF |
| **INPUT VOLTAGE RANGE**[1] | | | | | |
| Common-Mode Input Range | | 2.0 | ±2.5 | | V |
| Common-Mode Rejection | $V_{IN}$ = ±0.5VDC, $V_O$ = ±1.25V | 75 | 85 | | dB |
| **OPEN-LOOP GAIN, DC**[1] | | | | | |
| Open-Loop Voltage Gain | | 50 | 60 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Closed-Loop Bandwidth | Gain = +1V/V, $C_C$ = 9pF | 140 | 200 | | MHz |
| | Gain = +2V/V, $C_C$ = 7pF | | 100 | | MHz |
| | Gain = +5V/V, $C_C$ = 1pF | | 70 | | MHz |
| Crosstalk | Gain = +1V/V, f = 100kHz | | –102 | | dBC[2] |
| | f = 1MHz | | –83 | | dBC |
| | f = 10MHz | | –64 | | dBC |
| | f = 100MHz | | –44 | | dBC |
| Harmonic Distortion: 5MHz | G = +1V/V, $R_L$= 150Ω, $V_O$ = 0.25Vp-p | | | | |
| | Second Harmonic | | –71 | | dBC[3] |
| | Third Harmonic | | –82 | | dBC |
| Large Signal Response[4] | $V_O$ = 2.5Vp-p, Gain = +1V/V | 32 | 45 | | MHz |
| Slew Rate | Gain = +1V/V | 250 | 350 | | V/µs |
| Settling Time: 1% | Gain = –1V/V, $1V_{OUT}$ Step | | 11 | | ns |
| 0.1% | | | 22 | | ns |
| 0.01% | | | 30 | | ns |
| Differential Gain (0V to 0.7V) | 4.5MHz, Gain = +2V/V, $C_C$ = 2.2pF | | 0.02 | | % |
| Differential Phase (0V to 0.7V) | 4.5MHz, Gain = +2V/V, $C_C$ = 2.2pF | | 0.02 | | Degrees |
| **INPUT SELECTION**[5] | | | | | |
| Transition Time | ECL: Operation | | 4 | 8 | ns |
| 50% In to 50% Out | TTL: Operation | | 4 | 8 | ns |
| **DIGITAL INPUT** | | | | | |
| TTL Logic Levels: $V_{IL}$ | Logic "LO" | 0 | | +0.8 | V |
| $V_{IH}$ | Logic "HI" | +2.0 | | +5 | V |
| $I_{IL}$ | Logic "LO", $V_{IL}$ = 0V | | –0.05 | –0.2 | mA |
| $I_{IH}$ | Logic "HI", $V_{IH}$ = +2.7V | | 1 | 20 | µA |
| ECL Logic Levels: $V_{IL}$ | Logic "LO" | –1.81 | | –1.475 | V |
| $V_{IH}$ | Logic "HI" | –1.15 | | – 0.88 | V |
| $I_{IL}$ | Logic "LO", $V_{IL}$ = –1.6V | | –50 | –100 | µA |
| $I_{IH}$ | Logic "HI", $V_{IH}$ = –1.0V | | –50 | –100 | µA |
| **RATED OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 150Ω | ±2.5 | ±3.75 | | V |
| | $R_L$ = 50Ω | ±1.7 | ±2.2 | | V |
| Current Output | | ±30 | ±44 | | mA |
| Output Resistance | 1MHz, Open-Loop, $C_C$ = 5pF | | 5 | | Ω |
| Load Capacitance Stability | $R_F$ = 100Ω, Gain = +1V/V, $C_C$ = 10pF | | 17 | | pF |
| Short Circuit Current | Continuous to Gnd | | +45 | | mA |

# SPECIFICATIONS (CONT)

## ELECTRICAL

At $V_{CC}$ = ±5VDC, $R_L$ = 150Ω, $C_{COMP}$ = 5pF, and $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA678AP, AU MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | |
| Rated Voltage | ±$V_{CC}$ | | 5 | | VDC |
| Derated Performance | ±$V_{CC}$ | 4.5 | | 5.5 | VDC |
| Current, Quiescent | $I_O$ = 0mADC | | 26 | 30 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | Ambient Temp AP, AU | –40 | | +85 | °C |
| Thermal Impedance | Junction-to-Ambient | | | | |
| AP | | | 90 | | °C/W |
| AU | | | 100 | | °C/W |

NOTES: (1) Specifications are for both inputs (A and B). (2) dBC = Level referred to carrier-input signal. (3) Harmonic distortion will typically be improved significantly in the inverting mode. (4) Large Signal Response is calculated from the formula LSBW = $\frac{SR}{2\pi V_{PEAK}}$. (5) Switching time from application of digital logic signal to input signal selection.

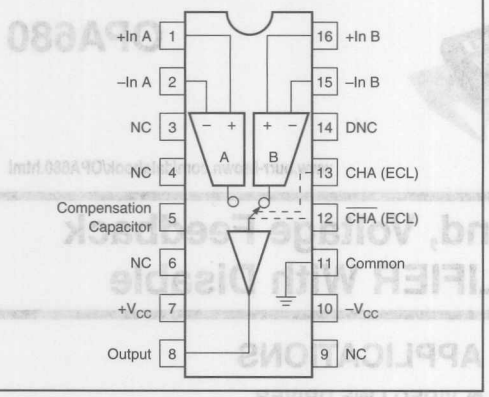
## ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC}$ = ±5VDC, $R_L$ = 150Ω, $C_{COMP}$ = 5pF, and $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

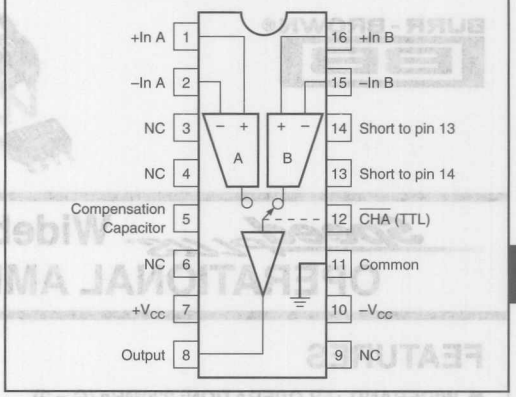
| PARAMETER | CONDITIONS | OPA678AP, AU MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **TEMPERATURE RANGE** | | | | | |
| Specification | Ambient Temp AP/AU | –40 | | +85 | °C |
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | 600 | ±2.4mV | µV |
| Offset Voltage Drift | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | ±3 | ±15 | µV/°C |
| Supply Rejection | ±$V_{CC}$ = 4.5V to 5.5V | 60 | 70 | | dB |
| **BIAS CURRENT** | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC | | 15 | 85 | µA |
| **OFFSET CURRENT** | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC | | 0.5 | 5 | µA |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range | | ±2.0 | ±2.5 | | V |
| Common-Mode Rejection | $V_{IN}$ = ±0.5VDC, $V_O$ = ±1.25V | 60 | 80 | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | |
| Open-Loop Voltage Gain | | 50 | 60 | | dB |
| **DIGITAL INPUT** | | | | | |
| TTL Logic Levels: $V_{IL}$ | Logic "LO" | 0 | | +0.8 | V |
| $V_{IH}$ | Logic "HI" | +2.0 | | +5 | V |
| $I_{IL}$ | Logic "LO", $V_{IL}$ = 0V | | –0.08 | –0.4 | mA |
| $I_{IH}$ | Logic "HI", $V_{IH}$ = +2.7V | | 5 | 50 | µA |
| ECL Logic Levels: $V_{IL}$ | Logic "LO" | –1.81 | | –1.475 | V |
| $V_{IH}$ | Logic "HI" | –1.15 | | –0.88 | V |
| $I_{IL}$ | Logic "LO", $V_{IL}$ = –1.6V | | –50 | | µA |
| $I_{IH}$ | Logic "HI", $V_{IH}$ = –1.0V | | –50 | | µA |
| **RATED OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 150Ω | ±2.5 | ±3.75 | | V |
| | $R_L$ = 50Ω | ±1.5 | ±2.0 | | V |
| Output Current | | | 44 | | mA |
| **POWER SUPPLY** | | | | | |
| Current, Quiescent | $I_O$ = 0mADC | | 25 | 35 | mA |

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

**Pin Assignments for Differential ECL Channel Switching**




**Pin Assignments for TTL Channel Switching**




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply | ±7VDC |
| Differential Input Voltage | Total $V_{cc}$ |
| Input Voltage Range (Analog and Digital) | ±$V_{cc}$ |
| Storage Temperature Range | –65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short Circuit to Ground (+25°C) | Continuous to ground |
| Junction Temperature | +175°C |

## ORDERING INFORMATION

OPA678 ( ) ( )

Basic Model Number
Performance Grade Code
A: –40°C to +85°C
Package Code
P: 16-Pin Plastic DIP
U: 16-Lead SOIC

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| OPA678AP | 16-Pin Plastic DIP | 180 |
| OPA678AU | 16-Pin SOIC | 211 |

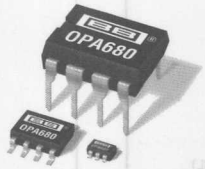
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR - BROWN®




# OPA680

www.burr-brown.com/databook/OPA680.html

## SpeedPlus™ Wideband, Voltage Feedback OPERATIONAL AMPLIFIER With Disable

## FEATURES

- WIDEBAND +5V OPERATION: 220MHz (G = 2)
- UNITY GAIN STABLE: 400MHz (G = 1)
- HIGH OUTPUT CURRENT: 150mA
- OUTPUT VOLTAGE SWING: ±4.0V
- HIGH SLEW RATE: 1800V/µs
- LOW SUPPLY CURRENT: 6.4mA
- LOW DISABLED CURRENT: 200µA
- ENABLE/DISABLE TIME: 25ns/100ns

## APPLICATIONS

- VIDEO LINE DRIVER
- xDSL LINE DRIVER/RECEIVER
- HIGH SPEED IMAGING CHANNELS
- ADC BUFFERS
- PORTABLE INSTRUMENTS
- TRANSIMPEDANCE AMPLIFIERS
- ACTIVE FILTERS

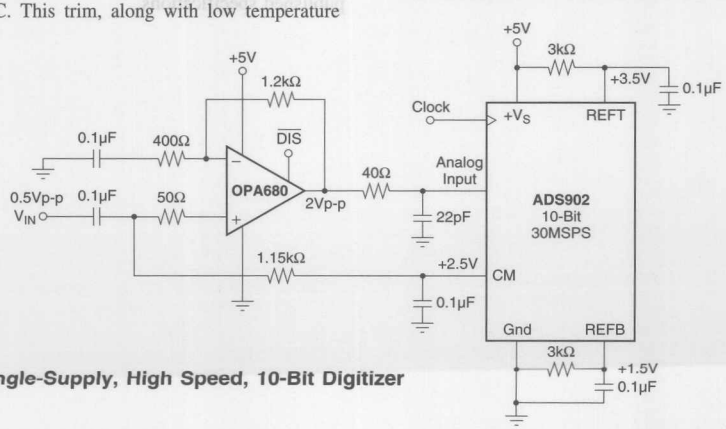
## DESCRIPTION

The OPA680 represents a major step forward in unity gain stable, voltage feedback op amps. A new internal architecture provides slew rate and full power bandwidth previously found only in wideband current feedback op amps. A new output stage architecture delivers high currents with a minimal headroom requirement. These combine to give exceptional single supply operation. Using a single +5V supply, the OPA680 can deliver a 1V to 4V output swing with over 100mA drive current and 150MHz bandwidth. This combination of features makes the OPA680 an ideal RGB line driver or single supply ADC input driver.

The OPA680's low 6.4mA supply current is precisely trimmed at 25°C. This trim, along with low temperature drift, guarantees lower maximum supply current than competing products. System power may be reduced further using the optional disable control pin. Leaving this disable pin open, or holding it high, will operate the OPA680 normally. If pulled low, the OPA680 supply current drops to less than 200µA while the output goes to a high impedance state. This feature may be used for either power savings or to implement video MUX applications.

### OPA680 PRODUCT FAMILY

| | SINGLES | DUALS |
|---|---|---|
| Voltage Feedback | OPA680 | OPA2680 |
| Current Feedback | OPA681 | OPA2681 |




**Single-Supply, High Speed, 10-Bit Digitizer**

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS: $V_S = \pm 5V$

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2, (Figure 1 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA680P, U, N TYP +25°C | GUARANTEED +25°C[2] | GUARANTEED 0°C to 70°C[3] | GUARANTEED –40°C to +85°C[3] | UNITS | MIN/ MAX | TEST LEVEL[1] |
|---|---|---|---|---|---|---|---|---|
| **AC PERFORMANCE (Figure 1)** | | | | | | | | |
| Small Signal Bandwidth | G = +1, $V_O$ = 0.5Vp-p, $R_F = 25\Omega$ | 400 | | | | MHz | Typ | C |
| | G = +2, $V_O$ = 0.5Vp-p | 220 | 210 | 200 | 190 | MHz | Min | B |
| | G = +10, $V_O$ = 0.5Vp-p | 30 | 20 | 20 | 20 | MHz | Min | B |
| Gain-Bandwidth Product | G ≥ 10 | 300 | 200 | 200 | 200 | MHz | Min | B |
| Bandwidth for 0.1dB Gain Flatness | G = +2, $V_O$ < 0.5Vp-p | 30 | | | | MHz | Typ | C |
| Peaking at a Gain of +1 | $V_O$ < 0.5Vp-p | 4 | | | | dB | Typ | C |
| Large Signal Bandwidth | G = +2, $V_O$ = 5Vp-p | 175 | | | | MHz | Typ | C |
| Slew Rate | G = +2, 4V Step | 1800 | 1400 | 1200 | 900 | V/µs | Min | B |
| Rise/Fall Time | G = +2, $V_O$ = 0.5V Step | 1.4 | — | — | | ns | Max | B |
| | G = +2, $V_O$ = 5V Step | 2.8 | — | — | | ns | Max | B |
| Settling Time to 0.02% | G = +2, $V_O$ = 2V Step | 8 | | | | ns | Typ | C |
| 0.1% | G = +2, $V_O$ = 2V Step | 6 | | | | ns | Typ | C |
| Harmonic Distortion | G = +2, f = 5MHz, $V_O$ = 2Vp-p | | | | | | | |
| 2nd Harmonic | $R_L = 100\Omega$ | –68 | –63 | — | — | dBc | Max | B |
| | $R_L \geq 500\Omega$ | –80 | –70 | — | — | dBc | Max | B |
| 3rd Harmonic | $R_L = 100\Omega$ | –80 | –75 | — | — | dBc | Max | B |
| | $R_L \geq 500\Omega$ | –88 | –85 | — | — | dBc | Max | B |
| Input Voltage Noise | f > 1MHz | 4.8 | 5.3 | 5.9 | 6.1 | nV/√Hz | Max | B |
| Input Current Noise | f > 1MHz | 2.5 | 2.8 | 3.0 | 3.6 | pA/√Hz | Max | B |
| Differential Gain | G = +2, NTSC, $V_O$ = 1.4Vp, $R_L$ = 150 | 0.05 | | | | % | Typ | C |
| Differential Phase | G = +2, NTSC, $V_O$ = 1.4Vp, $R_L$ = 150 | 0.03 | | | | deg | Typ | C |
| **DC PERFORMANCE[4]** | | | | | | | | |
| Open-Loop Voltage Gain ($A_{OL}$) | $V_O$ ±2V, $R_L = 100\Omega$ | 62 | **56** | 54 | 52 | dB | Min | A |
| Input Offset Voltage | $V_{CM}$ = 0V | ±1.0 | **±4.5** | ±5.2 | ±60 | mV | Max | A |
| Average Offset Voltage Drift | $V_{CM}$ = 0V | | | — | — | µV/°C | Max | B |
| Input Bias Current | $V_{CM}$ = 0V | +8 | **+14** | +19 | +32 | µA | Max | A |
| Average Bias Current Drift | $V_{CM}$ = 0V | | | — | — | nA/°C | Max | B |
| Input Offset Current | $V_{CM}$ = 0V | ±0.1 | **±0.7** | ±1.0 | ±1.2 | µA | Max | A |
| Average Offset Current Drift | $V_{CM}$ = 0V | | | — | — | nA/°C | Max | B |
| **INPUT** | | | | | | | | |
| Common-Mode Input Range (CMIR)[5] | | ±3.5 | **±3.4** | — | — | V | Min | A |
| Common-Mode Rejection (CMR) | $V_{CM}$ = ±1V | 59 | **56** | 51 | 50 | dB | Min | A |
| Input Impedance | | | | | | | | |
| Differential-Mode | $V_{CM}$ = 0 | 190 ‖ 0.6 | | | | kΩ ‖ pF | Typ | C |
| Common-Mode | $V_{CM}$ = 0 | 3.2 ‖ 0.9 | | | | MΩ ‖ pF | Typ | C |
| **OUTPUT** | | | | | | | | |
| Voltage Output Swing | No Load | ±4.0 | **±3.8** | ±3.7 | ±3.6 | V | Min | A |
| | 100Ω Load | ±3.9 | **±3.7** | ±3.6 | ±3.3 | V | Min | A |
| Current Output, Sourcing | $V_O$ = 0 | +190 | **+160** | +140 | +80 | mA | Min | A |
| Current Output, Sinking | $V_O$ = 0 | –150 | **–135** | –130 | –80 | mA | Min | A |
| Closed-Loop Output Impedance | G = +2, f = 100kHz | 0.03 | | | | Ω | Typ | C |
| **DISABLE (Disabled Low)** | | | | | | | | |
| Power Down Supply Current (+$V_S$) | $V_{\overline{DIS}}$ = 0 | –200 | | | | µA | Typ | C |
| Disable Time | | 100 | | | | ns | Typ | C |
| Enable Time | | 25 | | | | ns | Typ | C |
| Off Isolation | G = +2, 5MHz | 70 | | | | dB | Typ | C |
| Output Capacitance in Disable | | 4 | | | | pF | Typ | C |
| Turn On Glitch | G = +2, $R_L = 150\Omega$, $V_{IN}$ = 0 | ±50 | | | | mV | Typ | C |
| Turn Off Glitch | G = +2, $R_L = 150\Omega$, $V_{IN}$ = 0 | ±20 | | | | mV | Typ | C |
| Enable Voltage | | 2.0 | **2.4** | 2.7 | 2.8 | V | Min | A |
| Disable Voltage | | 1.1 | **1.5** | 1.7 | 2.0 | V | Max | A |
| Control Pin Input Bias Current ($V_{\overline{DIS}}$) | $V_{\overline{DIS}}$ = 0 | 100 | **160** | — | — | µA | Max | A |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | ±5 | | | | V | Typ | C |
| Maximum Operating Voltage Range | | | **±6** | ±6 | ±6 | V | Max | A |
| Max Quiescent Current | $V_S = \pm 5V$ | 6.4 | **6.8** | 7.0 | 7.2 | mA | Max | A |
| Min Quiescent Current | $V_S = \pm 5V$ | 6.4 | **6.0** | 6.0 | 5.3 | mA | Min | A |
| Power Supply Rejection (+PSR) | Input Referred | 70 | **60** | — | — | dB | Min | A |
| **THERMAL CHARACTERISTICS** | | | | | | | | |
| Specified Operating Range P, U, N Package | | –40 to +85 | | | | °C | Typ | C |
| Thermal Resistance, $\theta_{JA}$ | Junction-to-Ambient | | | | | | | |
| P 8-Pin DIP | | 100 | | | | °C/W | Typ | C |
| U SO-8 | | 125 | | | | °C/W | Typ | C |
| N SOT23-6 | | 150 | | | | °C/W | Typ | C |

NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction Temperature = Ambient for 25°C guaranteed specifications. (3) Junction Temperature = Ambient at low temperature limit: Junction Temperature = Ambient +23°C at high temperature limit for over temperature guaranteed specifications. (4) Current is considered positive out of node. $V_{CM}$ is the input common-mode voltage. (5) Tested < 3dB below minimum CMR specification at ±CMIR limits.

# SPECIFICATIONS: $V_S$ = +5V

$R_F$ = 402Ω, $R_L$ = 100Ω to $V_S$/2, G = +2, (Figure 2 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA680P, U, N TYP +25°C | OPA680P, U, N GUARANTEED +25°C[2] | 0°C to 70°C[3] | –40°C to +85°C[3] | UNITS | MIN/ MAX | TEST LEVEL[1] |
|---|---|---|---|---|---|---|---|---|
| **AC PERFORMANCE (Figure 2)** | | | | | | | | |
| Small Signal Bandwidth | G = +1, $V_O$ < 0.5Vp-p, $R_F$ = ±25Ω | 300 | | | | MHz | Typ | C |
| | G = +2, $V_O$ < 0.5Vp-p | 220 | 160 | 160 | 140 | MHz | Min | B |
| | G = +10, $V_O$ < 0.5Vp-p | 25 | 20 | 19 | 18 | MHz | Min | B |
| Gain-Bandwidth Product | G ≥ 10 | 250 | 200 | 190 | 180 | MHz | Min | B |
| Bandwidth for 0.1dB Gain Flatness | G = +2, $V_O$ < 0.5Vp-p | 20 | | | | MHz | Typ | C |
| Peaking at a Gain of +1 | $V_O$ < 0.5Vp-p | 5 | | | | dB | Typ | C |
| Large Signal Bandwidth | G = +2, $V_O$ = 2Vp-p | 200 | | | | MHz | Typ | C |
| Slew Rate | G = +2, 2V Step | 1000 | 700 | 670 | 550 | V/µs | Min | B |
| Rise Time/Fall Time | G = +2, $V_O$ = 0.5V Step | 1.6 | | | | ns | Typ | C |
| | G = +2, $V_O$ = 2V Step | 2.0 | | | | ns | Typ | C |
| Settling Time to 0.02% | G = +2, $V_O$ = 2V Step | 9 | | | | ns | Typ | C |
| 0.1% | G = +2, $V_O$ = 2V Step | 8 | | | | ns | Typ | C |
| Harmonic Distortion | G = +2, f = 5MHz, $V_O$ = 2Vp-p | | | | | | | |
| 2nd Harmonic | $R_L$ = 100Ω to $V_S$/2 | –60 | — | — | — | dBc | Max | B |
| | $R_L$ ≥ 500Ω to $V_S$/2 | –70 | — | — | — | dBc | Max | B |
| 3rd Harmonic | $R_L$ = 100Ω to $V_S$/2 | –72 | — | — | — | dBc | Max | B |
| | $R_L$ ≥ 500Ω to $V_S$/2 | –80 | — | — | — | dBc | Max | B |
| Input Voltage Noise | f > 1MHz | 5 | 5.3 | 6.0 | 6.2 | nV/√Hz | Max | B |
| Input Current Noise | f > 1MHz | 2.5 | 2.8 | 3.0 | 3.4 | pA/√Hz | Max | B |
| Differential Gain | G = +2, NTSC, $V_O$ = 1.4Vp, $R_L$ = 150 to $V_S$/2 | 0.06 | | | | % | Typ | C |
| Differential Phase | G = +2, NTSC, $V_O$ = 1.4Vp, $R_L$ = 150 to $V_S$/2 | 0.03 | | | | deg | Typ | C |
| **DC PERFORMANCE[4]** | | | | | | | | |
| Open-Loop Voltage Gain ($A_{OL}$) | $V_O$ = 2.5V, $R_L$ = 100Ω to 2.5V | 62 | **56** | 54 | 52 | dB | Min | A |
| Input Offset Voltage | $V_{CM}$ = 2.5V | ±2.0 | **±6.0** | ±7 | ±8.5 | mV | Max | A |
| Average Offset Voltage Drift | $V_{CM}$ = 2.5V | | | — | — | µV/°C | Max | B |
| Input Bias Current | $V_{CM}$ = 2.5V | +8 | **+15** | +18 | +32 | µA | Max | A |
| Average Bias Current Drift | $V_{CM}$ = 2.5V | | | — | — | nA/°C | Max | B |
| Input Offset Current | $V_{CM}$ = 2.5V | ±0.1 | **±0.6** | ±1.0 | ±1.2 | µA | Max | A |
| Average Offset Current Drift | $V_{CM}$ = 2.5V | | | — | — | nA/°C | Max | B |
| **INPUT** | | | | | | | | |
| Least Positive Input Voltage[5] | | 1.5 | **1.6** | — | — | V | Max | A |
| Most Positive Input Voltage[5] | | 3.5 | **3.4** | — | — | V | Min | A |
| Common-Mode Rejection (CMR) | $V_{CM}$ = 2.5V ±0.5V | 59 | | | | dB | Typ | C |
| Input Impedance | | | | | | | | |
| Differential-Mode | $V_{CM}$ = 2.5V | 92 ll 1.4 | | | | kΩ ll pF | Typ | C |
| Common-Mode | $V_{CM}$ = 2.5V | 2.2 ll 1.5 | | | | MΩ ll pF | Typ | C |
| **OUTPUT** | | | | | | | | |
| Most Positive Output Voltage | No Load | 4 | **3.8** | 3.6 | 3.5 | V | Min | A |
| | $R_L$ = 100Ω to 2.5V | 3.9 | **3.7** | 3.5 | 3.4 | V | Min | A |
| Least Positive Output Voltage | No Load | 1 | **1.2** | 1.4 | 1.5 | V | Min | A |
| | $R_L$ = 100Ω to 2.5V | 1.1 | **1.3** | 1.5 | 1.7 | V | Max | A |
| Current Output, Sourcing | | +150 | **+110** | +110 | +60 | mA | Max | A |
| Current Output, Sinking | | –110 | **–80** | –70 | –50 | mA | Min | A |
| Closed-Loop Output Impedance | G =+2, f = 100kHz | 0.03 | | | | Ω | Typ | C |
| **DISABLE (Disable Low)** | | | | | | | | |
| Power Down Supply Current (+$V_S$) | $V_{\overline{DIS}}$ = 0 | –130 | | | | µA | Typ | C |
| Disable Time | | 100 | | | | ns | Typ | C |
| Enable Time | | 25 | | | | ns | Typ | C |
| Off Isolation | G = +2, 5MHz | 65 | | | | dB | Typ | C |
| Output Capacitance in Disable | | 4 | | | | pF | Typ | C |
| Turn On Glitch | G = +2, $R_L$ = 150Ω, $V_{IN}$ = $V_S$/2 | ±50 | | | | mV | Typ | C |
| Turn Off Glitch | G = +2, $R_L$ = 150Ω, $V_{IN}$ = $V_S$/2 | ±20 | | | | mV | Typ | C |
| Enable Voltage | | 2.0 | **2.4** | 2.9 | 3.0 | V | Min | A |
| Disable Voltage | | 1.1 | **1.5** | 2.9 | 3.0 | V | Max | A |
| Control Pin Input Bias Current ($V_{\overline{DIS}}$) | $V_{\overline{DIS}}$ = 0 | 100 | | | | µA | Typ | C |
| **POWER SUPPLY** | | | | | | | | |
| Specified Single Supply Operating Voltage | | 5 | | | | V | Typ | C |
| Maximum Single Supply Operating Voltage | | | 12 | 12 | 12 | V | Max | B |
| Max Quiescent Current | $V_S$ = +5V | 5.1 | **6.0** | 6.0 | 6.0 | mA | Max | A |
| Min Quiescent Current | $V_S$ = +5V | 5.1 | **4.0** | 4.0 | 3.8 | mA | Min | A |
| Power Supply Rejection (+PSR) | Input Referred | 59 | | | | dB | Typ | C |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: P, U, N | | –40 to +85 | | | | °C | Typ | C |
| Thermal Resistance, $\theta_{JA}$ | Junction-to-Ambient | | | | | | | |
| P 8-Pin DIP | | 100 | | | | °C/W | Typ | C |
| U SO-8 | | 125 | | | | °C/W | Typ | C |
| N SOT23-6 | | 150 | | | | °C/W | Typ | C |

NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction Temperature = Ambient for 25°C guaranteed specifications. (3) Junction Temperature = Ambient at low temperature limit: Junction Temperature = Ambient +23°C at high temperature limit for over temperature guaranteed specifications. (4) Current is considered positive out of node. $V_{CM}$ is the input common-mode voltage. (5) Tested < 3dB below minimum CMR specification at ±CMIR limits.

## ABSOLUTE MAXIMUM RATINGS

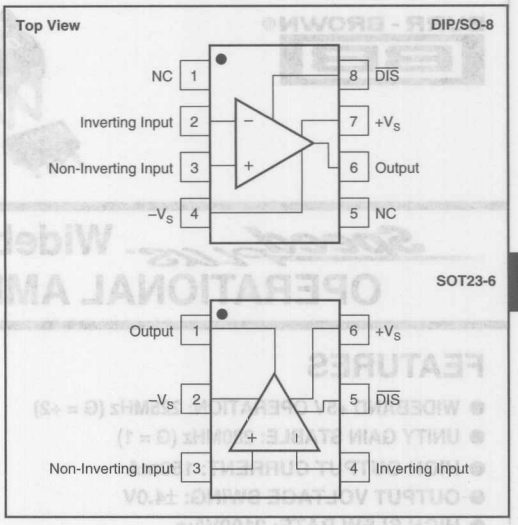
| | |
|---|---|
| Power Supply | $\pm 6.5 V_{DC}$ |
| Internal Power Dissipation | See Thermal Analysis |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: P, U, N | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SO-8 3s) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION



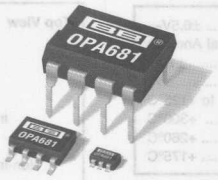

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER |
|---|---|---|---|---|---|
| OPA680P | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA680P | OPA680P |
| OPA680U | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA680U | OPA680U |
| OPA680N | 6-Pin SOT23 | 332 | –40°C to +85°C | A80 | Contact Factory for Availability |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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# OPA681

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## SpeedPLUS™ Wideband, Current Feedback OPERATIONAL AMPLIFIER With Disable

## FEATURES

- WIDEBAND +5V OPERATION: 225MHz (G = +2)
- UNITY GAIN STABLE: 280MHz (G = 1)
- HIGH OUTPUT CURRENT: 150mA
- OUTPUT VOLTAGE SWING: ±4.0V
- HIGH SLEW RATE: 2100V/µs
- LOW dG/d0: .001%/.01°
- LOW SUPPLY CURRENT: 6mA
- LOW DISABLED CURRENT: 200µA

## APPLICATIONS

- xDSL LINE DRIVER
- BROADBAND VIDEO BUFFERS
- HIGH SPEED IMAGING CHANNELS
- PORTABLE INSTRUMENTS
- ADC BUFFERS
- ACTIVE FILTERS
- WIDEBAND INVERTING SUMMING
- HIGH SFDR IF AMPLIFIER

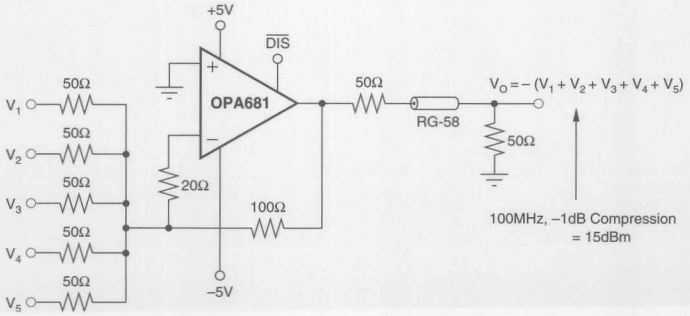
## DESCRIPTION

The OPA681 sets a new level of performance for broadband current feedback op amps. Operating on a very low 6mA supply current, the OPA681 offers a slew rate and output power normally associated with a much higher supply current. A new output stage architecture delivers a high output current with minimal voltage headroom and crossover distortion. This gives exceptional single supply operation. Using a single +5V supply, the OPA681 can deliver a 1V to 4V output swing with over 100mA drive current and 150MHz bandwidth. This combination of features makes the OPA681 an ideal RGB line driver or single supply ADC input driver.

The OPA681's low 6mA supply current is precisely trimmed at 25°C. This trim, along with low drift over temperature, guarantees lower guaranteed maximum supply current than competing products. System power may be further reduced by using the optional disable control pin. Leaving this disable pin open, or holding it high, gives normal operation. If pulled low, the OPA681 supply current drops to less than 200µA while the output goes into a high impedance state. This feature may be used for either power savings or for video MUX applications.

### OPA681 PRODUCT FAMILY

| | SINGLES | DUALS |
|---|---|---|
| Voltage Feedback | OPA680 | OPA2680 |
| Current Feedback | OPA681 | OPA2681 |




**200MHz RF Summing Amplifier**

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS: $V_S = \pm 5V$

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2, (Figure 1 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA681P, U, N TYP +25°C | GUARANTEED +25°C(2) | GUARANTEED 0°C to 70°C(3) | GUARANTEED –40°C to +85°C(3) | UNITS | MIN/ MAX | TEST LEVEL(1) |
|---|---|---|---|---|---|---|---|---|
| **AC PERFORMANCE (Figure 1)** | | | | | | | | |
| Small Signal Bandwidth ($V_O$ = 0.5Vp-p) | G = +1, $R_F = 453\Omega$ | 280 | | | | MHz | Typ | C |
| | G = +2, $R_F = 402\Omega$ | 220 | 220 | 210 | 190 | MHz | Min | B |
| | G = +5, $R_F = 261\Omega$ | 185 | | | | MHz | Typ | C |
| | G = +10, $R_F = 180\Omega$ | 180 | | | | MHz | Typ | C |
| Bandwidth for 0.1dB Gain Flatness | G = +2, $V_O$ = 0.5Vp-p | 90 | | | | MHz | Typ | C |
| Peaking at a Gain of +1 | $R_F$ = 453, $V_O$ = 0.5Vp-p | 0.4 | 2 | 4 | — | dB | Max | B |
| Large Signal Bandwidth | G = +2, $V_O$ = 5Vp-p | 150 | | | | MHz | Typ | C |
| Slew Rate | G = +2, 4V Step | 2100 | 1600 | 1600 | 1200 | V/µs | Min | B |
| Rise/Fall Time | G = +2, $V_O$ = 0.5V Step | 1.7 | — | — | — | ns | Max | B |
| | G = +2, 5V Step | 2.0 | — | — | — | ns | Max | B |
| Settling Time to 0.02% | G = +2, $V_O$ = 2V Step | 12 | | | | ns | Typ | C |
| 0.1% | G = +2, $V_O$ = 2V Step | 8 | | | | ns | Typ | C |
| Harmonic Distortion | G = +2, f = 5MHz, $V_O$ = 2Vp-p | | | | | | | |
| 2nd Harmonic | $R_L = 100\Omega$ | –79 | –73 | — | — | dBc | Max | B |
| | $R_L \geq 500\Omega$ | –85 | –82 | — | — | dBc | Max | B |
| 3rd Harmonic | $R_L = 100\Omega$ | –74 | –71 | — | — | dBc | Max | B |
| | $R_L \geq 500\Omega$ | –77 | –75 | — | — | dBc | Max | B |
| Input Voltage Noise | f > 1MHz | 2.5 | 3.0 | 3.4 | 3.6 | $nV/\sqrt{Hz}$ | Max | B |
| Non-Inverting Input Current Noise | f > 1MHz | 12 | — | — | — | $pA/\sqrt{Hz}$ | Max | B |
| Inverting Input Current Noise | f > 1MHz | 15 | — | — | — | $pA/\sqrt{Hz}$ | Max | B |
| Differential Gain | G = +2, NTSC, $V_O$ = 1.4Vp, $R_L = 150\Omega$ | 0.001 | | | | % | Typ | C |
| | $R_L = 37.5\Omega$ | 0.008 | | | | % | Typ | C |
| Differential Phase | G = +2, NTSC, $V_O$ = 1.4Vp, $R_L = 150\Omega$ | 0.01 | | | | deg | Typ | C |
| | $R_L = 37.5\Omega$ | 0.05 | | | | deg | Typ | C |
| **DC PERFORMANCE(4)** | | | | | | | | |
| Open-Loop Transimpedance Gain ($Z_{OL}$) | $V_O$ ±2V, $R_L = 100\Omega$ | 100 | **50** | 50 | 50 | kΩ | Min | A |
| Input Offset Voltage | $V_{CM}$ = 0V | ±1.3 | **±5** | ±6.5 | ±7.5 | mV | Max | A |
| Average Offset Voltage Drift | $V_{CM}$ = 0V | | | +35 | +40 | µV/°C | Max | B |
| Non-Inverting Input Bias Current | $V_{CM}$ = 0V | +30 | **+55** | ±65 | ±85 | µA | Max | A |
| Average Non-Inverting Input Bias Current Drift | $V_{CM}$ = 0V | | | –400 | –450 | nA/°C | Max | B |
| Inverting Input Bias Current | $V_{CM}$ = 0V | ±10 | **±40** | ±50 | ±55 | µA | Max | A |
| Average Inverting Input Bias Current Drift | $V_{CM}$ = 0V | | | –125 | –150 | nA°/C | Max | B |
| **INPUT** | | | | | | | | |
| Common-Mode Input Range(5) | | ±3.5 | **±3.4** | — | — | V | Min | A |
| Common-Mode Rejection | $V_{CM} = \pm 1.0V$ | 52 | **47** | 46 | 45 | dB | Min | A |
| Non-Inverting Input Impedance | | 100 ll 2 | | | | kΩ ll pF | Typ | C |
| Minimum Inverting Input Resistance ($R_I$) | Open Loop | 45 | **30** | 28 | 27 | Ω | Min | A |
| Maximum Inverting Input Resistance ($R_I$) | Open Loop | 45 | **52** | 54 | 60 | Ω | Max | A |
| **OUTPUT** | | | | | | | | |
| Voltage Output Swing | No Load | ±4.0 | **±3.8** | ±3.7 | ±3.6 | V | Min | A |
| | 100Ω Load | ±3.9 | **±3.7** | ±3.6 | ±3.3 | V | Min | A |
| Current Output, Sourcing | $V_O$ = 0 | +190 | **+160** | +140 | +80 | mA | Min | A |
| Current Output, Sinking | $V_O$ = 0 | –150 | **–135** | –130 | –80 | mA | Min | A |
| Closed-Loop Output Impedance | G = +2, f = 100kHz | 0.03 | | | | Ω | Typ | C |
| **DISABLE (Disabled Low)** | | | | | | | | |
| Power Down Supply Current (+$V_S$) | $V_{\overline{DIS}}$ = 0 | –200 | | | | µA | Typ | C |
| Disable Time | | 100 | | | | ns | Typ | C |
| Enable Time | | 25 | | | | ns | Typ | C |
| Off Isolation | G = +2, 5MHz | 70 | | | | dB | Typ | C |
| Output Capacitance in Disable | | 4 | | | | pF | Typ | C |
| Turn On Glitch | G = +2, $R_L = 150\Omega$, $V_{IN}$ = 0 | ±50 | | | | mV | Typ | C |
| Turn Off Glitch | G = +2, $R_L = 150\Omega$, $V_{IN}$ = 0 | ±20 | | | | mV | Typ | C |
| Enable Voltage | | 2.0 | **2.4** | — | — | V | Min | A |
| Disable Voltage | | 1.1 | **.8** | — | — | V | Max | A |
| Control Pin Input Bias Current ($\overline{DIS}$) | $V_{\overline{DIS}}$ = 0 | 100 | **160** | — | — | µA | Max | A |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | ±5 | | | | V | Typ | C |
| Maximum Operating Voltage Range | | | **±6** | ±6 | ±6 | V | Max | A |
| Max Quiescent Current | $V_S = \pm 5V$ | 6 | **6.4** | 6.5 | 6.6 | mA | Max | A |
| Min Quiescent Current | $V_S = \pm 5V$ | 6 | **5.6** | 5.5 | 5.0 | mA | Min | A |
| Power Supply Rejection Ratio (–PSR) | Input Referred | 58 | | | | dB | Typ | C |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: P, U, N | | –40 to +85 | | | | °C | Typ | C |
| Thermal Resistance, $\theta_{JA}$ | Junction-to-Ambient | | | | | | | |
| P 8-Pin DIP | | 100 | | | | °C/W | Typ | C |
| U SO-8 | | 125 | | | | °C/W | Typ | C |
| N SOT23-6 | | 150 | | | | °C/W | Typ | C |

NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction Temperature = Ambient for 25°C guaranteed specifications. (3) Junction Temperature = Ambient at low temperature limit: Junction Temperature = Ambient +23°C at high temperature limit for over temperature guaranteed specifications. (4) Current is considered positive out of node. $V_{CM}$ is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMR at ± CMIR limits.

# SPECIFICATIONS: $V_S$ = +5V

$R_F$ = 499Ω, $R_L$ = 100Ω to $V_S$/2, G = +2, (Figure 2 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA681P, U, N TYP +25°C | GUARANTEED +25°C[2] | GUARANTEED 0°C to 70°C[3] | GUARANTEED −40°C to +85°C[3] | UNITS | MIN/ MAX | TEST LEVEL[1] |
|---|---|---|---|---|---|---|---|---|
| **AC PERFORMANCE (Figure 2)** | | | | | | | | |
| Small Signal Bandwidth ($V_O$ = 0.5Vp-p) | G = +1, $R_F$ = 649Ω | 250 | | | | MHz | Typ | C |
| | G = +2, $R_F$ = 499Ω | 225 | 180 | — | — | MHz | Min | B |
| | G = +5, $R_F$ = 360Ω | 180 | | | | MHz | Typ | C |
| | G = +10, $R_F$ = 200Ω | 165 | | | | MHz | Typ | C |
| Bandwidth for 0.1dB Gain Flatness | G = +2, $V_O$ < 0.5Vp-p | 150 | 60 | 35 | — | MHz | Min | B |
| Peaking at a Gain of +1 | $R_F$ = 649Ω, $V_O$ < 0.5Vp-p | 0.4 | 2 | 4 | — | dB | Max | B |
| Large Signal Bandwidth | G = +2, $V_O$ = 2Vp-p | 200 | — | — | — | MHz | Min | B |
| Slew Rate | G = +2, 2V Step | 830 | 700 | — | — | V/µs | Min | B |
| Rise/Fall Time | G = +2, $V_O$ = 0.5V Step | 1.5 | — | — | — | ns | Max | B |
| | G = +2, $V_O$ = 2V Step | 2.0 | — | — | — | ns | Typ | C |
| Settling Time to 0.02% | G = +2, $V_O$ = 2V Step | — | | | | ns | Typ | C |
| 0.1% | G = +2, $V_O$ = 2V Step | — | | | | ns | Typ | C |
| Harmonic Distortion | G = +2, f = 5MHz, $V_O$ = 2Vp-p | | | | | | | |
| 2nd Harmonic | $R_L$ = 100Ω to $V_S$/2 | −64 | — | — | — | dBc | Max | B |
| | $R_L$ ≥ 500Ω to $V_S$/2 | −72 | — | — | — | dBc | Max | B |
| 3rd Harmonic | $R_L$ = 100Ω to $V_S$/2 | −72 | — | — | — | dBc | Max | B |
| | $R_L$ ≥ 500Ω to $V_S$/2 | −73 | — | — | — | dBc | Max | B |
| Input Voltage Noise | f > 1MHz | 2.2 | 3 | 3.4 | 3.6 | nV/√Hz | Max | B |
| Non-Inverting Input Current Noise | f > 1MHz | 12 | — | — | — | pA/√Hz | Max | B |
| Inverting Input Current Noise | f > 1MHz | 15 | — | — | — | pA/√Hz | Max | B |
| **DC PERFORMANCE[4]** | | | | | | | | |
| Open-Loop Transimpedance Gain ($Z_{OL}$) | $V_O$ = $V_S$/2, $R_L$ = 100Ω to $V_S$/2 | 100 | **60** | — | — | kΩ | Min | A |
| Input Offset Voltage | $V_{CM}$ = 2.5V | ±1 | **±4** | ±6.0 | ±7 | mV | Max | A |
| Average Offset Voltage Drift | $V_{CM}$ = 2.5V | | | +15 | +20 | µV/°C | Max | B |
| Non-Inverting Input Bias Current | $V_{CM}$ = 2.5V | +40 | **+65** | +75 | +95 | µA | Max | A |
| Average Non-Inverting Input Bias Current Drift | $V_{CM}$ = 2.5V | | | −300 | −350 | nA/°C | Max | B |
| Inverting Input Bias Current | $V_{CM}$ = 2.5V | ±5 | **±20** | ±25 | ±35 | µA | Max | A |
| Average Inverting Input Bias Current Drift | $V_{CM}$ = 2.5V | | | −125 | −175 | nA/°C | Max | B |
| **INPUT** | | | | | | | | |
| Least Positive Input Voltage[5] | | 1.5 | **1.6** | — | — | V | Max | A |
| Most Positive Input Voltage[5] | | 3.5 | **3.4** | — | — | V | Min | A |
| Common-Mode Rejection (CMR) | $V_{CM}$ = 2.5V | 51 | **45** | — | — | dB | Min | A |
| Non-Inverting Input Impedance | | 100 ll 2 | | | | kΩ ll pF | Typ | C |
| Minimum Inverting Input Resistance ($R_I$) | Open Loop | 45 | **32** | — | — | Ω | Min | A |
| Maximum Inverting Input Resistance ($R_I$) | Open Loop | 45 | **59** | — | — | Ω | Max | A |
| **OUTPUT** | | | | | | | | |
| Most Positive Output Voltage | $R_I$ = 1kΩ, 2.5V | 4 | **3.8** | 3.7 | 3.5 | V | Min | A |
| | $R_I$ = 100Ω, 2.5V | 3.9 | **3.7** | 3.6 | 3.4 | V | Min | A |
| Least Positive Output Voltage | $R_I$ = 1kΩ, 2.5V | 1 | **1.2** | 1.3 | 1.5 | V | Max | A |
| | $R_I$ = 100Ω, 2.5V | 1.1 | **1.3** | 1.4 | 1.6 | V | Max | A |
| Current Output, Sourcing | $V_O$ = $V_S$/2 | 150 | **110** | — | — | mA | Min | A |
| Current Output, Sinking | $V_O$ = $V_S$/2 | −110 | **−90** | — | — | mA | Min | A |
| Closed-Loop Output Impedance | G = +2, f = 100kHz | 0.03 | | | | Ω | Typ | C |
| **DISABLE (Disable Low)** | | | | | | | | |
| Power Down Supply Current (+$V_S$) | $V_{\overline{DIS}}$ = 0 | −130 | | | | µA | Typ | C |
| Disable Time | | 100 | | | | ns | Typ | C |
| Enable Time | | 25 | | | | ns | Typ | C |
| Off Isolation | G = +2, 5MHz | 65 | | | | dB | Typ | C |
| Output Capacitance in Disable | | 4 | | | | pF | Typ | C |
| Turn On Glitch | G = +2, $R_L$ = 150Ω, $V_{IN}$ = $V_S$/2 | ±50 | | | | mV | Typ | C |
| Turn Off Glitch | G = +2, $R_L$ = 150Ω, $V_{IN}$ = $V_S$/2 | ±20 | | | | mV | Typ | C |
| Enable Voltage | | 2.0 | **2.4** | — | — | V | Min | A |
| Disable Voltage | | 1.1 | **.8** | — | — | V | Max | A |
| Control Pin Input Bias Current ($\overline{DIS}$) | $V_{\overline{DIS}}$ = 0 | 100 | | | | µA | Typ | C |
| **POWER SUPPLY** | | | | | | | | |
| Specified Single Supply Operating Voltage | | 5 | | | | V | Typ | C |
| Maximum Single Supply Operating Voltage | | | **12** | 12 | 12 | V | Max | A |
| Max Quiescent Current | $V_S$ = +5V | 4.8 | **5.3** | 5.4 | 5.4 | mA | Max | A |
| Min Quiescent Current | $V_S$ = +5V | 4.8 | **4.1** | 4.0 | 4.0 | mA | Min | A |
| Power Supply Rejection Ratio (+PSR) | Input Referred | 50 | | | | dB | Typ | C |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: P, U, N | | −40 to +85 | | | | °C | Typ | C |
| Thermal Resistance, $\theta_{JA}$ | Junction-to-Ambient | | | | | | | |
| P 8-Pin DIP | | 100 | | | | °C/W | Typ | C |
| U SO-8 | | 125 | | | | °C/W | Typ | C |
| N SOT23-6 | | 150 | | | | °C/W | Typ | C |

*NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction Temperature = Ambient for 25°C guaranteed specifications. (3) Junction Temperature = Ambient at low temperature limit: Junction Temperature = Ambient +23°C at high temperature limit for over temperature guaranteed specifications. (4) Current is considered positive out of node. $V_{CM}$ is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMR at ±CMIR limits.*

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply | ±6.5VDC |
| Internal Power Dissipation[1] | See Thermal Information |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: P, U, N | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SO-8 3s) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

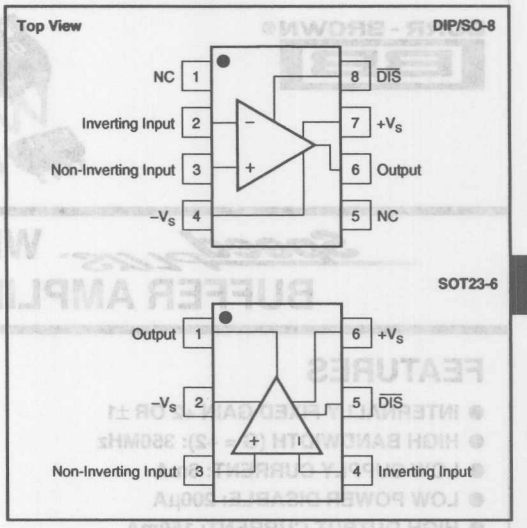
NOTE: (1) Packages must be derated based on specified $\theta_{JA}$. Maximum $T_J$ must be observed.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION



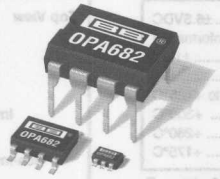

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER |
|---|---|---|---|---|---|
| OPA681P | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA681P | Contact Factory for Availability |
| OPA681U | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA681U | OPA681U |
| OPA681N | 6-Pin SOT23 | 332 | –40°C to +85°C | A81 | Contact Factory for Availability |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

BURR - BROWN®




# OPA682

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

www.burr-brown.com/databook/OPA682.html

## SpeedPLUS™ Wideband, Fixed Gain BUFFER AMPLIFIER With Disable

## FEATURES

- INTERNALLY FIXED GAIN +2 OR ±1
- HIGH BANDWIDTH (G = +2): 350MHz
- LOW SUPPLY CURRENT: 6mA
- LOW POWER DISABLE: 200µA
- HIGH OUTPUT CURRENT: 150mA
- OUTPUT VOLTAGE SWING: ±4.0V
- ±5V OR SINGLE +5V OPERATION
- SOT23-6 AVAILABLE

## APPLICATIONS

- BROADBAND VIDEO LINE DRIVERS
- VIDEO MULTIPLEXORS
- MULTIPLE LINE VIDEO DA
- PORTABLE INSTRUMENTS
- ADC BUFFERS
- ACTIVE FILTERS

## DESCRIPTION

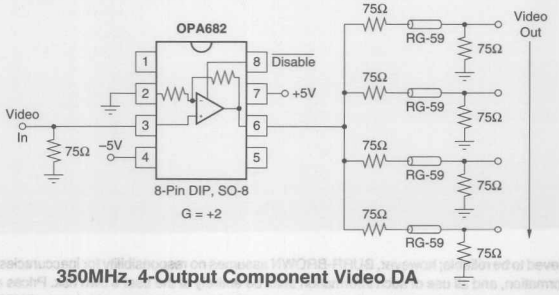
The OPA682 provides an easy to use, broadband fixed gain buffer amplifier. Depending on the external connections, the internal resistor network may be used to provide either a fixed gain of +2 video buffer or a gain of +1 or –1 voltage buffer. Operating on a very low 6mA supply current, the OPA682 offers a slew rate and output power normally associated with a much higher supply current. A new output stage architecture delivers high output current with a minimal headroom and crossover distortion. This gives exceptional single supply operation. Using a single +5V supply, the OPA682 can deliver a 1V to 4V output swing with over 100mA drive current and 250MHz bandwidth. This combination of features makes the OPA682 an ideal RGB line driver or single supply ADC input driver.

The OPA682's low 6mA supply current is precisely trimmed at 25°C. This trim, along with low drift over temperature, guarantees lower maximum supply current than competing products that report only a room temperature nominal supply current. System power may be further reduced by using the optional disable control pin. Leaving this disable pin open, or holding it high, gives normal operation. If pulled low, the OPA682 supply current drops to less than 200µA while the output goes into a high impedance state. This feature may be used for either power savings or for video MUX applications.

### PRODUCT FAMILY MEMBERS

| | SINGLES | DUALS | TRIPLES |
|---|---|---|---|
| Voltage Feedback | OPA680 | OPA2680 | OPA3680 |
| Current Feedback | OPA681 | OPA2681 | OPA3681 |
| Fixed Gain | OPA682 | OPA2682 | OPA3682 |

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350MHz, 4-Output Component Video DA

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS—$V_S$ = ±5V (Preliminary)

–In Grounded, $R_l$ = 100Ω, and G = +2, (Figure 1 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA682 TYP +25°C | OPA682 GUARANTEED +25°C[2] | 0°C to 70°C[3] | –40°C to +85°C[3] | UNITS | MIN/MAX | TEST LEVEL[1] |
|---|---|---|---|---|---|---|---|---|
| **AC PERFORMANCE** | | | | | | | | |
| Small Signal Bandwidth ($V_O$ < 0.5Vp-p) | G = +1, –In Open | 500 | | | | MHz | Min | C |
| | G = +2, –In Grounded | 410 | 240 | 220 | 210 | MHz | Min | B |
| Bandwidth for 0.1dB Gain Flatness | G = +2, $V_O$ < 0.5Vp-p | 150 | TBD | TBD | | MHz | Min | B |
| Peaking at a Gain of +1 | –In Open, $V_O$ < 0.5Vp-p | | 2 | 4 | | dB | Max | B |
| Large Signal Bandwidth | G = +2, $V_O$ = ±3V | 150 | 120 | 110 | 100 | MHz | Min | B |
| Slew Rate | G = +2, 4V Step | 2500 | 2100 | 1800 | 1600 | V/µs | Min | B |
| Rise Time | G = +2, $V_O$ = 0.5V Step | TBD | TBD | TBD | | ns | Max | B |
| Fall Time | G = +2, $V_O$ = 4V Step | TBD | TBD | TBD | | ns | Max | B |
| Settling Time to 0.02% | G = +2, $V_O$ = 0 ≥ 2V Step | 12 | TBD | TBD | | ns | Max | B |
| 0.1% | G = +2, $V_O$ = 0 ≥ 2V Step | 8 | TBD | TBD | | ns | Max | B |
| Spurious Free Dynamic Range | G = +2, f = 5MHz, $V_O$ = 2Vp-p | | | | | | | |
| | $R_l$ = 100Ω | 67 | 60 | 55 | | dBc | Min | B |
| | $R_l$ = 1kΩ | 70 | 66 | 65 | | dBc | Min | B |
| Two-Tone Intermodulation Intercept | 10MHz, at matched 50Ω Load | 45 | | | | dBm | Typ | C |
| Input Voltage Noise | f > 1MHz | 2.5 | TBD | TBD | TBD | nV/√Hz | Max | B |
| Non-Inverting Input Current Noise | f > 1MHz | 15 | TBD | TBD | TBD | pA/√Hz | Max | B |
| Inverting Input Current Noise | f > 1MHz | 12 | TBD | TBD | TBD | pA/√Hz | Max | B |
| Total Output Voltage Noise Density | f > 1MHz | 8 | TBD | TBD | TBD | nV/√Hz | Max | B |
| Differential Gain | G = +2, NTSC, $V_O$ = 1.4Vp, $R_l$ = 150 | 0.03 | | | | % | Typ | C |
| | $R_l$ = 37.5 | 0.05 | | | | % | Typ | C |
| Differential Phase | G = +2, NTSC, $V_O$ = 1.4Vp, $R_l$ = 150 | 0.08 | | | | deg | Typ | C |
| | $R_l$ = 37.5 | 0.1 | | | | deg | Typ | C |
| **DC PERFORMANCE** | | | | | | | | |
| Open-Loop Transimpedance Gain | $V_O$ ±2V, $R_l$ = 100Ω | 400 | 300 | 250 | 200 | kΩ | Min | A |
| Gain Accuracy | G = +2 nom., –In Connected to Ground | | ±0.2 | ±1 | ±1.5 | % | Max | A |
| Input Offset Voltage | $V_{CM}$ = 0V | ±1 | ±4 | TBD | ±7 | mV | Max | A |
| Average Offset Voltage Drift | $V_{CM}$ = 0V | | | 15 | 20 | µV/°C | Max | B |
| Non-Inverting Input Bias Current | $V_{CM}$ = 0V | 30 | 60 | TBD | 90 | µA | Max | A |
| Average Non-Inverting Input Bias Current Drift | $V_{CM}$ = 0V | | | TBD | TBD | nA/°C | Max | B |
| Inverting Input Bias Current | $V_{CM}$ = 0V | 10 | 25 | TBD | 40 | µA | Max | A |
| Average Inverting Input Bias Current Drift | $V_{CM}$ = 0V | | | TBD | TBD | nA°C | Max | B |
| **INPUT** | | | | | | | | |
| Common-Mode Input Range | | ±3.5 | ±3.2 | ±3 | ±2.7 | V | Min | B |
| Common-Mode Rejection | $V_{CM}$ = ±1.0V | 55 | 50 | 48 | 46 | dB | Min | B |
| Non-Inverting Input Impedance | | 100 ll 2 | | | | kΩ ll pF | Typ | C |
| Internal Resistor Value Tolerance | $R_F$ = $R_G$ = 400Ω Nominal | | ±20 | ±25 | ±30 | % | Max | A |
| **OUTPUT** | | | | | | | | |
| Voltage Output Swing | No Load | ±4.1 | ±3.9 | ±3.6 | ±3.5 | V | Min | A |
| | 100Ω Load | ±3.9 | ±3.7 | ±3.4 | ±3.3 | V | Min | A |
| Current Output, Sourcing | | 110 | 95 | 90 | 80 | mA | Min | A |
| Current Output, Sinking | | 130 | 110 | 100 | 95 | mA | Min | A |
| Short-Circuit Current | $V_O$ = 0 | 180 | 200 | | | mA | Max | B |
| Closed-Loop Output Impedance | G = +2, f = 100kHz | TBD | | | | | Typ | C |
| **DISABLE/POWER DOWN (Pin 8)** | (Disable Low) | | | | | | | |
| Power Down Supply Current | | 200 | 300 | 500 | 600 | µA | Max | A |
| Disable Time | | 200 | | | | ns | Typ | C |
| Enable Time | | 20 | | | | ns | Typ | C |
| Off Isolation | G = +2, 5MHz | 65 | | | | dB | Typ | C |
| Output Capacitance in Disable | | 5 | | | | pF | Typ | C |
| Turn On Glitch | G = +2, $R_l$ = 150Ω | 120 | 150 | 170 | | mV | Max | B |
| Turn Off Glitch | G = +2, $R_l$ = 150Ω | 5 | 20 | 25 | | mV | Max | B |
| Maximum Turn Off Voltage | | TBD | TBD | TBD | TBD | V | Min | A |
| Minimum Turn On Voltage | | TBD | TBD | TBD | TBD | V | Max | A |
| Control Pin Input Bias Current | $V_D$ = 0 ≥ 5V | TBD | TBD | TBD | TBD | µA | Max | A |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | ±5 | | | | V | Typ | C |
| Maximum Operating Voltage Range | | | ±6 | ±6 | ±6 | V | Max | A |
| Max Quiescent Current | $V_S$ = ±5V | 6 | 6.1 | 6.4 | 6.6 | mA | Max | A |
| Min Quiescent Current | $V_S$ = ±5V | 6 | 5.9 | 5.4 | 5 | mA | Min | A |
| Power Supply Rejection Ratio | Input Referred | 50 | 46 | TBD | | dB | Min | A |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: P, U, N | | –40 to +85 | | | | °C | Typ | C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| P 8-Pin DIP | | 100 | | | | °C/W | Typ | C |
| U SO-8 | | 125 | | | | °C/W | Typ | C |
| N SOT23-6 | | 150 | | | | °C/W | Typ | C |

NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction Temperature = Ambient for 25°C guaranteed specifications. (3) Junction Temperature = Ambient at low temperature limit: Junction Temperature = Ambient +23°C at high temperature limit for over temperature guaranteed specifications.

## SPECIFICATIONS—$V_S$ = +5V (Preliminary)

–In Grounded though 0.1µF, $R_l$ = 100Ω to 2.5V, G = +2, (Figure 2 for AC performance only), unless otherwise noted.

| | | OPA682 | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | TYP | GUARANTEED | | | | | |
| PARAMETER | CONDITIONS | +25°C | +25°C(2) | 0°C to 70°C(3) | –40°C to +85°C(3) | UNITS | MIN/ MAX | TEST LEVEL(1) |
| **AC PERFORMANCE** | | | | | | | | |
| Small Signal Bandwidth ($V_O$ < 0.5Vp-p) | G = +1, –In Open | 500 | | | | MHz | Min | C |
| | G = +2 | 400 | 300 | TBD | TBD | MHz | Min | B |
| Bandwidth for 0.1dB Gain Flatness | G = +2, $V_O$ < 0.5Vp-p | 150 | 60 | 35 | | MHz | Min | B |
| Peaking at a Gain of +1 | $V_O$ < 0.5Vp-p | | 2 | 4 | | dB | Max | B |
| Large Signal Bandwidth | G = +2, $V_O$ = 2Vp-p | 300 | 250 | TBD | TBD | MHz | Min | B |
| Slew Rate | G = +2, 2V Step | 2500 | 2100 | 1800 | 1600 | V/µs | Min | B |
| Rise Time | G = +2, $V_O$ = 0.5V Step | TBD | TBD | TBD | | ns | Max | B |
| Fall Time | G = +2, $V_O$ = 2V Step | TBD | TBD | TBD | | ns | Max | B |
| Settling Time to 0.02% | G = +2, $V_O$ = 2V Step | 12 | TBD | TBD | | ns | Max | B |
| 0.1% | G = +2, $V_O$ = 2V Step | 8 | TBD | TBD | | ns | Max | B |
| Spurious Free Dynamic Range | G = +2, f = 5MHz, $V_O$ = 2Vp-p | | | | | | | |
| | $R_l$ = 100Ω, $V_S$/2 | 67 | 60 | 55 | | dBc | Min | B |
| | $R_l$ = 1kΩ, $V_S$/2 | 70 | 66 | 65 | | dBc | Min | B |
| Two-Tone Intermodulation Intercept | 10MHz, at matched 50Ω Load | 45 | | | | dBm | Typ | C |
| Input Voltage Noise | f > 1MHz | 2.5 | TBD | TBD | TBD | nV/√Hz | Max | B |
| Non-Inverting Input Current Noise | f > 1MHz | 15 | TBD | TBD | TBD | pA/√Hz | Max | B |
| Inverting Input Current Noise | f > 1MHz | 12 | TBD | TBD | TBD | pA/√Hz | Max | B |
| Total Output Voltage Noise Density | f > 1MHz | 8 | TBD | TBD | TBD | nV/√Hz | Max | B |
| Differential Gain | G = +2, NTSC, $V_O$ = 1.4Vp, $R_l$ = 150 | 0.03 | | | | % | Typ | C |
| | $R_l$ = 37.5 | 0.05 | | | | % | Typ | C |
| Differential Phase | G = +2, NTSC, $V_O$ = 1.4Vp, $R_l$ = 150 | 0.08 | | | | deg | Typ | C |
| | $R_l$ = 37.5 | 0.1 | | | | deg | Typ | C |
| **DC PERFORMANCE** | | | | | | | | |
| Open-Loop Transimpedance Gain | $V_O$ = $V_S$/2, $R_l$ = 100Ω to $V_S$/2 | 100 | 56 | | 45 | kΩ | Min | A |
| Gain Accuracy | G = +2 nom., –In Connected to Ground | | ±0.2 | ±1 | ±1.5 | % | Max | A |
| Input Offset Voltage | $V_{CM}$ = 2.5V | ±1 | ±4 | TBD | ±7 | mV | Max | A |
| Average Offset Voltage Drift | $V_{CM}$ = 2.5V | | | 15 | 20 | µV/°C | Max | B |
| Non-Inverting Input Bias Current | $V_{CM}$ = 2.5V | 30 | 60 | TBD | 90 | µA | Max | A |
| Average Non-Inverting Input Bias Current Drift | $V_{CM}$ = 2.5V | | | TBD | TBD | nA/°C | Max | B |
| Inverting Input Bias Current | $V_{CM}$ = 2.5V | 10 | 25 | TBD | 40 | µA | Max | A |
| Average Inverting Input Bias Current Drift | $V_{CM}$ = 2.5V | | | TBD | TBD | nA°C | Max | B |
| **INPUT** | | | | | | | | |
| Least Positive Input Voltage | | 1.5 | 1.8 | 2 | 2.3 | V | Min | B |
| Most Positive Input Voltage | | 3.5 | 3.2 | 3 | 2.7 | V | Max | B |
| Common-Mode Rejection | $V_{CM}$ = 2.5V | 44 | 42 | 40 | 40 | dB | Min | B |
| Non-Inverting Input Impedance | | 100 ll 2 | | | | kΩ ll pF | Typ | C |
| Internal Resistor Value Tolerance | $R_F$ = $R_G$ = 400Ω Nominal | | ±20 | ±25 | ±30 | % | Max | A |
| **OUTPUT** | | | | | | | | |
| Least Positive Output Voltage | $R_l$ = 1kΩ, 2.5V | 3.8 | 3.7 | 3.6 | 3.5 | V | Min | A |
| | $R_l$ = 100Ω, 2.5V | 3.7 | 3.6 | 3.5 | 3.4 | V | Min | A |
| Most Positive Output Voltage | $R_l$ = 1kΩ, 2.5V | 1.2 | 1.3 | 1.4 | 1.5 | V | Min | A |
| | $R_l$ = 100Ω, 2.5V | 1.3 | 1.4 | 1.5 | 1.6 | V | Min | A |
| Current Output, Sourcing | | 80 | 70 | 60 | 45 | mA | Min | A |
| Current Output, Sinking | | 80 | 70 | 60 | 45 | mA | Min | A |
| Short-Circuit Current | $V_O$ Shorted to Either Supply | 130 | 160 | | | mA | Max | B |
| Output Impedance | G = +2, f = 100kHz | 0.2 | | | | Ω | Typ | C |
| **DISABLE** | (Disable Low) | | | | | | | |
| Power Down Supply Current | | 400 | 500 | 800 | 1000 | µA | Max | A |
| Disable Time | | 400 | | | | ns | Typ | C |
| Enable Time | | 50 | | | | ns | Typ | C |
| Off Isolation | G = +2, 5MHz | 70 | | | | dB | Typ | C |
| Output Capacitance in Disable | | 5 | | | | pF | Typ | C |
| Turn On Glitch | G = +2, $R_l$ = 150Ω | 5 | 20 | 25 | | mV | Max | B |
| Turn Off Glitch | G = +2, $R_l$ = 150Ω | 5 | 20 | 25 | | mV | Max | B |
| Maximum Turn Off Voltage | | TBD | TBD | TBD | TBD | V | Min | A |
| Minimum Turn On Voltage | | TBD | TBD | TBD | TBD | V | Max | A |
| Control Pin Input Bias Current | $V_D$ = 0 ≥ 5V | TBD | TBD | TBD | TBD | µA | Max | A |
| **POWER SUPPLY** | | | | | | | | |
| Specified Single Supply Operating Voltage | | 5 | | | | V | Typ | C |
| Maximum Single Supply Operating Voltage | | | 12 | 12 | 12 | V | Max | A |
| Max Quiescent Current | $V_S$ = ±5V | 6 | 6.1 | 6.4 | 6.6 | mA | Max | A |
| Min Quiescent Current | $V_S$ = ±5V | 6 | 5.9 | 5.4 | 5 | mA | Min | A |
| Power Supply Rejection Ratio | Input Referred | 50 | 46 | TBD | | dB | Min | A |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: P, U, N | | –40 to +85 | | | | °C | Typ | C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| P 8-Pin DIP | | 100 | | | | °C/W | Typ | C |
| U SO-8 | | 125 | | | | °C/W | Typ | C |
| N SOT23-6 | | 150 | | | | °C/W | Typ | C |

NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction Temperature = Ambient for 25°C guaranteed specifications. (3) Junction Temperature = Ambient at low temperature limit: Junction Temperature = Ambient +23°C at high temperature limit for over temperature guaranteed specifications.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply | ±6.5VDC |
| Internal Power Dissipation[1] | See Thermal Information |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: P, PB, U, UB, N, NB | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SOIC 3s) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

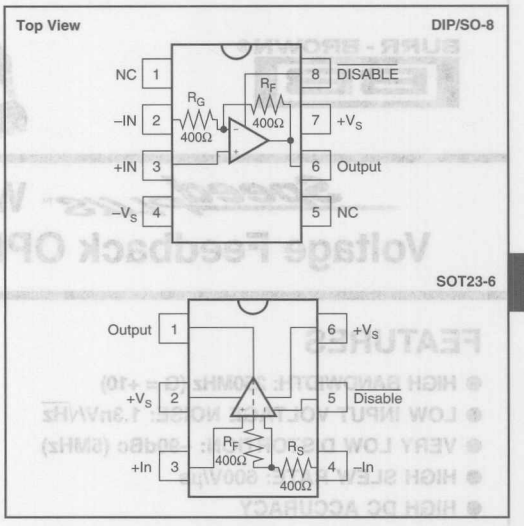
NOTE: (1) Packages must be derated based on specified $\theta_{JA}$. Maximum $T_J$ must be observed.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION




## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER[2] |
|---|---|---|---|---|---|
| OPA682P | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA682P | OPA682P |
| OPA682U | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA682U | OPA682U |
| OPA682N | 6-Pin SOT23 | 332 | –40°C to +85°C | A82 | OPA682N-250<br>OPA682N-3K |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The SOT23-6 is only available on a 7" tape and reel (e.g. ordering 250 pieces of OPA682N will get a single 250 piece tape and reel. Please refer to Appendix B of Burr-Brown IC Data Book for detailed Tape and Reel Mechanical information.

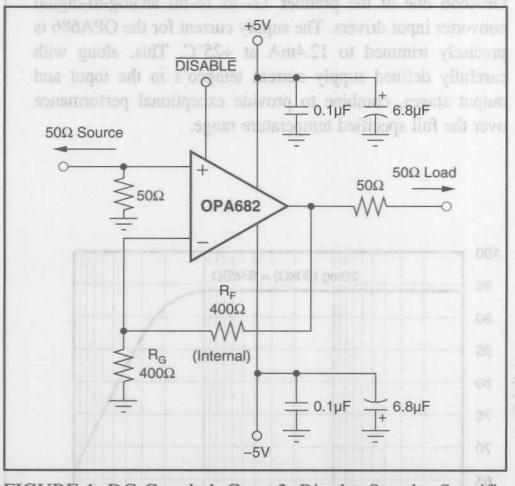



FIGURE 1. DC-Coupled, G = +2, Bipolar Supply, Specification and Test Circuit.

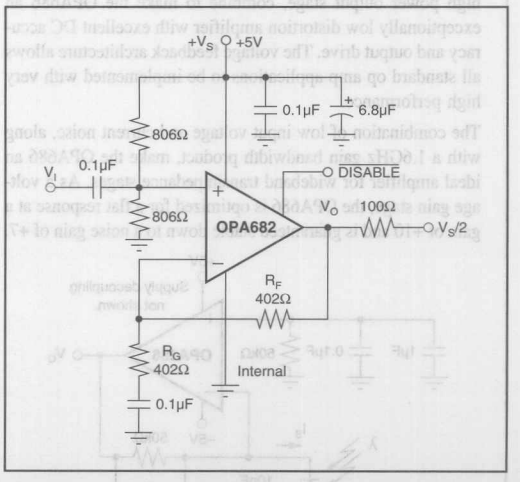
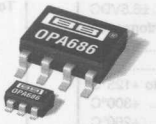



FIGURE 2. AC-Coupled, G = +2, Single Supply Specification and Test Circuit.

BURR-BROWN®




# OPA686

www.burr-brown.com/databook/OPA686.html

## SpeedPLUS™ Wideband, Low Noise, Voltage Feedback OPERATIONAL AMPLIFIER

## FEATURES

- HIGH BANDWIDTH: 250MHz (G = +10)
- LOW INPUT VOLTAGE NOISE: 1.3nV/√Hz
- VERY LOW DISTORTION: –90dBc (5MHz)
- HIGH SLEW RATE: 600V/µs
- HIGH DC ACCURACY
- LOW SUPPLY CURRENT: 12mA
- HIGH GAIN BANDWIDTH PRODUCT: 1600MHz
- STABLE FOR GAINS ≥ 7

## APPLICATIONS

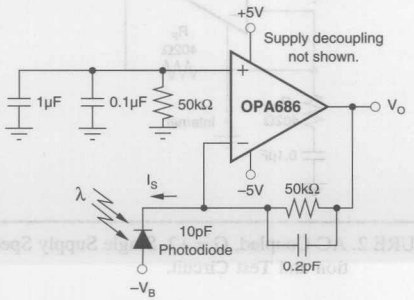
- HIGH DYNAMIC RANGE ADC PREAMP
- LOW NOISE, WIDEBAND, TRANSIMPEDANCE AMPLIFIER
- WIDEBAND, HIGH GAIN AMPLIFIER
- LOW NOISE DIFFERENTIAL RECEIVER
- VDSL LINE RECEIVER
- ULTRASOUND CHANNEL AMPLIFIER
- IMPROVED REPLACEMENT FOR THE CLC425

## DESCRIPTION

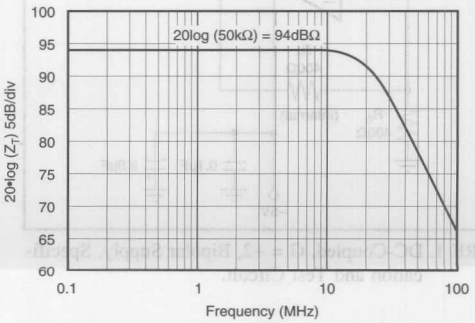
The OPA686 combines very high gain bandwidth and large signal performance with very low input voltage noise while dissipating a low 12mA supply current. The classical differential input stage, along with two stages of forward gain and a high power output stage, combine to make the OPA686 an exceptionally low distortion amplifier with excellent DC accuracy and output drive. The voltage feedback architecture allows all standard op amp applications to be implemented with very high performance.

The combination of low input voltage and current noise, along with a 1.6GHz gain bandwidth product, make the OPA686 an ideal amplifier for wideband transimpedance stages. As a voltage gain stage, the OPA686 is optimized for a flat response at a gain of +10 and is guaranteed stable down to a noise gain of +7.

A new external compensation technique can be used to give a very flat frequency response below the minimum stable gain for the OPA686, further improving its already exceptional distortion performance. Using this compensation makes the OPA686 one of the premier 12- to 14-bit analog-to-digital converter input drivers. The supply current for the OPA686 is precisely trimmed to 12.4mA at +25°C. This, along with carefully defined supply current tempco's in the input and output stages, combine to provide exceptional performance over the full specified temperature range.




High Gain, 20MHz Transimpedance Amplifier




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS: $V_S = \pm 5V$

$R_F = 453\Omega$, $R_L = 100\Omega$, and G =+10, unless otherwise noted. Figure 1 for AC performance.

| PARAMETER | CONDITIONS | OPA686U, N | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | TYP | GUARANTEED | | | | | |
| | | +25°C | +25°C[2] | 0°C to 70°C[3] | –40°C to +85°C[3] | UNITS | MIN/ MAX | TEST LEVEL[1] |
| **AC PERFORMANCE (Figure 1)** | | | | | | | | |
| Closed-Loop Bandwidth | G = +7, $R_G = 50\Omega$, $V_O = 200mVp\text{-}p$ | 425 | | | | MHz | Typ | C |
| | G = +10, $R_G = 50\Omega$, $V_O = 200mVp\text{-}p$ | 250 | 200 | 170 | 140 | MHz | Min | B |
| | G = +20, $R_G = 50\Omega$, $V_O = 200mVp\text{-}p$ | 100 | 80 | 65 | 55 | MHz | Min | B |
| Gain Bandwidth Product | G ≥ +40 | 1600 | 1250 | 1100 | 1000 | MHz | Min | B |
| Bandwidth for 0.1dB Gain Flatness | G = +10, $R_L = 100\Omega$, $V_O = 200mVp\text{-}p$ | 40 | 35 | 30 | 25 | MHz | Min | B |
| Peaking at a Gain of +7 | | 2 | | | | dB | Typ | C |
| Harmonic Distortion | G = +10, f = 5MHz, $V_O = 2Vp\text{-}p$ | | | | | | | |
| 2nd Harmonic | $R_L = 100\Omega$ | –75 | –70 | –65 | –60 | dBc | Max | B |
| | $R_L = 500\Omega$ | –90 | –85 | –80 | –75 | dBc | Max | B |
| 3rd Harmonic | $R_L = 100\Omega$ | –95 | –90 | –85 | –80 | dBc | Max | B |
| | $R_L = 500\Omega$ | –110 | –105 | –100 | –95 | dBc | Max | B |
| Two-Tone, 3rd-Order Intercept | G = +10, f = 10MHz | 43 | 40 | 39 | 37 | dBm | Min | B |
| Input Voltage Noise | f > 1MHz | 1.3 | 1.5 | 1.6 | 1.7 | $nV/\sqrt{Hz}$ | Max | B |
| Input Current Noise | f > 1MHz | 1.8 | 2.3 | 2.4 | 2.5 | $pA/\sqrt{Hz}$ | Max | B |
| Rise/Fall Time | 0.2V Step | 1.4 | 1.75 | 2 | 2.5 | ns | Max | B |
| Slew Rate | 2V Step | 600 | 500 | 400 | 310 | V/µs | Min | B |
| Settling Time to 0.01% | 2V Step | 18 | | | | ns | Typ | C |
| 0.1% | 2V Step | 16 | 14 | 21 | 25 | ns | Max | B |
| 1% | 2V Step | 11 | 12 | 14 | 18 | ns | Max | B |
| Differential Gain | G = +10, NTSC, $R_L = 150\Omega$ | 0.02 | | | | % | Typ | C |
| Differential Phase | G = +10, NTSC, $R_L = 150\Omega$ | 0.02 | | | | deg | Typ | C |
| **DC PERFORMANCE[4]** | | | | | | | | |
| Open-Loop Voltage Gain ($A_{OL}$) | $V_O = 0V$ | 80 | **75** | 70 | 70 | dB | Min | A |
| Input Offset Voltage | $V_{CM} = 0V$ | ±0.35 | **±1.0** | ±1.2 | ±1.5 | mV | Max | A |
| Average Offset Voltage Drift | $V_{CM} = 0V$ | | | 5 | 10 | µV/°C | Max | B |
| Input Bias Current | $V_{CM} = 0V$ | –10 | **–17** | –18 | –20 | µA | Max | A |
| Input Bias Current Drift | $V_{CM} = 0V$ | | | 50 | 100 | nA/°C | Max | B |
| Input Offset Current | $V_{CM} = 0V$ | ±0.5 | **±1.0** | ±1.5 | ±1.8 | µA | Max | A |
| Input Offset Current Drift | $V_{CM} = 0V$ | | | 5 | 10 | nA/°C | Max | B |
| **INPUT** | | | | | | | | |
| Common-Mode Input Range (CMIR)[5] | | ±3.7 | **±3.2** | ±3.1 | ±3.0 | V | Min | A |
| Common-Mode Rejection (CMR) | $V_{CM} = \pm 1V$, Input Referred | 100 | **90** | 85 | 75 | dB | Min | A |
| Input Impedance | | | | | | | | |
| Differential-Mode | $V_{CM} = 0V$ | 6 ll 2 | | | | kΩ ll pF | Typ | C |
| Common-Mode | $V_{CM} = 0V$ | 2.9 ll 1 | | | | MΩ ll pF | Typ | C |
| **OUTPUT** | | | | | | | | |
| Output Voltage Swing | ≥ 400Ω Load | ±3.5 | **±3.2** | ±3.1 | ±3.0 | V | Min | A |
| | 100Ω Load | ±3.3 | **±3.0** | ±2.8 | ±2.8 | V | Min | A |
| Current Output, Sourcing | $V_O = 0V$ | 80 | **60** | 55 | 50 | mA | Min | A |
| Current Output, Sinking | $V_O = 0V$ | –80 | **–60** | –55 | –40 | mA | Min | A |
| Closed-Loop Output Impedance | G = +10, f = 100kHz | 0.008 | | | | Ω | Typ | C |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | ±5 | | | | V | Typ | C |
| Maximum Operating Voltage | | | **±6** | ±6 | ±6 | V | Max | A |
| Max Quiescent Current | $V_S = \pm 5V$ | 12.4 | **12.9** | 13 | 13.9 | mA | Max | A |
| Min Quiescent Current | $V_S = \pm 5V$ | 12.4 | **11.9** | 11.9 | 11 | mA | Min | A |
| Power Supply Rejection Ratio | | | | | | | | |
| +PSR, –PSR | $\|V_S\| = 4.5$ to 5.5, Input Referred | 78 | **70** | 70 | 65 | dB | Min | A |
| **THERMAL CHARACTERISTICS** | | | | | | | | |
| Specified Operating Range: U, N Package | | –40 to +85 | | | | °C | Typ | C |
| Thermal Resistance, $\theta_{JA}$ | Junction-to-Ambient | | | | | | | |
| U 8-Pin, SO-8 | | 125 | | | | °C/W | Typ | C |
| N 5-Pin, SOT23 | | 150 | | | | °C/W | Typ | C |

NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction Temperature = Ambient for 25°C guaranteed specifications. (3) Junction Temperature = Ambient at low temperature limit: Junction Temperature = Ambient +23°C at high temperature limit for over temperature guaranteed specifications. (4) Current is considered positive out of node. $V_{CM}$ is the input common-mode voltage. (5) Tested <3dB below minimum specified CMR at ±CMIR limits.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## ABSOLUTE MAXIMUM RATINGS

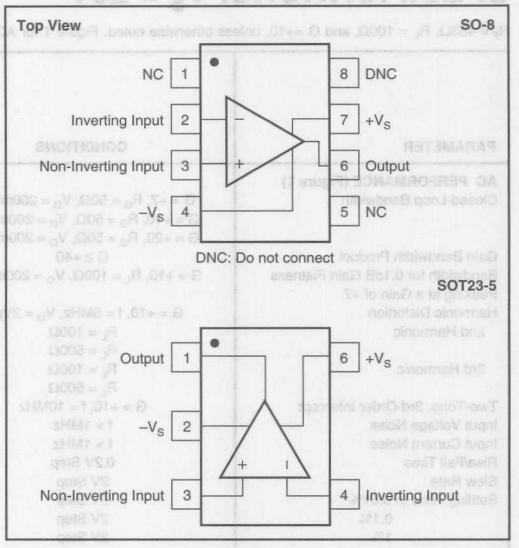
| | |
|---|---|
| Power Supply | $\pm 6.5 V_{DC}$ |
| Internal Power Dissipation | See Thermal Analysis |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: U, N | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SO-8) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN CONFIGURATION



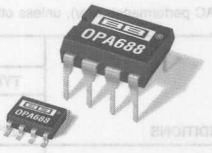

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER |
|---|---|---|---|---|---|
| OPA686U | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA686U | OPA686U |
| OPA686N | 5-Pin SOT23 | 331 | –40°C to +85°C | A86 | Contact Factory for Availability |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR - BROWN®

# OPA688




www.burr-brown.com/databook/OPA688.html



## SpeedPlus™ Unity Gain Stable, Wideband VOLTAGE LIMITING AMPLIFIER

## FEATURES

- HIGH LINEARITY NEAR LIMITING
- FAST RECOVERY FROM OVERDRIVE: 2.4ns
- LIMITING VOLTAGE ACCURACY: ±15mV
- –3dB BANDWIDTH (G = +1): 530MHz
- SLEW RATE: 1000V/µs
- ±5V AND 5V SUPPLY OPERATION
- HIGH GAIN VERSION: OPA689

## APPLICATIONS

- FAST LIMITING ADC INPUT BUFFER
- CCD PIXEL CLOCK STRIPPING
- VIDEO SYNC STRIPPING
- HF MIXER
- IF LIMITING AMPLIFIER
- AM SIGNAL GENERATION
- NON-LINEAR ANALOG SIGNAL PROCESSING
- COMPARATOR

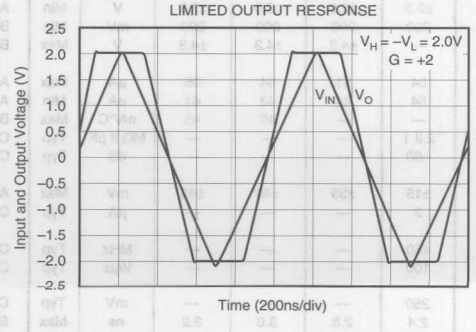
## DESCRIPTION

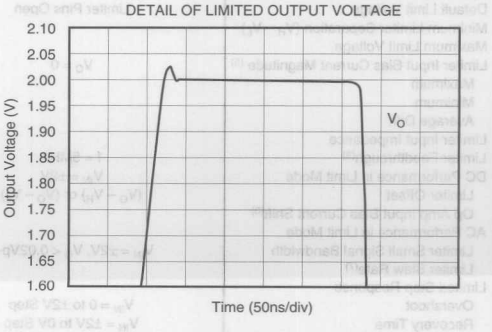
The OPA688 is a wideband, unity gain stable voltage feedback op amp that offers bipolar output voltage limiting. Two buffered limiting voltages take control of the output when it attempts to drive beyond these limits. This new output limiting architecture holds the limiter offset error to ±15mV. The op amp operates linearly to within 30mV of the limits.

The combination of narrow nonlinear range and low limiting offset allows the limiting voltages to be set within 100mV of the desired linear output range. A fast 2.4ns recovery from limiting ensures that overdrive signals will be transparent to the signal channel. Implementing the limiting function at the output, as opposed to the input, gives the specified limiting accuracy for any gain, and allows the OPA688 to be used in all standard op amp applications.

Non-linear analog signal processing will benefit from the OPA688's sharp transition from linear operation to output limiting. The quick recovery time supports high speed applications.

The OPA688 is available in an industry standard pinout in 8-pin PDIP and SO-8 packages. For higher gain, or transimpedance applications requiring output limiting with fast recovery, consider the OPA689.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

$G = +2$, $R_L = 500\Omega$, $R_F = 402\Omega$, $V_H = -V_L = 2V$ (Figure 1 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA688U, P | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | TYP | GUARANTEED[1] | | | | | |
| | | +25°C | +25°C | 0°C to +70°C | −40°C to +85°C | UNITS | MIN/ MAX | TEST LEVEL[2] |
| **AC PERFORMANCE (see Figure 1)** | | | | | | | | |
| Small Signal Bandwidth | $V_O < 0.2Vp-p$ | | | | | | | |
| | $G = +1$, $R_F = 25\Omega$ | 530 | — | — | — | MHz | Typ | C |
| | $G = +2$ | 260 | 150 | 140 | 135 | MHz | Min | B |
| | $G = -1$ | 230 | — | — | — | MHz | Typ | C |
| Gain-Bandwidth Product ($G \geq +5$) | $V_O < 0.2Vp-p$ | 290 | 175 | 170 | 160 | MHz | Min | B |
| Gain Peaking | $G = +1$, $R_F = 25\Omega$, $V_O < 0.2Vp-p$ | 11 | — | — | — | dB | Typ | C |
| 0.1dB Gain Flatness Bandwidth | $V_O < 0.2Vp-p$ | 50 | — | — | — | MHz | Typ | C |
| Large Signal Bandwidth | $V_O = 4Vp-p$, $V_H = -V_L = 2.5V$ | 145 | 100 | 95 | 90 | MHz | Min | B |
| Step Response: | | | | | | | | |
| Slew Rate | 4V Step, $V_H = -V_L = 2.5V$ | 1000 | 800 | 770 | 650 | V/µs | Min | B |
| Rise/Fall Time | 0.2V Step | 1.2 | 2.6 | 2.7 | 3 | ns | Max | B |
| Settling Time: 0.05% | 2V Step | 7 | — | — | — | ns | Typ | C |
| Spurious Free Dynamic Range | $f = 5MHz$, $V_O = 2Vp-p$ | 66 | 62 | 58 | 53 | dB | Min | B |
| Differential Gain | NTSC, PAL, $R_L = 500\Omega$ | 0.02 | — | — | — | % | Typ | C |
| Differential Phase | NTSC, PAL, $R_L = 500\Omega$ | 0.01 | — | — | — | ° | Typ | C |
| Input Noise: | | | | | | | | |
| Voltage Noise Density | $f \geq 1MHz$ | 6.3 | 7.2 | 7.8 | 8 | $nV/\sqrt{Hz}$ | Max | B |
| Current Noise Density | $f \geq 1MHz$ | 2.0 | 2.5 | 2.9 | 3.6 | $pA/\sqrt{Hz}$ | Max | B |
| **DC PERFORMANCE ($V_{CM} = 0$)** | | | | | | | | |
| Open Loop Voltage Gain ($A_{OL}$) | $V_O = \pm 0.5V$ | 54 | 48 | 46 | 45 | dB | Min | A |
| Input Offset Voltage | | ±2 | ±6 | ±7 | ±9 | mV | Max | A |
| Average Drift | | — | — | ±14 | ±14 | µV/°C | Max | B |
| Input Bias Current[3] | | +6 | ±12 | ±13 | ±20 | µA | Max | A |
| Average Drift | | — | — | −60 | −90 | nA/°C | Max | B |
| Input Offset Current | | ±0.3 | ±2 | ±3 | ±4 | µA | Max | A |
| Average Drift | | — | — | ±10 | ±10 | nA/°C | Max | B |
| **INPUT** | | | | | | | | |
| Common-Mode Rejection | Input Referred, $V_{CM} = \pm 0.5V$ | 57 | 50 | 49 | 47 | dB | Min | A |
| Common-Mode Input Range[4] | | ±3.3 | ±3.2 | ±3.2 | ±3.1 | V | Min | A |
| Input Impedance | | | | | | | | |
| Differential-Mode | | 0.4 ‖ 1 | — | — | — | MΩ ‖ pF | Typ | C |
| Common-Mode | | 1 ‖ 1 | — | — | — | MΩ ‖ pF | Typ | C |
| **OUTPUT** | $V_H = -V_L = 4.3V$ | | | | | | | |
| Output Voltage Range | $R_L \geq 500\Omega$ | ±4.1 | ±3.9 | ±3.9 | ±3.8 | V | Min | A |
| Current Output, Sourcing | $V_O = 0$ | 140 | 125 | 115 | 100 | mA | Min | A |
| Sinking | $V_O = 0$ | −100 | −85 | −80 | −70 | mA | Min | A |
| Closed-Loop Output Impedance | $G = +1$, $R_F = 25\Omega$, $f < 100kHz$ | 0.2 | — | — | — | Ω | Typ | C |
| **POWER SUPPLY** | | | | | | | | |
| Operating Voltage, Specified | | ±5 | — | — | — | V | Typ | C |
| Maximum | | — | ±6 | ±6 | ±6 | V | Max | C |
| Quiescent Current, Maximum | | 15.8 | 17 | 19 | 20 | mA | Max | A |
| Minimum | | 15.8 | 14 | 12.8 | 11 | mA | Min | A |
| Power Supply Rejection Ratio | $+V_S = 4.5V$ to $5.5V$ | | | | | | | |
| +PSR (Input Referred) | | 65 | 58 | 57 | 55 | dB | Min | A |
| **OUTPUT VOLTAGE LIMITERS** | | | | | | | | |
| Default Limit Voltage | Limiter Pins Open | ±3.3 | ±3.0 | ±3.0 | ±2.9 | V | Min | A |
| Minimum Limiter Separation ($V_H - V_L$) | | 200 | 200 | 200 | 200 | mV | Min | B |
| Maximum Limit Voltage | | — | ±4.3 | ±4.3 | ±4.3 | V | Max | B |
| Limiter Input Bias Current Magnitude[5] | $V_O = 0$ | | | | | | | |
| Maximum | | 54 | 61 | 64 | 66 | µA | Max | A |
| Minimum | | 54 | 44 | 43 | 41 | µA | Min | A |
| Average Drift | | — | — | 40 | 45 | nA/°C | Max | B |
| Limiter Input Impedance | | 2 ‖ 1 | — | — | — | MΩ ‖ pF | Typ | C |
| Limiter Feedthrough[6] | $f = 5MHz$ | −60 | — | — | — | dB | Typ | C |
| DC Performance in Limit Mode | $V_{IN} = \pm 2V$ | | | | | | | |
| Limiter Offset | $(V_O - V_H)$ or $(V_O - V_L)$ | ±15 | ±35 | ±40 | ±40 | mV | Max | A |
| Op Amp Input Bias Current Shift[3] | | 3 | — | — | — | µA | Typ | C |
| AC Performance in Limit Mode | | | | | | | | |
| Limiter Small Signal Bandwidth | $V_{IN} = \pm 2V$, $V_O < 0.02Vp-p$ | 450 | — | — | — | MHz | Typ | C |
| Limiter Slew Rate[7] | | 100 | — | — | — | V/µs | Typ | C |
| Limited Step Response | | | | | | | | |
| Overshoot | $V_{IN} = 0$ to $\pm 2V$ Step | 250 | — | — | — | mV | Typ | C |
| Recovery Time | $V_{IN} = \pm 2V$ to 0V Step | 2.4 | 2.8 | 3.0 | 3.2 | ns | Max | B |
| Linearity Guardband[8] | $f = 5MHz$, $V_O = 2Vp-p$ | 30 | — | — | — | mV | Typ | C |

## SPECIFICATIONS— $V_S$ = ±5V (CONT)

G = +2, $R_L$ = 500Ω, $R_F$ = 402Ω, $V_H$ = $-V_L$ = 2V (Figure 1 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA688U, P TYP +25°C | GUARANTEED[1] +25°C | 0°C to +70°C | −40°C to +85°C | UNITS | MIN/ MAX | TEST LEVEL[2] |
|---|---|---|---|---|---|---|---|---|
| **THERMAL CHARACTERISTICS** | | | | | | | | |
| Temperature Range | Specification: P, U | −40 to +85 | — | — | — | °C | Typ | C |
| Thermal Resistance | Junction-to-Ambient | | | | | | | |
| P 8-Pin DIP | | 100 | — | — | — | °C/W | Typ | C |
| U 8-Pin SO-8 | | 125 | — | — | — | °C/W | Typ | C |

NOTES: (1) Junction Temperature = Ambient Temperature for low temperature limit and 25°C guaranteed specifications. Junction Temperature = Ambient Temperature + 23°C at high temperature limit guaranteed specifications. (2) TEST LEVELS: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value for information only. (3) Current is considered positive out of node. (4) CMIR tested as < 3dB degradation from minimum CMRR at specified limits. (5) $I_{VH}$ ($V_H$ bias current) is positive, and $I_{VL}$ ($V_L$ bias current) is negative, under these conditions. See Figures 1 and 7. (6) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to $V_H$ (or $V_L$) when $V_{IN}$ = 0. (7) $V_H$ slew rate conditions are: $V_{IN}$ = +2V, G = +2, $V_L$ = −2V, $V_H$ = step between 2V and 0V. $V_L$ slew rate conditions are similar. (8) Linearity Guardband is defined for an output sinusoid (f = 5MHz, $V_O$ = $0V_{DC}$ ±1Vp-p) centered between the limiter levels ($V_H$ and $V_L$). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB (see Figure 8).

## SPECIFICATIONS— $V_S$ = +5V

G = +2, $R_L$ = 500Ω tied to $V_{CM}$ = 2.5V, $R_F$ = 402Ω, $V_L$ = $V_{CM}$ −1.2V, $V_H$ = $V_{CM}$ +1.2V (Figure 2 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA688U, P TYP +25°C | GUARANTEED[1] +25°C | 0°C to +70°C | −40°C to +85°C | UNITS | MIN/ MAX | TEST LEVEL[2] |
|---|---|---|---|---|---|---|---|---|
| **AC PERFORMANCE (see Figure 2)** | | | | | | | | |
| Small Signal Bandwidth | $V_O$ < 0.2Vp-p | | | | | | | |
| | G = +1, $R_F$ = 25Ω | 515 | — | — | — | MHz | Typ | C |
| | G = +2 | 240 | 110 | 105 | 100 | MHz | Min | B |
| | G = −1 | 190 | — | — | — | MHz | Typ | C |
| Gain-Bandwidth Product (G ≥ +5) | $V_O$ < 0.2Vp-p | 275 | 130 | 125 | 120 | MHz | Min | B |
| Gain Peaking | G = +1, $R_F$ = 25Ω, $V_O$ < 0.2Vp-p | 10 | — | — | — | dB | Typ | C |
| 0.1dB Gain Flatness Bandwidth | $V_O$ < 0.2Vp-p | 50 | — | — | — | MHz | Typ | C |
| Large Signal Bandwidth | $V_O$ = 2Vp-p | 240 | 110 | 105 | 100 | MHz | Min | B |
| Step Response: | | | | | | | | |
| Slew Rate | 2V Step | 1000 | 800 | 770 | 650 | V/µs | Min | B |
| Rise/Fall Time | 0.2V Step | 2.3 | 2.6 | 2.7 | 3 | ns | Max | B |
| Settling Time: 0.05% | 1V Step | 12 | — | — | — | ns | Typ | C |
| Spurious Free Dynamic Range | f = 5MHz, $V_O$ = 2Vp-p | 64 | 60 | 56 | 51 | dB | Min | B |
| Input Noise: | | | | | | | | |
| Voltage Noise Density | f ≥ 1MHz | 6.3 | 7.2 | 7.8 | 8 | nV/√Hz | Max | B |
| Current Noise Density | f ≥ 1MHz | 2.0 | 2.5 | 2.9 | 3.6 | pA/√Hz | Max | B |
| **DC PERFORMANCE** | $V_{CM}$ = 2.5V | | | | | | | |
| Open Loop Voltage Gain ($A_{OL}$) | $V_O$ = ±0.5V | 54 | 48 | 46 | 45 | dB | Min | A |
| Input Offset Voltage | | ±2 | ±6 | ±7 | ±9 | mV | Max | A |
| Average Drift | | — | — | ±14 | ±14 | µV/°C | Max | B |
| Input Bias Current[3] | | +6 | ±12 | ±13 | ±20 | µA | Max | A |
| Average Drift | | — | — | −60 | −90 | nA/°C | Max | B |
| Input Offset Current | | ±0.3 | ±2 | ±3 | ±4 | µA | Max | A |
| Average Drift | | — | — | ±10 | ±10 | nA/°C | Max | B |

## SPECIFICATIONS— $V_S$ = +5V (CONT)

G = +2, $R_L$ = 500Ω tied to $V_{CM}$ = 2.5V, $R_F$ = 402Ω, $V_L$ = –1.2V, $V_H$ = +1.2V (Figure 2 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA688U, P TYP +25°C | OPA688U, P GUARANTEED[1] +25°C | 0°C to +70°C | –40°C to +85°C | UNITS | MIN/MAX | TEST LEVEL[2] |
|---|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | | |
| Common-Mode Rejection | Input Referred, $V_{CM}$ = ±0.5V | 55 | **48** | 47 | 45 | dB | Min | A |
| Common-Mode Input Range[4] | | $V_{CM}$ ±0.8 | **$V_{CM}$ ±0.7** | $V_{CM}$ ±0.7 | $V_{CM}$ ±0.6 | V | Min | A |
| Input Impedance | | | | | | | | |
| Differential-Mode | | 0.4 ll 1 | — | — | — | MΩ ll pF | Typ | C |
| Common-Mode | | 1 ll 1 | — | — | — | MΩ ll pF | Typ | C |
| **OUTPUT** | $V_H$ = $V_{CM}$ +1.8V, $V_L$ = = $V_{CM}$ –1.8V | | | | | | | |
| Output Voltage Range | $R_L$ ≥ 500Ω | $V_{CM}$ ±1.6 | **$V_{CM}$ ±1.4** | $V_{CM}$ ±1.4 | $V_{CM}$ ±1.3 | V | Min | A |
| Current Output, Sourcing | $V_O$ = 2.5V | 100 | **80** | 75 | 65 | mA | Min | A |
| Sinking | $V_O$ = 2.5V | –80 | **–65** | –60 | –50 | mA | Min | A |
| Closed-Loop Output Impedance | G = +1, $R_L$ = 25Ω, f < 100kHz | 0.2 | — | — | — | Ω | Typ | C |
| **POWER SUPPLY** | Single Supply Operation | | | | | | | |
| Operating Voltage, Specified | | +5 | — | — | — | V | Typ | C |
| Maximum | | — | **+12** | +12 | +12 | V | Max | A |
| Quiescent Current, Maximum | | 13 | **15** | 15 | 16 | mA | Max | A |
| Minimum | | 13 | **11** | 10 | 9 | mA | Min | A |
| Power Supply Rejection Ratio | $V_S$ = 4.5V to 5.5V | | | | | | | |
| +PSR (Input Referred) | | 65 | — | — | — | dB | Typ | C |
| **OUTPUT VOLTAGE LIMITERS** | | | | | | | | |
| Default Limiter Voltage | Limiter Pins Open | $V_{CM}$ ±0.9 | **$V_{CM}$ ±0.6** | $V_{CM}$ ±0.6 | $V_{CM}$ ±0.6 | V | Min | A |
| Minimum Limiter Separation ($V_H$ – $V_L$) | | 200 | 200 | 200 | 200 | mV | Min | B |
| Maximum Limit Voltage | | — | $V_{CM}$ ±1.8 | $V_{CM}$ ±1.8 | $V_{CM}$ ±1.8 | V | Max | B |
| Limiter Input Bias Current Magnitude[5] | $V_O$ = 2.5V | | | | | | | |
| Maximum | | 35 | **60** | 70 | 80 | µA | Max | A |
| Minimum | | 35 | **0** | 0 | 0 | µA | Min | A |
| Average Drift | | — | — | 30 | 50 | nA/°C | Max | B |
| Limiter Input Impedance | | 2 ll 1 | — | — | — | MΩ ll pF | Typ | C |
| Limiter Feedthrough[6] | f = 5MHz | –60 | — | — | — | dB | Typ | C |
| DC Performance in Limit Mode | $V_{IN}$ = $V_{CM}$ ±1.2V | | | | | | | |
| Limiter Voltage Accuracy | ($V_O$ – $V_H$) or ($V_O$ – $V_L$) | ±15 | **±35** | ±40 | ±40 | mV | Max | A |
| Op Amp Bias Current Shift[3] | | 5 | — | — | — | µA | Typ | C |
| AC Performance in Limit Mode | | | | | | | | |
| Limiter Small Signal Bandwidth | $V_{IN}$ = $V_{CM}$ ±1.2V, $V_O$ < 0.02Vp-p | 300 | — | — | — | MHz | Typ | C |
| Limiter Slew Rate[7] | | 20 | — | — | — | V/µs | Typ | C |
| Limited Step Response | | | | | | | | |
| Overshoot | $V_{IN}$ = $V_{CM}$ to $V_{CM}$ ±1.2V Step | 55 | — | — | — | mV | Typ | C |
| Recovery Time | $V_{IN}$ = $V_{CM}$ ±1.2V to $V_{CM}$ Step | 2.4 | 2.9 | 3.7 | 4.1 | ns | Max | B |
| Linearity Guardband[8] | f = 5MHz, $V_O$ = 2Vp-p | 30 | — | — | — | mV | Max | C |
| **THERMAL CHARACTERISTICS** | | | | | | | | |
| Temperature Range | Specification: P, U | –40 to +85 | — | — | — | °C | Typ | C |
| Thermal Resistance | Junction-to-Ambient | | | | | | | |
| P 8-Pin DIP | | 100 | — | — | — | °C/W | Typ | C |
| U 8-Pin SO-8 | | 125 | — | — | — | °C/W | Typ | C |

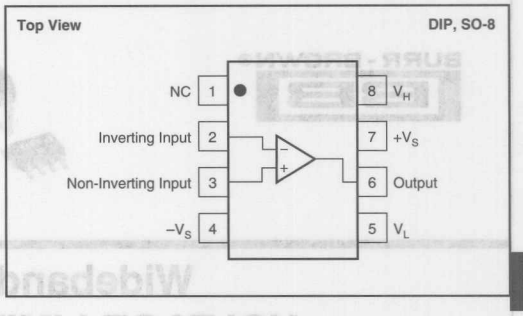
NOTES: (1) Junction Temperature = Ambient Temperature for low temperature limit and 25°C guaranteed specifications. Junction Temperature = Ambient Temperature + 23°C at high temperature limit guaranteed specifications. (2) TEST LEVELS: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value for information only. (3) Current is considered positive out of node. (4) CMIR tested as < 3dB degradation from minimum CMRR at specified limits. (5) $I_{VH}$ ($V_H$ bias current) is negative, and $I_{VL}$ ($V_L$ bias current) is positive, under these conditions. See Figures 2 and 7. (6) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to $V_H$ (or $V_L$) when $V_{IN}$ = 0. (7) $V_H$ slew rate conditions are: $V_{IN}$ = $V_{CM}$ +0.4V, G = +2, $V_L$ = $V_{CM}$ –1.2V, $V_H$ = step between $V_{CM}$ + 1.2V and $V_{CM}$. $V_L$ slew rate conditions are similar. (8) Linearity Guardband is defined for an output sinusoid (f = 5MHz, $V_O$ = $V_{CM}$ ±1Vp-p) centered between the limiter levels ($V_H$ and $V_L$). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB (see Figure 8).

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±6.5V |
| Internal Power Dissipation | See Thermal Characteristics |
| Common-Mode Input Voltage | $\pm V_S$ |
| Differential Input Voltage | $\pm V_S$ |
| Limiter Voltage Range | $\pm(V_S - 0.7V)$ |
| Storage Temperature Range: P, U | –40°C to +125°C |
| Lead Temperature (DIP, soldering, 10s) | +300°C |
| (SO-8, soldering, 3s) | +260°C |
| Junction Temperature | +175°C |

## PIN CONFIGURATION

Top View DIP, SO-8




## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

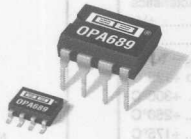
## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER |
|---|---|---|---|---|---|
| OPA688P | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA688P | OPA688P |
| OPA688U | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA688U | OPA688U |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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# OPA689

www.burr-brown.com/databook/OPA689.html

# Wideband, High Gain VOLTAGE LIMITING AMPLIFIER

## FEATURES

- HIGH LINEARITY NEAR LIMITING
- FAST RECOVERY FROM OVERDRIVE: 2.4ns
- LIMITING VOLTAGE ACCURACY: ±15mV
- –3dB BANDWIDTH (G = +6): 280MHz
- STABLE FOR G ≥ +4
- SLEW RATE: 1600V/µs
- ±5V AND +5V SUPPLY OPERATION
- LOW GAIN VERSION: OPA688

## APPLICATIONS

- TRANSIMPEDANCE WITH FAST OVERDRIVE RECOVERY
- FAST LIMITING ADC INPUT DRIVER
- LOW PROP DELAY COMPARATOR
- NON-LINEAR ANALOG SIGNAL PROCESSING
- DIFFERENCE AMPLIFIER
- IF LIMITING AMPLIFIER
- AM SIGNAL GENERATION

## DESCRIPTION

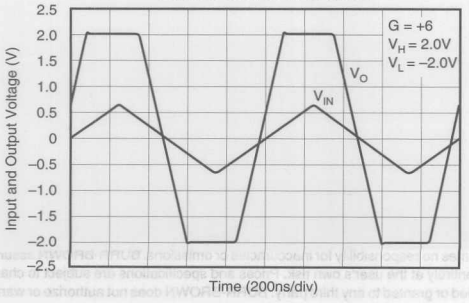
The OPA689 is a wideband, voltage feedback op amp that offers bipolar output voltage limiting, and is stable for gains ≥ +4. Two buffered limiting voltages take control of the output when it attempts to drive beyond these limits. This new output limiting architecture holds the limiter offset error to ±15mV. The op amp operates linearly to within 30mV of the limits.

The combination of narrow nonlinear range and low limiting offset allows the limiting voltages to be set within 100mV of the desired linear output range. A fast 2.4ns recovery from limiting ensures that overdrive signals will be transparent to the signal channel. Implementing the limiting function at the output, as opposed to the input, gives the specified limiting accuracy for any gain, and allows the OPA689 to be used in all standard op amp applications.

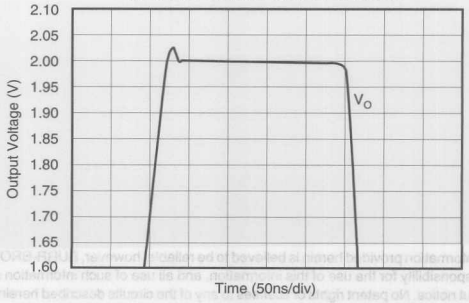
Non-linear analog signal processing circuits will benefit from the OPA689's sharp transition from linear operation to output limiting. The quick recovery time supports high speed applications.

The OPA689 is available in an industry-standard pinout in 8-pin PDIP and SO-8 packages. For lower gain applications requiring output limiting with fast recovery, consider the OPA688.

LIMITED OUTPUT RESPONSE




DETAIL OF LIMITED OUTPUT VOLTAGE




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS — $V_S$ = ±5V

G = +6, $R_L$ = 500Ω, $R_F$ = 750Ω, $V_H$ = $-V_L$ = 2V, (Figure 1 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA689U, P TYP +25°C | GUARANTEED[1] +25°C | 0°C to +70°C | −40°C to +85°C | UNITS | MIN/ MAX | TEST LEVEL[2] |
|---|---|---|---|---|---|---|---|---|
| **AC PERFORMANCE (see Fig. 1)** | | | | | | | | |
| Small Signal Bandwidth | $V_O$ < 0.5Vp-p | | | | | | | |
| | G = +6 | 280 | 220 | 210 | 200 | MHz | Min | B |
| | G = +12 | 90 | — | — | — | MHz | Typ | C |
| | G = −6 | 220 | — | — | — | MHz | Typ | C |
| Gain Bandwidth Product (G ≥ +20) | $V_O$ < 0.5Vp-p | 720 | 490 | 460 | 430 | MHz | Min | B |
| Gain Peaking | $V_O$ < 0.5Vp-p, G = +4 | 8 | — | — | — | dB | Typ | C |
| 0.1dB Gain Flatness Bandwidth | $V_O$ < 0.5Vp-p | 110 | — | — | — | MHz | Typ | C |
| Large Signal Bandwidth | $V_O$ = 2Vp-p | 290 | 185 | 175 | 170 | MHz | Min | B |
| Step Response: | | | | | | | | |
| Slew Rate | 2V Step | 1600 | 1300 | 1250 | 950 | V/µs | Min | B |
| Rise/Fall Time | 0.5V Step | 1.2 | 1.8 | 1.9 | 2.4 | ns | Max | B |
| Settling Time: 0.05% | 2V Step | 7 | — | — | — | ns | Typ | C |
| Spurious Free Dynamic Range | f = 5MHz, $V_O$ = 2Vp-p | 61 | 57 | 53 | 48 | dB | Min | B |
| Differential Gain | NTSC, PAL, $R_L$ = 500Ω | 0.02 | — | — | — | % | Typ | C |
| Differential Phase | NTSC, PAL, $R_L$ = 500Ω | 0.01 | — | — | — | ° | Typ | C |
| Input Noise Density: | | | | | | | | |
| Voltage Noise | f ≥ 1MHz | 4.6 | 5.3 | 6.0 | 6.1 | nV/√Hz | Max | B |
| Current Noise | f ≥ 1MHz | 2.0 | 2.5 | 2.9 | 3.6 | pA/√Hz | Max | B |
| **DC PERFORMANCE ($V_{CM}$ = 0V)** | | | | | | | | |
| Open-Loop Voltage Gain ($A_{OL}$) | $V_O$ = ±0.5V | 58 | 52 | 50 | 49 | dB | Min | A |
| Input Offset Voltage | | ±1 | ±5 | ±6 | ±7 | mV | Max | A |
| Average Drift | | — | — | ±14 | ±14 | µV/°C | Max | B |
| Input Bias Current[3] | | +8 | ±12 | ±13 | ±20 | µA | Max | A |
| Average Drift | | — | — | −60 | −90 | nA/°C | Max | B |
| Input Offset Current | | ±0.3 | ±2 | ±3 | ±4 | µA | Max | A |
| Average Drift | | — | — | ±10 | ±10 | nA/°C | Max | B |
| **INPUT** | | | | | | | | |
| Common-Mode Rejection Ratio | Input Referred, $V_{CM}$ = ±0.5V | 60 | 53 | 52 | 50 | dB | Min | A |
| Common-Mode Input Range[4] | | ±3.3 | ±3.2 | ±3.2 | ±3.1 | V | Min | B |
| Input Impedance | | | | | | | | |
| Differential-Mode | | 0.4 ‖ 1 | — | — | — | MΩ ‖ pF | Typ | C |
| Common-Mode | | 1 ‖ 1 | — | — | — | MΩ ‖ pF | Typ | C |
| **OUTPUT** | $V_H$ = $-V_L$ = 4.3V | | | | | | | |
| Output Voltage Range | $R_L$ ≥ 500Ω | ±4.1 | ±3.9 | ±3.9 | ±3.8 | V | Min | A |
| Current Output, Sourcing | | 140 | 125 | 115 | 100 | mA | Min | A |
| Sinking | | −100 | −85 | −80 | −70 | mA | Min | A |
| Closed-Loop Output Impedance | G = +4, f < 100kHz | 0.8 | — | — | — | Ω | Typ | C |
| **POWER SUPPLY** | | | | | | | | |
| Operating Voltage, Specified | | ±5 | — | — | — | V | Typ | C |
| Maximum | | — | ±6 | ±6 | ±6 | V | Max | A |
| Quiescent Current, Maximum | | 15.8 | 17 | 19 | 20 | mA | Max | A |
| Minimum | | 15.8 | 14 | 12.8 | 11 | mA | Min | A |
| Power Supply Rejection Ratio | $+V_S$ = 4.5V to 5.5V | | | | | | | |
| +PSR (Input Referred) | | 65 | 58 | 57 | 55 | dB | Min | A |
| **OUTPUT VOLTAGE LIMITERS** | | | | | | | | |
| Default Limit Voltage | Limiter Pins Open | ±3.3 | ±3.2 | ±3.1 | ±3.0 | V | Min | A |
| Minimum Limiter Separation ($V_H$ − $V_L$) | | 200 | 200 | 200 | 200 | mV | Min | B |
| Maximum Limit Voltage | | — | ±4.3 | ±4.3 | ±4.3 | V | Max | B |
| Limiter Input Bias Current Magnitude[5] | $V_O$ = 0 | | | | | | | |
| Maximum | | 53 | 61 | 64 | 66 | µA | Max | A |
| Minimum | | 53 | 44 | 43 | 41 | µA | Min | A |
| Average Drift | | — | — | 40 | 45 | nA/°C | Max | B |
| Limiter Input Impedance | | 2 ‖ 1 | — | — | — | MΩ ‖ pF | Typ | C |
| Limiter Feedthrough[6] | f = 5MHz | −60 | — | — | — | dB | Typ | C |
| DC Performance in Limit Mode | $V_{IN}$ = ±0.7V | | | | | | | |
| Limiter Offset Voltage | ($V_O$ − $V_H$) or ($V_O$ − $V_L$) | ±15 | ±35 | ±40 | ±40 | mV | Max | A |
| Op Amp Input Bias Current Shift[3] | | 3 | — | — | — | µA | Typ | C |

## SPECIFICATIONS — $V_S$ = ±5V (CONT)

G = +6, $R_L$ = 500Ω, $R_F$ = 750Ω, $V_H$ = $-V_L$ = 2V, (Figure 1 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA689U, P | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | TYP | GUARANTEED[1] | | | | | |
| | | +25°C | +25°C | 0°C to +70°C | −40°C to +85°C | UNITS | MIN/ MAX | TEST LEVEL[2] |
| **OUTPUT VOLTAGE LIMITERS (CONT)** | | | | | | | | |
| AC Performance in Limit Mode | | | | | | | | |
| Limiter Small Signal Bandwidth | $V_{IN}$ = ±0.7V, $V_O$ < 0.02Vp-p | 450 | — | — | — | MHz | Typ | C |
| Limiter Slew Rate[7] | | 100 | — | — | — | V/µs | Typ | C |
| Limited Step Response | | | | | | | | |
| Overshoot | $V_{IN}$ = 0 to ±0.7V Step | 250 | — | — | — | mV | Typ | C |
| Recovery Time | $V_{IN}$ = ±0.7V to 0 Step | 2.4 | 2.8 | 3.0 | 3.2 | ns | Max | B |
| Linearity Guardband[8] | f = 5MHz, $V_O$ = 2Vp-p | 30 | — | — | — | mV | Typ | C |
| **THERMAL CHARACTERISTICS** | | | | | | | | |
| Temperature Range | Specification: P, U | −40 to +85 | — | — | — | °C | Typ | C |
| Thermal Resistance | | | | | | | | |
| P 8-Pin DIP | | 100 | — | — | — | °C/W | Typ | C |
| U 8-Pin SO-8 | | 125 | — | — | — | °C/W | Typ | C |

NOTES: (1) Junction Temperature = Ambient Temperature for low temperature limit and 25°C guaranteed specifications. Junction Temperature = Ambient Temperature + 23°C at high temperature limit guaranteed specifications. (2) TEST LEVELS: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value for information only. (3) Current is considered positive out of node. (4) CMIR tested as < 3dB degradation from minimum CMRR at specified limits. (5) $I_{VH}$ ($V_H$ bias current) is positive, and $I_{VL}$ ($V_L$ bias current) is negative, under these conditions. See Figures 1 and 7. (6) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to $V_H$ (or $V_L$) when $V_{IN}$ = 0. (7) $V_H$ slew rate conditions are: $V_{IN}$ = +0.7V, G = +6, $V_L$ = −2V, $V_H$ = step between 2V and 0V. $V_L$ slew rate conditions are similar. (8) Linearity Guardband is defined for an output sinusoid (f = 1MHz, $V_O$ = 2Vpp) centered between the limiter levels ($V_H$ and $V_L$). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB (see Figure 8).

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# SPECIFICATIONS — $V_S$ = +5V

G = +6, $R_F$ = 750Ω, $R_L$ = 500Ω tied to $V_{CM}$ = 2.5V, $V_L = V_{CM} - 1.2V$, $V_H = V_{CM} + 1.2V$, (Figure 2 for AC performance only), unless otherwise noted.

| | | OPA689U, P | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | TYP | GUARANTEED[1] | | | | | |
| PARAMETER | CONDITIONS | +25°C | +25°C | 0°C to +70°C | −40°C to +85°C | UNITS | MIN/ MAX | TEST LEVEL[2] |
| **AC PERFORMANCE (see Fig. 2)** | | | | | | | | |
| Small Signal Bandwidth | $V_O$ < 0.5Vp-p | | | | | | | |
| | G = +6 | 210 | 180 | 160 | 150 | MHz | Min | B |
| | G = +12 | 70 | — | — | — | MHz | Typ | C |
| | G = −6 | 180 | — | — | — | MHz | Typ | C |
| Gain Bandwidth Product (G ≥ +20) | $V_O$ < 0.5Vp-p | 440 | 330 | 310 | 300 | MHz | Min | B |
| Gain Peaking | $V_O$ < 0.5Vp-p, G = +4 | 4 | — | — | — | dB | Typ | B |
| 0.1dB Gain Flatness Bandwidth | $V_O$ < 0.5Vp-p | 35 | — | — | — | MHz | Typ | C |
| Large Signal Bandwidth | $V_O$ = 2Vp-p | 175 | 150 | 140 | 125 | MHz | Min | B |
| Step Response: | | | | | | | | |
| Slew Rate | 2V Step | 1600 | 1300 | 1250 | 950 | V/µs | Min | B |
| Rise/Fall Time | 0.5V Step | 1.9 | 2.1 | 2.2 | 2.6 | ns | Max | B |
| Settling Time: 0.05% | 2V Step | 7 | — | — | — | ns | Typ | C |
| Spurious Free Dynamic Range | f = 5MHz, $V_O$ = 2Vp-p | 59 | 55 | 51 | 46 | dB | Min | B |
| Input Noise: | | | | | | | | |
| Voltage Noise Density | f ≥ 1MHz | 4.6 | 5.3 | 6.0 | 6.1 | nV/√Hz | Max | B |
| Current Noise Density | f ≥ 1MHz | 2.0 | 2.5 | 2.9 | 3.6 | pA/√Hz | Max | B |
| **DC PERFORMANCE** | | | | | | | | |
| Open-Loop Voltage Gain ($A_{OL}$) | $V_O$ = ±0.5V | 58 | **52** | 50 | 49 | dB | Min | A |
| Input Offset Voltage | | ±1 | **±5** | ±6 | ±8 | mV | Max | A |
| Average Drift | | — | — | ±14 | ±14 | µV/°C | Max | B |
| Input Bias Current[3] | | +8 | **±12** | ±13 | ±20 | µA | Max | A |
| Average Drift | | — | — | −60 | −90 | nA/°C | Max | B |
| Input Offset Current | | ±0.3 | **±2** | ±3 | ±4 | µA | Max | A |
| Average Drift | | — | — | ±10 | ±10 | nA/°C | Max | B |
| **INPUT** | | | | | | | | |
| Common-Mode Rejection Ratio | Input Referred, $V_{CM}$ ±0.5V | 58 | **51** | 50 | 48 | dB | Min | A |
| Common-Mode Input Range[4] | | $V_{CM}$ ±0.8 | $V_{CM}$ ±0.7 | $V_{CM}$ ±0.7 | $V_{CM}$ ±0.6 | V | Min | B |
| Input Impedance | | | | | | | | |
| Differential-Mode | | 0.4 ‖ 1 | — | — | — | MΩ ‖ pF | Typ | C |
| Common-Mode | | 1 ‖ 1 | — | — | — | MΩ ‖ pF | Typ | C |
| **OUTPUT** | $V_H = V_{CM} + 1.8V$, $V_L = V_{CM} - 1.8V$ | | | | | | | |
| Output Voltage Range | $R_L$ ≥ 500Ω | $V_{CM}$ ±1.6 | **$V_{CM}$ ±1.4** | $V_{CM}$ ±1.4 | $V_{CM}$ ±1.3 | V | Min | A |
| Current Output, Sourcing | | 100 | **80** | 75 | 65 | mA | Min | A |
| Sinking | | −80 | **−65** | −60 | −50 | mA | Min | A |
| Closed-Loop Output Impedance | G = +4, f < 100kHz | 0.8 | — | — | — | Ω | Typ | C |
| **POWER SUPPLY** | | | | | | | | |
| Operating Voltage, Specified | | 5 | — | — | — | V | Typ | C |
| Maximum | | — | 12 | 12 | 12 | V | Max | C |
| Quiescent Current, Maximum | | 13 | **15** | 15 | 16 | mA | Max | A |
| Minimum | | 13 | **11** | 10 | 9 | mA | Min | A |
| Power Supply Rejection Ratio | $V_S$ = 4.5V to 5.5V | | | | | | | |
| +PSR (Input Referred) | | 65 | — | — | — | dB | Typ | C |
| **OUTPUT VOLTAGE LIMITERS** | | | | | | | | |
| Default Limiter Voltage | Limiter Pins Open | $V_{CM}$ ±0.9 | **$V_{CM}$ ±0.6** | $V_{CM}$ ±0.6 | $V_{CM}$ ±0.6 | V | Min | A |
| Minimum Limiter Separation ($V_H - V_L$) | | 200 | 200 | 200 | 200 | mV | Min | B |
| Maximum Limit Voltage | | — | $V_{CM}$ ±1.8 | $V_{CM}$ ±1.8 | $V_{CM}$ ±1.8 | V | Max | B |
| Limiter Input Bias Current Magnitude[5] | $V_O$ = 2.5V | | | | | | | |
| Maximum | | 35 | **60** | 70 | 80 | µA | Max | A |
| Minimum | | 35 | **0** | 0 | 0 | µA | Min | A |
| Average Drift | | — | — | 30 | 50 | nA/°C | Max | B |
| Limiter Input Impedance | | 2 ‖ 1 | — | — | — | MΩ ‖ pF | Typ | C |
| Limiter Isolation[6] | f = 5MHz | −60 | — | — | — | dB | Typ | C |
| DC Performance in Limit Mode | $V_{IN} = V_{CM}$ ±0.4V | | | | | | | |
| Limiter Voltage Accuracy | $(V_O - V_H)$ or $(V_O - V_L)$ | ±15 | **±35** | ±40 | ±40 | mV | Max | A |
| Op Amp Bias Current Shift[3] | | 5 | — | — | — | µA | Typ | C |
| AC Performance in Limit Mode | | | | | | | | |
| Limiter Small Signal Bandwidth | $V_{IN}$ = ±0.4V, $V_O$ < 0.02Vp-p | 300 | — | — | — | MHz | Typ | C |
| Limiter Slew Rate[7] | | 20 | — | — | — | V/µs | Typ | C |
| Limited Step Response | | | | | | | | |
| Overshoot | $V_{IN} = V_{CM}$ to $V_{CM}$ ±0.4V Step | 55 | — | — | — | mV | Typ | C |
| Recovery Time | $V_{IN} = V_{CM}$ ±0.4V to $V_{CM}$ Step | 2.4 | 2.9 | 3.7 | 4.1 | ns | Max | B |
| Linearity Guardband[8] | f = 5MHz, $V_O$ = 2Vp-p | 30 | — | — | — | mV | Typ | C |

## SPECIFICATIONS — $V_S$ = +5V (CONT)

G = +6, $R_F$ = 750Ω, $R_L$ = 500Ω tied to $V_{CM}$ = 2.5V, $V_L$ = $V_{CM}$ −1.2V, $V_H$ = $V_{CM}$ +1.2V, (Figure 2 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA689U, P | | | | | | TEST LEVEL(2) |
|---|---|---|---|---|---|---|---|---|
| | | TYP | GUARANTEED(1) | | | | | |
| | | +25°C | +25°C | 0°C to +70°C | −40°C to +85°C | UNITS | MIN/ MAX | |
| **THERMAL CHARACTERISTICS** | | | | | | | | |
| Temperature Range | Specification: P, U | −40 to +85 | — | — | — | °C | Typ | C |
| Thermal Resistance | | | | | | | | |
| P 8-Pin DIP | | 100 | — | — | — | °C/W | Typ | C |
| U 8-Pin SO-8 | | 125 | — | — | — | °C/W | Typ | C |

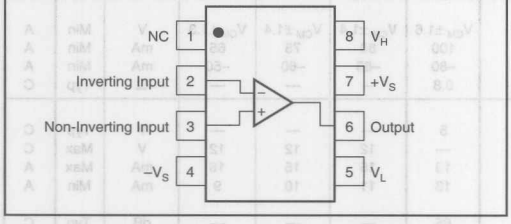
NOTES: (1) Junction Temperature = Ambient Temperature for low temperature limit and 25°C guaranteed specifications. Junction Temperature = Ambient Temperature + 23°C at high temperature limit guaranteed specifications. (2) TEST LEVELS: (A) 100% tested at 25°C, Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value for information only. (3) Current is considered positive out of node. (4) CMIR tested as < 3dB degradation from minimum CMRR at specified limits. (5) $I_{VH}$ ($V_H$ bias current) is negative, and $I_{VL}$ ($V_L$ bias current) is positive, under these conditions. See Figures 2 and 7. (6) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to $V_H$ (or $V_L$) when $V_{IN}$ = 0. (7) $V_H$ slew rate conditions are: $V_{IN}$ = $V_{CM}$ +0.4V, G = +6, $V_L$ = $V_{CM}$ −1.2V, $V_H$ = step between $V_{CM}$ +1.2V and $V_{CM}$. $V_L$ slew rate conditions are similar. (8) Linearity Guardband is defined for an output sinusoid (f = 5MHz, $V_O$ = $V_{CM}$ ±1Vp-p) centered between the limiter levels ($V_H$ and $V_L$). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB (see Figure 8).

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±6.5V |
| Internal Power Dissipation | See Thermal Characteristics |
| Input Voltage Range | ±$V_S$ |
| Differential Input Voltage | ±$V_S$ |
| Limiter Voltage Range | ±($V_S$ − 0.7V) |
| Storage Temperature Range: P, U | −40°C to +125°C |
| Lead Temperature (DIP, soldering, 10s) | +300°C |
| (SO-8, soldering, 3s) | +260°C |
| Junction Temperature | +175°C |

### ABSOLUTE MAXIMUM RATINGS

Top View — DIP, SO-8




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

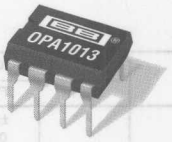
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER |
|---|---|---|---|---|---|
| OPA689P | 8-Pin Plastic DIP | 006 | −40°C to +85°C | OPA689P | OPA689P |
| OPA689U | SO-8 Surface Mount | 182 | −40°C to +85°C | OPA689U | OPA689U |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR-BROWN®




# OPA1013

www.burr-brown.com/databook/OPA1013.html

# Precision, Single-Supply DUAL OPERATIONAL AMPLIFIER

## FEATURES

- SINGLE POWER SUPPLY OPERATION
- INPUT VOLTAGE RANGE TO GROUND
- OUTPUT SWINGS NEAR GROUND
- LOW QUIESCENT CURRENT: 550µA max
- LOW $V_{os}$: 300µV max
- LOW DRIFT: 2.5µV/°C max
- LOW $I_{os}$: 1.5nA max
- LOW NOISE: 0.55µVp-p, 0.1Hz to 10Hz

## APPLICATIONS

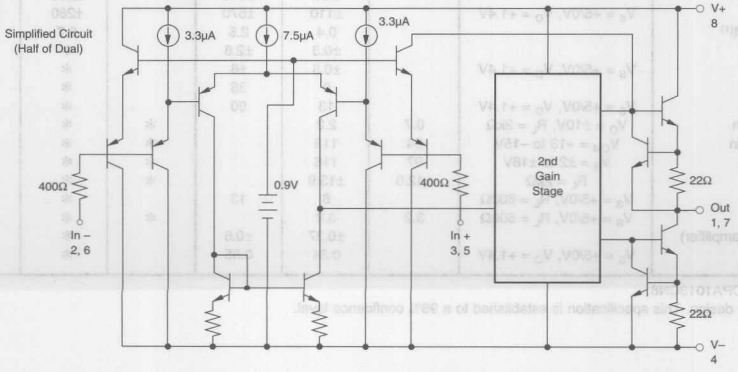
- PRECISION INSTRUMENTATION
- BATTERY-POWERED EQUIPMENT
- BRIDGE AMPLIFIERS
- 4-20mA CURRENT TRANSMITTERS
- VOLTAGE COMPARATOR

## DESCRIPTION

The OPA1013 dual operational amplifier provides precision performance in single power supply and low power applications. It is laser trimmed for low offset voltage and drift, greatly reducing the large errors common with LM324-type op amps. Input offset current is also trimmed to reduce errors in high impedance applications.

The OPA1013 is characterized for operation at both +5V (single supply) and ±15V power supplies. When operated from a single supply, the input common-mode range includes ground and the output can swing to within 15mV of ground. Completely independent biasing networks eliminate interaction between the two amplifiers—even when one is used as a comparator.

The OPA1013 is available in an 8-pin plastic DIP specified for the 0°C to +70°C temperature range.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $V_S$ = ±15V, $V_{CM}$ = 0V, $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITION | OPA1013CN8 MIN | OPA1013CN8 TYP | OPA1013CN8 MAX | OPA1013DN8 MIN | OPA1013DN8 TYP | OPA1013DN8 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | | | ±50 | ±300 | | ±200 | ±800 | µV |
| Time Stability | | | 0.5 | | | * | | µV/Mo |
| Input Offset Current | | | ±0.08 | ±1.5 | | * | * | nA |
| Input Bias Current | | | 7 | 30 | | * | * | nA |
| Voltage Noise, BW = 0.1 to 10Hz | | | 0.55 | | | * | | µVp-p |
| Noise Density, f = 10Hz | | | 28 | | | * | | nV/√Hz |
| f = 1kHz | | | 25 | | | * | | nV/√Hz |
| Current Noise Density, f = 10Hz | | | 0.12 | | | * | | pA/√Hz |
| Input Resistance: Differential | | 70 | 300 | | * | * | | MΩ |
| Input Resistance: Common-Mode | | | 4 | | | * | | GΩ |
| Open-Loop Voltage Gain | $V_O$ = ±10V, $R_L$ = 2kΩ | 1.2 | 2.9 | | * | * | | V/µV |
| | $V_O$ = ±10V, $R_L$ = 600Ω | 0.5 | 1.9 | | * | * | | V/µV |
| Common-Mode Input Range | | +13.5 | +13.8 | | * | * | | V |
| | | −15 | −15.3 | | * | * | | V |
| Common-Mode Rejection | $V_{CM}$ = +13.5 to −15V | 97 | 114 | | * | * | | dB |
| Power Supply Rejection | $V_S$ = ±2 to ±18V | 100 | 117 | | * | * | | dB |
| Channel Separation | $V_O$ = ±10V, $R_L$ = 2kΩ | 120 | 137 | | * | * | | dB |
| Voltage Output | $R_L$ = 2kΩ | ±12.5 | ±14 | | * | * | | V |
| Slew Rate | | 0.2 | 0.35 | | * | * | | V/µs |
| Quiescent Current (per amplifier) | | | ±0.35 | ±0.55 | | * | * | mA |

* Specification same as OPA1013CN8.

At $V_S$ = +5V/0V, $V_{CM}$ = 0V, $V_O$ = +1.4V, $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITION | OPA1013CN8 MIN | OPA1013CN8 TYP | OPA1013CN8 MAX | OPA1013DN8 MIN | OPA1013DN8 TYP | OPA1013DN8 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | | | ±90 | ±450 | | ±250 | ±950 | µV |
| Input Offset Current | | | ±3.0 | ±2.0 | | * | * | nA |
| Input Bias Current | | | 10 | 50 | | * | * | nA |
| Open-Loop Voltage Gain | $V_O$ = 5mV to 4V, $R_L$ = 500Ω | | 0.1 | | | * | | V/µV |
| Common-Mode Input Range | | +3.5 | +3.8 | | * | * | | V |
| | | 0 | −0.3 | | * | * | | V |
| Voltage Output Low | No Load | | 15 | 25 | | * | * | mV |
| Low | $R_L$ = 600Ω to Ground | | 5 | 10 | | * | * | mV |
| Low | $I_{SINK}$ = 1mA | | 200 | 350 | | * | * | mV |
| High | No Load | 4 | 4.4 | | * | * | | V |
| High | $R_L$ = 600Ω to Ground | 3.4 | 4 | | * | * | | V |
| Quiescent Current (per amplifier) | | | 0.33 | 0.5 | | * | * | mA |

* Specification same as OPA1013CN8.

At $T_A$ = 0°C to +70°C, $V_S$ = ±15V, $V_{CM}$ = 0V, unless otherwise noted.

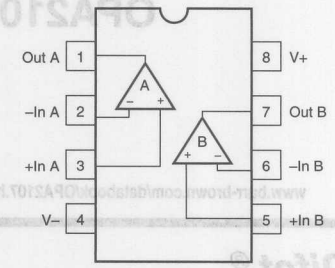
| PARAMETER | CONDITION | OPA1013CN8 MIN | OPA1013CN8 TYP | OPA1013CN8 MAX | OPA1013DN8 MIN | OPA1013DN8 TYP | OPA1013DN8 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | | | ±80 | ±400 | | ±230 | ±1000 | µV |
| | $V_S$ = +5/0V, $V_O$ = +1.4V | | ±110 | ±570 | | ±280 | ±1200 | µV |
| Input Offset Voltage Drift[1] | | | 0.4 | 2.5 | | 0.7 | 5 | µV/°C |
| Input Offset Current | | | ±0.3 | ±2.8 | | * | * | nA |
| | $V_S$ = +5/0V, $V_O$ = +1.4V | | ±0.5 | ±6 | | * | * | nA |
| Input Bias Current | | | 9 | 38 | | * | * | nA |
| | $V_S$ = +5/0V, $V_O$ = +1.4V | | 13 | 90 | | * | * | nA |
| Open-Loop Voltage Gain | $V_O$ = ±10V, $R_L$ = 2kΩ | 0.7 | 2.2 | | * | * | | V/µV |
| Common-Mode Rejection | $V_{CM}$ = +13 to −15V | 94 | 113 | | * | * | | dB |
| Power Supply Rejection | $V_S$ = ±2 to ±18V | 97 | 116 | | * | * | | dB |
| Voltage Output | $R_L$ = 2kΩ | ±12.0 | ±13.9 | | * | * | | V |
| $V_O$ Low | $V_S$ = +5/0V, $R_L$ = 600Ω | | 6 | 13 | | * | * | mV |
| $V_O$ High | $V_S$ = +5/0V, $R_L$ = 600Ω | 3.2 | 3.9 | | * | * | | V |
| Quiescent Current (per amplifier) | | | ±0.37 | ±0.6 | | * | * | mA |
| | $V_S$ = +5/0V, $V_O$ = +1.4V | | 0.34 | 0.55 | | * | * | mA |

* Specification same as OPA1013CN8.

NOTE: (1) Guaranteed by design. This specification is established to a 98% confidence level.

## CONNECTION DIAGRAM

N8 — Plastic Package — Top View




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | ±22V |
| Differential Input Voltage | ±30V |
| Input Voltage | V+ to (V–) –5V |
| Output Short Circuit ($T_A$ = 25°C) | Continuous |
| Operating Temperature: | 0°C to +70°C |
| Storage Temperature | –65 to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

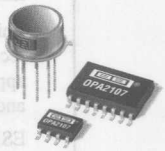
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| OPA1013CN8 | Plastic DIP | 006 | 0°C to +70°C |
| OPA1013DN8 | Plastic DIP | 006 | 0°C to +70°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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# OPA2107

www.burr-brown.com/databook/OPA2107.html

# Precision Dual *Difet* ® OPERATIONAL AMPLIFIER

## FEATURES

- VERY LOW NOISE: 8nV/√Hz at 10kHz
- LOW $V_{OS}$: 500µV max
- LOW DRIFT: 5µV/°C max
- LOW $I_B$: 5pA max
- FAST SETTLING TIME: 2µs to 0.01%
- UNITY-GAIN STABLE

## APPLICATIONS

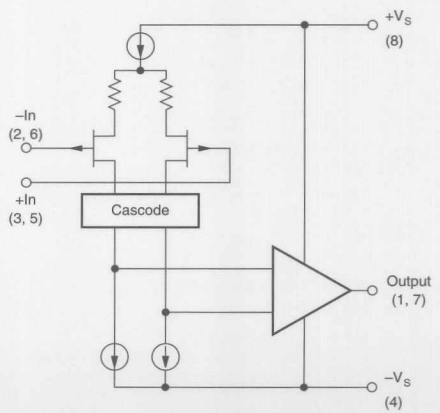
- DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- MEDICAL EQUIPMENT, CT SCANNERS

## DESCRIPTION

The OPA2107 dual operational amplifier provides precision ***Difet*** performance with the cost and space savings of a dual op amp. It is useful in a wide range of precision and low-noise analog circuitry and can be used to upgrade the performance of designs currently using BIFET® type amplifiers.

The OPA2107 is fabricated on a proprietary dielectrically isolated (***Difet***) process. This holds input bias currents to very low levels without sacrificing other important parameters, such as input offset voltage, drift and noise. Laser-trimmed input circuitry yields excellent DC performance. Superior dynamic performance is achieved, yet quiescent current is held to under 2.5mA per amplifier. The OPA2107 is unity-gain stable.

The OPA2107 is available in plastic DIP, metal TO-99, and SOIC packages. Industrial and Military temperature range versions are available.




*Difet*® Burr-Brown Corp.
BIFET® National Semiconductor

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# SPECIFICATIONS

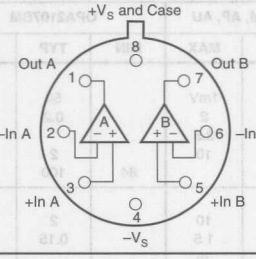
At $T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

| PARAMETER | CONDITION | OPA2107AM, SM, AP, AU | | | OPA2107BM | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OFFSET VOLTAGE**[1] | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0V | | 100 | 1mV | | 50 | 500 | µV |
| Over Specified Temperature | | | 0.5 | 2 | | 0.2 | 1 | mV |
| SM Grade | | | 0.8 | 2.5 | | | | mV |
| Average Drift Over Specified Temperature | | | 3 | 10 | | 2 | 5 | µV/°C |
| Power Supply Rejection | $V_S$ = ±10 to ±18V | 80 | 96 | | 84 | 100 | | dB |
| **INPUT BIAS CURRENT**[1] | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | 4 | 10 | | 2 | 5 | pA |
| Over Specified Temperature | | | 0.25 | 1.5 | | 0.15 | 1 | nA |
| SM Grade | | | 4 | 35 | | | | nA |
| Input Offset Current | $V_{CM}$ = 0V | | 1 | 8 | | 0.5 | 3 | pA |
| Over Specified Temperature | | | | 1 | | | 0.5 | nA |
| SM Grade | | | 1 | 28 | | | | nA |
| **INPUT NOISE** | | | | | | | | |
| Voltage: f = 10Hz | $R_S$ = 0 | | 30 | | | * | | nV/√Hz |
| f = 100Hz | | | 12 | | | * | | nV/√Hz |
| f = 1kHz | | | 9 | | | * | | nV/√Hz |
| f = 10kHz | | | 8 | | | * | | nV/√Hz |
| BW = 0.1 to 10Hz | | | 1.2 | | | * | | µVp-p |
| BW = 10 to 10kHz | | | 0.85 | | | * | | µVrms |
| Current: f = 0.1Hz thru 20kHz | | | 1.2 | | | 0.9 | | fA/√Hz |
| BW = 0.1Hz to 10Hz | | | 23 | | | 17 | | fAp-p |
| **INPUT IMPEDANCE** | | | | | | | | |
| Differential | | | $10^{13}$ \|\| 2 | | | * | | Ω \|\| pF |
| Common-Mode | | | $10^{14}$ \|\| 4 | | | * | | Ω \|\| pF |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | ±10.5 | ±11 | | * | * | | V |
| Over Specified Temperature | | ±10.2 | ±10.5 | | * | * | | V |
| SM Grade | | ±10 | ±10.3 | | | | | V |
| Common-Mode Rejection | $V_{CM}$ = ±10V | 80 | 94 | | 84 | 100 | | dB |
| **OPEN-LOOP GAIN** | | | | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±10V, $R_L$ = 2kΩ | 82 | 96 | | 84 | 100 | | dB |
| Over Specified Temperature | | 80 | 94 | | 82 | 96 | | dB |
| SM Grade | | 80 | 92 | | | | | dB |
| **DYNAMIC RESPONSE** | | | | | | | | |
| Slew Rate | G = +1 | 13 | 18 | | * | * | | V/µs |
| Settling Time: 0.1% | G = –1, 10V Step | | 1.5 | | | * | | µs |
| 0.01% | | | 2 | | | * | | µs |
| Gain-Bandwidth Product | G = 100 | | 4.5 | | | * | | MHz |
| THD + Noise | G = +1, f = 1kHz | | 0.001 | | | * | | % |
| Channel Separation | f = 100Hz, $R_L$ = 2kΩ | | 120 | | | * | | dB |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | | ±15 | | | * | | V |
| Operating Voltage Range | | ±4.5 | | ±18 | * | | * | V |
| Current | | | ±4.5 | ±5 | | * | * | mA |
| **OUTPUT** | | | | | | | | |
| Voltage Output | $R_L$ = 2kΩ | ±11 | ±12 | | * | * | | V |
| Over Specified Temperature | | ±10.5 | ±11.5 | | * | * | | V |
| SM Grade | | ±10.2 | ±11.3 | | | | | V |
| Short Circuit Current | | ±10 | ±40 | | * | * | | mA |
| Output Resistance, Open-Loop | 1MHz | | 70 | | | * | | Ω |
| Capacitive Load Stability | G = +1 | | 1000 | | | * | | pF |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | | | | | | | |
| AP, AU, AM, BM | | –25 | | +85 | * | | * | °C |
| SM | | –55 | | +125 | | | | °C |
| Operating | | | | | | | | |
| AP, AU | | –25 | | +85 | | | | °C |
| AM, BM, SM | | –55 | | +125 | * | | * | °C |
| Storage | | | | | | | | |
| AP, AU | | –40 | | +125 | | | | °C |
| AM, BM, SM | | –65 | | +150 | * | | * | °C |
| Thermal Resistance ($\theta_{J-A}$) | | | | | | | | |
| AP | | | 90 | | | | | °C/W |
| AU | | | 175 | | | | | °C/W |
| AM, BM, SM | | | 200 | | | * | | °C/W |

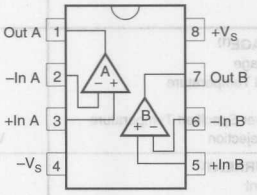
* Specifications same as OPA2107AM. NOTE: (1) Specified with devices fully warmed up.

## PIN CONFIGURATIONS

**Top View – M Package**




**Top View – P & U Packages**




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Input Voltage Range | ±$V_S$±2V |
| Differential Input Voltage | Total $V_S$±4V |
| Operating Temperature | |
| M Package | –55°C to +125°C |
| P and U Packages | –25°C to + 85°C |
| Storage Temperature | |
| M Package | –65°C to +150°C |
| P and U Packages | –40°C to +125°C |
| Output Short Circuit to Ground ($T_A$ = +25°C) | Continuous |
| Junction Temperature | +175°C |
| Lead Temperature | |
| M and P Packages (soldering, 10s) | +300°C |
| U Package, SOIC (3s) | +260°C |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| OPA2107AP | Plastic DIP | 006 | –25 to +85°C |
| OPA2107AM | Metal TO-99 | 001 | –25 to +85°C |
| OPA2107BM | Metal TO-99 | 001 | –25 to +85°C |
| OPA2107SM | Metal TO-99 | 001 | –55 to +125°C |
| OPA2107AU | SO-8 SOIC | 182 | –25 to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

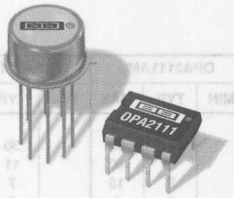
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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# OPA2111

www.burr-brown.com/databook/OPA2111.html

# Dual Low Noise Precision *Difet*® OPERATIONAL AMPLIFIER

## FEATURES

- LOW NOISE: 100% Tested, 8nV/√Hz max at 10kHz
- LOW BIAS CURRENT: 4pA max
- LOW OFFSET: 500μV max
- LOW DRIFT: 2.8μV/°C
- HIGH OPEN-LOOP GAIN: 114dB min
- HIGH COMMON-MODE REJECTION: 96dB min

## APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DETECTOR ARRAYS

## DESCRIPTION

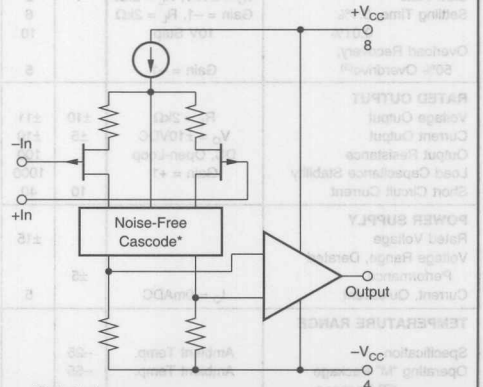
The OPA2111 is a high precision monolithic dielectrically isolated FET (***Difet***) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with patented circuit design techniques. A cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard dual op amp pin configuration allows upgrading of existing designs to higher performance levels.




OPA2111 Simplified Circuit
(Each Amplifier)

*BIFET® National Semiconductor Corp., **Difet®** Burr-Brown Corp.*

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

## ELECTRICAL

At $V_{CC}$ = ±15VDC and $T_A$ = +25°C, unless otherwise noted

| PARAMETER | CONDITION | OPA2111AM | | | OPA2111BM | | | OPA2111SM | | | OPA2111KM, KP | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT NOISE** | | | | | | | | | | | | | | |
| Voltage, $f_O$ = 10Hz | 100% Tested | | 40 | 80 | | 30 | 60 | | 40 | 80 | | 40 | | nV/√Hz |
| $f_O$ = 100Hz | 100% Tested | | 15 | 40 | | 11 | 30 | | 15 | 40 | | 15 | | nV/√Hz |
| $f_O$ = 1kHz | 100% Tested | | 8 | 15 | | 7 | 12 | | 8 | 15 | | 8 | | nV/√Hz |
| $f_O$ = 10kHz | (1) | | 6 | 8 | | 6 | 8 | | 6 | 8 | | 6 | | nV/√Hz |
| $f_B$ = 10Hz to 10kHz | (1) | | 0.7 | 1.2 | | 0.6 | 1 | | 0.7 | 1.2 | | 0.7 | | µVrms |
| $f_B$ = 0.1Hz to 10Hz | (1) | | 1.6 | 3.3 | | 1.2 | 2.5 | | 1.6 | 3.3 | | 1.6 | | µVp-p |
| Current, $f_B$ = 0.1Hz to 10Hz | (1) | | 15 | 24 | | 12 | 19 | | 15 | 24 | | 15 | | fAp-p |
| $f_O$ = 0.1Hz to 20kHz | (1) | | 0.8 | 1.3 | | 0.6 | 1 | | 0.8 | 1 | | 0.8 | | fA/√Hz |
| **OFFSET VOLTAGE**(2) | | | | | | | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0VDC | | ±0.1 | ±0.75 | | ±0.05 | ±0.5 | | ±0.1 | ±0.75 | | ±0.3 | ±2 | mV |
| Average Drift | $T_A = T_{MIN}$ to $T_{MAX}$ | | ±2 | ±6 | | ±0.5 | ±2.8 | | ±2 | ±6 | | ±8 | ±15 | µV/°C |
| Match | | | ±1 | | | ±0.5 | | | 2 | | | 2 | | µV/°C |
| Supply Rejection | | 90 | 110 | | 96 | 110 | | 90 | 110 | | 86 | 110 | | dB |
| | | | ±3 | ±31 | | ±3 | ±16 | | ±3 | ±31 | | ±3 | ±50 | µV/V |
| Channel Separation | 100Hz, $R_L$ = 2kΩ | | 136 | | | 136 | | | 136 | | | 136 | | dB |
| **BIAS CURRENT**(2) | | | | | | | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC | | ±2 | ±8 | | ±1.2 | ±4 | | ±2 | ±8 | | ±3 | ±15 | pA |
| Match | | | ±1 | | | ±0.5 | | | ±1 | | | 2 | | pA |
| **OFFSET CURRENT**(2) | | | | | | | | | | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC | | ±1.2 | ±6 | | ±0.6 | ±3 | | ±1.2 | ±6 | | ±3 | ±12 | pA |
| **IMPEDANCE** | | | | | | | | | | | | | | |
| Differential | | | $10^{13}$ \|\| 1 | | | $10^{13}$ \|\| 1 | | | $10^{13}$ \|\| 1 | | | $10^{13}$ \|\| 1 | | Ω \|\| pF |
| Common-Mode | | | $10^{14}$ \|\| 3 | | | $10^{14}$ \|\| 3 | | | $10^{14}$ \|\| 3 | | | $10^{14}$ \|\| 3 | | Ω \|\| pF |
| **VOLTAGE RANGE** | | | | | | | | | | | | | | |
| Common-Mode Input Range | | ±10 | ±11 | | ±10 | ±11 | | ±10 | ±11 | | ±10 | ±11 | | V |
| Common-Mode Rejection | $V_{IN}$ = ±10VDC | 90 | 110 | | 96 | 110 | | 90 | 110 | | 82 | 110 | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | | | | | | | |
| Open-Loop Voltage Gain | $R_L$ ≥ 2kΩ | 110 | 125 | | 114 | 125 | | 110 | 125 | | 106 | 125 | | dB |
| Match | | | 3 | | | 2 | | | 3 | | | 3 | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | | | | | | | |
| Unity Gain, Small Signal | | | 2 | | | 2 | | | 2 | | | 2 | | MHz |
| Full Power Response | 20Vp-p, $R_L$ = 2kΩ | 16 | 32 | | 16 | 32 | | 16 | 32 | | | 32 | | kHz |
| Slew Rate | $V_O$ = ±10V, $R_L$ = 2kΩ | 1 | 2 | | 1 | 2 | | 1 | 2 | | | 2 | | V/µs |
| Settling Time, 0.1% | Gain = –1, $R_L$ = 2kΩ | | 6 | | | 6 | | | 6 | | | 6 | | µs |
| 0.01% | 10V Step | | 10 | | | 10 | | | 10 | | | 10 | | µs |
| Overload Recovery, 50% Overdrive(3) | Gain = –1 | | 5 | | | 5 | | | 5 | | | 5 | | µs |
| **RATED OUTPUT** | | | | | | | | | | | | | | |
| Voltage Output | $R_L$ = 2kΩ | ±10 | ±11 | | ±10 | ±11 | | ±10 | ±11 | | ±10 | ±11 | | V |
| Current Output | $V_O$ = ±10VDC | ±5 | ±10 | | ±5 | ±10 | | ±5 | ±10 | | ±5 | ±10 | | mA |
| Output Resistance | DC, Open-Loop | | 100 | | | 100 | | | 100 | | | 100 | | Ω |
| Load Capacitance Stability | Gain = +1 | | 1000 | | | 1000 | | | 1000 | | | 1000 | | pF |
| Short Circuit Current | | 10 | 40 | | 10 | 40 | | 10 | 40 | | 10 | 40 | | mA |
| **POWER SUPPLY** | | | | | | | | | | | | | | |
| Rated Voltage | | | ±15 | | | ±15 | | | ±15 | | | ±15 | | VDC |
| Voltage Range, Derated Performance | | ±5 | | ±18 | ±5 | | ±18 | ±5 | | ±18 | ±5 | | ±18 | VDC |
| Current, Quiescent | $I_O$ = 0mADC | | 5 | 7 | | 5 | 7 | | 5 | 7 | | 5 | 9 | mA |
| **TEMPERATURE RANGE** | | | | | | | | | | | | | | |
| Specification | Ambient Temp. | –25 | | +85 | –25 | | +85 | –55 | | +125 | 0 | | +70 | °C |
| Operating "M" Package | Ambient Temp. | –55 | | +125 | –55 | | +125 | –55 | | +125 | –55 | | +125 | °C |
| "P" Package | | | | | | | | | | | –40 | | +85 | °C |
| Storage "M" Package | Ambient Temp. | –65 | | +150 | –65 | | +150 | –65 | | +150 | –65 | | +150 | °C |
| "P" Package | | | | | | | | | | | –40 | | +85 | °C |
| θ Junction-Ambient | | | 200 | | | 200 | | | 200 | | | 200(4) | | °C/W |

NOTES: (1) Sample tested—this parameter is guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) Typical $\theta_{J-A}$ = 150°C/W for plastic DIP.

## ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

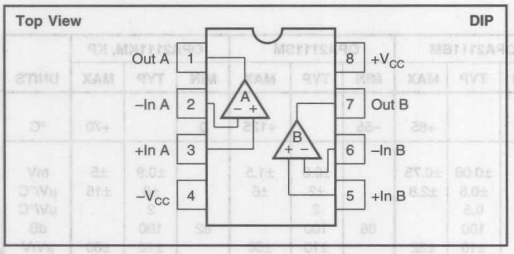
At $V_{CC}$ = ±15VDC and $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

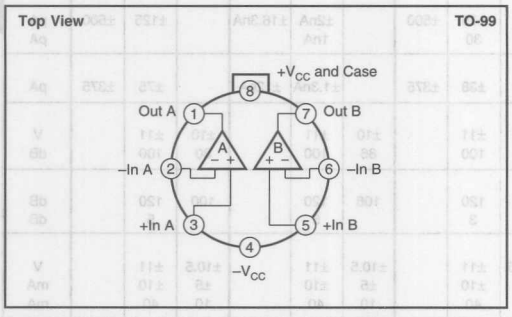
| PARAMETER | CONDITION | OPA2111AM | | | OPA2111BM | | | OPA2111SM | | | OPA2111KM, KP | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **TEMPERATURE RANGE** | | | | | | | | | | | | | | |
| Specification Range | Ambient Temp. | –25 | | +85 | –25 | | +85 | –55 | | +125 | 0 | | +70 | °C |
| **INPUT OFFSET VOLTAGE**(1) | | | | | | | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0VDC | | ±0.22 | ±1.2 | | ±0.08 | ±0.75 | | ±0.3 | ±1.5 | | ±0.9 | ±5 | mV |
| Average Drift | | | ±2 | ±6 | | ±0.5 | ±2.8 | | ±2 | ±6 | | ±8 | ±15 | µV/°C |
| Match | | | 1 | | | 0.5 | | | 2 | | | 2 | | µV/°C |
| Supply Rejection | | 86 | 100 | | 90 | 100 | | 86 | 100 | | 82 | 100 | | dB |
| | | | ±10 | ±50 | | ±10 | ±32 | | ±10 | ±50 | | ±10 | ±80 | µV/V |
| **BIAS CURRENT**(1) | | | | | | | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC | | ±125 | ±1nA | | ±75 | ±500 | | ±2nA | ±16.3nA | | ±125 | ±500 | pA |
| Match | | | 60 | | | 30 | | | 1nA | | | | | pA |
| **OFFSET CURRENT**(1) | | | | | | | | | | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC | | ±75 | ±750 | | ±38 | ±375 | | ±1.3nA | ±12nA | | ±75 | ±375 | pA |
| **VOLTAGE RANGE** | | | | | | | | | | | | | | |
| Common-Mode Input Range | | ±10 | ±11 | | ±10 | ±11 | | ±10 | ±11 | | ±10 | ±11 | | V |
| Common-Mode Rejection | $V_{IN}$ = ±10VDC | 86 | 100 | | 90 | 100 | | 86 | 100 | | 80 | 100 | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | | | | | | | |
| Open-Loop Voltage Gain | $R_L \geq 2k\Omega$ | 106 | 120 | | 110 | 120 | | 106 | 120 | | 100 | 120 | | dB |
| Match | | | 5 | | | 3 | | | 5 | | | 5 | | dB |
| **RATED OUTPUT** | | | | | | | | | | | | | | |
| Voltage Output | $R_L = 2k\Omega$ | ±10.5 | ±11 | | ±10.5 | ±11 | | ±10.5 | ±11 | | ±10.5 | ±11 | | V |
| Current Output | $V_O$ = ±10VDC | ±5 | ±10 | | ±5 | ±10 | | ±5 | ±10 | | ±5 | ±10 | | mA |
| Short Circuit Current | $V_O$ = 0VDC | 10 | 40 | | 10 | 40 | | 10 | 40 | | 10 | 40 | | mA |
| **POWER SUPPLY** | | | | | | | | | | | | | | |
| Current, Quiescent | $I_O$ = 0mADC | | 5 | 8 | | 5 | 8 | | 5 | 8 | | 5 | 10 | mA |

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

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## CONNECTION DIAGRAMS




## ELECTROSTATIC DISCHARGE SENSITIVITY

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply | ±18VDC |
| Internal Power Dissipation ($T_J \leq +175°C$) | 500mW |
| Differential Input Voltage | Total $V_{CC}$ |
| Input Voltage Range | ±$V_{CC}$ |
| Storage Temperature Range: "M" Package | –65°C to +150°C |
| "P" Package | –40°C to +85°C |
| Operating Temperature Range: "M" Package | –55°C to +125°C |
| "P" Package | –40°C to +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short Circuit to Ground (+25°C) | Continuous |
| Junction Temperature | +175°C |

## ORDERING INFORMATION

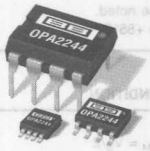
| PRODUCT | PACKAGE | TEMPERATURE RANGE | OFFSET VOLTAGE, max (mV) |
|---|---|---|---|
| OPA2111AM | TO-99 | –25°C to +85°C | ±0.75 |
| OPA2111BM | TO-99 | –25°C to +85°C | ±0.5 |
| OPA2111KM | TO-99 | 0°C to +70°C | ±2 |
| OPA2111SM | TO-99 | –55°C to +125°C | ±0.75 |
| OPA2111KP | 8-Pin Plastic DIP | 0°C to +70°C | ±2 |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| OPA2111AM | TO-99 | 001 |
| OPA2111BM | TO-99 | 001 |
| OPA2111KM | TO-99 | 001 |
| OPA2111SM | TO-99 | 001 |
| OPA2111KP | 8-Pin Plastic DIP | 006 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR-BROWN®



# OPA2244

www.burr-brown.com/databook/OPA2244.html



# Single-Supply OPERATIONAL AMPLIFIER

## *Micro*Amplifier™ Series

## FEATURES

- *Micro*SIZE PACKAGE
- SINGLE SUPPLY OPERATION
- *Micro*POWER: $I_Q$ = 40μA/amp
- WIDE BANDWIDTH: 350kHz
- WIDE SUPPLY RANGE:
  Single Supply: 2.2V to 36V
  Dual Supply: ±1.1V to ±18V

## APPLICATIONS

- BATTERY POWERED SYSTEMS
- PORTABLE EQUIPMENT
- PCMCIA CARDS
- BATTERY PACKS AND POWER SUPPLIES
- CONSUMER PRODUCTS

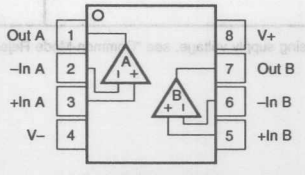
## DESCRIPTION

The OPA2244 is designed for high density, space-limited applications, such as PCMCIA cards, battery packs, and portable instruments. In addition to small size, the OPA2244 features very low quiescent current (40μA/amp), wide bandwidth (350kHz), low offset voltage (1.5mV max), and low bias current (8nA).

The OPA2244 is easy to use and free from phase inversion and overload problems found in some other op amps. This amplifier is stable in unity gain and excellent performance is maintained as it swings to its specified limits. It can be operated from single (+2.2V to +36V) or dual supplies (±1.1V to ±18V). The input common-mode voltage range includes ground—ideal for many single supply applications. The OPA2244 features completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

The OPA2244 is offered in miniature, surface-mount packages. It is available in the MSOP-8 surface mount, SO-8 surface-mount, and 8-pin DIP. It is fully specified from –40°C to +85°C and operates from –55°C to +125°C. A SPICE Macromodel is available for design analysis.

OPA2244




8-Pin DIP, SO-8, MSOP-8

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

## SPECIFICATIONS: $V_S$ = +2.6V to +36V

At $T_A$ = +25°C, and $R_L$ = 20kΩ connected to ground, unless otherwise noted.
**Boldface** limits apply over the specified temperature range, –40°C to +85°C.

| PARAMETER | | CONDITION | OPA2244EA, PA, UA MIN | TYP[1] | MAX | UNITS |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | $V_{CM}$ = $V_S$/2 | | ±0.3 | ±1.5 | mV |
| **$T_A$ = –40°C to 85°C** | | | | | **±2** | mV |
| vs Temperature | $dV_{OS}/dT$ | **$T_A$ = –40°C to 85°C** | | **±2.3** | | µV/°C |
| vs Power Supply | PSRR | $V_S$ = +2.6V to +36V | | 5 | 50 | µV/V |
| **$T_A$ = –40°C to 85°C** | | $V_S$ = +2.6V to +36V | | | **50** | µV/V |
| Channel Separation, dc | | | | 0.5 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | |
| Input Bias Current | $I_B$ | $V_{CM}$ = $V_S$/2 | | –8 | –25 | nA |
| Input Offset Current | $I_{OS}$ | $V_{CM}$ = $V_S$/2 | | ±2 | ±10 | nA |
| **NOISE** | | | | | | |
| Input Voltage Noise, f = 0.1 to 10kHz | | | | 0.4 | | µVp-p |
| Input Voltage Noise Density, f = 1kHz | $e_n$ | | | 22 | | $nV/\sqrt{Hz}$ |
| Current Noise Density, f = 1kHz | $i_n$ | | | 40 | | $fA/\sqrt{Hz}$ |
| **INPUT VOLTAGE RANGE** | | | | | | |
| Common-Mode Voltage Range | $V_{CM}$ | | 0 | | (V+) –1 | V |
| Common-Mode Rejection | CMRR | $V_{CM}$ = 0 to (V+) – 1 | 72[2] | 90 | | dB |
| **$T_A$ = –40°C to 85°C** | | $V_{CM}$ = 0 to (V+) – 1 | **72** | | | dB |
| **INPUT IMPEDANCE** | | | | | | |
| Differential | | | | $10^6$ ll 2 | | Ω ll pF |
| Common-Mode | | | | $10^9$ ll 2 | | Ω ll pF |
| **OPEN-LOOP GAIN** | | | | | | |
| Open-Loop Voltage Gain | $A_{OL}$ | $V_O$ = 0.5V to (V+) – 1 | 80 | 106 | | dB |
| **$T_A$ = –40°C to 85°C** | | $V_O$ = 0.5V to (V+) – 1 | **80** | | | dB |
| **FREQUENCY RESPONSE** | | | | | | |
| Gain-Bandwidth Product | GBW | | | 350 | | kHz |
| Slew Rate | SR | G = 1 | | 0.1 | | V/µs |
| Settling Time 0.1% | | | | 150 | | µs |
| Overload Recovery Time | | $V_{IN}$ • G = $V_S$ | | 8 | | µs |
| **OUTPUT** | | | | | | |
| Voltage Output, Positive | | $A_{OL}$ ≥ 80dB | (V+) – 1 | (V+) – 0.75 | | V |
| **$T_A$ = –40°C to 85°C** | | $A_{OL}$ ≥ 80dB | **(V+) – 1** | | | V |
| Voltage Output, Negative | | $A_{OL}$ ≥ 80dB | 0.5 | 0.3 | | V |
| **$T_A$ = –40°C to 85°C** | | $A_{OL}$ ≥ 80dB | **0.5** | | | V |
| Short-Circuit Current | $I_{SC}$ | | | –25/+12 | | mA |
| Capacitive Load Drive | $C_{LOAD}$ | | | See Typical Curve | | |
| **POWER SUPPLY** | | | | | | |
| Specified Voltage Range | $V_S$ | | +2.6 | | +36 | V |
| Minimum Operating Voltage | | | | +2.2 | | V |
| Quiescent Current (per amplifier) | $I_Q$ | $I_O$ = 0 | | 40 | 50 | µA |
| **$T_A$ = –40°C to 85°C** | | $I_O$ = 0 | | | **63** | µA |
| **TEMPERATURE RANGE** | | | | | | |
| Specified Range | | | –40 | | 85 | °C |
| Operating Range | | | –55 | | 125 | °C |
| Storage Range | | | –55 | | 125 | °C |
| Thermal Resistance | $\theta_{JA}$ | | | | | |
| MSOP-8 Surface-Mount | | | | 150 | | °C/W |
| SO-8 Surface-Mount | | | | 150 | | °C/W |
| 8-Pin DIP | | | | 100 | | °C/W |

NOTES: (1) $V_S$ = +15V. (2) CMRR improves with increasing supply voltage, see "Common-Mode Rejection vs Supply Voltage" typical curve.

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## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Supply Voltage | 36V |
| Input Voltage | (V–) –0.5V to (V+) +0.5V |
| Output Short-Circuit[2] | Continuous |
| Operating Temperature | –55°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering, 10s) | 300°C |

NOTES: (1) Stresses above these ratings may cause permanent damage. (2) Short-circuit to ground, one amplifier per package.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER[2] | TRANSPORT MEDIA |
|---|---|---|---|---|---|---|
| OPA2244EA | MSOP-8 Surface-Mount | 337 | –40°C to +85°C | A44 | OPA2244EA/250 | Tape and Reel |
| " | " | " | " | " | OPA2244EA/2K5 | Tape and Reel |
| OPA2244PA | 8-Pin DIP | 006 | –40°C to +85°C | OPA2244PA | OPA2244PA | Rails |
| OPA2244UA | SO-8 Surface-Mount | 182 | –40°C to +85°C | OPA2244UA | OPA2244UA | Rails[3] |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) OPA2244EA is available only in Tape and Reel in 250 and 2500 piece quantities. Ordering 2500 pieces of "OPA2244EA/2K5" will get a single 2500 piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book. (3) OPA2244UA also available in Tape and Reel.

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# OPA2337

www.burr-brown.com/databook/OPA2337.html

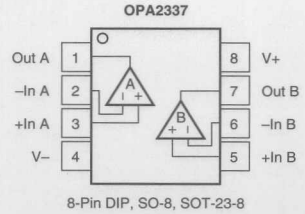
# *Micro*SIZE, Single-Supply CMOS OPERATIONAL AMPLIFIER *MicroAmplifier*™ Series

## FEATURES

- *Micro*SIZE PACKAGE: SOT-23-8
- SINGLE SUPPLY OPERATION
- RAIL-TO-RAIL OUTPUT SWING
- FET-INPUT: $I_B$ = 10pA max
- HIGH SPEED: 3MHz, 1V/μs
- OPERATION FROM 2.5V to 5.5V
- HIGH OPEN-LOOP GAIN: 120dB
- LOW QUIESCENT CURRENT: 525μA/amp

## APPLICATIONS

- BATTERY POWERED INSTRUMENTS
- PHOTODIODE PRE-AMPS
- MEDICAL INSTRUMENTS
- TEST EQUIPMENT
- AUDIO SYSTEMS
- DRIVING ADCs
- CONSUMER PRODUCTS




8-Pin DIP, SO-8, SOT-23-8

## DESCRIPTION

The OPA2337 rail-to-rail output CMOS operational amplifier is designed for low cost and miniature applications. Packaged in the new SOT-23-8, the OPA2337EA is the world's *smallest* dual op amp. At only 1/4 the size of a conventional SO-8 surface mount, it is ideal for space-sensitive applications.

Performance is not sacrificed for size. Utilizing advanced CMOS technology, the OPA2337 provides low bias current, high speed operation, high open-loop gain, and rail-to-rail output swing. It operates on a single supply with operation as low as 2.5V while drawing only 525μA quiescent current. In addition, the input common-mode voltage range includes ground—ideal for single supply operations.

The OPA2337 is easy to use and free from phase inversion and overload problems found in some other op amps. It is stable in unity gain and excellent performance is maintained as the amplifier swings to its specified limits. The OPA2337 features completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

In addition to the miniature SOT-23-8 surface-mount package, the OPA2337 is available in standard 8-pin DIP and SO-8 surface-mount packages. It is fully specified from –40°C to +85°C and operates from –55°C to +125°C.

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# SPECIFICATIONS: $V_S$ = 2.7V to 5.5V

At $T_A$ = +25°C, and $R_L$ = 25kΩ connected to $V_S$/2, unless otherwise noted.

| PARAMETER | | CONDITION | OPA2337EA, UA, PA MIN | TYP[1] | MAX | UNITS |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | | | ±0.5 | ±3 | mV |
| vs Temperature | $dV_{OS}/dT$ | | | ±2 | | µV/°C |
| vs Power Supply | PSRR | $V_S$ = 2.7V to 5.5V | | 25 | 125 | µV/V |
| Channel Separation | | dc | | 0.3 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | |
| Input Bias Current | $I_B$ | | | ±0.2 | ±10 | pA |
| Input Offset Current | $I_{OS}$ | | | ±0.2 | ±10 | pA |
| **NOISE** | | | | | | |
| Input Voltage Noise, f = 0.1 to 10Hz | | | | 6 | | µVp-p |
| Input Voltage Noise Density, f = 1kHz | $e_n$ | | | 26 | | $nV/\sqrt{Hz}$ |
| Current Noise Density, f = 1kHz | $i_n$ | | | 0.6 | | $fA/\sqrt{Hz}$ |
| **INPUT VOLTAGE RANGE** | | | | | | |
| Common-Mode Voltage Range | $V_{CM}$ | | –0.2 | | (V+) –1.2 | V |
| Common-Mode Rejection Ratio | CMRR | –0.2V < $V_{CM}$ < (V+) –1.2V | 74 | 90 | | dB |
| **INPUT IMPEDANCE** | | | | | | |
| Differential | | | | $10^{13}$ \|\| 2 | | Ω \|\| pF |
| Common-Mode | | | | $10^{13}$ \|\| 4 | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | | |
| Open-Loop Voltage Gain | $A_{OL}$ | $R_L$ = 25kΩ, 125mV < $V_O$ < (V+) –125mV | 100 | 120 | | dB |
| | | $R_L$ = 5kΩ, 500mV < $V_O$ < (V+) –500mV | 100 | 114 | | dB |
| **FREQUENCY RESPONSE** | | | | | | |
| Gain-Bandwidth Product | GBW | $V_S$ = 5V, G = 1 | | 3 | | MHz |
| Slew Rate | SR | $V_S$ = 5V, G = 1 | | 1.2 | | V/µs |
| Settling Time 0.1% | | $V_S$ = 5V, 2V Step, $C_L$ = 100pF, G = 1 | | 2 | | µs |
| 0.01% | | $V_S$ = 5V, 2V Step, $C_L$ = 100pF, G = 1 | | 2.5 | | µs |
| Overload Recovery Time | | $V_{IN}$ • G = $V_S$ | | 2 | | µs |
| Total Harmonic Distortion + Noise | THD+N | $V_S$ = 5V, $V_O$ = 3Vp-p, G = 1, f = 1kHz | | 0.001 | | % |
| **OUTPUT** | | | | | | |
| Voltage Output Swing from Rail[2] | | $R_L$ = 25kΩ | | 40 | 125 | mV |
| | | $R_L$ = 5kΩ | | 150 | 500 | mV |
| Short-Circuit Current | $I_{SC}$ | | | ±9 | | mA |
| Capacitive Load Drive | $C_{LOAD}$ | | | See Typical Curve | | |
| **POWER SUPPLY** | | | | | | |
| Specified Voltage Range | $V_S$ | | 2.7 | | 5.5 | V |
| Minimum Operating Voltage | | | | 2.5 | | V |
| Quiescent Current (per amplifier) | $I_Q$ | $I_O$ = 0 | | 525 | 750 | µA |
| **TEMPERATURE RANGE** | | | | | | |
| Specified Range | | | –40 | | +85 | °C |
| Operating Range | | | –55 | | +125 | °C |
| Storage Range | | | –55 | | +125 | °C |
| Thermal Resistance | $\theta_{JA}$ | | | | | |
| SOT-23-8 Surface-Mount | | | | 200 | | °C/W |
| SO-8 Surface-Mount | | | | 150 | | °C/W |
| 8-Pin DIP | | | | 100 | | °C/W |

NOTES: (1) $V_S$ = 5V.

(2) Output voltage swings are measured between the output and negative and positive power supply rails.

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## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Supply Voltage | 5.5V |
| Input Voltage[2] | (V–) –0.3V to (V+) +0.3V |
| Input Current[2] | 10mA |
| Output Short-Circuit[3] | Continuous |
| Operating Temperature | –55°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering, 10s) | 300°C |

NOTES: (1) Stresses above these ratings may cause permanent damage. (2) Input signal voltage is limited by internal diodes connected to power supplies. See text. (3) Short-circuit to ground, one amplifier per package.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

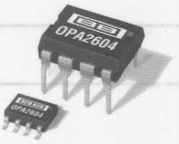
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER[2] | TRANSPORT MEDIA |
|---|---|---|---|---|---|---|
| OPA2337EA | SOT-23-8 Surface-Mount | 348 | –40°C to +85°C | A7 | OPA2337EA-250 | Tape and Reel |
| " | " | " | " | " | OPA2337EA-3K | Tape and Reel |
| OPA2337PA | 8-Pin DIP | 006 | –40°C to +85°C | OPA2337PA | OPA2337PA | Rails |
| OPA2337UA | SO-8 Surface-Mount | 182 | –40°C to +85°C | OPA2337UA | OPA2337UA | Rails[3] |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with -250 and -3K are available only in Tape and Reel in the quantities indicated (e.g., -250 indicates 250 devices per reel). Ordering 3000 pieces of "OPA2337-3K" will get a single 3000 piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book. (3) SO-8 models also available in Tape and Reel.

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# OPA2604

www.burr-brown.com/databook/OPA2604.html



# Dual FET-Input, Low Distortion OPERATIONAL AMPLIFIER

## FEATURES

- LOW DISTORTION: 0.0003% at 1kHz
- LOW NOISE: 10nV/√Hz
- HIGH SLEW RATE: 25V/µs
- WIDE GAIN-BANDWIDTH: 20MHz
- UNITY-GAIN STABLE
- WIDE SUPPLY RANGE: $V_S$ = ±4.5 to ±24V
- DRIVES 600Ω LOADS

## APPLICATIONS

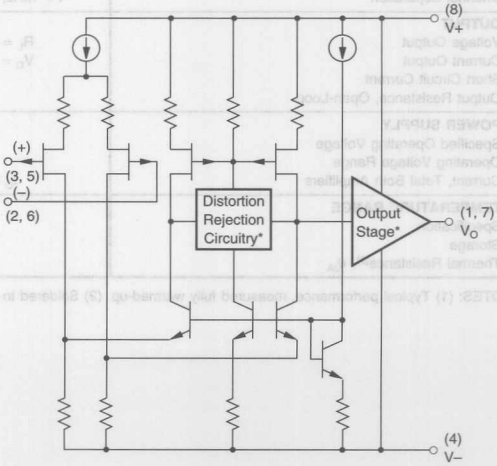
- PROFESSIONAL AUDIO EQUIPMENT
- PCM DAC I/V CONVERTER
- SPECTRAL ANALYSIS EQUIPMENT
- ACTIVE FILTERS
- TRANSDUCER AMPLIFIER
- DATA ACQUISITION

## DESCRIPTION

The OPA2604 is a dual, FET-input operational amplifier designed for enhanced AC performance. Very low distortion, low noise and wide bandwidth provide superior performance in high quality audio and other applications requiring excellent dynamic performance.

New circuit techniques and special laser trimming of dynamic circuit performance yield very low harmonic distortion. The result is an op amp with exceptional sound quality. The low-noise FET input of the OPA2604 provides wide dynamic range, even with high source impedance. Offset voltage is laser-trimmed to minimize the need for interstage coupling capacitors.

The OPA2604 is available in 8-pin plastic mini-DIP and SO-8 surface-mount packages, specified for the –25°C to +85°C temperature range.




* Patents Granted:
#5053718, 5019789

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# SPECIFICATIONS

## ELECTRICAL

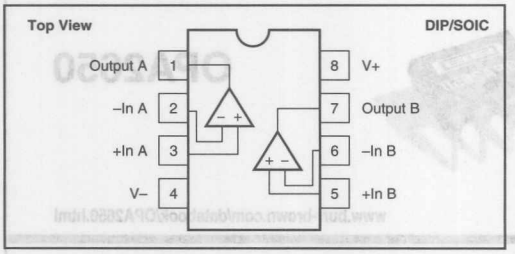
At $T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

| PARAMETER | CONDITION | OPA2604AP, AU | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | | | ±1 | ±5 | mV |
| Average Drift | | | ±8 | | µV/°C |
| Power Supply Rejection | $V_S$ = ±5 to ±24V | 70 | 80 | | dB |
| **INPUT BIAS CURRENT**[1] | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | 100 | | pA |
| Input Offset Current | $V_{CM}$ = 0V | | ±4 | | pA |
| **NOISE** | | | | | |
| Input Voltage Noise | | | | | |
| Noise Density: f = 10Hz | | | 25 | | nV/√Hz |
| f = 100Hz | | | 15 | | nV/√Hz |
| f = 1kHz | | | 11 | | nV/√Hz |
| f = 10kHz | | | 10 | | nV/√Hz |
| Voltage Noise, BW = 20Hz to 20kHz | | | 1.5 | | µVp-p |
| Input Bias Current Noise | | | | | |
| Current Noise Density, f = 0.1Hz to 20kHz | | | 6 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range | | ±12 | ±13 | | V |
| Common-Mode Rejection | $V_{CM}$ = ±12V | 80 | 100 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $10^{12}$ \|\| 8 | | Ω \|\| pF |
| Common-Mode | | | $10^{12}$ \|\| 10 | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±10V, $R_L$ = 1kΩ | 80 | 100 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product | G = 100 | | 20 | | MHz |
| Slew Rate | 20Vp-p, $R_L$ = 1kΩ | 15 | 25 | | V/µs |
| Settling Time: 0.01% | G = –1, 10V Step | | 1.5 | | µs |
| 0.1% | | | 1 | | µs |
| Total Harmonic Distortion + Noise (THD+N) | G = 1, f = 1kHz<br>$V_O$ = 3.5Vrms, $R_L$ = 1kΩ | | 0.0003 | | % |
| Channel Separation | f = 1kHz, $R_L$ = 1kΩ | | 142 | | dB |
| **OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 600Ω | ±11 | ±12 | | V |
| Current Output | $V_O$ = ±12V | | ±35 | | mA |
| Short Circuit Current | | | ±40 | | mA |
| Output Resistance, Open-Loop | | | 25 | | Ω |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±15 | | V |
| Operating Voltage Range | | ±4.5 | | ±24 | V |
| Current, Total Both Amplifiers | $I_O$ = 0 | | ±10.5 | ±12 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –25 | | +85 | °C |
| Storage | | –40 | | +125 | °C |
| Thermal Resistance[2], $\theta_{JA}$ | | | 90 | | °C/W |

NOTES: (1) Typical performance, measured fully warmed-up. (2) Soldered to circuit board—see text.

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## PIN CONFIGURATION




## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Power Supply Voltage | ±25V |
| Input Voltage | (V–)–1V to (V+)+1V |
| Output Short Circuit to Ground | Continuous |
| Operating Temperature | –40°C to +100°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) AP | +300°C |
| Lead Temperature (soldering, 3s) AU | +260°C |

NOTE: (1) Stresses above these ratings may cause permanent damage.

## ORDERING INFORMATION

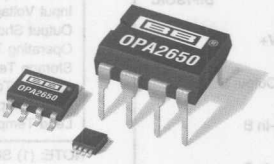
| PRODUCT | PACKAGE | TEMP. RANGE |
|---|---|---|
| OPA2604AP | 8-Pin Plastic DIP | –25°C to +85°C |
| OPA2604AU | SO-8 Surface-Mount | –25°C to +85°C |

## PACKAGING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| OPA2604AP | 8-Pin Plastic DIP | 006 |
| OPA2604AU | SO-8 Surface-Mount | 182 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# OPA2650

www.burr-brown.com/databook/OPA2650.html

# Dual Wideband, Low Power Voltage Feedback OPERATIONAL AMPLIFIER

## FEATURES

- LOW POWER: 50mW/Chan.
- UNITY GAIN STABLE BANDWIDTH: 360MHz
- FAST SETTLING TIME: 20ns to 0.01%
- LOW HARMONICS: –77dBc at 5MHz
- DIFFERENTIAL GAIN/PHASE ERROR: 0.01%/0.025°
- HIGH OUTPUT CURRENT: 85mA

## APPLICATIONS

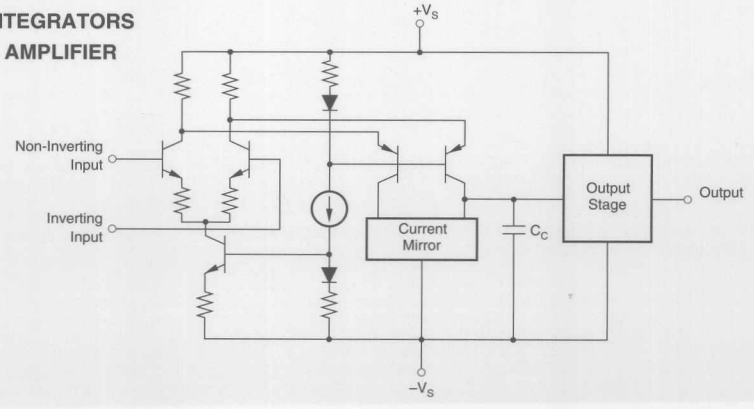
- HIGH RESOLUTION VIDEO
- BASEBAND AMPLIFIER
- CCD IMAGING AMPLIFIER
- ULTRASOUND SIGNAL PROCESSING
- ADC/DAC GAIN AMPLIFIER
- ACTIVE FILTERS
- HIGH SPEED INTEGRATORS
- DIFFERENTIAL AMPLIFIER

## DESCRIPTION

The OPA2650 is a dual, low power, wideband voltage feedback operational amplifier. It features a high bandwidth of 360MHz as well as a 12-bit settling time of only 20ns. The low distortion allows its use in communications applications, while the wide bandwidth and true differential input stage make it suitable for use in a variety of active filter applications. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA2650 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Its unusual combination of speed, accuracy and low power make it an outstanding choice for many portable, multi-channel and other high speed applications, where power is at a premium.

The OPA2650 is also available in single (OPA650) and quad (OPA4650) configurations.




NOTE: Diagram shows only one-half of the OPA2650.

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PDS-1266C

BURR - BROWN®

# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = ±5V, $R_L$ = 100Ω, and $R_{FB}$ = 402Ω, unless otherwise noted. $R_{FB}$ = 25Ω for a gain of +1.

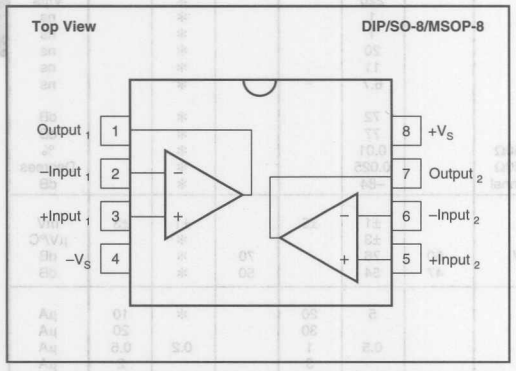
| PARAMETER | CONDITIONS | OPA2650P, U, E | | | OPA2650PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Closed-Loop Bandwidth[2] | G = +1 | | 360 | | | *[1] | | MHz |
| | G = +2 | | 108 | | | * | | MHz |
| | G = +5 | | 32 | | | * | | MHz |
| | G = +10 | | 16 | | | * | | MHz |
| Gain Bandwidth Product | G ≥ +5 | | 160 | | | | | MHz |
| Bandwidth for 0.1dB Flatness[2] | G = +2 | | 21 | | | * | | MHz |
| Slew Rate[3] | G = +1, 2V Step | | 240 | | | * | | V/µs |
| Over Temperature Range | | | 220 | | | * | | V/µs |
| Rise Time | G = +1, 0.2V Step | | 1 | | | * | | ns |
| Fall Time | G = +1, 0.2V Step | | 1 | | | * | | ns |
| Settling Time 0.01% | G = +1, 2V Step | | 20 | | | * | | ns |
| 0.1% | G = +1, 2V Step | | 11 | | | * | | ns |
| 1% | G = +1, 2V Step | | 6.7 | | | * | | ns |
| Spurious Free Dynamic Range | G = +1, f = 5.0MHz, $V_O$ = 2Vp-p | | | | | | | |
| | $R_L$ = 100Ω | | 72 | | | * | | dB |
| | $R_L$ = 402Ω | | 77 | | | * | | dB |
| Differential Gain | G = +2, NTSC, $V_O$ = 1.4Vp-p, $R_L$ = 150Ω | | 0.01 | | | * | | % |
| Differential Phase | G = +2, NTSC, $V_O$ = 1.4Vp-p, $R_L$ = 150Ω | | 0.025 | | | * | | Degrees |
| Crosstalk[2] | Input Referred, 5MHz, Channel-to-Channel | | –84 | | | * | | dB |
| **INPUT OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0V | | ±1 | ±5 | | ±1 | ±3 | mV |
| Average Drift | | | ±3 | | | * | | µV/°C |
| Power Supply Rejection (+$V_S$) | Input Referred, $V_S$ = ±4.5V to ±5.5V | 60 | 76 | | 70 | * | | dB |
| (–$V_S$) | | 47 | 54 | | 50 | * | | dB |
| **INPUT BIAS CURRENT** | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | 5 | 20 | | * | 10 | µA |
| Over Temperature Range | | | | 30 | | | 20 | µA |
| Input Offset Current | $V_{CM}$ = 0V | | 0.5 | 1 | | 0.2 | 0.5 | µA |
| Over Temperature Range | | | | 3 | | | 2 | µA |
| **INPUT NOISE** | | | | | | | | |
| Input Voltage Noise | | | | | | | | |
| Noise Density, f = 100Hz | | | 43 | | | * | | nV/√Hz |
| f = 10kHz | | | 9.4 | | | * | | nV/√Hz |
| f ≥ 1MHz | | | 8.4 | | | * | | nV/√Hz |
| Integrated Noise | | | | | | | | |
| $f_B$ = 10Hz to 100MHz | | | 84 | | | * | | µVrms |
| Input Bias Current Noise | | | | | | | | |
| Noise Density, f ≥ 0.1MHz | | | 1.2 | | | * | | pA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | | ±2.8 | | | * | | V |
| Over Temperature Range | | ±2.2 | | | * | | | V |
| Common-Mode Rejection | Input Referred, $V_{CM}$ = ±0.5V | 65 | 90 | | 70 | * | | dB |
| **INPUT IMPEDANCE** | | | | | | | | |
| Differential | | | 15 ‖ 1 | | | * | | KΩ ‖ pF |
| Common-Mode | | | 16 ‖ 1 | | | * | | MΩ ‖ pF |
| **OPEN-LOOP GAIN** | | | | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±2V, $R_L$ = 100Ω | 45 | 51 | | 47 | * | | dB |
| Over Temperature Range | | 43 | | | 45 | | | dB |
| **OUTPUT** | | | | | | | | |
| Voltage Output | | | | | | | | |
| Over Temperature Range | No Load | ±2.2 | ±3.0 | | ±2.4 | * | | V |
| | $R_L$ = 250Ω | ±2.2 | ±2.5 | | ±2.4 | * | | V |
| | $R_L$ = 100Ω | ±2.0 | ±2.3 | | ±2.2 | * | | V |
| Output Current, Sourcing | | 75 | 110 | | * | * | | mA |
| Over Temperature Range | | 65 | | | * | | | mA |
| Output Current, Sinking | | 65 | 85 | | * | * | | mA |
| Over Temperature Range | | 35 | | | * | | | mA |
| Short Circuit Current | | | 150 | | | * | | mA |
| Output Resistance | f < 100kHz, G = +1 | | 0.08 | | | * | | Ω |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | | ±5 | | | * | | V |
| Operating Voltage Range | | ±4.5 | | ±5.5 | * | | * | V |
| Quiescent Current | Both Channels, $V_S$ = ±5V | | ±11 | ±15.5 | | * | ±13.5 | mA |
| Over Temperature Range | | | | ±17.5 | | * | ±16 | mA |
| **THERMAL CHARACTERISTICS** | | | | | | | | |
| Temperature Range | Specification: P, U, E, PB, UB | –40 | | +85 | * | | * | °C |
| Thermal Resistance, $\theta_{JA}$ | Junction to Ambient | | | | | | | |
| P 8-Pin DIP | | | 100 | | | * | | °C/W |
| U SO-8 | | | 125 | | | * | | °C/W |
| E MSOP-8 | | | 150 | | | * | | °C/W |

NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Frequency response can be strongly influenced by PC board parasitics. The demonstration boards show low parasitic layouts for this part. Refer to the demonstration board layout for details. (3) Slew rate is rate of change from 10% to 90% of output voltage step.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±5.5V |
| Internal Power Dissipation | See Thermal Characteristics |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: P, PB, U, UB, E | –40°C to +125°C |
| Lead Temperature (DIP, soldering, 10s) | +300°C |
| (SO-8 and MSOP-8, soldering, 3s) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

## PIN CONFIGURATION




## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

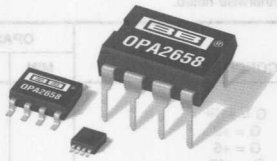
## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE | PACKAGE MARKING(2) | ORDERING NUMBER(3) |
|---|---|---|---|---|---|
| OPA2650P | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA2650P | OPA2650P |
| OPA2650PB | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA2650PB | OPA2650PB |
| OPA2650U | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA2650U | OPA2650U |
| OPA2650UB | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA2650UB | OPA2650UB |
| OPA2650E | MSOP-8 | 337 | –40°C to +85°C | B50 | OPA2650E-250<br>OPA2650E-2500 |

NOTE: (1) For detailed drawing and dimension table, see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade will be marked with a "B" by pin 8. (3) The MSOP-8 is available on 7" tape and reel with 250 parts, and on 14" tape and reel with 2500 parts. For example, ordering 250 pieces of "OPA2650E-250" will get a single 250 piece tape and reel. Refer to Appendix B of Burr-Brown IC Data Book for detailed Tape and Reel Mechanical information.

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# OPA2658

www.burr-brown.com/databook/OPA2658.html

# Dual Wideband, Low Power, Current Feedback OPERATIONAL AMPLIFIER

## FEATURES

- UNITY GAIN STABLE BANDWIDTH: 800MHz
- LOW POWER: 50mW/Chan.
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.01%/0.03°
- HIGH SLEW RATE: 1700V/μs
- PACKAGE: 8-Pin DIP, SO-8 and MSOP-8

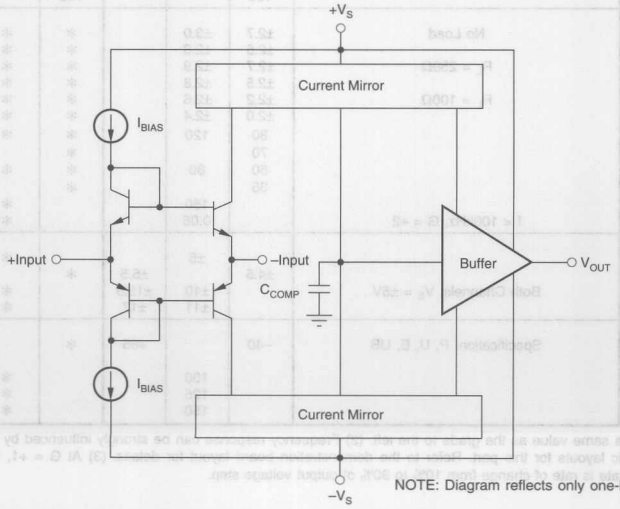
## APPLICATIONS

- MEDICAL IMAGING
- HIGH-RESOLUTION VIDEO
- HIGH-SPEED SIGNAL PROCESSING
- COMMUNICATIONS
- PULSE AMPLIFIERS
- ADC/DAC GAIN AMPLIFIER
- MONITOR PREAMPLIFIER
- CCD IMAGING AMPLIFIER

## DESCRIPTION

The OPA2658 is a dual, ultra-wideband, low power current feedback video operational amplifier featuring high slew rate and low differential gain/phase error. The current feedback design allows for superior large signal bandwidth, even at high gains. The low differential gain/phase errors, wide bandwidth and low quiescent current make the OPA2658 a perfect choice for numerous video, imaging and communications applications.

The OPA2658 is optimized for low gain operation, and is also available in single, OPA658 and quad, OPA4658 configurations.




NOTE: Diagram reflects only one-half of the OPA2658

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = ±5V, $R_L$ = 100Ω, $R_{FB}$ = 402Ω, unless otherwise noted.

| PARAMETER | CONDITION | OPA2658P, U, E | | | OPA2658UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Closed-Loop Bandwidth[2] | G = +1[3] | | 800 | | | *[1] | | MHz |
| | G = +2 | | 500 | | 300 | * | | MHz |
| | G = +5 | | 210 | | | * | | MHz |
| | G = +10 | | 130 | | | * | | MHz |
| Bandwidth for 0.1dB Flatness[2] | $V_O$ < 0.5Vp-p | | 135 | | | * | | MHz |
| Slew Rate[4] | G = +2, 2V Step | | 1700 | | 1000 | * | | V/µs |
| Over Temperature Range | | | 1500 | | 900 | * | | V/µs |
| Settling Time: 0.01% | G = +2, 2V Step | | 15 | | | * | | ns |
| 0.1% | G = +2, 2V Step | | 12.6 | | | * | | ns |
| 1% | G = +2, 2V Step | | 4.8 | | | * | | ns |
| Spurious Free Dynamic Range | f = 5MHz, G = +2, $V_O$ = 2Vp-p | | 68 | | | * | | dB |
| | f = 20MHz, G = +2, $V_O$ = 2Vp-p | | 56 | | | * | | dB |
| Third-Order Intercept Point | f = 10MHz, 4dBm, Each Tone | | 39 | | | * | | dBm |
| Differential Gain | G = +2, NTSC, $V_O$ = 1.4Vp-p, $R_L$ = 150Ω | | 0.01 | | | * | | % |
| Differential Phase | G = +2, NTSC, $V_O$ = 1.4Vp-p, $R_L$ = 150Ω | | 0.03 | | | * | | degrees |
| Crosstalk | Input Referred, 5MHz, Channel-to-Channel | | –78 | | | * | | dB |
| **OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0V | | ±3 | ±5.5 | | ±2 | ±4.5 | mV |
| Over Temperature Range | | | ±5 | ±8 | | ±4 | ±7 | mV |
| Power Supply Rejection | Input Referred, $V_S$ = ±4.5 to ±5.5V | 55 | 64 | | 58 | 68 | | dB |
| **INPUT BIAS CURRENT** | | | | | | | | |
| Non-Inverting | $V_{CM}$ = 0V | | ±4.0 | ±30 | | * | ±18 | µA |
| Over Temperature Range | | | ±10 | ±80 | | * | ±35 | µA |
| Inverting | $V_{CM}$ = 0V | | ±2.9 | ±35 | | * | * | µA |
| Over Temperature Range | | | ±30 | ±75 | | * | * | µA |
| **NOISE** | | | | | | | | |
| Input Voltage Noise | | | | | | | | |
| Noise Density: f = 100Hz | | | 16 | | | * | | nV/√Hz |
| f = 10kHz | | | 3.6 | | | * | | nV/√Hz |
| f ≥ 1MHz | | | 3.2 | | | * | | nV/√Hz |
| Integrated Noise: | | | | | | | | |
| $f_B$ = 100Hz to 200MHz | | | 45 | | | * | | µVrms |
| Input Bias Current Noise Density | | | | | | | | |
| Inverting: f ≥ 1MHz | | | 32 | | | * | | pA/√Hz |
| Non-Inverting: f ≥ 1MHz | | | 11.9 | | | * | | pA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-mode Input Range | | | ±2.9 | | | * | | V |
| Over Temperature Range | | ±2.5 | | | * | | | V |
| Common-mode Rejection | Input Referred, $V_{CM}$ = ±1V | 45 | 50 | | * | * | | dB |
| **INPUT IMPEDANCE** | | | | | | | | |
| Non-Inverting | | | 500 ll 1 | | | * | | kΩ ll pF |
| Inverting | | | 50 | | | * | | Ω |
| **OPEN-LOOP TRANSIMPEDANCE** | | | | | | | | |
| Open-loop Transimpedance | $V_O$ = ±2V, $R_L$ = 100Ω | 150 | 180 | | 200 | * | | kΩ |
| Over Temperature Range | | 100 | | | 150 | | | kΩ |
| **OUTPUT** | | | | | | | | |
| Voltage Output | No Load | ±2.7 | ±3.0 | | * | * | | V |
| Over Temperature Range | | ±2.5 | ±2.8 | | * | * | | V |
| Voltage Output | $R_L$ = 250Ω | ±2.7 | ±2.9 | | * | * | | V |
| Over Temperature Range | | ±2.5 | ±2.8 | | * | * | | V |
| Voltage Output | $R_L$ = 100Ω | ±2.2 | ±2.6 | | * | * | | V |
| Over Temperature Range | | ±2.0 | ±2.4 | | * | * | | V |
| Output Current, Sourcing | | 80 | 120 | | * | * | | mA |
| Over Temperature Range | | 70 | | | * | | | mA |
| Output Current, Sinking | | 60 | 80 | | * | * | | mA |
| Over Temperature Range | | 35 | | | * | | | mA |
| Short Circuit Current | | | 150 | | | * | | mA |
| Output Resistance | f < 100kHz, G = +2 | | 0.06 | | | * | | Ω |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | | ±5 | | | * | | V |
| Operating Voltage Range | | ±4.5 | | ±5.5 | * | | * | V |
| Quiescent Current | Both Channels, $V_S$ = ±5V | | ±10 | ±15.5 | | * | ±11.5 | mA |
| Over Temperature | | | ±11 | ±17 | | * | ±13 | mA |
| **THERMAL CHARACTERISTICS** | | | | | | | | |
| Temperature Range | Specification: P, U, E, UB | –40 | | +85 | * | | * | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| P 8-Pin DIP | | | 100 | | | * | | °C/W |
| U SO-8 | | | 125 | | | * | | °C/W |
| E MSOP-8 | | | 150 | | | * | | °C/W |

*NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Frequency response can be strongly influenced by PC board parasitics. The demonstration boards show low parasitic layouts for this part. Refer to the demonstration board layout for details. (3) At G = +1, $R_{FB}$ = 560Ω for DIP and MSOP-8, and 402Ω for SO-8. (4) Slew rate is rate of change from 10% to 90% of output voltage step.*

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±5.5V |
| Internal Power Dissipation | See Thermal Characteristics |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: P, U, UB, E | –40°C to +125°C |
| Lead Temperature (DIP, soldering, 10s) | +300°C |
| (SO-8 and MSOP-8, soldering, 3s) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

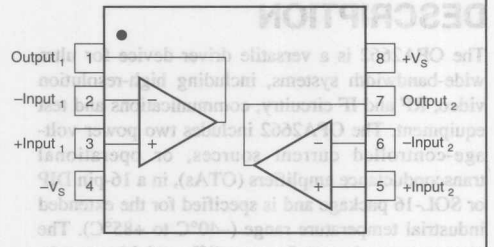
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN CONFIGURATION

Top View DIP/SO-8/MSOP-8

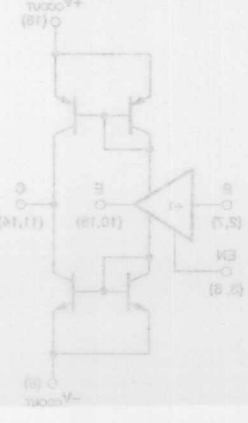



## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE | PACKAGE MARKING(2) | ORDERING NUMBER(3) |
|---|---|---|---|---|---|
| OPA2658P | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA2658P | OPA2658P |
| OPA2658U | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA2658U | OPA2658U |
| OPA2658UB | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA2658UB | OPA2658UB |
| OPA2658E | 8-Pin MSOP-8 | 337 | –40°C to +85°C | B58 | OPA2658E-250<br>OPA2658E-2500 |

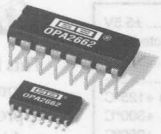
NOTE: (1) For detailed drawing and dimension table, see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade will be marked with a "B" by pin 8. (3) The MSOP-8 is available on 7" tape and reel with 250 parts, and on 14" tape and reel with 2500 parts. For example, ordering 250 pieces of "OPA2658E-250" will get a single 250 piece tape and reel. Refer to Appendix B of Burr-Brown IC Data Book for detailed Tape and Reel Mechanical information.





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# OPA2662

www.burr-brown.com/databook/OPA2662.html

# Dual, Wide Bandwidth OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

## FEATURES

- 370MHz BANDWIDTH
- 58mA/ns SLEW RATE
- HIGH OUTPUT CURRENT: ±75mA
- 400Mbit/s DATA RATE
- VOLTAGE-CONTROLLED CURRENT SOURCE
- ENABLE/DISABLE FUNCTION

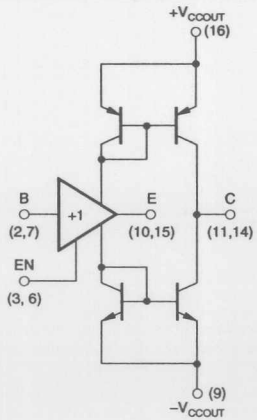
## APPLICATIONS

- HEAD DRIVE AMPLIFIER FOR ANALOG/ DIGITAL VIDEO TAPES AND DATA RECORDERS
- LED AND LASER DIODE DRIVER
- HIGH CURRENT VIDEO BUFFER OR LINE DRIVER
- RF OUTPUT STAGE DRIVER
- HIGH DENSITY DISK DRIVES

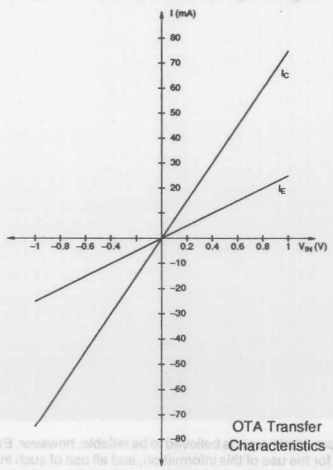
## DESCRIPTION

The OPA2662 is a versatile driver device for ultra wide-bandwidth systems, including high-resolution video, RF and IF circuitry, communications and test equipment. The OPA2662 includes two power voltage-controlled current sources, or operational transconductance amplifiers (OTAs), in a 16-pin DIP or SOL-16 package and is specified for the extended industrial temperature range (–40°C to +85°C). The output current is zero-for-zero differential input voltage. The OTAs provide a 250MHz large-signal bandwidth, a 58mA/ns slew rate, and each current source delivers up to ±75mA output current.

The transconductance of both OTAs can be adjusted between pin 5 and $-V_{CC}$ by an external resistor, allowing bandwidth, quiescent current, harmonic distortion and gain trade-offs to be optimized. The output current can be set with a degeneration resistor between the emitter and GND. The current mirror ratio between the collector and emitter currents is fixed to three. Switching stages compatible to logic TTL levels make it possible to turn each OTA separately on within 30ns and off within 200ns at full power.




1/2 OPA2662




OTA Transfer Characteristics


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# SPECIFICATIONS

## ELECTRICAL

## DC-SPECIFICATIONS

At $V_{CC}$ = ±5V, $R_Q$ = 750Ω, $T_A$ = +25°C, and configured as noted under "CONDITIONS".

| PARAMETER | CONDITIONS | OPA2662AP, AU MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **OTA INPUT OFFSET VOLTAGE** | | | | | |
| Initial | $R_E$ = 50kΩ, $R_C$ = 40Ω | | 12 | ±30 | mV |
| vs Temperature | | | 35 | | µV/°C |
| vs Supply (tracking) | $V_{CC}$ = ±4.5V to ±5.5V, $R_E$ = 50kΩ, $R_C$ = 1kΩ | | 27 | | dB |
| vs Supply (non-tracking) | $V_{CC}$ = +4.5V to +5.5V, $R_E$ = 50kΩ, $R_C$ = 1kΩ | | 15 | | dB |
| vs Supply (non-tracking) | $V_{CC}$ = –4.5V to –5.5V, $R_E$ = 50kΩ, $R_C$ = 1kΩ | | 40 | | dB |
| Matching | | | 2 | ±7 | mV |
| **OTA B-INPUT BIAS CURRENT** | | | | | |
| Initial | $R_E$ = 100Ω, $R_C$ = 40Ω | | 1 | –1/+5 | µA |
| vs Temperature | | | –5 | | nA/°C |
| vs Supply (tracking) | $V_{CC}$ = ±4.5V to ±5.5V, $R_E$ = 50kΩ, $R_C$ = 1kΩ | | 60 | | nA/V |
| vs Supply (non-tracking) | $V_{CC}$ = +4.5V to +5.5V, $R_E$ = 50kΩ, $R_C$ = 1kΩ | | 160 | | nA/V |
| vs Supply (non-tracking) | $V_{CC}$ = –4.5V to –5.5V, $R_E$ = 50kΩ, $R_C$ = 1kΩ | | 40 | | nA/V |
| Matching | | | 0.2 | ±1 | µA |
| **OTA C-OUTPUT BIAS CURRENT** | $R_E$ = 100Ω, $R_C$ = 1kΩ | | | | |
| Initial | | | 0.5 | –0.5/+1.5 | mA |
| vs Temperature | | | 1.5 | | µA/°C |
| vs Supply (tracking) | $V_{CC}$ = ±4.5V to ±5.5V | | 72 | | µA/V |
| vs Supply (non-tracking) | $V_{CC}$ = +4.5V to +5.5V | | 236 | | µA/V |
| vs Supply (non-tracking) | $V_{CC}$ = –4.5V to –5.5V | | 92 | | µA/V |
| Matching | | | 0.06 | ±0.5 | mA |
| **B-INPUT IMPEDANCE** | | | | | |
| Impedance | $I_O$ = ±17mA | | 4.5 ll 1.5 | | MΩ ll pF |
| **OTA INPUT NOISE** | | | | | |
| Input Noise Voltage Density | f = 20kHz to 100MHz | | 4.4 | | $nV/\sqrt{Hz}$ |
| Output Noise Current Density | | | 0.09 | | $nA/\sqrt{Hz}$ |
| Signal-to-Noise Ratio | S/N = 20 log • (0.7/$V_N$ • $\sqrt{5MHz}$) | | 97 | | dB |
| **OTA C-RATED OUTPUT** | | | | | |
| Output Voltage Compliance | $I_C$ = ±5mA, $R_E$ = 100Ω, $R_C$ = 1kΩ | | ±3.4 | | V |
| Output Current | $R_C$ = 40Ω, $R_E$ = 100Ω | | ±75 | | mA |
| | $V_{IN}$ = ±3V | | | | |
| Output Impedance, $r_C$ | $I_O$ = ±17mA | | 4.5 ll 6.5 | | kΩ ll pF |
| **OTA E-RATED OUTPUT** | | | | | |
| Voltage Output | $R_E$ = 100Ω, $R_C$ = 40Ω | | ±3.0 | | V |
| DC Current Output | $R_E$ = 100Ω, $R_C$ = 40Ω | | | | |
| | $V_{IN}$ = ±4V | | ±25 | | mA |
| Voltage Gain | $V_{IN}$ = ±2.5V | | | | |
| | $R_E$ = 100Ω | | 0.86 | | V/V |
| | $R_E$ = 50kΩ | | 0.98 | | V/V |
| Output Impedance, $r_E$ | $I_O$ = ±17mA | | 16 ll 2.2 | | Ω ll pF |
| **POWER SUPPLY** | | | | | |
| Rated Voltage | $R_E$ = 50kΩ, $R_C$ = 1kΩ | ±4.5 | | ±5.5 | VDC |
| Derated Performance | $R_E$ = 50kΩ, $R_C$ = 40Ω | ±3 | | ±6 | VDC |
| Positive Quiescent Current for both OTAs[4] | $R_Q$ = 750Ω, $R_E$ = 50kΩ, $R_C$ = 1kΩ, Both Channels Enabled | +15 | +17 | +18 | mA |
| Positive Quiescent Current for both OTAs[4] | $R_Q$ = 750Ω, $R_E$ = 50kΩ, $R_C$ = 1kΩ, Both Channels Disabled | | +4 | | mA |
| Quiescent Current Range | Programmable | | | | |
| | $R_Q$ = 3kΩ to 30Ω | ±3 | | ±65 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | Ambient Temperature | –40 | | +85 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| AP | | | 90 | | °C/W |
| AU | | | 100 | | °C/W |

NOTES: (1) Characterization sample. (2) "Typical Values" are Mean values. The average of the two amplifiers is used for amplifier specific parameters. (3) "Min" and "Max" Values are mean ±3 Standard Deviations. Worst case of the two amplifiers (Mean ±3 Standard Deviations) is used for amplifier specific parameters. (4) $I^-_O$ typically 2mA less than $I^+_O$ due to OTA C-Output Bias Current and TTL Select Circuit Current.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

# SPECIFICATIONS (CONT)

## ELECTRICAL

## AC-SPECIFICATION

Typical at $V_{CC}$ = ±5VDC, $R_Q$ = 750Ω, $I_C$ = ±37.5mA ($V_{IN}$ = 2.5Vpp, $R_E$ = 100Ω), $I_C$ = ±75mA ($V_{IN}$ = 2.5Vpp, $R_E$ = 50Ω), $R_{SOURCE}$ = 50Ω, and $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA2662AP, AU MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **FREQUENCY DOMAIN** | | | | | |
| **LARGE SIGNAL BANDWIDTH** | | | | | |
| $I_C$ = ±37.5mA | $R_E$ = 100Ω, $R_C$ = 50Ω | | 150 | | MHz |
| $I_C$ = ±75mA | $R_E$ = 100Ω, $R_C$ = 25Ω | | 200 | | MHz |
| $I_C$ = ±37.5mA (Optimized) | $R_E$ = 100Ω, $R_C$ = 50Ω, $C_E$ = 5.6pF | | 370 | | MHz |
| $I_C$ = ±75mA (Optimized) | $R_E$ = 100Ω, $R_C$ = 25Ω, $C_E$ = 5.6pF | | 250 | | MHz |
| **GROUP DELAY TIME** | $R_E$ = 100Ω, $R_C$ = 50Ω | | | | |
| Measured Input to Output | B to E | | 1.2 | | ns |
| (Demo Board Used) | B to C | | 2.5 | | ns |
| **HARMONIC DISTORTION** | | | | | |
| Second Harmonic | f = 10MHz, $I_C$ = ±37.5mA | | –31 | | dBc |
| Third Harmonic | | | –37 | | dBc |
| Second Harmonic | f = 10MHz, $I_C$ = ±75mA | | –33 | | dBc |
| Third Harmonic | | | –32 | | dBc |
| Second Harmonic | f = 30MHz, $I_C$ = ±37.5mA | | –29 | | dBc |
| Third Harmonic | | | –32 | | dBc |
| Second Harmonic | f = 30MHz, $I_C$ = ±75mA | | –30 | | dBc |
| Third Harmonic | | | –25 | | dBc |
| Second Harmonic | f = 50MHz, $I_C$ = ±37.5mA | | –31 | | dBc |
| Third Harmonic | | | –30 | | dBc |
| Second Harmonic | f = 50MHz, $I_C$ = ±75mA | | –28 | | dBc |
| Third Harmonic | | | –23 | | dBc |
| **CROSSTALK** | Typical Curve Number 3 | | | | |
| | $I_C$ = ±37.5mA, f = 30MHz | | –51 | | dB |
| | $I_C$ = ±75mA, f = 30MHz | | –56 | | dB |
| **FEEDTHROUGH** | | | | | |
| Off Isolation | $R_E$ = 100Ω, f = 30MHz | | –90 | | dB |
| | $R_E$ = 50Ω, f = 30MHz | | –90 | | dB |
| **TIME DOMAIN** | | | | | |
| Rise Time | 10% to 90% | | | | |
| | 75mA Step $I_C$ | | 2 | | ns |
| | 150mA Step $I_C$ | | 2.6 | | ns |
| Slew Rate | $I_C$ = 75mA | | 37.5 | | mA/ns |
| | $I_C$ = 150mA | | 58 | | mA/ns |

## CHANNEL SELECTION

| PARAMETER | CONDITIONS | OPA2662AP, AU MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **ENABLE INPUTS** | | | | | |
| Logic 1 Voltage | | 2 | | $V_{CC}$ + 0.6 | V |
| Logic 0 Voltage | | 0 | | 0.8 | V |
| Logic 1 Current | $V_{SEL}$ = 2.0V to 5V | 0.8 | 1.1 | 10 | µA |
| Logic 0 Current | $V_{SEL}$ = 0V to 0.8V | –1 | 0.05 | | µA |
| **SWITCHING CHARACTERISTICS** | $I_C$ = 150mAp-p, f = 5MHz | | | | |
| EN to Channel ON Time | 90% Point of $V_O$ = 1Vp-p | | 30 | | ns |
| EN to Channel OFF Time | 10% Point of $V_O$ = 1Vp-p | | 200 | | ns |
| Switching Transient, Positive | (Measured While Switching | | 30 | | mV |
| Switching Transient, Negative | Between the Grounded Channels) | | –80 | | mV |

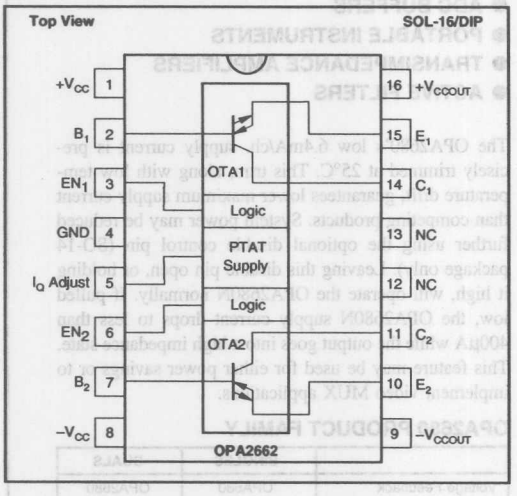
# SPECIFICATIONS (CONT)

## ELECTRICAL (Full Temperature Range –40°C to +85°C)

At $V_{CC}$ = ±5VDC, $R_Q$ = 750Ω, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted, and configured as noted under "CONDITIONS".

| PARAMETER | CONDITIONS | OPA2662AP, AU | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **OTA INPUT OFFSET VOLTAGE** | $R_E$ = 50kΩ, $R_C$ = 40Ω | | | | |
| Initial | | | 12 | ±36 | mV |
| Matching | | | 2 | ±7.2 | mV |
| **OTA INPUT BIAS CURRENT** | $R_E$ = 100Ω, $R_C$ = 40Ω | | | | |
| Initial | | –1.9 | 1 | 5.9 | µA |
| Matching | | –1.2 | 0.2 | 1.2 | µA |
| **OTA TRANSCONDUCTANCE** | | | | | |
| Transconductance | $I_C$ = 75mA, $R_E$ = 0 | 580 | | 610 | mA/V |
| **OTA C-RATED OUTPUT** | | | | | |
| Output Voltage Compliance | $I_C$ = ±5mA, $R_E$ = 100Ω, $R_C$ = 16Ω | ±3.2 | | | V |
| **POWER SUPPLY** | | | | | |
| Positive Quiescent Current for both OTAs[4] | $R_Q$ = 750Ω, $R_E$ = 50kΩ, $R_C$ = 1kΩ, Both Channels Selected | +8 | +17 | +25 | mA |

## PIN CONFIGURATION




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | ±6V |
| Input Voltage[1] | $\pm V_{CC}$ to ±0.7V |
| Operating Temperature | –40°C to +85°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +175°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Digital Input Voltages ($EN_1$, $EN_2$) | –0.5 to $+V_{CC}$ +0.7V |

NOTE: (1) Inputs are internally diode-clamped to $\pm V_{CC}$.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| OPA2662AP | 16-Pin Plastic DIP | 180 | –40°C to +85°C |
| OPA2662AU | SOL-16 Surface Mount | 211 | –40°C to +85°C |

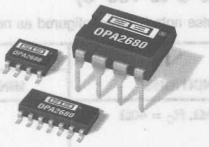
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. ESD can cause damage ranging from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

Burr-Brown's standard ESD test method consists of five 1000V positive and negative discharges (100pF in series with 1.5kΩ) applied to each pin.

BURR - BROWN®



# OPA2680

www.burr-brown.com/databook/OPA2680.html

## SpeedPlus™ Dual Wideband, Voltage Feedback OPERATIONAL AMPLIFIER With Disable

## FEATURES

- WIDEBAND +5V OPERATION: 220MHz (G = 2)
- HIGH OUTPUT CURRENT: 150mA
- OUTPUT VOLTAGE SWING: ±4.0V
- HIGH SLEW RATE: 1800V/µs
- LOW SUPPLY CURRENT: 6.4mA/Ch.
- LOW DISABLED CURRENT: 200µA/Ch.
- ENABLE/DISABLE TIME: 25ns/100ns

## APPLICATIONS

- VIDEO LINE DRIVING
- xDSL LINE DRIVER/RECEIVER
- HIGH SPEED IMAGING CHANNELS
- ADC BUFFERS
- PORTABLE INSTRUMENTS
- TRANSIMPEDANCE AMPLIFIERS
- ACTIVE FILTERS

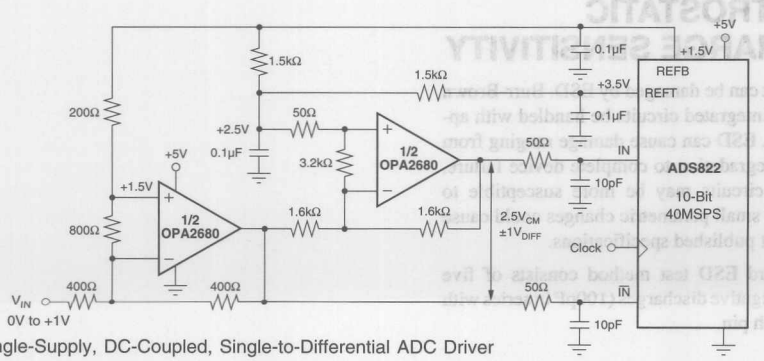
## DESCRIPTION

The OPA2680 represents a major step forward in unity gain stable, voltage feedback op amps. A new internal architecture provides slew rate and full power bandwidth previously found only in wideband current feedback op amps. A new output stage architecture delivers high currents with a minimal headroom requirement. These combine to give exceptional single supply operation. Using a single +5V supply, the OPA2680 can deliver a 1V to 4V output swing with over 100mA drive current and 150MHz bandwidth. This combination of features makes the OPA2680 an ideal RGB line driver or single supply ADC input driver.

The OPA2680's low 6.4mA/ch. supply current is precisely trimmed at 25°C. This trim, along with low temperature drift, guarantees lower maximum supply current than competing products. System power may be reduced further using the optional disable control pin (SO-14 package only). Leaving this disable pin open, or holding it high, will operate the OPA2680N normally. If pulled low, the OPA2680N supply current drops to less than 400µA while the output goes into a high impedance state. This feature may be used for either power savings or to implement video MUX applications.

### OPA2680 PRODUCT FAMILY

| | SINGLES | DUALS |
|---|---|---|
| Voltage Feedback | OPA680 | OPA2680 |
| Current Feedback | OPA681 | OPA2681 |




Single-Supply, DC-Coupled, Single-to-Differential ADC Driver

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS: $V_S$ = ±5V

$R_F$ = 402Ω, $R_L$ = 100Ω, and G = +2, (Figure 1 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA2680P, U, N TYP +25°C | GUARANTEED +25°C[2] | GUARANTEED 0°C to 70°C[3] | GUARANTEED –40°C to +85°C[3] | UNITS | MIN/ MAX | TEST LEVEL[1] |
|---|---|---|---|---|---|---|---|---|
| **AC PERFORMANCE (Figure 1)** | | | | | | | | |
| Small Signal Bandwidth | G = +1, $V_O$ = 0.5Vp-p, $R_F$ = 25Ω | 400 | | | | MHz | Typ | C |
| | G = +2, $V_O$ = 0.5Vp-p | 220 | 210 | 200 | 190 | MHz | Min | B |
| | G = +10, $V_O$ = 0.5Vp-p | 30 | 20 | — | — | MHz | Min | B |
| Gain-Bandwidth Product | G ≥ 10 | 300 | 200 | — | — | MHz | Min | B |
| Bandwidth for 0.1dB Gain Flatness | G = +2, $V_O$ < 0.5Vp-p | 30 | | | | MHz | Typ | C |
| Peaking at a Gain of +1 | $V_O$ < 0.5Vp-p | 4 | | | | dB | Typ | C |
| Large Signal Bandwidth | G = +2, $V_O$ = 5Vp-p | 175 | | | | MHz | Typ | C |
| Slew Rate | G = +2, 4V Step | 1800 | 1400 | 1200 | 900 | V/µs | Min | B |
| Rise/Fall Time | G = +2, $V_O$ = 0.5V Step | 1.4 | — | — | — | ns | Max | B |
| | G = +2, $V_O$ = 5V Step | 2.8 | — | — | — | ns | Max | B |
| Settling Time to 0.02% | G = +2, $V_O$ = 2V Step | — | | | | ns | Typ | C |
| 0.1% | G = +2, $V_O$ = 2V Step | — | | | | ns | Typ | C |
| Harmonic Distortion | G = +2, f = 5MHz, $V_O$ = 2Vp-p | | | | | | | |
| 2nd Harmonic | $R_L$ = 100Ω | –68 | –63 | — | — | dBc | Max | B |
| | $R_L$ ≥ 500Ω | –80 | –70 | — | — | dBc | Max | B |
| 3rd Harmonic | $R_L$ = 100Ω | –80 | –75 | — | — | dBc | Max | B |
| | $R_L$ ≥ 500Ω | –88 | –85 | — | — | dBc | Max | B |
| Channel-to-Channel Crosstalk | f = 5MHz | –70 | | | | dBc | Typ | C |
| Input Voltage Noise | f > 1MHz | 4.8 | — | — | — | nV/√Hz | Max | B |
| Input Current Noise | f > 1MHz | 2.5 | — | — | — | pA/√Hz | Max | B |
| Differential Gain | G = +2, NTSC, $V_O$ = 1.4Vp, $R_L$ = 150 | 0.05 | | | | % | Typ | C |
| Differential Phase | G = +2, NTSC, $V_O$ = 1.4Vp, $R_L$ = 150 | 0.03 | | | | deg | Typ | C |
| **DC PERFORMANCE[4]** | | | | | | | | |
| Open-Loop Voltage Gain ($A_{OL}$) | $V_O$ ±2V, $R_L$ = 100Ω | 62 | **56** | 54 | 52 | dB | Min | A |
| Input Offset Voltage | $V_{CM}$ = 0V | ±1.0 | **±4.5** | — | — | mV | Max | A |
| Average Offset Voltage Drift | $V_{CM}$ = 0V | | | — | — | µV/°C | Max | B |
| Input Bias Current | $V_{CM}$ = 0V | +8 | **+14** | — | — | µA | Max | A |
| Average Bias Current Drift | $V_{CM}$ = 0V | | | — | — | nA/°C | Max | B |
| Input Offset Current | $V_{CM}$ = 0V | ±0.1 | **±0.7** | — | — | µA | Max | A |
| Average Offset Current Drift | $V_{CM}$ = 0V | | | — | — | nA/°C | Max | B |
| **INPUT** | | | | | | | | |
| Common-Mode Input Range (CMIR)[5] | | ±3.5 | **±3.4** | — | — | V | Min | A |
| Common-Mode Rejection (CMR) | $V_{CM}$ = ±1V | 59 | **56** | — | — | dB | Min | A |
| Input Impedance | | | | | | | | |
| Differential-Mode | $V_{CM}$ = 0 | — | | | | kΩ II pF | Typ | C |
| Common-Mode | $V_{CM}$ = 0 | — | | | | MΩ II pF | Typ | C |
| **OUTPUT** | | | | | | | | |
| Voltage Output Swing | No Load | ±4.0 | **±3.8** | ±3.7 | ±3.6 | V | Min | A |
| | 100Ω Load | ±3.9 | **±3.7** | ±3.6 | ±3.3 | V | Min | A |
| Current Output, Sourcing | $V_O$ = 0 | +190 | **+160** | +140 | +80 | mA | Min | A |
| Current Output, Sinking | $V_O$ = 0 | –150 | **–135** | –130 | –80 | mA | Min | A |
| Closed-Loop Output Impedance | G = +2, f = 100kHz | 0.03 | | | | Ω | Typ | C |
| **DISABLE (SO-14 Only)** | Disabled Low | | | | | | | |
| Power Down Supply Current (+$V_S$) | $V_{\overline{DIS}}$ = 0, Both Channels | –400 | | | | µA | Typ | C |
| Disable Time | | 100 | | | | ns | Typ | C |
| Enable Time | | 25 | | | | ns | Typ | C |
| Off Isolation | G = +2, 5MHz | 70 | | | | dB | Typ | C |
| Output Capacitance in Disable | | 4 | | | | pF | Typ | C |
| Turn On Glitch | G = +2, $R_L$ = 150Ω, $V_{IN}$ = 0 | ±50 | | | | mV | Typ | C |
| Turn Off Glitch | G = +2, $R_L$ = 150Ω, $V_{IN}$ = 0 | ±20 | | | | mV | Typ | C |
| Enable Voltage | | 2.0 | **2.4** | — | — | V | Min | A |
| Disable Voltage | | 1.1 | **.8** | — | — | V | Max | A |
| Control Pin Input Bias Current ($V_{\overline{DIS}}$) | $V_{\overline{DIS}}$ = 0, Each Channel | 100 | **160** | — | — | µA | Max | A |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | ±5 | | | | V | Typ | C |
| Maximum Operating Voltage Range | | | **±6** | ±6 | ±6 | V | Max | A |
| Max Quiescent Current | $V_S$ = ±5V | 12.8 | **13.6** | 14.0 | 14.4 | mA | Max | A |
| Min Quiescent Current | $V_S$ = ±5V | 12.8 | **12.0** | 12.0 | 10.6 | mA | Min | A |
| Power Supply Rejection (+PSR) | Input Referred | 70 | **60** | — | — | dB | Min | A |
| **THERMAL CHARACTERISTICS** | | | | | | | | |
| Specified Operating Range P, U, N Package | | –40 to +85 | | | | °C | Typ | C |
| Thermal Resistance, $\theta_{JA}$ | Junction-to-Ambient | | | | | | | |
| P 8-Pin DIP | | 100 | | | | °C/W | Typ | C |
| U SO-8 | | 125 | | | | °C/W | Typ | C |
| N SO-14 | | 100 | | | | °C/W | Typ | C |

NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction Temperature = Ambient for 25°C guaranteed specifications. (3) Junction Temperature = Ambient at low temperature limit: Junction Temperature = Ambient +23°C at high temperature limit for over temperature guaranteed specifications. (4) Current is considered positive out of node. $V_{CM}$ is the input common-mode voltage. (5) Tested < 3dB below minimum CMR specification at ±CMIR limits.

# SPECIFICATIONS: $V_S$ = +5V

$R_F$ = 402Ω, $R_L$ = 100Ω to $V_S$/2, G = +2, (Figure 2 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA2680P, U, N TYP +25°C | GUARANTEED +25°C[2] | GUARANTEED 0°C to 70°C[3] | GUARANTEED –40°C to +85°C[3] | UNITS | MIN/ MAX | TEST LEVEL[1] |
|---|---|---|---|---|---|---|---|---|
| **AC PERFORMANCE (Figure 2)** | | | | | | | | |
| Small Signal Bandwidth | G = +1, $V_O$ < 0.5Vp-p, $R_F$ = ±25Ω | 300 | | | | MHz | Typ | C |
| | G = +2, $V_O$ < 0.5Vp-p | 220 | 120 | — | — | MHz | Min | B |
| | G = +10, $V_O$ < 0.5Vp-p | 25 | — | — | — | MHz | Min | B |
| Gain-Bandwidth Product | G ≥ 10 | 250 | — | — | — | MHz | Min | B |
| Bandwidth for 0.1dB Gain Flatness | G = +2, $V_O$ < 0.5Vp-p | 20 | | | | MHz | Typ | C |
| Peaking at a Gain of +1 | $V_O$ < 0.5Vp-p | 5 | | | | dB | Typ | C |
| Large Signal Bandwidth | G = +2, $V_O$ = 2Vp-p | 200 | | | | MHz | Typ | C |
| Slew Rate | G = +2, 2V Step | 1000 | 700 | — | — | V/µs | Min | B |
| Rise/Fall Time | G = +2, $V_O$ = 0.5V Step | 1.6 | | | | ns | Typ | C |
| | G = +2, $V_O$ = 2V Step | 2.0 | | | | ns | Typ | C |
| Settling Time to 0.02% | G = +2, $V_O$ = 2V Step | — | | | | ns | Typ | C |
| 0.1% | G = +2, $V_O$ = 2V Step | — | | | | ns | Typ | C |
| Harmonic Distortion | G = +2, f = 5MHz, $V_O$ = 2Vp-p | | | | | | | |
| 2nd Harmonic | $R_L$ = 100Ω to $V_S$/2 | –60 | — | — | — | dBc | Max | B |
| | $R_L$ ≥ 500Ω to $V_S$/2 | –70 | — | — | — | dBc | Max | B |
| 3rd Harmonic | $R_L$ = 100Ω to $V_S$/2 | –72 | — | — | — | dBc | Max | B |
| | $R_L$ ≥ 500Ω to $V_S$/2 | –80 | — | — | — | dBc | Max | B |
| Channel-to-Channel Crosstalk | f = 5MHz | –70 | | | | dBc | Typ | C |
| Input Voltage Noise | f > 1MHz | 5 | — | — | — | nV/√Hz | Max | B |
| Input Current Noise | f > 1MHz | 2.5 | — | — | — | pA/√Hz | Max | B |
| Differential Gain | G = +2, NTSC, $V_O$ = 1.4Vp, $R_L$ = 150 to $V_S$/2 | 0.06 | | | | % | Typ | C |
| Differential Phase | G = +2, NTSC, $V_O$ = 1.4Vp, $R_L$ = 150 to $V_S$/2 | 0.03 | | | | deg | Typ | C |
| **DC PERFORMANCE[4]** | | | | | | | | |
| Open-Loop Voltage Gain | $V_O$ = 2.5V, $R_L$ = 100Ω to 2.5V | 62 | **56** | — | — | dB | Min | A |
| Input Offset Voltage | $V_{CM}$ = 2.5V | ±2.0 | **±6.0** | — | — | mV | Max | A |
| Average Offset Voltage Drift | $V_{CM}$ = 2.5V | | | — | — | µV/°C | Max | B |
| Input Bias Current | $V_{CM}$ = 2.5V | +8 | **+15** | — | — | µA | Max | A |
| Average Bias Current Drift | $V_{CM}$ = 2.5V | | | — | — | nA/°C | Max | B |
| Input Offset Current | $V_{CM}$ = 2.5V | ±0.1 | **±0.6** | — | — | µA | Max | A |
| Average Offset Current Drift | $V_{CM}$ = 2.5V | | | — | — | nA/°C | Max | B |
| **INPUT** | | | | | | | | |
| Least Positive Input Voltage[5] | | 1.5 | **1.6** | — | — | V | Max | A |
| Most Positive Input Voltage[5] | | 3.5 | **3.4** | — | — | V | Min | A |
| Common-Mode Rejection (CMR) | $V_{CM}$ = 2.5V ±0.5V | 59 | **56** | | | dB | Min | A |
| Input Impedance | | | | | | | | |
| Differential-Mode | $V_{CM}$ = 2.5V | — | | | | kΩ ll pF | Typ | C |
| Common-Mode | $V_{CM}$ = 2.5V | — | | | | MΩ ll pF | Typ | C |
| **OUTPUT** | | | | | | | | |
| Most Positive Output Voltage | No Load | 4 | **3.8** | 3.6 | 3.5 | V | Min | A |
| | $R_L$ = 100Ω to 2.5V | 3.9 | **3.7** | 3.5 | 3.4 | V | Min | A |
| Least Positive Output Voltage | No Load | 1 | **1.2** | 1.4 | 1.5 | V | Max | A |
| | $R_L$ = 100Ω to 2.5V | 1.1 | **1.3** | 1.5 | 1.7 | V | Max | A |
| Current Output, Sourcing | | +150 | **+110** | +110 | +60 | mA | Min | A |
| Current Output, Sinking | | –110 | **–80** | –70 | –50 | mA | Min | A |
| Closed-Loop Output Impedance | G =+2, f = 100kHz | 0.03 | | | | Ω | Typ | C |
| **DISABLE (SO-14 Only)** | Disabled Low | | | | | | | |
| Power Down Supply Current (+$V_S$) | $V_{\overline{DIS}}$ = 0, Both Channels | –260 | | | | µA | Typ | C |
| Disable Time | | 100 | | | | ns | Typ | C |
| Enable Time | | 25 | | | | ns | Typ | C |
| Off Isolation | G = +2, 5MHz | 65 | | | | dB | Typ | C |
| Output Capacitance in Disable | | 4 | | | | pF | Typ | C |
| Turn On Glitch | G = +2, $R_L$ = 150Ω, $V_{IN}$ = $V_S$/2 | ±50 | | | | mV | Typ | C |
| Turn Off Glitch | G = +2, $R_L$ = 150Ω, $V_{IN}$ = $V_S$/2 | ±20 | | | | mV | Typ | C |
| Enable Voltage | | 2.0 | **2.4** | — | — | V | Min | A |
| Disable Voltage | | 1.1 | **.8** | — | — | V | Max | A |
| Control Pin Input Bias Current ($V_{\overline{DIS}}$) | $V_{\overline{DIS}}$ = 0, Each Channel | 100 | | | | µA | Typ | C |
| **POWER SUPPLY** | | | | | | | | |
| Specified Single Supply Operating Voltage | | 5 | | | | V | Typ | C |
| Maximum Single Supply Operating Voltage | | | 12 | 12 | 12 | V | Max | B |
| Max Quiescent Current | $V_S$ = +5V | 10.2 | **12.0** | 12.0 | 12.0 | mA | Max | A |
| Min Quiescent Current | $V_S$ = +5V | 10.2 | **8.0** | 8.0 | 7.6 | mA | Min | A |
| Power Supply Rejection (+PSR) | Input Referred | 59 | | | | dB | Typ | C |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: P, U, N | | –40 to +85 | | | | °C | Typ | C |
| Thermal Resistance, $\theta_{JA}$ | Junction-to-Ambient | | | | | | | |
| P 8-Pin DIP | | 100 | | | | °C/W | Typ | C |
| U SO-8 | | 125 | | | | °C/W | Typ | C |
| N SO-14 | | 100 | | | | °C/W | Typ | C |

NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction Temperature = Ambient for 25°C guaranteed specifications. (3) Junction Temperature = Ambient at low temperature limit: Junction Temperature = Ambient +23°C at high temperature limit for over temperature guaranteed specifications. (4) Current is considered positive out of node. $V_{CM}$ is the input common-mode voltage. (5) Tested < 3dB below minimum CMR specification at ±CMIR limits.

## ABSOLUTE MAXIMUM RATINGS

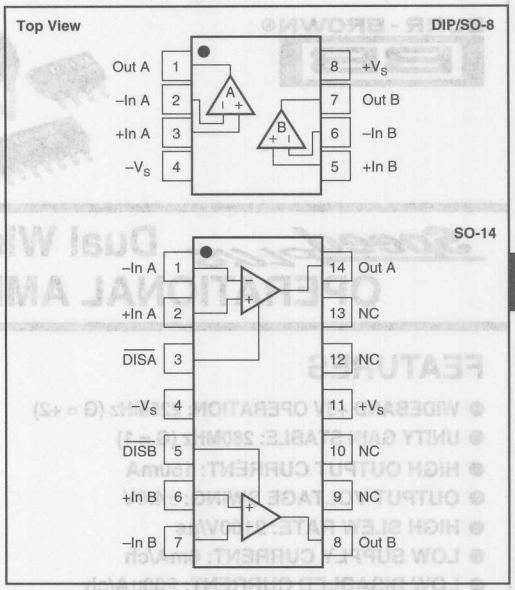
| | |
|---|---|
| Power Supply | ±6.5VDC |
| Internal Power Dissipation | See Thermal Analysis |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: P, U, N | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SOIC 3s) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATIONS



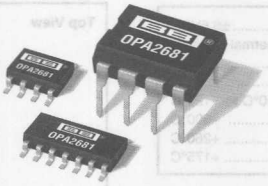

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER |
|---|---|---|---|---|---|
| OPA2680P | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA2680P | Contact Factory for Availability |
| OPA2680U | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA2680U | OPA2680U |
| OPA2680N | SO-14 Surface Mount | 235 | –40°C to +85°C | OPA2680N | Contact Factory for Availability |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

BURR - BROWN®



# OPA2681

www.burr-brown.com/databook/OPA2681.html

## SpeedPLUS™ Dual Wideband, Current Feedback OPERATIONAL AMPLIFIER With Disable

## FEATURES

- WIDEBAND +5V OPERATION: 225MHz (G = +2)
- UNITY GAIN STABLE: 280MHz (G = 1)
- HIGH OUTPUT CURRENT: 150mA
- OUTPUT VOLTAGE SWING: ±4.0V
- HIGH SLEW RATE: 2100V/µs
- LOW SUPPLY CURRENT: 6mA/ch
- LOW DISABLED CURRENT: 200µA/ch
- ENABLE/DISABLE TIME: 25ns/100ns

## APPLICATIONS

- xDSL LINE DRIVER
- BROADBAND VIDEO BUFFERS
- HIGH SPEED IMAGING CHANNELS
- PORTABLE INSTRUMENTS
- ADC BUFFERS
- ACTIVE FILTERS
- WIDEBAND INVERTING SUMMING

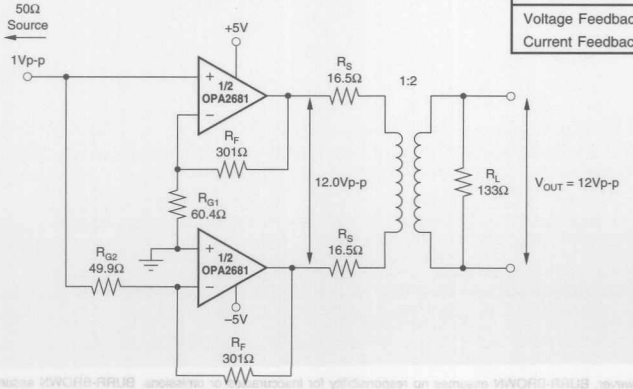
## DESCRIPTION

The OPA2681 sets a new level of performance for broadband dual current feedback op amps. Operating on a very low 6mA/ch supply current, the OPA2681 offers a slew rate and output power normally associated with a much higher supply current. A new output stage architecture delivers a high output current with minimal voltage headroom and crossover distortion. This gives exceptional single supply operation. Using a single +5V supply, the OPA2681 can deliver a 1V to 4V output swing with over 100mA drive current and 150MHz bandwidth. This combination of features makes the OPA2681 an ideal RGB line driver or single supply ADC input driver.

The OPA2681's low 6mA/ch supply current is precisely trimmed at 25°C. This trim, along with low drift over temperature, guarantees lower guaranteed maximum supply current than competing products. System power may be further reduced by using the optional disable control pin (SO-14 only). Leaving this disable pin open, or holding it high, gives normal operation. If pulled low, the OPA2681 supply current drops to less than 400µA while the output goes into a high impedance state. This feature may be used for either power savings or for video MUX applications.

### OPA2681 PRODUCT FAMILY

| | SINGLES | DUALS |
|---|---|---|
| Voltage Feedback | OPA680 | OPA2680 |
| Current Feedback | OPA681 | OPA2681 |




**High Power Twisted Pair Driver**

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS: $V_S$ = ±5V

$R_F$ = 402Ω, $R_L$ = 100Ω, and G = +2, (Figure 1 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA2681P, U, N TYP +25°C | GUARANTEED +25°C[2] | GUARANTEED 0°C to 70°C[3] | GUARANTEED –40°C to +85°C[3] | UNITS | MIN/ MAX | TEST LEVEL[1] |
|---|---|---|---|---|---|---|---|---|
| **AC PERFORMANCE (Figure 1)** | | | | | | | | |
| Small Signal Bandwidth ($V_O$ = 0.5Vp-p) | G = +1, $R_F$ = 453Ω | 280 | | | | MHz | Typ | C |
| | G = +2, $R_F$ = 402Ω | 220 | 220 | 210 | 190 | MHz | Min | B |
| | G = +5, $R_F$ = 261Ω | 185 | | | | MHz | Typ | C |
| | G = +10, $R_F$ = 180Ω | 125 | | | | MHz | Typ | C |
| Bandwidth for 0.1dB Gain Flatness | G = +2, $V_O$ = 0.5Vp-p | 90 | | | | MHz | Typ | C |
| Peaking at a Gain of +1 | $R_F$ = 453, $V_O$ = 0.5Vp-p | 0.4 | 2 | 4 | — | dB | Max | B |
| Large Signal Bandwidth | G = +2, $V_O$ = 5Vp-p | 150 | | | | MHz | Typ | C |
| Slew Rate | G = +2, 4V Step | 2100 | 1600 | 1600 | 1200 | V/µs | Min | B |
| Rise/Fall Time | G = +2, $V_O$ = 0.5V Step | 1.7 | — | — | — | ns | Max | B |
| | G = +2, 5V Step | 2.0 | — | — | — | ns | Max | B |
| Settling Time to 0.02% | G = +2, $V_O$ = 2V Step | 12 | | | | ns | Typ | C |
| 0.1% | G = +2, $V_O$ = 2V Step | 8 | | | | ns | Typ | C |
| Harmonic Distortion | G = +2, f = 5MHz, $V_O$ = 2Vp-p | | | | | | | |
| 2nd Harmonic | $R_L$ = 100Ω | –79 | –73 | — | — | dBc | Max | B |
| | $R_L$ ≥ 500Ω | –85 | –82 | — | — | dBc | Max | B |
| 3rd Harmonic | $R_L$ = 100Ω | –74 | –71 | — | — | dBc | Max | B |
| | $R_L$ ≥ 500Ω | –77 | –75 | — | — | dBc | Max | B |
| Input Voltage Noise | f > 1MHz | 2.5 | 3.0 | 3.4 | 3.6 | nV/√Hz | Max | B |
| Non-Inverting Input Current Noise | f > 1MHz | 12 | — | — | — | pA/√Hz | Max | B |
| Inverting Input Current Noise | f > 1MHz | 15 | — | — | — | pA/√Hz | Max | B |
| Differential Gain | G = +2, NTSC, $V_O$ = 1.4Vp, $R_L$ = 150Ω | 0.001 | | | | % | Typ | C |
| | $R_L$ = 37.5Ω | 0.005 | | | | % | Typ | C |
| Differential Phase | G = +2, NTSC, $V_O$ = 1.4Vp, $R_L$ = 150Ω | 0.01 | | | | deg | Typ | C |
| | $R_L$ = 37.5Ω | 0.05 | | | | deg | Typ | C |
| Channel-to-Channel Crosstalk | f = 5MHz | –70 | | | | dBc | Typ | C |
| **DC PERFORMANCE[4]** | | | | | | | | |
| Open-Loop Transimpedance Gain ($Z_{OL}$) | $V_O$ ±2V, $R_L$ = 100Ω | 100 | **50** | 50 | 50 | kΩ | Min | A |
| Input Offset Voltage | $V_{CM}$ = 0V | ±1.3 | **±5** | ±6.5 | ±7.5 | mV | Max | A |
| Average Offset Voltage Drift | $V_{CM}$ = 0V | | | +35 | +40 | µV/°C | Max | B |
| Non-Inverting Input Bias Current | $V_{CM}$ = 0V | +30 | **+55** | ±65 | ±85 | µA | Max | A |
| Average Non-Inverting Input Bias Current Drift | $V_{CM}$ = 0V | | | –400 | –450 | nA/°C | Max | B |
| Inverting Input Bias Current | $V_{CM}$ = 0V | ±10 | **±40** | ±50 | ±55 | µA | Max | A |
| Average Inverting Input Bias Current Drift | $V_{CM}$ = 0V | | | –125 | –150 | nA°/C | Max | B |
| **INPUT** | | | | | | | | |
| Common-Mode Input Range[5] | | ±3.5 | **±3.4** | — | — | V | Min | A |
| Common-Mode Rejection | $V_{CM}$ = ±1.0V | 52 | **47** | 46 | 45 | dB | Min | A |
| Non-Inverting Input Impedance | | 100 ll 2 | | | | kΩ ll pF | Typ | C |
| Minimum Inverting Input Resistance ($R_I$) | Open Loop | 45 | **30** | 30 | 30 | Ω | Min | A |
| Maximum Inverting Input Resistance ($R_I$) | Open Loop | 45 | **52** | 54 | 60 | Ω | Max | A |
| **OUTPUT** | | | | | | | | |
| Voltage Output Swing | No Load | ±4.0 | **±3.8** | — | — | V | Min | A |
| | 100Ω Load | ±3.9 | **±3.7** | ±3.6 | ±3.3 | V | Min | A |
| Current Output, Sourcing | $V_O$ = 0 | +190 | **+160** | +140 | +80 | mA | Min | A |
| Current Output, Sinking | $V_O$ = 0 | –150 | **–135** | –130 | –80 | mA | Min | A |
| Closed-Loop Output Impedance | G = +2, f = 100kHz | 0.03 | | | | Ω | Typ | C |
| **DISABLE (Disabled Low) (SO-14 only)** | | | | | | | | |
| Power Down Supply Current (+$V_S$) | $V_{\overline{DIS}}$ = 0, Both Channels | –400 | | | | µA | Typ | C |
| Disable Time | | 100 | | | | ns | Typ | C |
| Enable Time | | 25 | | | | ns | Typ | C |
| Off Isolation | G = +2, 5MHz | 70 | | | | dB | Typ | C |
| Output Capacitance in Disable | | 4 | | | | pF | Typ | C |
| Turn On Glitch | G = +2, $R_L$ = 150Ω, $V_{IN}$ = 0 | ±50 | | | | mV | Typ | C |
| Turn Off Glitch | G = +2, $R_L$ = 150Ω, $V_{IN}$ = 0 | ±20 | | | | mV | Typ | C |
| Enable Voltage | | 2.0 | **2.4** | — | — | V | Min | A |
| Disable Voltage | | 1.1 | **.8** | — | — | V | Max | A |
| Control Pin Input Bias Current ($\overline{DIS}$) | $V_{\overline{DIS}}$ = 0, Each Channel | 100 | **160** | — | — | µA | Max | A |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | ±5 | | | | V | Typ | C |
| Maximum Operating Voltage Range | | | **±6** | ±6 | ±6 | V | Max | A |
| Max Quiescent Current | $V_S$ = ±5V | 12 | **12.8** | 13 | 13.2 | mA | Max | A |
| Min Quiescent Current | $V_S$ = ±5V | 12 | **11.2** | 11 | 10 | mA | Min | A |
| Power Supply Rejection Ratio (–PSR) | Input Referred | 58 | | | | dB | Typ | C |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: P, U, N | | –40 to +85 | | | | °C | Typ | C |
| Thermal Resistance, $\theta_{JA}$ | Junction-to-Ambient | | | | | | | |
| P 8-Pin DIP | | 100 | | | | °C/W | Typ | C |
| U SO-8 | | 125 | | | | °C/W | Typ | C |
| N SO-14 | | 100 | | | | °C/W | Typ | C |

NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction Temperature = Ambient for 25°C guaranteed specifications. (3) Junction Temperature = Ambient at low temperature limit: Junction Temperature = Ambient +23°C at high temperature limit for over temperature guaranteed specifications. (4) Current is considered positive out of node. $V_{CM}$ is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMR at ± CMIR limits.

# SPECIFICATIONS: $V_S$ = +5V

$R_F$ = 499Ω, $R_L$ = 100Ω to $V_S$/2, G = +2, (Figure 2 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA681P, U, N TYP +25°C | GUARANTEED +25°C[2] | GUARANTEED 0°C to 70°C[3] | GUARANTEED –40°C to +85°C[3] | UNITS | MIN/ MAX | TEST LEVEL[1] |
|---|---|---|---|---|---|---|---|---|
| **AC PERFORMANCE (Figure 2)** | | | | | | | | |
| Small Signal Bandwidth ($V_O$ = 0.5Vp-p) | G = +1, $R_F$ = 649Ω | 250 | | | | MHz | Typ | C |
| | G = +2, $R_F$ = 499Ω | 225 | 180 | — | — | MHz | Min | B |
| | G = +5, $R_F$ = 360Ω | 180 | | | | MHz | Typ | C |
| | G = +10, $R_F$ = 200Ω | 165 | | | | MHz | Typ | C |
| Bandwidth for 0.1dB Gain Flatness | G = +2, $V_O$ < 0.5Vp-p | 150 | 60 | 35 | — | MHz | Min | B |
| Peaking at a Gain of +1 | $R_F$ = 649Ω, $V_O$ < 0.5Vp-p | 0.4 | 2 | 4 | — | dB | Max | B |
| Large Signal Bandwidth | G = +2, $V_O$ = 2Vp-p | 200 | — | — | — | MHz | Min | B |
| Slew Rate | G = +2, 2V Step | 830 | 700 | — | — | V/µs | Min | B |
| Rise/Fall Time | G = +2, $V_O$ = 0.5V Step | 1.5 | — | — | — | ns | Max | B |
| | G = +2, $V_O$ = 2V Step | 2.0 | — | — | — | ns | Max | B |
| Settling Time to 0.02% | G = +2, $V_O$ = 2V Step | — | | | | ns | Typ | C |
| 0.1% | G = +2, $V_O$ = 2V Step | — | | | | ns | Typ | C |
| Harmonic Distortion | G = +2, f = 5MHz, $V_O$ = 2Vp-p | | | | | | | |
| 2nd Harmonic | $R_L$ = 100Ω to $V_S$/2 | –64 | — | — | — | dBc | Max | B |
| | $R_L$ ≥ 500Ω to $V_S$/2 | –72 | — | — | — | dBc | Max | B |
| 3rd Harmonic | $R_L$ = 100Ω to $V_S$/2 | –72 | — | — | — | dBc | Max | B |
| | $R_L$ ≥ 500Ω to $V_S$/2 | –73 | — | — | — | dBc | Max | B |
| Input Voltage Noise | f > 1MHz | 2.2 | 3 | 3.4 | 3.6 | nV/√Hz | Max | B |
| Non-Inverting Input Current Noise | f > 1MHz | 12 | — | — | — | pA/√Hz | Max | B |
| Inverting Input Current Noise | f > 1MHz | 15 | — | — | — | pA/√Hz | Max | B |
| **DC PERFORMANCE[4]** | | | | | | | | |
| Open-Loop Transimpedance Gain ($Z_{OL}$) | $V_O$ = $V_S$/2, $R_L$ = 100Ω to $V_S$/2 | 100 | 60 | — | — | kΩ | Min | A |
| Input Offset Voltage | $V_{CM}$ = 2.5V | ±1 | ±4 | ±6.0 | ±7 | mV | Max | A |
| Average Offset Voltage Drift | $V_{CM}$ = 2.5V | | | +15 | +20 | µV/°C | Max | B |
| Non-Inverting Input Bias Current | $V_{CM}$ = 2.5V | +40 | +65 | +75 | +95 | µA | Max | A |
| Average Non-Inverting Input Bias Current Drift | $V_{CM}$ = 2.5V | | | –300 | –350 | nA/°C | Max | B |
| Inverting Input Bias Current | $V_{CM}$ = 2.5V | ±5 | ±20 | ±25 | ±35 | µA | Max | A |
| Average Inverting Input Bias Current Drift | $V_{CM}$ = 2.5V | | | –125 | –175 | nA/°C | Max | B |
| **INPUT** | | | | | | | | |
| Least Positive Input Voltage[5] | | 1.5 | 1.6 | — | — | V | Max | A |
| Most Positive Input Voltage[5] | | 3.5 | 3.4 | — | — | V | Min | A |
| Common-Mode Rejection (CMR) | $V_{CM}$ = 2.5V | 51 | 45 | — | — | dB | Min | A |
| Non-Inverting Input Impedance | | 100 ll 2 | | | | kΩ ll pF | Typ | C |
| Minimum Inverting Input Resistance ($R_I$) | Open Loop | 45 | 32 | — | — | Ω | Min | A |
| Maximum Inverting Input Resistance ($R_I$) | Open Loop | 45 | 59 | — | — | Ω | Max | A |
| **OUTPUT** | | | | | | | | |
| Most Positive Output Voltage | $R_I$ = 1kΩ, 2.5V | 4 | 3.8 | 3.7 | 3.5 | V | Min | A |
| | $R_I$ = 100Ω, 2.5V | 3.9 | 3.7 | 3.6 | 3.4 | V | Min | A |
| Least Positive Output Voltage | $R_I$ = 1kΩ, 2.5V | 1 | 1.2 | 1.3 | 1.5 | V | Max | A |
| | $R_I$ = 100Ω, 2.5V | 1.1 | 1.3 | 1.4 | 1.6 | V | Max | A |
| Current Output, Sourcing | $V_O$ = $V_S$/2 | 150 | 110 | — | — | mA | Min | A |
| Current Output, Sinking | $V_O$ = $V_S$/2 | –110 | –90 | — | — | mA | Min | A |
| Closed-Loop Output Impedance | G = +2, f = 100kHz | 0.03 | | | | Ω | Typ | C |
| **DISABLE (Disable Low) (SO-14 only)** | | | | | | | | |
| Power Down Supply Current (+$V_S$) | $V_{\overline{DIS}}$ = 0, Both Channels | –260 | | | | µA | Typ | C |
| Disable Time | | 100 | | | | ns | Typ | C |
| Enable Time | | 25 | | | | ns | Typ | C |
| Off Isolation | G = +2, 5MHz | 65 | | | | dB | Typ | C |
| Output Capacitance in Disable | | 4 | | | | pF | Typ | C |
| Turn On Glitch | G = +2, $R_L$ = 150Ω, $V_{IN}$ = $V_S$/2 | ±50 | | | | mV | Typ | C |
| Turn Off Glitch | G = +2, $R_L$ = 150Ω, $V_{IN}$ = $V_S$/2 | ±20 | | | | mV | Typ | C |
| Enable Voltage | | 2.0 | 2.4 | — | — | V | Min | A |
| Disable Voltage | | 1.1 | .8 | — | — | V | Max | A |
| Control Pin Input Bias Current ($\overline{DIS}$) | $V_{\overline{DIS}}$ = 0, Each Channel | 100 | | | | µA | Typ | C |
| **POWER SUPPLY** | | | | | | | | |
| Specified Single Supply Operating Voltage | | 5 | | | | V | Typ | C |
| Maximum Single Supply Operating Voltage | | | 12 | 12 | 12 | V | Max | A |
| Max Quiescent Current | $V_S$ = +5V | 9.6 | 10.6 | 10.8 | 10.8 | mA | Max | A |
| Min Quiescent Current | $V_S$ = +5V | 9.6 | 8.2 | 8.0 | 8.0 | mA | Min | A |
| Power Supply Rejection Ratio (+PSR) | Input Referred | 50 | | | | dB | Typ | C |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: P, U, E, N | | –40 to +85 | | | | °C | Typ | C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| P 8-Pin DIP | | 100 | | | | °C/W | Typ | C |
| U SO-8 | | 125 | | | | °C/W | Typ | C |
| N SO-14 | | 100 | | | | °C/W | Typ | C |

NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction Temperature = Ambient for 25°C guaranteed specifications. (3) Junction Temperature = Ambient at low temperature limit: Junction Temperature = Ambient +23°C at high temperature limit for over temperature guaranteed specifications. (4) Current is considered positive out of node. $V_{CM}$ is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMR at ±CMIR limits.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply | ±6.5VDC |
| Internal Power Dissipation[1] | See Thermal Information |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: P, U, N | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SO-8 3s) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

NOTE: (1) Packages must be derated based on specified $\theta_{JA}$. Maximum $T_J$ must be observed.

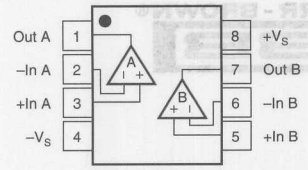
## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

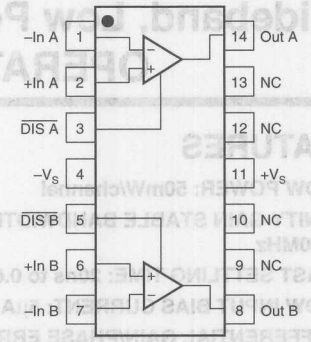
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATIONS

Top View — DIP/SO-8



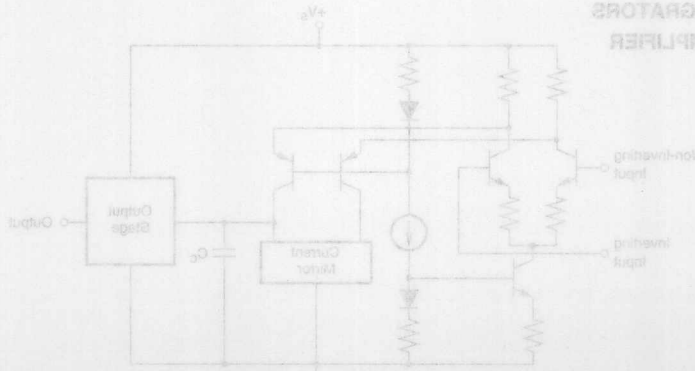

SO-14




## PACKAGE/ORDERING INFORMATION

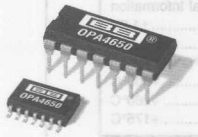
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER |
|---|---|---|---|---|---|
| OPA2681P | 8-Pin Plastic DIP | 006 | –40°C to +85°C | OPA2681P | Contact Factory for Availability |
| OPA2681U | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA2681U | OPA2681U |
| OPA2681N | SO-14 Surface Mount | 235 | –40°C to +85°C | OPA2681N | Contact Factory for Availability |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



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# OPA4650

**DEMO BOARD AVAILABLE**
**See Appendix A**

www.burr-brown.com/databook/OPA4650.html

# Wideband, Low Power, Quad Voltage Feedback OPERATIONAL AMPLIFIER

## FEATURES

- LOW POWER: 50mW/channel
- UNITY GAIN STABLE BANDWIDTH: 360MHz
- FAST SETTLING TIME: 20ns to 0.01%
- LOW INPUT BIAS CURRENT: 5μA
- DIFFERENTIAL GAIN/PHASE ERROR: 0.01%/0.025°
- 14-PIN DIP and SO-14 SURFACE MOUNT PACKAGES AVAILABLE

## APPLICATIONS

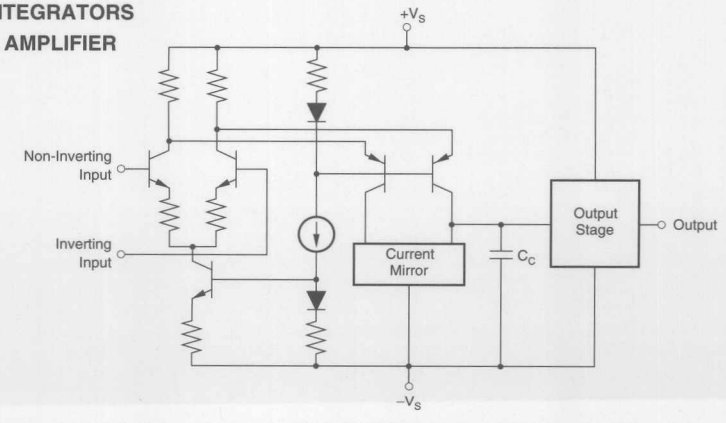
- HIGH RESOLUTION VIDEO
- MONITOR PREAMPLIFIER
- CCD IMAGING AMPLIFIER
- ULTRASOUND SIGNAL PROCESSING
- ADC/DAC BUFFER AMPLIFIER
- ACTIVE FILTERS
- HIGH SPEED INTEGRATORS
- DIFFERENTIAL AMPLIFIER

## DESCRIPTION

The OPA4650 is a quad, low power, wideband voltage feedback operational amplifier. It features a high bandwidth of 360MHz as well as a 12-bit settling time of only 20ns. The low input bias current allows its use in high speed integrator applications, while the wide bandwidth and true differential input stage make it suitable for use in a variety of active filter applications. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA4650 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Its unusual combination of speed, accuracy and low power make it an outstanding choice for many portable, multi-channel and other high speed applications, where power is at a premium.

The OPA4650 is also available in single (OPA650) and dual (OPA2650) configurations.




Simplified Schematic
1 of 4 Channels

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = ±5V, $R_L$ = 100Ω, and $R_{FB}$ = 402Ω, unless otherwise noted. $R_{FB}$ = 25Ω for a gain of +1.

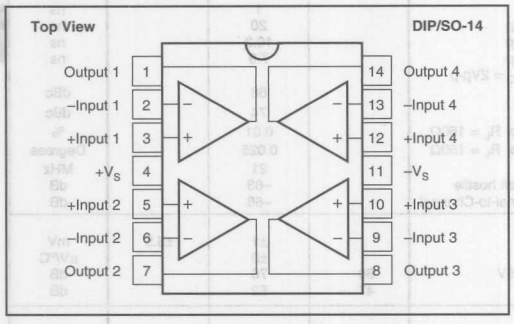
| PARAMETER | CONDITIONS | OPA4650P, U MIN | OPA4650P, U TYP | OPA4650P, U MAX | UNITS |
|---|---|---|---|---|---|
| **FREQUENCY RESPONSE** | | | | | |
| Closed-Loop Bandwidth[1] | G = +1 | | 360 | | MHz |
| | G = +2 | | 120 | | MHz |
| | G = +5 | | 35 | | MHz |
| | G = +10 | | 16 | | MHz |
| Gain Bandwidth Product | | | 160 | | MHz |
| Slew Rate[2] | G = +1, 2V Step | | 240 | | V/µs |
| Over Specified Temperature | | | 220 | | V/µs |
| Rise Time | 0.2V Step | | 1 | | ns |
| Fall Time | 0.2V Step | | 1 | | ns |
| Settling Time 0.01% | G = +1, 2V Step | | 20 | | ns |
| 0.1% | G = +1, 2V Step | | 10.3 | | ns |
| 1% | G = +1, 2V Step | | 7.9 | | ns |
| Spurious Free Dynamic Range | G = +1, f = 5.0 MHz, $V_O$ = 2Vp-p | | | | |
| | $R_L$ = 100Ω | | 68 | | dBc |
| | $R_L$ = 402Ω | | 74 | | dBc |
| Differential Gain | G = +2, NTSC, $V_O$ = 1.4Vp, $R_L$ = 150Ω | | 0.01 | | % |
| Differential Phase | G = +2, NTSC, $V_O$ = 1.4Vp, $R_L$ = 150Ω | | 0.025 | | Degrees |
| Bandwidth for 0.1dB Flatness | G = +2 | | 21 | | MHz |
| Crosstalk | Input Referred, 5MHz, all hostile | | –63 | | dB |
| | Input Referred, 5MHz, Channel-to-Channel | | –66 | | dB |
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | | | ±1 | ±5.5 | mV |
| Average Drift | | | ±3 | | µV/°C |
| Power Supply Rejection (+$V_S$) | $\|V_S\|$ = 4.5V to 5.5V | 60 | 76 | | dB |
| (–$V_S$) | | 47 | 52 | | dB |
| **INPUT BIAS CURRENT** | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | 5 | 20 | µA |
| Over Temperature | | | | 30 | µA |
| Input Offset Current | $V_{CM}$ = 0V | | 0.5 | 1.0 | µA |
| Over Temperature | | | | 3.0 | µA |
| **INPUT NOISE** | | | | | |
| Input Voltage Noise | | | | | |
| Noise Density, f = 100Hz | | | 43 | | nV/√Hz |
| f = 10kHz | | | 9.4 | | nV/√Hz |
| f = 1MHz | | | 8.4 | | nV/√Hz |
| f = 1MHz to 100MHz | | | 8.4 | | nV/√Hz |
| Integrated Noise, BW = 10Hz to 100MHz | | | 84 | | µVp-p |
| Input Bias Current Noise | | | | | |
| Current Noise Density, f = 0.1MHz to 100MHz | | | 1.2 | | pA/√Hz |
| Noise Figure (NF) | | | | | |
| | $R_S$ = 10kΩ | | 4.0 | | dBm |
| | $R_S$ = 50Ω | | 19.5 | | dBm |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range | | | ±2.8 | | V |
| Over Specified Temperature | | ±2.2 | | | V |
| Common-Mode Rejection | $V_{CM}$ = ±0.5V | 65 | 90 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | 15 \|\| 1 | | kΩ \|\| pF |
| Common-Mode | | | 16 \|\| 1 | | MΩ \|\| pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±2V, $R_L$ = 100Ω | 45 | 51 | | dB |
| Over Specified Temperature | $V_O$ = ±2V, $R_L$ = 100Ω | 43 | | | dB |
| **OUTPUT** | | | | | |
| Voltage Output | | | | | |
| Over Specified Temperature | No Load | ±2.2 | ±3.0 | | V |
| | $R_L$ = 250Ω | ±2.2 | ±2.5 | | V |
| | $R_L$ = 100Ω | ±2.0 | ±2.3 | | V |
| Output Current, Sourcing | | 75 | 110 | | mA |
| Over Temperature Range | | 65 | | | mA |
| Output Current, Sinking | | 65 | 85 | | mA |
| Over Temperature Range | | 35 | | | mA |
| Short-Circuit Current | | | 150 | | mA |
| Output Resistance | 0.1MHz, G = +1 | | 0.08 | | Ω |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±5 | | V |
| Operating Voltage Range | | ±4.5 | | ±5.5 | V |
| Quiescent Current | All Channels | | ±23 | ±32 | mA |
| Over Specified Temperature | | | | ±35 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification: P, U | | –40 | | +85 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| P | | | 75 | | °C/W |
| U | | | 75 | | °C/W |

NOTES: (1) Frequency response can be strongly influenced by PC board parasites. The OPA4650 is nominally compensated assuming 2pF parasitic load. The demonstration board, DEM-OPA465xP, shows a low parasitic layout for this part. (2) Slew rate is rate of change from 10% to 90% of output voltage step.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Total Supply Voltage Across Device | 11V |
| Internal Power Dissipation | See Thermal Considerations |
| Differential Input Voltage | ±2.7V |
| Common-Mode Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: P, U, | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SOIC 3s) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

## PIN CONFIGURATION




## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| OPA4650U | SO-14 Surface Mount | 235 |
| OPA4650P | 14-Pin Plastic DIP | 010 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

| PRODUCT | PACKAGE | TEMPERATURE RANGE |
|---|---|---|
| OPA4650U | SO-14 Surface Mount | –40°C to +85°C |
| OPA4650P | 14-Pin Plastic DIP | –40°C to +85°C |

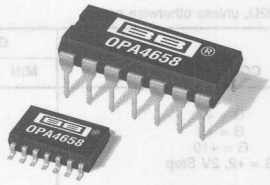
## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

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# OPA4658

www.burr-brown.com/databook/OPA4658.html

# Quad Wideband, Low Power Current Feedback OPERATIONAL AMPLIFIER

## FEATURES

- GAIN BANDWIDTH: 900MHz at G = 2
- GAIN OF 2 STABLE
- LOW POWER: 50mW PER AMP
- LOW DIFF GAIN/PHASE ERRORS: 0.015%/0.02°
- HIGH SLEW RATE: 1700V/µs
- PACKAGE: 14-Pin DIP and SO-14

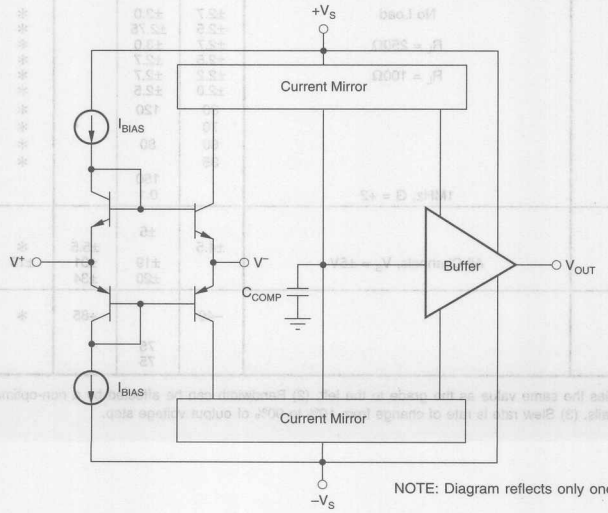
## APPLICATIONS

- MEDICAL IMAGING
- HIGH-RESOLUTION VIDEO
- HIGH-SPEED SIGNAL PROCESSING
- COMMUNICATIONS
- PULSE AMPLIFIERS
- ADC/DAC GAIN AMPLIFIER
- MONITOR PREAMPLIFIER
- CCD IMAGING AMPLIFIER

## DESCRIPTION

The OPA4658 is a quad ultra-wideband, low power current feedback video operational amplifier featuring high slew rate and low differential gain/phase error. The current feedback design allows for superior large signal bandwidth, even at high gains. The low differential gain/phase errors, wide bandwidth and low quiescent current make the OPA4658 a perfect choice for numerous video, imaging and communications applications.

The OPA4658 is internally compensated for stability in gains of 2 or greater. The OPA4658 is also available in dual (OPA2658) and single (OPA658) configurations.




NOTE: Diagram reflects only one-fourth of the OPA4658.

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At $T_A$ = +25°C, $V_S$ = ±5V, $R_L$ = 100Ω, $C_L$ = 2pF, $R_{FB}$ = 402Ω, unless otherwise noted.

| PARAMETER | CONDITION | OPA4658P, U | | | OPA4658UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Closed-Loop Bandwidth[2] | G = +2 | | 450 | | | ✻[1] | | MHz |
| | G = +5 | | 195 | | | ✻ | | MHz |
| | G = +10 | | 130 | | | ✻ | | MHz |
| Slew Rate[3] | G = +2, 2V Step | | 1700 | | 1000 | ✻ | | V/µs |
| At Minimum Specified Temperature | | | 1500 | | 900 | ✻ | | V/µs |
| Settling Time: 0.01% | G = +2, 2V Step | | 20 | | | ✻ | | ns |
| 0.1% | G = +2, 2V Step | | 15.1 | | | ✻ | | ns |
| 1% | G = +2, 2V Step | | 4.8 | | | ✻ | | ns |
| Spurious Free Dynamic Range | f = 5MHz, G = +2, $V_O$ = 2Vp-p | | 66 | | | ✻ | | dBc |
| | f = 20MHz, G = +2, $V_O$ = 2Vp-p | | 57 | | | ✻ | | dBc |
| Third-Order Intercept Point | f = 10MHz | | 38 | | | ✻ | | dBm |
| Differential Gain | G = +2, NTSC, $V_O$ = 1.4Vp-p, $R_L$ = 150Ω | | 0.015 | | | ✻ | | % |
| Differential Phase | G = +2, NTSC, $V_O$ = 1.4Vp-p, $R_L$ = 150Ω | | 0.02 | | | ✻ | | degrees |
| Crosstalk | Input Referred, 5MHz, Three Active Channels | | –74 | | | ✻ | | dB |
| | Input Referred, 5MHz, Channel-to-Channel | | –85 | | | ✻ | | dB |
| **OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | | | ±1.5 | ±5.5 | | ±2 | ±5 | mV |
| Over Temperature | | | ±5 | ±8 | | ±4 | ±8 | mV |
| Power Supply Rejection | $V_S$ = ±4.5 to ±5.5V | 55 | 70 | | 58 | 75 | | dB |
| **INPUT BIAS CURRENT** | | | | | | | | |
| Non-Inverting | $V_{CM}$ = 0V | | ±6.5 | ±30 | | ✻ | ±18 | µA |
| Over Temperature | | | ±10 | ±80 | | ✻ | ±35 | µA |
| Inverting | $V_{CM}$ = 0V | | ±1.1 | ±35 | | ✻ | ✻ | µA |
| Over Temperature | | | ±30 | ±75 | | ✻ | ✻ | µA |
| **NOISE** | | | | | | | | |
| Input Voltage Noise Density | | | | | | | | |
| f = 100Hz | | | 16 | | | ✻ | | nV/√Hz |
| f = 10kHz | | | 3.6 | | | ✻ | | nV/√Hz |
| f = 1MHz | | | 3.2 | | | ✻ | | nV/√Hz |
| $f_B$ = 100Hz to 200MHz | | | 45 | | | ✻ | | µVrms |
| Inverting Input Bias Current | | | | | | | | |
| Noise Density: f = 10MHz | | | 32 | | | ✻ | | pA/√Hz |
| Non-Inverting Input Current | | | | | | | | |
| Noise Density: f = 10MHz | | | 12 | | | ✻ | | pA/√Hz |
| Noise Figure (NF) | $R_S$ = 100Ω | | 9.5 | | | ✻ | | dBm |
| | $R_S$ = 50Ω | | 11 | | | ✻ | | dBm |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | | ±2.9 | | | ✻ | | V |
| Over Temperature | | ±2.5 | | | ✻ | | | V |
| Common-Mode Rejection | $V_{CM}$ = ±1V | 45 | 52 | | ✻ | ✻ | | dB |
| **INPUT IMPEDANCE** | | | | | | | | |
| Non-Inverting | | | 500 ‖ 1 | | | ✻ | | kΩ ‖pF |
| Inverting | | | 25 | | | ✻ | | Ω |
| **OPEN-LOOP TRANSIMPEDANCE** | | | | | | | | |
| Open-Loop Transimpedance | $V_O$ = ±2V, $R_L$ = 100Ω | 150 | 350 | | 200 | 360 | | kΩ |
| Over Temperature | $V_O$ = ±2V, $R_L$ = 100Ω | 100 | 290 | | 150 | 300 | | kΩ |
| **OUTPUT** | | | | | | | | |
| Voltage Output | No Load | ±2.7 | ±3.0 | | ✻ | ✻ | | V |
| Over Temperature | | ±2.5 | ±2.75 | | ✻ | ✻ | | V |
| Voltage Output | $R_L$ = 250Ω | ±2.7 | ±3.0 | | ✻ | ✻ | | V |
| Over Temperature | | ±2.5 | ±2.7 | | ✻ | ✻ | | V |
| Voltage Output | $R_L$ = 100Ω | ±2.2 | ±2.7 | | ✻ | ✻ | | V |
| Over Temperature | | ±2.0 | ±2.5 | | ✻ | ✻ | | V |
| Output Current, Sourcing | | 80 | 120 | | ✻ | ✻ | | mA |
| Over Temperature Range | | 70 | | | ✻ | | | mA |
| Output Current, Sinking | | 60 | 80 | | ✻ | ✻ | | mA |
| Over Temperature Range | | 35 | | | ✻ | | | mA |
| Short Circuit Current | | | 150 | | | ✻ | | mA |
| Output Resistance | 1MHz, G = +2 | | 0.1 | | | ✻ | | Ω |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | | ±5 | | | ✻ | | V |
| Operating Voltage Range | | ±4.5 | | ±5.5 | ✻ | | ✻ | V |
| Quiescent Current | All Channels, $V_S$ = ±5V | | ±19 | ±31 | ±13 | ±20 | ±23 | mA |
| Over Temperature | | | ±20 | ±34 | | ±21 | ±26 | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: P, U, UB | | –40 | | +85 | ✻ | | ✻ | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| P | | | 75 | | | ✻ | | °C/W |
| U | | | 75 | | | ✻ | | °C/W |

NOTES: (1) An asterisk (✻) specifies the same value as the grade to the left. (2) Bandwidth can be affected by a non-optimal PC board layout. Refer to the demonstration board layout for details. (3) Slew rate is rate of change from 10% to 90% of output voltage step.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply | ±5.5VDC |
| Internal Power Dissipation(1) | See Applications Information |
| Differential Input Voltage | Total $V_S$ |
| Input Voltage Range | See Applications Information |
| Storage Temperature Range: P, U, UB | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SOIC 3s) | +260°C |
| Junction Temperature ($T_J$) | +175°C |

NOTE: (1) Packages must be derated based on specified $\theta_{JA}$. Maximum $T_J$ must be observed.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| OPA4658P | 14-Pin Plastic DIP | 010 |
| OPA4658U, UB | SO-14 Surface Mount | 235 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

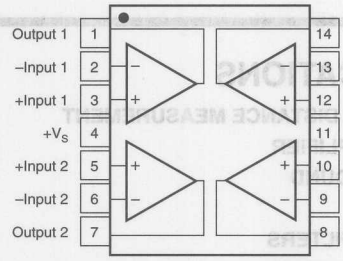
## ORDERING INFORMATION(1)

| PRODUCT | PACKAGE | TEMPERATURE RANGE |
|---|---|---|
| OPA4658P | 14-Pin Plastic DIP | –40°C to +85°C |
| OPA4658U, UB | SO-14 Surface Mount | –40°C to +85°C |

NOTE: (1) The "B" grade of the SOIC package will be marked with a "B" by pin 8. Refer to mechanical section for the location.

## PIN CONFIGURATION

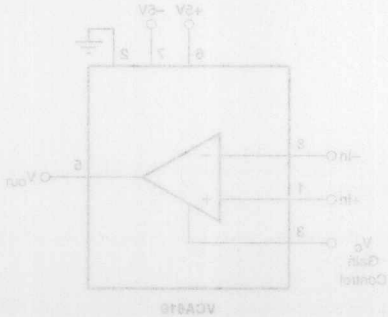
Top View DIP/SO-14




## ELECTROSTATIC DISCHARGE SENSITIVITY

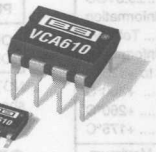
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



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# VCA610

www.burr-brown.com/databook/VCA610.html

# WIDEBAND VOLTAGE CONTROLLED AMPLIFIER

## FEATURES

- WIDE GAIN CONTROL RANGE: 80dB
- SMALL PACKAGE: 8-pin SOIC or DIP
- WIDE BANDWIDTH: 30MHz
- LOW VOLTAGE NOISE: 2.2nV/√Hz
- FAST GAIN SLEW RATE: 300dB/µs
- EASY TO USE

## APPLICATIONS

- OPTICAL DISTANCE MEASUREMENT
- AGC AMPLIFIER
- ULTRASOUND
- SONAR
- ACTIVE FILTERS
- LOG AMPLIFIER
- IF CIRCUITS
- CCD CAMERAS

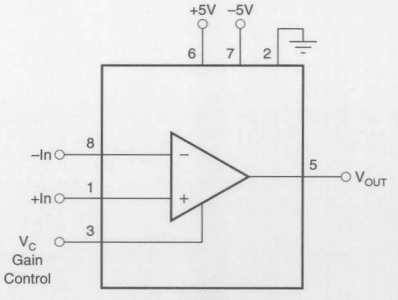
## DESCRIPTION

The VCA610 is a wideband, continuously variable, voltage controlled gain amplifier. It provides linear-dB gain control with high impedance inputs. It is designed to be used as a flexible gain control element in a variety of electronic systems.

The VCA610 has a gain control range of 80dB (–40dB to +40dB) providing both gain and attenuation for maximum flexibility in a small 8-lead SO-8 or plastic dual-in-line package. The broad attenuation range can be used for gradual or controlled channel turn-on and turn-off for applications in which abrupt gain changes can create artifacts or other errors. In addition, the output can be disabled to provide –80dB of attenuation. Group delay variation with gain is typically less than ±2ns across a bandwidth of 1 to 15MHz.

The VCA610 has a noise figure of 3.5dB (with an $R_S$ of 200Ω) including the effects of both current and voltage noise. Instantaneous output dynamic range is 70dB for gains of 0dB to +40dB with 1MHz noise bandwidth. The output is capable of driving 100Ω. The high speed, 300dB/µs, gain control signal is a unipolar (0 to –2V) voltage that varies the gain linearly in dB/V.

The VCA610 is designed with a very fast overload recovery time of only 200ns. This allows a large signal transient to overload the output at high gain, without obscuring low-level signals following closely behind. The excellent overload recovery time and distortion specifications optimize this device for low-level doppler measurements.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132



PDS-1140D

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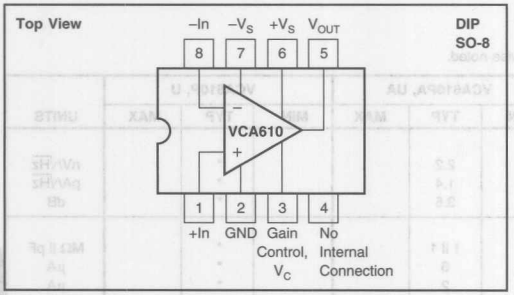
# SPECIFICATIONS

## ELECTRICAL

All specifications at $V_S$ = ±5V, $R_L$ = 500Ω, $R_S$ = 0Ω, and $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | VCA610PA, UA MIN | VCA610PA, UA TYP | VCA610PA, UA MAX | VCA610P, U MIN | VCA610P, U TYP | VCA610P, U MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **INPUT NOISE** | | | | | | | | |
| Input Voltage Noise | G = +40dB, $R_S$ = 0Ω | | 2.2 | | | * | | nV/√Hz |
| Input Current Noise | G = –40dB to +40dB | | 1.4 | | | * | | pA/√Hz |
| Noise Figure | G = +40dB, $R_S$ = 200Ω | | 3.5 | | | * | | dB |
| **INPUT** | | | | | | | | |
| Input Impedance | Common-Mode | | 1 \|\| 1 | | | * | | MΩ \|\| pF |
| Bias Current | All Gains | | 6 | | | * | | µA |
| Offset Current | All Gains | | 2 | | | * | | µA |
| Differential Voltage Range | | | (1) | | | * | | |
| Common-Mode Voltage Range | | | ±2.5 | | | * | | V |
| Common-Mode Rejection | | | 50 | | | * | | dB |
| **GAIN** | | | | | | | | |
| Specified Gain Range | | –40 | | +40 | * | | * | dB |
| Gain Accuracy[2] | –40dB ≤ G ≤ +40dB | | ±0.5 | ±2 | | ±2 | ±4 | dB |
| Gain Accuracy Temperature Drift | $T_A$ = –25°C to +85°C | | ±0.01 | | | * | | dB/°C |
| Gain with Output Disabled | +0.1V ≤ $V_C$ ≤ +2.0V, f = 1MHz | | –80 | | | * | | dB |
| **GAIN CONTROL** | | | | | | | | |
| Gain Scaling Factor | –40dB ≤ G ≤ +40dB | | 40 | | | * | | dB/V |
| Control Voltage ($V_C$) | G = –40dB ($V_C$ = 0V) to +40dB ($V_C$ = –2V) | 0 | | –2 | * | | * | V |
| Bandwidth | –3dB | | 1 | | | * | | MHz |
| Slew Rate | 80dB Gain Step | | 300 | | | * | | dB/µs |
| Settling Time: 1% | $V_{IN}$ = 10mVDC, Δ G = 80dB | | 800 | | | * | | ns |
| Input Impedance | | | 1 \|\| 1 | | | * | | MΩ \|\| pF |
| Input Bias Current | All Gains | | 2 | | | * | | µA |
| Output Offset Change[3] | Δ G = 80dB | | ±30 | ±75 | | * | ±125 | mV |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Bandwidth, Small-Signal | –3dB, All Gains | | 30 | | | * | | MHz |
| Bandwidth, Large-Signal | $V_O$ = 1Vp-p, G ≥ 0dB | | 25 | | | * | | MHz |
| Group Delay Unit-to-Unit Variation | | | | | | | | |
| 0dB ≤ G ≤ +40dB | f = 1 to 15MHz | | ±1 | | | * | | ns |
| –40dB ≤ G < 0dB | f = 1 to 15MHz | | ±2 | | | * | | ns |
| Output Slew Rate | $V_O$ = 1Vp-p | | 60 | | | * | | V/µs |
| Overload Recovery[4] | | | 200 | | | * | | ns |
| Two-tone Intermodulation Distortion[5] | Small-Signal | | –50 | | | * | | dBc |
| Two-tone, 3rd Order IMD Intercept[5] | Small-Signal | | 15 | | | * | | dBm |
| **OUTPUT** | | | | | | | | |
| Voltage Swing[1] | | | | | | | | |
| G = +40dB | | ±1 | ±1.6 | | * | * | | V |
| G = 0dB | | ±0.5 | ±0.75 | | * | * | | V |
| Output Voltage Limit | | | Symmetrical to Ground (±10%) | | | * | | |
| Short-Circuit Current | Continuous to Common | | ±80 | | | * | | mA |
| Instantaneous Dynamic Range (IDR)[6] | | | | | | | | |
| G = 0dB to +40dB | $V_O$ = 1.5Vp-p | | 70 | | | * | | dB |
| Offset | G = –40dB | | ±2 | ±30 | | * | * | mV |
| Output Resistance | f = 1MHz, All Gains | | 10 | | | * | | Ω |
| **POWER SUPPLY** | | | | | | | | |
| Specification | ±5V Recommended | ±4.5 | | ±5.5 | * | | * | V |
| PSR | G = 0dB | 40 | 50 | | | * | | dB |
| Quiescent Current | | | –26/+30 | ±32 | | * | * | mA |
| **TEMPERATURE** | | | | | | | | |
| Specification | Applies to Temperature Drift Specs | –25 | | +85 | * | | * | °C |
| Operation | | –40 | | +125 | * | | * | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| P, PA | | | 100 | | | * | | °C/W |
| U, UA | | | 125 | | | * | | °C/W |

NOTES: (1) See Input/Output Range discussion in Applications Information Section (Figure 2). (2) Gain is laser trimmed and tested at gains of –40dB, 0dB, +15dB, +25dB, and +40dB; $V_{IN}$ =1Vp-p for gains less than 0dB; $V_{OUT}$ = 1V for gains of 0dB to +40dB. (3) Output offset change from offset at G = –40dB. (4) Gain = +40dB; Input step of 2V to 2mV; time required for output to return from saturation to linear operation. (5) $V_{IN}$ = 7mVp-p, $V_{OUT}$ = 700mVp-p (250mVrms); Output Power = –10dBm/tone, equal amplitude tones of 5MHz ±500Hz, G = +40dB. See typical performance curves. (6) With $R_S$ = 0Ω, and noise bandwidth of 1MHz. IDR = 20 log ($V_{ORMS}$/($e_{ORMS}$ x √BW)); where $V_{ORMS}$ is rms output voltage, $e_{ORMS}$ is output noise spectral density, and BW is noise bandwidth.




| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| VCA610PA | 8-Pin Plastic DIP | 006 |
| VCA610P | 8-Pin Plastic DIP | 006 |
| VCA610UA | SO-8 Surface-Mount | 182 |
| VCA610U | SO-8 Surface-Mount | 182 |

NOTE:(1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply | ±7V |
| Differential Input Voltage | Total $V_S$ |
| Input Voltage Range | See Input Protection Section |
| Storage Temperature Range | –65°C to +150°C |
| Lead Temperature (soldering, DIP, 10s) | +300°C |
| Lead Temperature (soldering, SO-8, 3s) | +260°C |
| Output Short-Circuit to Ground (+25°C) | Continuous |
| Junction Temperature ($T_J$) | +175°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

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# 3 Power Operational Amplifiers

Burr-Brown power amplifiers are designed for high output voltage and/or high output current. Versatile power operational amplifiers can be used in virtually any op amp circuit configuration, yet can supply up to ±15A load current or ±140V output voltage.

Buffer amplifiers can be used with common op amps to drive long lines or heavy loads such as valves, voice-coils and actuators.

Choose from a wide variety of power amp types, including:

**OPA547, OPA548**—Continuous output ratings of 0.5A and 3A, respectively, allow these new-generation monolithic power op amps to serve a wide range of requirements. Advanced user-set current limit circuitry and digital shutdown/status I/O pin add to their versatility. Operation extends to 60V power supplies.

**BUF634**—250mA, 2000V/µs buffer amp. Used with a common op amp, this buffer amp boosts output current to 250mA and increases capacitive load drive capability. Versatile and rugged, it's available in SO-8, 8-pin DIP and 5-pin TO-220 packages.

**OPA541**—This monolithic power op amp delivers output current up to ±5A and operates from power supplies up to ±40V. Available in low cost plastic power SIP and hermetic 8-pin TO-3 packages.

**OPA544F**—A high-voltage/high-current op amp available in a surface-mount power package that solders flat on a circuit board for low profile, high density applications. Specifications include 2A output current, ±10V to ±35V power supply range, and 100pA max input bias current. It is also available in a 5-lead TO-220 plastic package.

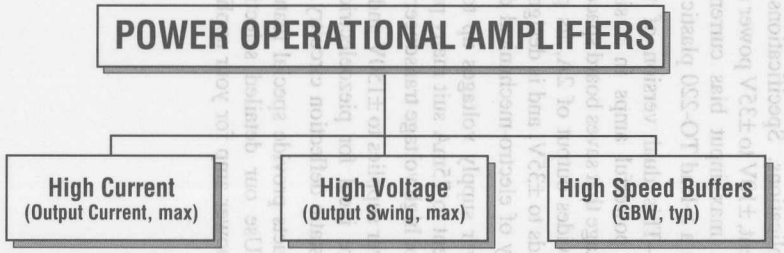
**OPA2544**—This dual version of the OPA544 packs two powerful amps in a single 11-lead plastic package that saves board space and reduces cost. It provides output of 2A, its power supply range extends to ±35V, and is designed to drive a wide variety of electro-mechanical devices.

**3583**—Power supply voltages up to ±150V and output current to 75mA suit many programmable V/I source or high voltage transducer applications.

**3584**—Power supplies to ±150V and slew rates to 150V/µs are ideal for piezoelectric transducers and electrostatic deflection circuitry.

Other products provide special features and performance. Use our detailed selection guide to locate the power amp for your application.

# Power Operational Amplifiers




| High Current (Output Current, max) | | High Voltage (Output Swing, max) | | High Speed Buffers (GBW, typ) | |
|---|---|---|---|---|---|
| OPA512 | (±15A) | 3584 | (±145V) | BUF601 | (900MHz) |
| OPA501 | (±10A) | 3583 | (±140V) | OPA660 | (850MHz) |
| OPA502 | (±10A) | 3581 | (±70V) | BUF600 | (650MHz) |
| OPA541 | (±5A) | OPA445 | (±35V) | OPA633 | (260MHz) |
| OPA2541 | (±5A, Dual) | **OPA547** | **(±30V)** | BUF634 | (180MHz) |
| **OPA548** | **(±3A)** | **OPA548** | **(±30V)** | | |
| OPA544 | (±2A) | | | | |
| OPA2544 | (±2A, Dual) | | | | |
| **OPA547** | **(±500mA)** | | | | |

**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

*For Immediate Assistance, Contact Your Local Salesperson*

## POWER - HIGH CURRENT

| Product | Rated Output Current min (±mA) | Rated Supply max (±V) | Offset Voltage 25°C max (±mV) | Offset Voltage Drift max (±µV/°C) | Bias Current 25°C max (pA) | Small Signal Unity Gain Bandwidth typ (MHz) | Slew Rate min (V/µs) | Open Loop Gain (dB) | Temp Range[1] | Pkg | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA501 | 10A | 34 | 5 | 40 | 20nA | 1 | 1.35 | 98 | Ind | TO-3 | High Current |
| OPA502 | 10A | 45 | 5 | 5* | 200 | 2 | 10 | 103 | XInd | TO-3 | High Current |
| OPA512BM | 10A | 45 | 6 | 65 | 30nA | 4 | 2.5 | 110 | Ind | TO-3 | High Current |
| OPA512SM | 15A | 45 | 3 | 40 | 20nA | 4 | 2.5 | 110 | Mil | TO-3 | High Current |
| OPA541BM | 5A | 40 | 1 | 30 | 50 | 1.6 | 6 | 90 | Ind/Mil | TO-3 | High Current |
| OPA541AP | 5A | 35 | 10 | 40 | 50 | 1.6 | 6 | 90 | Ind | Power Plastic | High Current |
| OPA544 | 2A | 35 | 5 | 10* | 100 | 1.4 | 8 | 90 | XInd | 5-Pin TO-220 | High Current |
| **OPA547** | **500** | **30** | **5** | **25*** | **500nA** | **1** | **6*** | **90** | **XInd** | **TO-220, DDPAK** | **Single Supply and High Current** |
| **OPA548** | **3A** | **30** | **5** | **25*** | **500nA** | **1** | **10*** | **90** | **XInd** | **TO-220, DDPAK** | **Single Supply and High Current** |
| OPA2541 | 5A | 40 | 1 | 30 | 50 | 1.6 | 6 | 90 | Ind/Mil | TO-3 | Dual |
| OPA2544 | 2A | 35 | 5 | 10* | 50 | 1.4 | 5 | 90 | XInd/Mil | TO-3, 11-Pin Plastic | Dual |

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, XInd = –40°C to +85°C, Mil = –55°C to +125°C. (2) Gain-bandwidth product. (3) 5A peak.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

* DENOTES TYPICAL
**BOLD DENOTES NEW PRODUCT**
***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

## POWER - HIGH VOLTAGE

| Product | Rated Output Current min (±mA) | Rated Supply max (±V) | Offset Voltage 25°C max (±mV) | Offset Voltage Drift max (±µV/°C) | Bias Current 25°C max (pA) | Unity Gain Bandwidth typ (MHz) | Slew Rate min (V/µs) | Open Loop Gain (dB) | Temp Range[1] | Pkg | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA445 | 15 | 45 | 3 | 10* | 50 | 2 | 5 | 100 | Ind/Mil | TO-99, DIP | |
| **OPA547** | **500** | **35** | **5** | **25*** | **500nA** | **1** | **6*** | **90** | **XInd** | **TO-220, DDPAK** | **Single Supply and High Current** |
| **OPA548** | **3A** | **35** | **5** | **25*** | **500nA** | **1** | **10*** | **90** | **XInd** | **TO-220, DDPAK** | **Single Supply and High Current** |
| 3581 | 30 | 70 | 3 | 25 | 20 | 5 | 20 | 112 | Com | TO-3 | Still Available |
| 3583 | 75 | 140 | 3 | 23 | 20 | 5 | 30* | 118 | Com/Ind | TO-3 | |
| 3584 | 15 | 145 | 3 | 25 | 20 | 20[2] | 150* | 120 | Com | TO-3 | |

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, XInd = –40°C to +85°C, Mil = –55°C to +125°C. (2) Gain-bandwidth product.

## POWER - HIGH SPEED BUFFERS

| Product | Rated Current Output min (±mA) | Rated Voltage Output min (±V) | Small Signal Bandwidth (MHz) | Full Power Bandwidth (MHz) | Slew Rate typ (V/µs) | Input Impedance typ (Ω ll pF) | Temp Range[1] | Pkg | Description |
|---|---|---|---|---|---|---|---|---|---|
| BUF600 | 20 | 2.5 | 650 | 320 | 3400 | 4.8M/1 | XInd | DIP, SOIC | High Slew Rate, Open Loop |
| BUF601 | 20 | 2.5 | 900 | 320 | 3600 | 2.5M/1 | XInd | DIP, SOIC | High Slew Rate, Open Loop |
| BUF634 | 250* | 10 | 180 | NS | 2000 | 8M/8 | Ind | DIP, SOIC, TO-220 | Low Cost, Open Loop |
| OPA633 | 80 | 11 | 260 | 40 | 2500 | 1.5M/1.6 | Ind | DIP | Low Cost, Open Loop |
| OPA660 | 10 | 3.7 | 850 | 570 | 3000 | 1M/2.1 | XInd | DIP, SOIC | Transconductance Amp and Buffer |

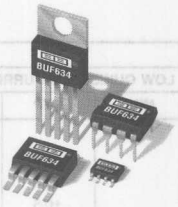
NOTES: (1) Ind = –25°C to +85°C, XInd = –40°C to +85°C.

* DENOTES TYPICAL
**BOLD DENOTES NEW PRODUCT**
***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

*For Immediate Assistance, Contact Your Local Salesperson*

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# BUF634

www.burr-brown.com/databook/BUF634.html



# 250mA HIGH-SPEED BUFFER

## FEATURES

- HIGH OUTPUT CURRENT: 250mA
- SLEW RATE: 2000V/µs
- PIN-SELECTED BANDWIDTH: 30MHz to 180MHz
- LOW QUIESCENT CURRENT: 1.5mA (30MHz BW)
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- INTERNAL CURRENT LIMIT
- THERMAL SHUTDOWN PROTECTION
- 8-PIN DIP, SO-8, 5-LEAD TO-220, 5-LEAD DDPAK SURFACE-MOUNT

## APPLICATIONS

- VALVE DRIVER
- SOLENOID DRIVER
- OP AMP CURRENT BOOSTER
- LINE DRIVER
- HEADPHONE DRIVER
- VIDEO DRIVER
- MOTOR DRIVER
- TEST EQUIPMENT
- ATE PIN DRIVER

## DESCRIPTION

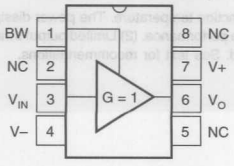
The BUF634 is a high speed unity-gain open-loop buffer recommended for a wide range of applications. It can be used inside the feedback loop of op amps to increase output current, eliminate thermal feedback and improve capacitive load drive.

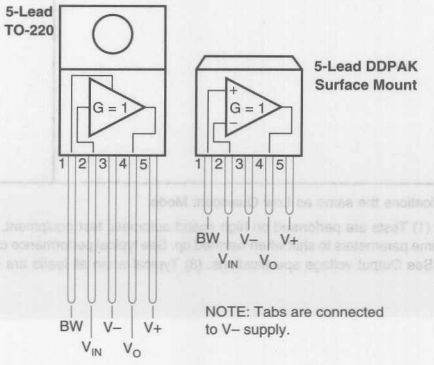
For low power applications, the BUF634 operates on 1.5mA quiescent current with 250mA output, 2000V/µs slew rate and 30MHz bandwidth. Bandwidth can be adjusted from 30MHz to 180MHz by connecting a resistor between V– and the BW Pin.

Output circuitry is fully protected by internal current limit and thermal shut-down making it rugged and easy to use.

The BUF634 is available in a variety of packages to suit mechanical and power dissipation requirements. Types include 8-pin DIP, SO-8 surface-mount, 5-lead TO-220, and a 5-lead DDPAK surface-mount plastic power package.

8-Pin DIP Package
SO-8 Surface-Mount Package




NOTE: Tabs are connected to V– supply.

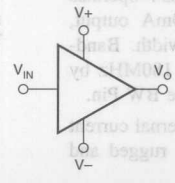
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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

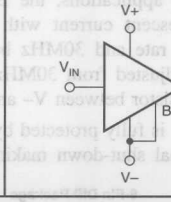
# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C[1], $V_S$ = ±15V, unless otherwise noted.

| PARAMETER | CONDITION | BUF634P, U, T, F | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | LOW QUIESCENT CURRENT MODE | | | WIDE BANDWIDTH MODE | | | |
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT** | | | | | | | | |
| Offset Voltage | | | ±30 | ±100 | | * | * | mV |
| vs Temperature | Specified Temperature Range | | ±100 | | | * | | µV/°C |
| vs Power Supply | $V_S$ = ±2.25V[2] to ±18V | | 0.1 | 1 | | * | * | mV/V |
| Input Bias Current | $V_{IN}$ = 0V | | ±0.5 | ±2 | | ±5 | ±20 | µA |
| Input Impedance | $R_L$ = 100Ω | | 80 ‖ 8 | | | 8 ‖ 8 | | MΩ ‖ pF |
| Noise Voltage | f = 10kHz | | 4 | | | * | | nV/√Hz |
| **GAIN** | $R_L$ = 1kΩ, $V_O$ = ±10V | 0.95 | 0.99 | | * | * | | V/V |
| | $R_L$ = 100Ω, $V_O$ = ±10V | 0.85 | 0.93 | | * | * | | V/V |
| | $R_L$ = 67Ω, $V_O$ = ±10V | 0.8 | 0.9 | | * | * | | V/V |
| **OUTPUT** | | | | | | | | |
| Current Output, Continuous | | | ±250 | | | * | | mA |
| Voltage Output, Positive | $I_O$ = 10mA | (V+) –2.1 | (V+) –1.7 | | * | * | | V |
| Negative | $I_O$ = –10mA | (V–) +2.1 | (V–) +1.8 | | * | * | | V |
| Positive | $I_O$ = 100mA | (V+) –3 | (V+) –2.4 | | * | * | | V |
| Negative | $I_O$ = –100mA | (V–) +4 | (V–) +3.5 | | * | * | | V |
| Positive | $I_O$ = 150mA | (V+) –4 | (V+) –2.8 | | * | * | | V |
| Negative | $I_O$ = –150mA | (V–) +5 | (V–) +4 | | * | * | | V |
| Short-Circuit Current | | | ±350 | ±550 | | ±400 | * | mA |
| **DYNAMIC RESPONSE** | | | | | | | | |
| Bandwidth, –3dB | $R_L$ = 1kΩ | | 30 | | | 180 | | MHz |
| | $R_L$ = 100Ω | | 20 | | | 160 | | MHz |
| Slew Rate | 20Vp-p, $R_L$ = 100Ω | | 2000 | | | * | | V/µs |
| Settling Time, 0.1% | 20V Step, $R_L$ = 100Ω | | 200 | | | * | | ns |
| 1% | 20V Step, $R_L$ = 100Ω | | 50 | | | * | | ns |
| Differential Gain | 3.58MHz, $V_O$ = 0.7V, $R_L$ = 150Ω | | 4 | | | 0.4 | | % |
| Differential Phase | 3.58MHz, $V_O$ = 0.7V, $R_L$ = 150Ω | | 2.5 | | | 0.1 | | ° |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | | ±15 | | | * | | V |
| Operating Voltage Range | ±2.25[2] | | | ±18 | * | | * | V |
| Quiescent Current, $I_Q$ | $I_O$ = 0 | | ±1.5 | ±2 | | ±15 | ±20 | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –40 | | +85 | * | | * | °C |
| Operating | | –40 | | +125 | * | | * | °C |
| Storage | | –55 | | +125 | * | | * | °C |
| Thermal Shutdown Temperature, $T_J$ | | | 175 | | | * | | °C |
| Thermal Resistance, $\theta_{JA}$ | "P" Package[3] | | 100 | | | * | | °C/W |
| $\theta_{JA}$ | "U" Package[3] | | 150 | | | * | | °C/W |
| $\theta_{JA}$ | "T" Package[3] | | 65 | | | * | | °C/W |
| $\theta_{JC}$ | "T" Package | | 6 | | | * | | °C/W |
| $\theta_{JA}$ | "F" Package[3] | | 65 | | | * | | °C/W |
| $\theta_{JC}$ | "F" Package | | 6 | | | * | | °C/W |

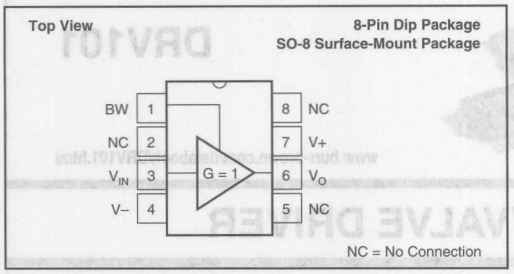


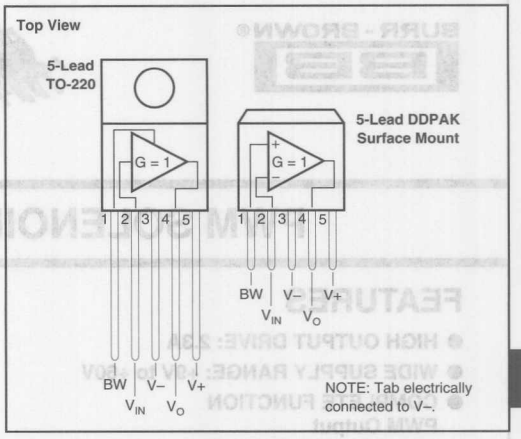




* Specifications the same as Low Quiescent Mode.

NOTES: (1) Tests are performed on high speed automatic test equipment, at approximately 25°C junction temperature. The power dissipation of this product will cause some parameters to shift when warmed up. See typical performance curves for over-temperature performance. (2) Limited output swing available at low supply voltage. See Output voltage specifications. (3) Typical when all leads are soldered to a circuit board. See text for recommendations.

## PIN CONFIGURATION




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Input Voltage Range | $\pm V_S$ |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering,10s) | +300°C |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| BUF634P | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| BUF634U | SO-8 Surface-Mount | 182 | –40°C to +85°C |
| BUF634T | 5-Lead TO-220 | 315 | –40°C to +85°C |
| BUF634F | 5-Lead DDPAK | 325 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

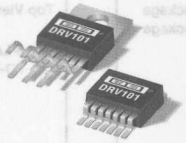
## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

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# DRV101

www.burr-brown.com/databook/DRV101.html

# PWM SOLENOID/VALVE DRIVER

## FEATURES

- HIGH OUTPUT DRIVE: 2.3A
- WIDE SUPPLY RANGE: +9V to +60V
- COMPLETE FUNCTION
  - PWM Output
  - Internal 24kHz Oscillator
  - Digital Control Input
  - Adjustable Delay and Duty Cycle
  - Over/Under Current Indicator
- FULLY PROTECTED
  - Thermal Shutdown with Indicator
  - Internal Current Limit
- PACKAGES: 7-Lead TO-220 and 7-Lead Surface-Mount DDPAK

## APPLICATIONS

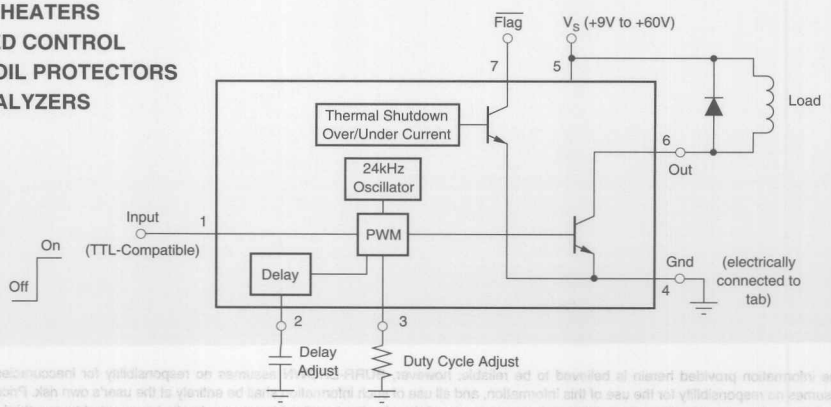
- ELECTROMECHANICAL DRIVER:
  - Solenoids
  - Actuators
  - Valves
  - Positioners
  - High Power Relays/Contactors
- FLUID AND GAS FLOW SYSTEMS
- INDUSTRIAL CONTROL
- FACTORY AUTOMATION
- PART HANDLERS
- PHOTOGRAPHIC PROCESSING
- ELECTRICAL HEATERS
- MOTOR SPEED CONTROL
- SOLENOID/COIL PROTECTORS
- MEDICAL ANALYZERS

## DESCRIPTION

The DRV101 is a low-side power switch employing a pulse-width modulated (PWM) output. Its rugged design is optimized for driving electromechanical devices such as valves, solenoids, relays, actuators, and positioners. The DRV101 is also ideal for driving thermal devices such as heaters and lamps. PWM operation conserves power and reduces heat rise, resulting in higher reliability. In addition, adjustable PWM allows fine control of the power delivered to the load. Time from dc output to PWM output is externally adjustable.

The DRV101 can be set to provide a strong initial closure, automatically switching to a "soft" hold mode for power savings. Duty cycle can be controlled by a resistor, analog voltage, or digital-to-analog converter for versatility. A flag output indicates thermal shutdown and over/under current limit. A wide supply range allows use with a variety of actuators.

The DRV101 is available in 7-lead staggered TO-220 package and a 7-lead surface-mount DDPAK plastic power package. It is specified over the extended industrial temperature range, –40°C to +85°C.




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# SPECIFICATIONS

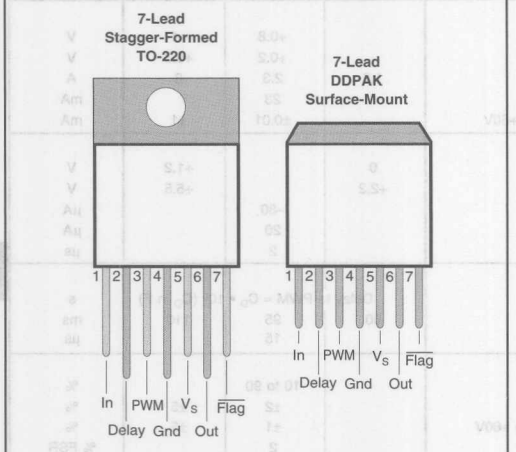
At $T_C$ = +25°C, $V_S$ = +24V, Load = 100Ω II 1000pF, and 4.99kΩ $\overline{\text{Flag}}$ pullup to +5V, unless otherwise noted.

| PARAMETER | COMMENTS | DRV101T, F MIN | DRV101T, F TYP | DRV101T, F MAX | UNITS |
|---|---|---|---|---|---|
| **OUTPUT** | | | | | |
| Output Saturation Voltage, Sink | $I_O$ = 1A | | +0.8 | +1 | V |
| | $I_O$ = 0.1A | | +0.2 | +0.3 | V |
| Current Limit | | 1.9 | 2.3 | 3 | A |
| Under-Scale Current(1) | | | 23 | | mA |
| Leakage Current | Output Transistor Off, $V_S$ = $V_O$ = +60V | | ±0.01 | ±1 | mA |
| **DIGITAL CONTROL INPUT(2)** | | | | | |
| $V_{CTR}$ Low (output disabled) | | 0 | | +1.2 | V |
| $V_{CTR}$ High (output enabled) | $V_{CTR}$ = 0V | +2.2 | | +5.5 | V |
| $I_{CTR}$ Low (output disabled) | $V_{CTR}$ = +5V | | –80 | | µA |
| $I_{CTR}$ High (output enabled) | | | 20 | | µA |
| Propagation Delay | On-to-Off and Off-to-On | | 2 | | µs |
| **DELAY TO PWM(3)** | dc to PWM Mode | | | | |
| Delay Equation(4) | | | Delay to PWM ≈ $C_D$ • $10^6$ ($C_D$ in F) | | s |
| Delay Time | $C_D$ = 0.1µF | 80 | 95 | 110 | ms |
| Minimum Delay Time(5) | $C_D$ = 0 | | 15 | | µs |
| **DUTY CYCLE ADJUST** | | | | | |
| Duty Cycle Range | | | 10 to 90 | | % |
| Duty Cycle Accuracy | 50% Duty Cycle | | ±2 | ±5 | % |
| vs Supply Voltage | 50% Duty Cycle, $V_S$ = $V_O$ = +9V to +60V | | ±1 | ±5 | % |
| Nonlinearity(6) | 10% to 80% Duty Cycle | | 2 | | % FSR |
| **DYNAMIC RESPONSE** | | | | | |
| Output Voltage Rise Time | $V_O$ = 10% to 90% of $V_S$ | | 1 | 2.5 | µs |
| Output Voltage Fall Time | $V_O$ = 10% to 90% of $V_S$ | | 0.1 | 2.5 | µs |
| Oscillator Frqeuency | | 19 | 24 | 29 | kHz |
| **$\overline{\text{FLAG}}$** | | | | | |
| Normal Operation | 20kΩ Pull-Up to +5V, $I_O$ < 1.5A | +4 | +4.9 | | V |
| Fault(7) | Sinking 1mA | | +0.2 | +0.8 | V |
| Sink Current | $V_{\overline{FLAG}}$ = 0.4V | | 2 | | mA |
| Under-Current Flag: Set | | | 4 | | µs |
| Reset | | | 2 | | µs |
| Over-Current Flag: Set | | | 2 | | µs |
| Reset | | | 2 | | µs |
| **THERMAL SHUTDOWN** | | | | | |
| Junction Temperature | | | | | |
| Shutdown | | | +165 | | °C |
| Reset from Shutdown | | | +150 | | °C |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | +24 | | V |
| Operating Voltage Range | | +9 | | +60 | V |
| Quiescent Current | $I_O$ = 0 | | 3.5 | 5 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specified Range | | –40 | | +85 | °C |
| Operating Range | | –55 | | +125 | °C |
| Storage Range | | –55 | | +125 | °C |
| Thermal Resistance, $\theta_{JC}$ | | | | | |
| 7-Lead DDPAK, 7-Lead TO-220 | | | 3 | | °C/W |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| 7-Lead DDPAK, 7-Lead TO-220 | No Heat Sink | | 65 | | °C/W |

NOTES:(1) Under-scale current for $T_C$ < 100°C—see Under-Scale Current vs Temperature typical performance curve. (2) Logic High enables output (normal operation). (3) Constant dc output to PWM (pulse-width modulated) time. (4) Maximum delay is determined by an external capacitor. Pulling the Delay Adjust Pin low corresponds to an infinite (continuous) delay. (5) Connecting the Delay Adjust pin to +5V reduces delay time to 3µs. (6) $V_{IN}$ at pin 3 to percent of duty cycle at pin 6. (7) A fault results from over-temperature, over-current, or under-current conditions.

## CONNECTION DIAGRAMS

Top Front View — TO-220, DDPAK




NOTE: Tabs are electrically connected to ground (pin 4).

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, $V_S$ | 60V |
| Input Voltage | –0.2V to $V_S$ |
| PWM Adjust Input | –0.2V to $V_S$ |
| Delay Adjust Input | –0.2V to $V_S$ (24V max) |
| Operating Temperature Range | –40°C to +125°C |
| Storage Temperature Range | –65°C to +150°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s)[2] | +300°C |

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Vapor-phase or IR reflow techniques are recommended for soldering the DRV101F surface-mount package. Wave soldering is not recommended due to excessive thermal shock and "shadowing" of nearby devices.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| DRV101T | 7-Lead Stagger-Formed TO-220 | 327 | –40°C to +85°C |
| DRV101F[2] | 7-Lead DDPAK Surface-Mount | 328 | –40°C to +85°C |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Available in Tape and Reel.

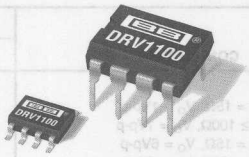
## ELECTROSTATIC DISCHARGE SENSITIVITY

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# DRV1100

www.burr-brown.com/databook/DRV1100.html

# HIGH POWER DIFFERENTIAL DRIVER AMPLIFIER

## FEATURES

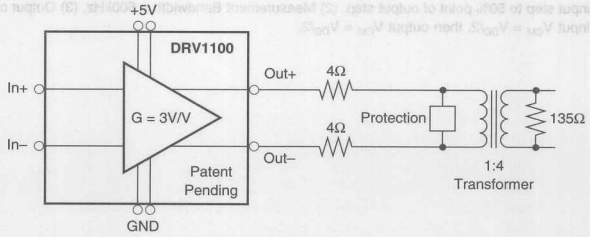
- HIGH OUTPUT CURRENT: 230mA
- SINGLE SUPPLY OPERATION: 5V
- 5MHz BANDWIDTH: 6Vp-p into 15Ω
- VERY LOW THD AT HIGH POWER: –72dBc at 6Vp-p, 100kHz, 100Ω
- LOW QUIESCENT CURRENT: 11mA
- FIXED DIFFERENTIAL GAIN: 3V/V

## APPLICATIONS

- xDSL TWISTED PAIR LINE DRIVER
- COMMUNICATIONS LINE DRIVER
- TRANSFORMER DRIVER
- SOLENOID DRIVER
- HIGH POWER AUDIO DRIVER
- CRT YOKE DRIVER

## DESCRIPTION

The DRV1100 is fixed gain differential line driver designed for very low harmonic distortion at the high powers required of xDSL line interface standards. Operating on a single +5V supply, it can deliver 230mA peak output current and 9.5Vp-p differential output voltage swing. This high output power on a single +5V supply makes the DRV1100 an excellent choice for the xDSL applications that require up to 17dBm power onto the line with high crest factors. The DRV1100 is available in both 8-pin plastic DIP and SO-8 packages.





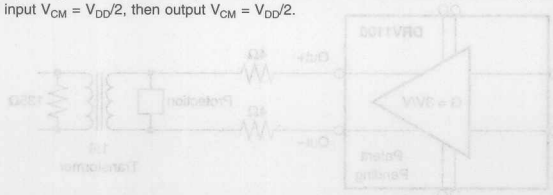

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# SPECIFICATIONS

At $V_{DD}$ = +5.0V, $V_{CM}$ = $V_{DD}$/2, $T_A$ = 25°C, unless otherwise specified.

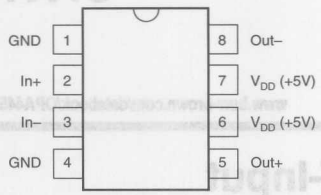
| PARAMETER | CONDITIONS | DRV1100P, U | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **AC PERFORMANCE** | | | | | |
| –3dB Bandwidth | $R_L$ = 15Ω, $V_O$ = 1Vp-p | | 8 | | MHz |
| | $R_L$ ≥ 100Ω, $V_O$ = 1Vp-p | | 11 | | MHz |
| | $R_L$ = 15Ω, $V_O$ = 6Vp-p | | 5 | | MHz |
| | $R_L$ ≥ 100Ω, $V_O$ = 6Vp-p | | 6 | | MHz |
| Differential Slew Rate | $R_L$ = 100Ω, $V_O$ = 6Vp-p | | 80 | | V/µs |
| Step Response Delay[1] | $V_O$ = 1Vp-p | | 25 | | ns |
| Settling Time to 1%, Step Input | $V_O$ = 1Vp-p, $R_L$ = 100Ω | | 0.25 | | µs |
| Settling Time to 1%, Step Input | $V_O$ = 6Vp-p, $R_L$ = 100Ω | | 0.3 | | µs |
| Settling Time to 0.1%, Step Input | $V_O$ = 1Vp-p, $R_L$ = 100Ω | | 0.8 | | µs |
| Settling Time to 0.1%, Step Input | $V_O$ = 6Vp-p, $R_L$ = 100Ω | | 1.1 | | µs |
| THD, Total Harmonic Distortion[2] | | | | | |
| f = 10kHz | $R_L$ = 100Ω, $V_O$ = 6Vp-p | | –85 | | dBc |
| f = 10kHz | $R_L$ = 15Ω, $V_O$ = 6Vp-p | –66 | –76 | | dBc |
| f = 100kHz | $R_L$ = 100Ω, $V_O$ = 6Vp-p | | –72 | | dBc |
| f = 100kHz | $R_L$ = 15Ω, $V_O$ = 6Vp-p | | –65 | | dBc |
| Input Voltage Noise | f = 100kHz | | 30 | | nV/√Hz |
| Input Current Noise | f = 100kHz | | 0.5 | | fA/√Hz |
| **INPUT CHARACTERISTICS** | | | | | |
| Differential Input Resistance | | | $10^{11}$ | | Ω |
| Differential Input Capacitance | | | 1 | | pF |
| Common-Mode Input Resistance | | | $10^{11}$ | | Ω |
| Common-Mode Input Capacitance | | | 6 | | pF |
| Input Offset Voltage | | | 5 | | mV |
| Input Bias Current | | | 1 | | pA |
| Common-Mode Rejection Ratio | Input Referred | | 62 | | dB |
| Power Supply Rejection Ratio | Input Referred | 60 | 76 | | dB |
| Input Common-Mode Voltage Range[3] | | 0.5 | | $V_{DD}$ –0.5 | V |
| **OUTPUT CHARACTERISTICS** | | | | | |
| Differential Output Offset, RTO | | | 10 | 25 | mV |
| Differential Output Offset Drift, RTO | –40°C to +85°C | | 30 | | µV/°C |
| Differential Output Resistance | | | 0.16 | | Ω |
| Peak Current (Continuous) | $R_L$ = 15Ω | 200 | 230 | | mA |
| Differential Output Voltage Swing | $R_L$ = 1kΩ | | 9.6 | | Vp-p |
| | $R_L$ = 100Ω | 8.5 | 9.5 | | Vp-p |
| | $R_L$ = 15Ω | 6.0 | 6.6 | | Vp-p |
| Output Voltage Swing, Each Side | $R_L$ = 1kΩ | 0.125 | | 4.875 | V |
| Gain | Fixed Gain, Differential | | 3 | | V/V |
| Gain Error | | | | ±0.25 | dB |
| **POWER SUPPLY** | | | | | |
| Operating Voltage Range | | +4.5 | +5.0 | +5.5 | V |
| Quiescent Current | $V_{DD}$ = 5.0V | | +11 | +16 | mA |
| **TEMPERATURE RANGE** | | –40 | | +85 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| DRV1100P 8-Pin DIP | | | 100 | | °C/W |
| DRV1100U 8-Pin SO-8 | | | 125 | | °C/W |

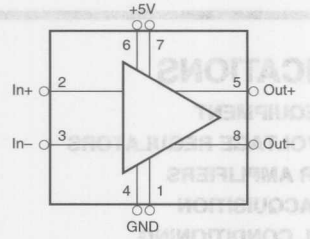
NOTES: (1) Time from 50% point of input step to 50% point of output step. (2) Measurement Bandwidth = 500kHz. (3) Output common-mode voltage follows input common-mode voltage; therefore, if input $V_{CM}$ = $V_{DD}$/2, then output $V_{CM}$ = $V_{DD}$/2.



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Top View




| | |
|---|---|
| Analog Inputs: Current | ±100mA, Momentary |
| | ±10mA, Continuous |
| Voltage | GND –0.3V to $V_{DD}$ +0.2V |
| Analog Outputs Short Circuit to Ground (+25°C) | Momentary |
| Analog Outputs Short Circuit to $V_{DD}$ (+25°C) | Momentary |
| $V_{DD}$ to GND | –0.3V to 6V |
| Junction Temperature | +150°C |
| Storage Temperature Range | –40°C to +125°C |
| Lead Temperature (soldering, 3s) | +260°C |
| Power Dissipation | (See Thermal/Analysis Discussion) |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| DRV1100P | 8-Pin PDIP | 006 |
| DRV1100U | 8-Lead SO-8 | 182 |

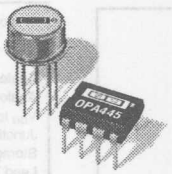
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®



# OPA445

www.burr-brown.com/databook/OPA445.html

# High Voltage FET-Input OPERATIONAL AMPLIFIER

## FEATURES

- WIDE POWER SUPPLY RANGE: ±10V to ±45V
- HIGH SLEW RATE: 10V/µs
- LOW INPUT BIAS CURRENT: 50pA max
- STANDARD-PINOUT TO-99 AND DIP PACKAGES

## APPLICATIONS

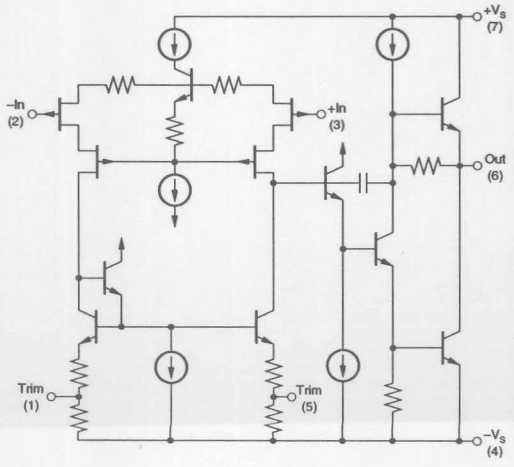
- TEST EQUIPMENT
- HIGH VOLTAGE REGULATORS
- POWER AMPLIFIERS
- DATA ACQUISITION
- SIGNAL CONDITIONING

## DESCRIPTION

The OPA445 is a monolithic operational amplifier capable of operation from power supplies up to ±45V and output currents of 15mA. It is useful in a wide variety of applications requiring high output voltage or large common-mode voltage swings.

The OPA445's high slew rate provides wide power-bandwidth response, which is often required for high voltage applications. FET input circuitry allows the use of high impedance feedback networks, thus minimizing their output loading effects. Laser trimming of the input circuitry yields low input offset voltage and drift.

The OPA445 is unity-gain stable and requires no external compensation components. It is available in both industrial (–25°C to +85°C) and military (–55°C to +125°C) temperature ranges.




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# SPECIFICATIONS

At $V_S$ = ±40V and $T_A$ = +25°C, unless otherwise specified.

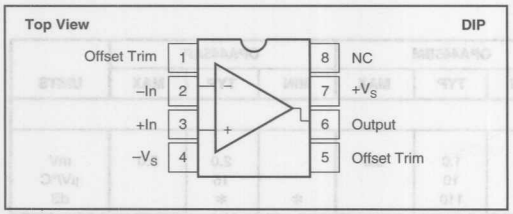
| PARAMETER | CONDITIONS | OPA445BM MIN | OPA445BM TYP | OPA445BM MAX | OPA445AP MIN | OPA445AP TYP | OPA445AP MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | | |
| **OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0V | | 1.0 | 3.0 | | 2.0 | 5.0 | mV |
| Average Drift | $T_A = T_{MIN}$ to $T_{MAX}$ | | 10 | | | 15 | | µV/°C |
| Supply Rejection | $V_S$ = ±10V to ±45V | 80 | 110 | | * | * | | dB |
| **BIAS CURRENT** | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | 20 | 50 | | 50 | 100 | pA |
| Over Temperature | | | | 10 | | | 20 | nA |
| **OFFSET CURRENT** | | | | | | | | |
| Input Offset Current | $V_{CM}$ = 0V | | 4 | 10 | | 20 | 40 | pA |
| Over Temperature | | | | 5 | | | 10 | nA |
| **IMPEDANCE** | | | | | | | | |
| Differential | | | $10^{13}$ ‖ 1 | | | * | | Ω ‖ pF |
| Common-Mode | | | $10^{14}$ ‖ 3 | | | * | | Ω ‖ pF |
| **VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | ±35 | | | * | | | V |
| Common-Mode Rejection | $V_{IN}$ = ±30V, | | | | | | | |
| | Over Temp. | 80 | 95 | | * | * | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | |
| Open-Loop Voltage Gain | $R_L$ = 5kΩ | 100 | 105 | | * | * | | dB |
| Over Temperature | | 97 | | | * | | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Gain Bandwidth | Small Signal | | 2 | | | * | | MHz |
| Full Power Response | 35Vp-p, $R_L$ = 5kΩ | 45 | 55 | | * | * | | kHz |
| **DYNAMIC RESPONSE** | | | | | | | | |
| Slew Rate | $V_O$ = ±35V, | | | | | | | |
| | $R_L$ = 5kΩ | 5 | 10 | | * | * | | V/µs |
| Rise Time | $V_O$ = ±200mV | | 100 | | | * | | ns |
| Overshoot | $A_V$ = +1 | | | | | | | |
| | $Z_L$ = 5kΩ ‖ 50pF | | 30 | | | * | | % |
| **OUTPUT** | | | | | | | | |
| Voltage Output, Over Temp. | $R_L$ = 5kΩ | ±35 | | | * | | | V |
| Current Output | $V_O$ = ±28V | ±15 | | | * | | | mA |
| Output Resistance | DC, Open Loop | | 220 | | | * | | Ω |
| Short Circuit Current | | | ±26 | | | * | | mA |
| **POWER SUPPLY** | | | | | | | | |
| Rated Voltage, ±$V_S$ | | | ±40 | | | * | | V |
| Voltage Range, ±$V_S$ | | | | | | | | |
| Derated Performance | Over Temperature | ±10 | | ±45 | * | | * | V |
| Current, Quiescent | $I_O$ = 0mA | | 3.8 | 4.5 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –25 | | +85 | * | | * | °C |
| Operating | Ambient Temperature | –55 | | +125 | –25 | | +85 | °C |
| θ Junction-Ambient | | | 200 | | | 100 | | °C/W |

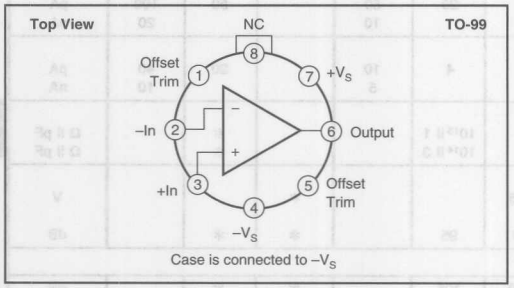
* Specifications same as OPA445BM.



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## CONNECTION DIAGRAMS




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply | ±50V |
| Internal Power Dissipation | 680mW |
| Differential Input Voltage | ±80V |
| Input Voltage Range | $\pm V_S$ –3V |
| Storage Temperature Range: M | –65°C to +150°C |
| P | –40°C to +85°C |
| Operating Temperature Range: M | –55°C to +125°C |
| P | –40°C to +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short-Circuit to Ground ($T_A$ = +25°C) | Continuous |
| Junction Temperature | +175°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| OPA445AP | 8-pin Plastic DIP | 006 | –25°C to +85°C |
| OPA445BM | 8-Pin TO-99 | 001 | –25°C to +85°C |

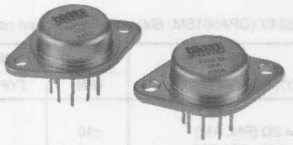
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

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BURR-BROWN®



# OPA501

www.burr-brown.com/databook/OPA501.html



# High Current, High Power OPERATIONAL AMPLIFIER

## FEATURES

- HIGH OUTPUT CURRENT: ±10A Peak
- WIDE POWER SUPPLY RANGE: ±10 to ±40V
- LOW QUIESCENT CURRENT: 2.6mA
- ISOLATED CASE TO-3 PACKAGE

## APPLICATIONS

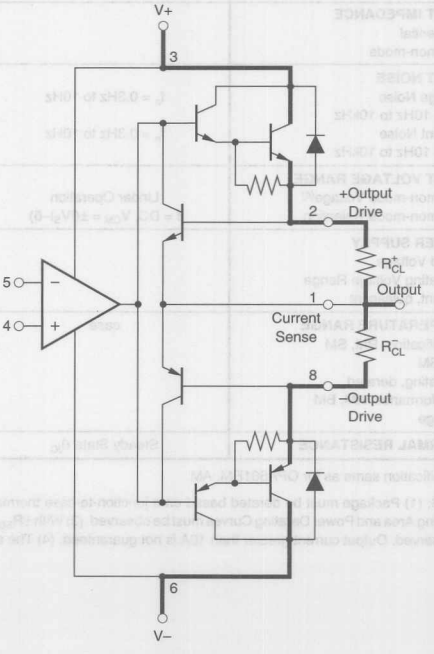
- MOTOR DRIVER
- SERVO AMPLIFIER
- VALVE ACTUATOR
- SYNCRO DRIVER
- PROGRAMMABLE POWER SUPPLY

## DESCRIPTION

The OPA501 is a high output current operational amplifier. It can be used in virtually all common op amp circuits, yet is capable of output currents up to ±10A. Power supply voltages up to ±40V allow very high output power for driving motors or other electro-mechanical loads.

Safe operating area is fully specified, and user-set current limits provide protection for both the amplifier and load. The class-B (zero output stage bias) provides low quiescent current during small-signal conditions.

This rugged hybrid integrated circuit is packaged in a metal 8-pin TO-3 package. Both industrial and military temperature range models are available.




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# SPECIFICATIONS

## ELECTRICAL

At $T_C$ = +25°C, $V_S$ = ±28V, (OPA501RM, AM); $V_S$ = ±34V (OPA501SM, BM), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA501RM, AM | | | OPA501SM, BM | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RATED OUTPUT**[1, 2] | | | | | | | | |
| Output Current | $R_L$ = 2Ω (RM, AM) | ±10 | | | * | | | A |
| Continuous[3] | $R_L$ = 2.6Ω (SM, BM) | ±10 | | | * | | | A |
| Output Voltage[3] | $I_O$ = 10A peak | ±20 | ±23 | | ±26 | ±29 | | V |
| **DYNAMIC RESPONSE** | | | | | | | | |
| Bandwidth, Unity Gain | Small Signal | | 1 | | | * | | MHz |
| Full Power Bandwidth | $V_O$ = 40Vp-p, $R_L$ = 8Ω | 10 | 16 | | * | * | | kHz |
| Slew Rate | $R_L$ = 5Ω (RM, AM) | 1.35 | | | * | | | V/µs |
| | $R_L$ = 6.5Ω (SM, BM) | 1.35 | | | * | | | v/µs |
| **INPUT OFFSET VOLTAGE** | | | | | | | | |
| Initial Offset | | | ±5 | ±10 | | ±2 | ±5 | mV |
| vs Temperature | –25°C < T < +85°C (AM, BM) | | ±10 | ±65 | | | | µV/°C |
| | –55°C < T < +125°C (RM, SM) | | | | | ±10 | ±40 | µV/°C |
| vs Supply Voltage | | | ±35 | | | * | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | | |
| Initial | $T_{CASE}$ = +25°C | | 15 | 40 | | * | 20 | nA |
| vs Temperature | | | ±0.05 | | | * | | nA/°C |
| vs Supply Voltage | | | ±0.02 | | | * | | nA/V |
| **INPUT DIFFERENCE CURRENT** | | | | | | | | |
| Initial | $T_{CASE}$ = +25°C | | ±5 | ±10 | | ±2 | ±3 | nA |
| vs Temperature | –25°C < T < +85°C (AM, BM) | | ±0.01 | | | | | nA/°C |
| | –55°C < T < +125°C (RM, SM) | | | | | ±0.01 | | nA/°C |
| **OPEN-LOOP GAIN, DC** | $R_L$ = 5Ω (RM, AM) | 94 | 115 | | | | | dB |
| $R_L$ = 6.5Ω (SM, BM) | | | | | 98 | 115 | | dB |
| **INPUT IMPEDANCE** | | | | | | | | |
| Differential | | | 10 | | | * | | MΩ |
| Common-mode | | | 250 | | | * | | MΩ |
| **INPUT NOISE** | | | | | | | | |
| Voltage Noise | $f_n$ = 0.3Hz to 10Hz | | 3 | | | * | | µVp-p |
| $f_n$ = 10Hz to 10kHz | | 5 | | | * | | µVrms | |
| Current Noise | $f_n$ = 0.3Hz to 10Hz | | 20 | | | * | | pAp-p |
| $f_n$ = 10Hz to 10kHz | | 4.5 | | | * | | pArms | |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-mode Voltage[4] | Linear Operation | ±($\|V_S\|$–6) | ±($\|V_S\|$–3) | | * | * | | V |
| Common-mode Rejection | f = DC, $V_{CM}$ = ±($\|V_S\|$–6) | 70 | 110 | | 80 | * | | dB |
| **POWER SUPPLY** | | | | | | | | |
| Rated Voltage | | | ±28 | | | ±34 | | V |
| Operating Voltage Range | | ±10 | | ±36 | * | | ±40 | V |
| Current, quiescent | | | ±2.6 | ±10 | | * | * | mA |
| **TEMPERATURE RANGE** | case | | | | | | | |
| Specification, RM, SM | | –55 | | +125 | * | | * | °C |
| AM, BM | | –25 | | +85 | * | | * | °C |
| Operating, derated performance, AM, BM | | –55 | | +125 | * | | * | °C |
| Storage | | –65 | | +150 | * | | * | °C |
| **THERMAL RESISTANCE** | Steady State $\theta_{JC}$ | | 2.0 | 2.2 | | * | * | °C/W |

* Specification same as for OPA501RM, AM.

NOTES: (1) Package must be derated based on a junction-to-case thermal resistance of 2.2°C/W or a junction-to-ambient thermal resistance of 30°C/W. (2) Safe Operating Area and Power Derating Curves must be observed. (3) With ±$R_{SC}$ = 0. Peak output current is typically greater than 10A if duty cycle and pulse width limitations are observed. Output current greater than 10A is not guaranteed. (4) The absolute maximum voltage is 3V less than supply voltage.

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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage ($V_S$) | ±40V |
| Power Dissipation at +25°C[1, 2] | 79W |
| Differential Input Voltage | $\pm V_S$ –3V |
| Common-Mode Input Voltage | $\pm V_S$ |
| Operating Temperature Range | –55°C to +125°C |
| Storage Temperature Range | –65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Junction Temperature | +200°C |
| Output Short-Circuit Duration[3] | Continuous |

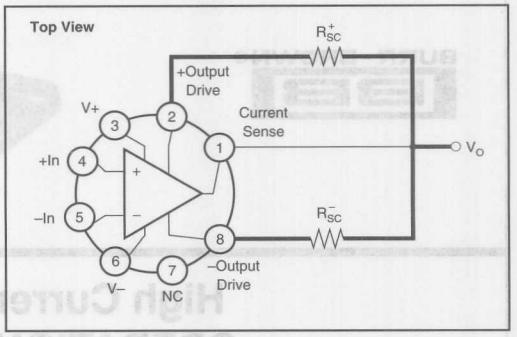
NOTES: (1) At case temperature of +25°C. Derate at 2.2°C/W above case temperature of +25°C. (2) Average dissipation. (3) Within safe operating area and with appropriate derating.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| OPA501AM | 8-Pin Metal TO-3 | 030 | –25°C to +85°C |
| OPA501BM | 8-Pin Metal TO-3 | 030 | –25°C to +85°C |
| OPA501RM | 8-Pin Metal TO-3 | 030 | –55°C to +125°C |
| OPA501SM | 8-Pin Metal TO-3 | 030 | –55°C to +125°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## CONNECTION DIAGRAM




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

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BURR-BROWN®



# OPA502

www.burr-brown.com/databook/OPA502.html

# High Current, High Power OPERATIONAL AMPLIFIER

## FEATURES

- HIGH OUTPUT CURRENT: 10A
- WIDE POWER SUPPLY VOLTAGE: ±10V to ±45V
- USER-SET CURRENT LIMIT
- SLEW RATE: 10V/µs
- FET INPUT: $I_B$ = 200pA max
- CLASS A/B OUTPUT STAGE
- QUIESCENT CURRENT: 25mA max
- HERMETIC TO-3 PACKAGE — ISOLATED CASE

## APPLICATIONS

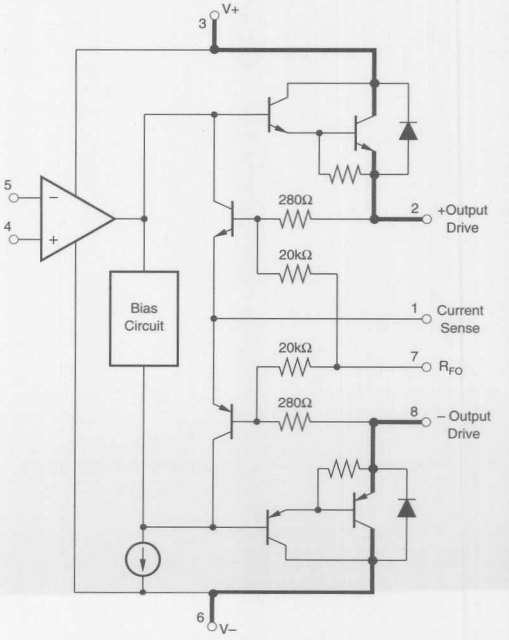
- MOTOR DRIVER
- SERVO AMPLIFIER
- PROGRAMMABLE POWER SUPPLY
- ACTUATOR DRIVER
- AUDIO AMPLIFIER
- TEST EQUIPMENT

## DESCRIPTION

The OPA502 is a high output current operational amplifier designed to drive a wide range of resistive and reactive loads. Its complementary class A/B output stage provides superior performance in applications requiring freedom from crossover distortion. Resistor-programmable current limits provide protection for both the amplifier and the load during abnormal operating conditions. An adjustable foldover current limit can also be used to protect against potentially damaging conditions.

The OPA502 employs a custom monolithic op amp/driver circuit and rugged complementary output transistors, providing excellent DC and dynamic performance.

The industry-standard 8-pin TO-3 package is electrically isolated from all circuitry. This allows the OPA502 to be mounted directly to a heat sink without cumbersome insulating hardware which degrade thermal performance. The OPA502 is available in –40°C to +85°C temperature range.




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# SPECIFICATIONS

$T_{CASE}$ = +25°C, $V_S$ = ±40V, unless otherwise noted.

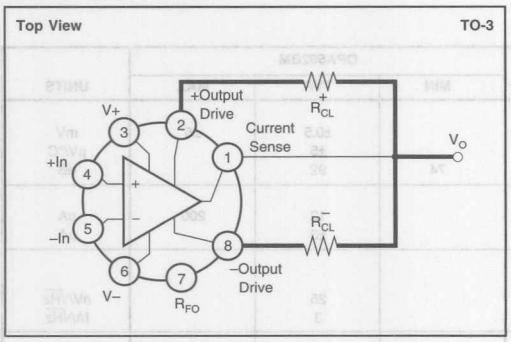
| PARAMETER | CONDITION | OPA502BM MIN | OPA502BM TYP | OPA502BM MAX | UNITS |
|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | | | ±0.5 | ±5 | mV |
| vs Temperature | Specified Temp. Range | | ±5 | | µV/°C |
| vs Power Supply | $V_S$ = ±10V to ±45V | 74 | 92 | | dB |
| **INPUT BIAS CURRENT**(1) | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | 12 | 200 | pA |
| Input Offset Current | $V_{CM}$ = 0V | | ±3 | | pA |
| **NOISE** | | | | | |
| Input Voltage Noise | | | | | |
| Noise Density, | f = 1kHz | | 25 | | nV/√Hz |
| Current Noise Density, | f = 1kHz | | 3 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range, Positive | Linear Operation | (V+) –5 | (V+) –4 | | V |
| Negative | Linear Operation | (V–) +5 | (V–) +4 | | V |
| Common-Mode Rejection | $V_{CM}$ = ±35V | 74 | 106 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $10^{12}$ \|\| 5 | | Ω \|\| pF |
| Common-Mode | | | $10^{12}$ \|\| 4 | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±34V, $R_L$ = 6Ω | 92 | 103 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product | G = +10, $R_L$ = 50Ω | | 2.0 | | MHz |
| Slew Rate | 68Vp-p, $R_L$ = 6Ω | 5 | 10 | | V/µs |
| Full-Power Bandwidth | | | See Typical Curves | | |
| Total Harmonic Distortion | G = +3, f = 20kHz | | 0.06 | | % |
| | $V_O$ = 20V, $R_L$ = 8Ω | | | | |
| Capacitive Load | | | See Figure 6 | | |
| **OUTPUT** | | | | | |
| Voltage Output, Positive | $I_O$ = 10A | (V+) –6 | (V+)–3.5 | | V |
| Negative | $I_O$ = 10A | (V–) +6 | (V–) +3.6 | | V |
| Positive | $I_O$ = 1A | | (V+) –2.5 | | V |
| Negative | $I_O$ = 1A | | (V–) +3.1 | | V |
| Current Output | | | See SOA Curves | | |
| Short Circuit Current | | | Resistor Programmed | | |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±40 | | V |
| Operating Voltage Range | | ±10 | | ±45 | V |
| Quiescent Current | $I_O$ = 0 | | ±20 | ±25 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –40 | | +85 | °C |
| Storage | | –55 | | +125 | °C |
| Thermal Resistance, $\theta_{JC}$ | DC | | 1.25 | 1.4 | °C/W |
| | AC f ≥ 50Hz | | 0.8 | 0.9 | °C/W |
| $\theta_{JA}$ | No Heat Sink | | 30 | | °C/W |

NOTE: (1) High-speed test at $T_J$ = 25°C.



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## PIN CONFIGURATION




## ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|---|
| Supply Voltage, V+ to V– | 90V |
| Output Current | See SOA Curve |
| Input Voltage | (V–) –1V to (V+)+1V |
| Case Temperature, Operating | 150°C |
| Junction Temperature | 200°C |

NOTE: (1) Stresses above these ratings may cause permanent damage.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| OPA502BM | 8-Pin TO-3 | 030 | –40°C to +85°C |

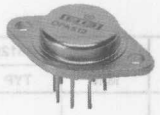
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR - BROWN®



# OPA512

www.burr-brown.com/databook/OPA512.html



# Very High Current—High Power OPERATIONAL AMPLIFIER

## FEATURES

- WIDE SUPPLY RANGE: ±10V to ±50V
- HIGH OUTPUT CURRENT: 15A Peak
- CLASS A/B OUTPUT STAGE: Low Distortion
- VOLTAGE-CURRENT LIMIT PROTECTION CIRCUIT
- SMALL TO-3 PACKAGE

## APPLICATIONS

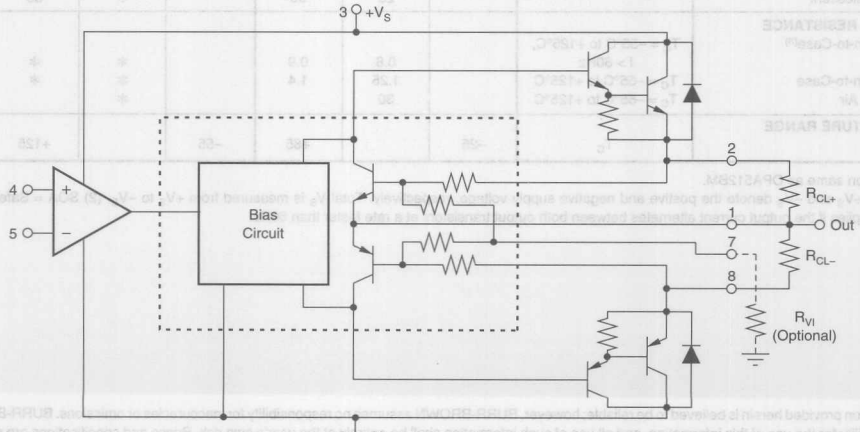
- SERVO AMPLIFIER
- MOTOR DRIVER
- SYNCRO EXCITATION
- AUDIO AMPLIFIER
- TEST PIN DRIVER

## DESCRIPTION

The OPA512 is a high voltage, very-high current operational amplifier designed to drive a wide variety of resistive and reactive loads. Its complementary class A/B output stage provides superior performance in applications requiring freedom from cross-over distortion. User-set current limit circuitry provides protection to the amplifier and load in fault conditions. A resistor-programmable voltage-current limiter circuit may be used to further protect the amplifier from damaging conditions.

The OPA512 employs a laser-trimmed monolithic integrated circuit to bias the output transistors, providing excellent low-level signal fidelity and high output voltage swing. The reduced internal parts count made possible with this monolithic IC improves performance and reliability.

This hybrid integrated circuit is housed in a hermetic TO-3 package and all circuitry is electrically-isolated from the case. This allows direct mounting to a chassis or heat sink without cumbersome insulating hardware and provides optimum heat transfer.




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# SPECIFICATIONS

## ELECTRICAL

At $T_C$ = +25°C, and $V_S$ = ±40V, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA512BM | | | OPA512SM | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT OFFSET VOLTAGE** | | | | | | | | |
| Initial Offset | | | ±2 | ±6 | | ±1 | ±3 | mV |
| vs Temperature | Specified Temp. Range | | ±10 | ±65 | | * | ±40 | µV/°C |
| vs Supply Voltage | | | ±30 | ±200 | | * | * | µV/V |
| vs Power | | | ±20 | | | * | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | | |
| Initial | | | 12 | 30 | | 10 | 20 | nA |
| vs Temperature | Specified Temp. Range | | ±50 | 400 | | * | * | pA/°C |
| vs Supply Voltage | | | ±10 | | | * | | pA/V |
| **INPUT OFFSET CURRENT** | | | | | | | | |
| Initial | | | ±12 | ±30 | | ±5 | ±10 | nA |
| vs Temperature | Specfied Temp. Range | | ±50 | | | * | | pA/°C |
| **INPUT IMPEDANCE, DC** | | | 200 | | | * | | MΩ |
| **INPUT CAPACITANCE** | | | 3 | | | * | | pF |
| **VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Voltage | Specified Temp. Range | ±($\|V_S\|$ – 5) | ±($\|V_S\|$ – 3) | | * | * | | V |
| Common-Mode Rejection | Specified Temp. Range | 74 | 100 | | * | * | | dB |
| **GAIN** | | | | | | | | |
| Open-Loop Gain at 10Hz | 1kΩ Load | | 110 | | | * | | dB |
| | Specified Temp. Range | | | | | | | |
| | 8Ω Load | 96 | 108 | | * | * | | dB |
| Gain-Bandwidth Product, 1MHz | 8Ω Load | | 4 | | | * | | MHz |
| Power Bandwidth | 8Ω Load | 13 | 20 | | * | * | | kHz |
| Phase Margin | Specified Temp. Range | | | | | | | |
| | 8Ω Load | | 20 | | | * | | Degrees |
| **OUTPUT** | | | | | | | | |
| Voltage Swing [1] | BM at 10A, SM at 15A | ±($\|V_S\|$ – 6) | | | ±($\|V_S\|$ – 7) | | | V |
| | Specified Temp. Range | | | | | | | |
| | $I_O$ = 80mA | ±($\|V_S\|$ – 5) | | | * | | | V |
| | $I_O$ = 5A | ±($\|V_S\|$ – 5) | | | * | | | V |
| Current, Peak | | 10 | | | 15 | | | A |
| Settling Time to 0.1% | 2V Step | | 2 | | | * | | µs |
| Slew Rate | | 2.5 | 4 | | * | * | | V/µs |
| Capacitive Load | Specified Temp. Range | | | | | | | |
| | G = 1 | | | 1.5 | | | * | nF |
| | Specified Temp. Range | | | | | | | |
| | G > 10 | | | SOA[2] | | | * | |
| **POWER SUPPLY** | | | | | | | | |
| Voltage | Specified Temp. Range | ±10 | ±40 | ±45 | * | * | ±50 | V |
| Current, Quiescent | | | 25 | 50 | | * | 35 | mA |
| **THERMAL RESISTANCE** | | | | | | | | |
| AC Junction-to-Case[3] | $T_C$ = –55°C to +125°C, | | | | | | | |
| | f > 60Hz | | 0.8 | 0.9 | | * | * | °C/W |
| DC Junction-to-Case | $T_C$ = –55°C to +125°C | | 1.25 | 1.4 | | * | * | °C/W |
| Junction to Air | $T_C$ = –55°C to +125°C | | 30 | | | * | | °C/W |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified | $T_C$ | –25 | | +85 | –55 | | +125 | °C |

* Specification same as OPA512BM.

NOTES: (1) $+V_S$ and $-V_S$ denote the postive and negative supply voltage, respectively. Total $V_S$ is measured from $+V_S$ to $-V_S$. (2) SOA = Safe Operating Area. (3) Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

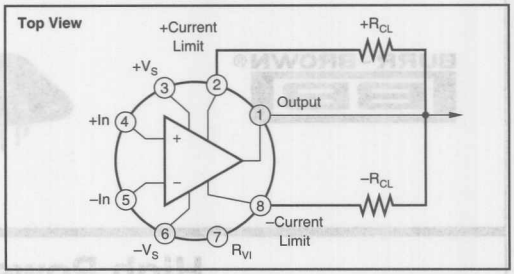
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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, $+V_S$ to $-V_S$ | 100V |
| Output Current: Source | 15A |
| Sink | see SOA |
| Power Dissipation, Internal[1] | 125W |
| Input Voltage: Differential | ±(\|$V_S$\| – 3V) |
| Common-mode | ±$V_S$ |
| Temperature: Pins (soldering, 10s) | +300°C |
| Junction[1] | +200°C |
| Temperature Range: Storage[2] | –65°C to +150°C |
| Operating (Case) | –55°C to +125°C |

NOTES: (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. (2) OPA512BM, –55°C to +100°C.

## CONNECTION DIAGRAM




## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| OPA512BM | 8-Pin TO-3 | 030 | –25°C to +85°C |
| OPA512SM | 8-Pin TO-3 | 030 | –55°C to +125°C |

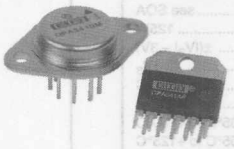
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®



# OPA541

www.burr-brown.com/databook/OPA541.html

# High Power Monolithic OPERATIONAL AMPLIFIER

## FEATURES

- POWER SUPPLIES TO ±40V
- OUTPUT CURRENT TO 10A PEAK
- PROGRAMMABLE CURRENT LIMIT
- INDUSTRY-STANDARD PIN OUT
- FET INPUT
- TO-3 AND LOW-COST POWER PLASTIC PACKAGES

## APPLICATIONS

- MOTOR DRIVER
- SERVO AMPLIFIER
- SYNCHRO EXCITATION
- AUDIO AMPLIFIER
- PROGRAMMABLE POWER SUPPLY

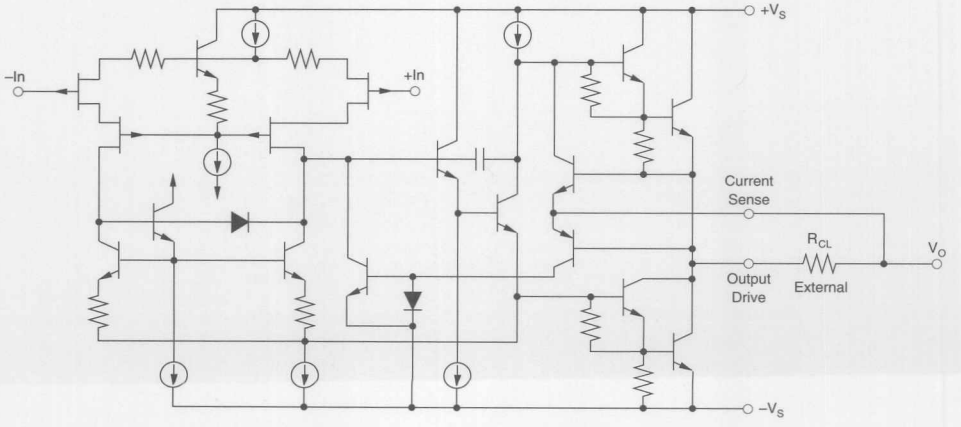
## DESCRIPTION

The OPA541 is a power operational amplifier capable of operation from power supplies up to ±40V and delivering continuous output currents up to 5A. Internal current limit circuitry can be user-programmed with a single external resistor, protecting the amplifier and load from fault conditions. The OPA541 is fabricated using a proprietary bipolar/FET process.

Pinout is compatible with popular hybrid power amplifiers such as the OPA511, OPA512 and the 3573.

The OPA541 uses a single current-limit resistor to set both the positive and negative current limits. Applications currently using hybrid power amplifiers requiring two current-limit resistors need not be modified.

The OPA541 is available in an 11-pin power plastic package and an industry-standard 8-pin TO-3 hermetic package. The power plastic package has a copper-lead frame to maximize heat transfer. The TO-3 package is isolated from all circuitry, allowing it to be mounted directly to a heat sink without special insulators.




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# SPECIFICATIONS

## ELECTRICAL

At $T_C$= +25°C and $V_S$ = ±35VDC, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA541AM/AP MIN | OPA541AM/AP TYP | OPA541AM/AP MAX | OPA541BM/SM MIN | OPA541BM/SM TYP | OPA541BM/SM MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **INPUT OFFSET VOLTAGE** | | | | | | | | |
| $V_{OS}$ | | | ±2 | ±10 | | ±0.1 | ±1 | mV |
| vs Temperature | Specified Temperature Range | | ±20 | ±40 | | ±15 | ±30 | µV/°C |
| vs Supply Voltage | $V_S$ = ±10V to $±V_{MAX}$ | | ±2.5 | ±10 | | * | * | µV/V |
| vs Power | | | ±20 | ±60 | | * | * | µV/W |
| **INPUT BIAS CURRENT** | | | | | | | | |
| $I_B$ | | | 4 | 50 | | * | * | pA |
| **INPUT OFFSET CURRENT** | | | | | | | | |
| $I_{OS}$ | | | ±1 | ±30 | | * | * | pA |
| | Specified Temperature Range | | | 5 | | * | | nA |
| **INPUT CHARACTERISTICS** | | | | | | | | |
| Common-Mode Voltage Range | Specified Temperature Range | ±($\|V_S\|$ – 6) | ±($\|V_S\|$ – 3) | | * | * | | V |
| Common-Mode Rejection | $V_{CM}$ = (±$\|V_S\|$ – 6V) | 95 | 113 | | * | * | | dB |
| Input Capacitance | | | 5 | | | * | | pF |
| Input Impedance, DC | | | 1 | | | * | | TΩ |
| **GAIN CHARACTERISTICS** | | | | | | | | |
| Open Loop Gain at 10Hz | $R_L$ = 6Ω | 90 | 97 | | * | * | | dB |
| Gain-Bandwidth Product | | | 1.6 | | | * | | MHz |
| **OUTPUT** | | | | | | | | |
| Voltage Swing | $I_O$ = 5A, Continuous | ±($\|V_S\|$ – 5.5) | ±($\|V_S\|$ – 4.5) | | * | * | | V |
| | $I_O$ = 2A | ±($\|V_S\|$ – 4.5) | ±($\|V_S\|$ – 3.6) | | * | * | | V |
| | $I_O$ = 0.5A | ±($\|V_S\|$ – 4) | ±($\|V_S\|$ – 3.2) | | * | * | | V |
| Current, Peak | | 9 | 10 | | * | * | | A |
| **AC PERFORMANCE** | | | | | | | | |
| Slew Rate | | 6 | 10 | | * | * | | V/µs |
| Power Bandwidth | $R_L$ = 8Ω, $V_O$ = 20Vrms | 45 | 55 | | * | * | | kHz |
| Settling Time to 0.1% | 2V Step | | 2 | | | * | | µs |
| Capacitive Load | Specified Temperature Range, G = 1 | 3.3 | | | | | * | nF |
| | Specified Temperature Range, G >10 | | | SOA[1] | | | * | |
| Phase Margin | Specified Temperature Range, $R_L$ = 8Ω | | 40 | | | * | | Degrees |
| **POWER SUPPLY** | | | | | | | | |
| Power Supply Voltage, $±V_S$ | Specified Temperature Range | ±10 | ±30 | ±35 | * | ±35 | ±40 | V |
| Current, Quiescent | | | 20 | 25 | | * | * | mA |
| **THERMAL RESISTANCE** | | | | | | | | |
| $\theta_{JC}$ (Junction-to-Case)[2] | AC Output f > 60Hz | | 2.5 | | | | | °C/W |
| $\theta_{JC}$[2] | DC Output | | 3 | | | | | °C/W |
| $\theta_{JA}$ (Junction-to-Ambient) | No Heat Sink | | 40 | | | | | °C/W |
| OPA541AP (Plastic) | | | 40 | | | | | °C/W |
| **TEMPERATURE RANGE** | | | | | | | | |
| $T_{CASE}$ | AM, BM, AP | –25 | | +85 | * | | * | °C |
| | SM | | | | –55 | | +125 | °C |

* Specification same as OPA541AM/AP.

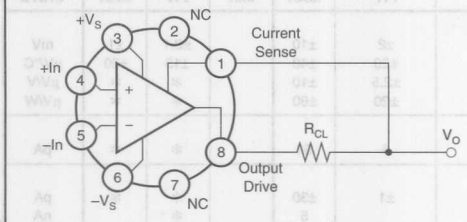
NOTE: (1) SOA is the Safe Operating Area shown in Figure 1. (2) Plastic package may require insulator which typically adds 1°C/W.



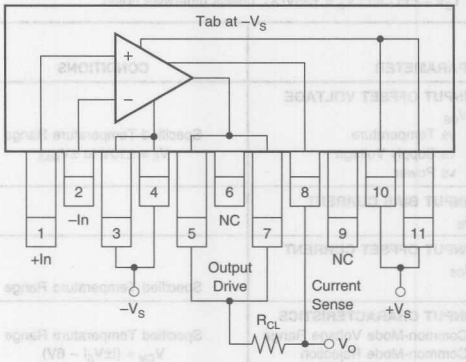
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## CONNECTION DIAGRAMS

Top View — TO-3




Plastic Package




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, $+V_S$ to $-V_S$ | 80V |
| Output Current | see SOA |
| Power Dissipation, Internal(1) | 125W |
| Input Voltage: Differential | $\pm V_S$ |
| Common-mode | $\pm V_S$ |
| Temperature: Pin solder, 10s | +300°C |
| Junction(1) | +150°C |
| Temperature Range: | |
| AM, BM SM | |
| Storage | –65°C to +150°C |
| Operating (case) | –55°C to +125°C |
| AP | |
| Storage | –40°C to +85°C |
| Operating (case) | –25°C to +85°C |

NOTE: (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

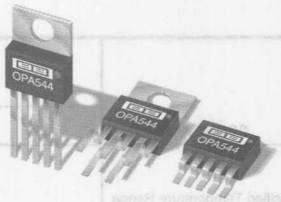
| PRODUCT | PACKAGE | TEMPERATURE RANGE | CONTINUOUS CURRENT |
|---|---|---|---|
| OPA541AP | Power Plastic | –25°C to +85°C | 5A at 25°C |
| OPA541AM | TO-3 | –25°C to +85°C | 5A at 25°C |
| OPA541BM | TO-3 | –25°C to +85°C | 5A at 25°C |
| OPA541SM | TO-3 | –55°C to +125°C | 5A at 25°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| OPA541AP | Power Plastic | 242 |
| OPA541AM | TO-3 | 030 |
| OPA541BM | TO-3 | 030 |
| OPA541SM | TO-3 | 030 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# OPA544

www.burr-brown.com/databook/OPA544.html



# High-Voltage, High-Current OPERATIONAL AMPLIFIER

## FEATURES

- HIGH OUTPUT CURRENT: 2A min
- WIDE POWER SUPPLY RANGE: ±10 to ±35V
- SLEW RATE: 8V/µs
- INTERNAL CURRENT LIMIT
- THERMAL SHUTDOWN PROTECTION
- FET INPUT: $I_B$ = 100pA max
- 5-LEAD TO-220 PLASTIC PACKAGE
- 5-LEAD SURFACE MOUNT PACKAGE

## APPLICATIONS

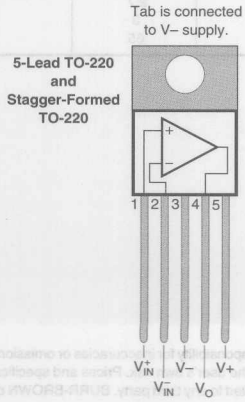
- MOTOR DRIVER
- PROGRAMMABLE POWER SUPPLY
- SERVO AMPLIFIER
- VALVES, ACTUATOR DRIVER
- MAGNETIC DEFLECTION COIL DRIVER
- AUDIO AMPLIFIER

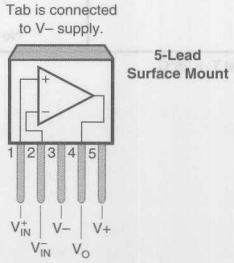
## DESCRIPTION

The OPA544 is a high-voltage/high-current operational amplifier suitable for driving a wide variety of high power loads. High performance FET op amp circuitry and high power output stage are combined on a single monolithic chip.

The OPA544 is protected by internal current limit and thermal shutdown circuits.

The OPA544 is available in industry-standard 5-lead TO-220 and 5-lead surface-mount power packages. Its copper tab allows easy mounting to a heat sink for excellent thermal performance. It is specified for operation over the extended industrial temperature range, –40°C to +85°C.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

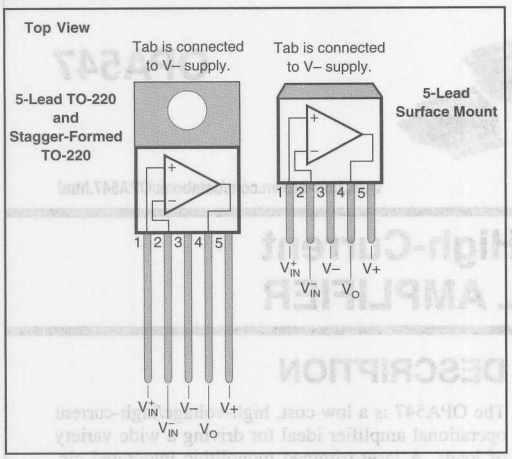
At $T_{CASE}$ = +25°C, $V_S$ = ±35V, unless otherwise noted.

| PARAMETER | CONDITION | OPA544T, OPA544T-1, OPA544F MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | | | ±1 | ±5 | mV |
| vs Temperature | Specified Temperature Range | | ±10 | | µV/°C |
| vs Power Supply | $V_S$ = ±10V to ±35V | | ±10 | ±100 | µV/V |
| **INPUT BIAS CURRENT**(1) | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | ±15 | ±100 | pA |
| vs Temperature | | | See Typical Curve | | |
| Input Offset Current | $V_{CM}$ = 0V | | ±10 | ±100 | pA |
| **NOISE** | | | | | |
| Input Voltage Noise | | | | | |
| Noise Density, f = 1kHz | | | 36 | | nV/√Hz |
| Current Noise Density, f = 1kHz | | | 3 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range, Positive | Linear Operation | (V+) –6 | (V+) –4 | | V |
| Negative | Linear Operation | (V–) +6 | (V–) +4 | | V |
| Common-Mode Rejection | $V_{CM} = \pm V_S - 6V$ | 90 | 106 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $10^{12}$ II 8 | | Ω II pF |
| Common-Mode | | | $10^{12}$ II 10 | | Ω II pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±30V, $R_L$ = 1kΩ | 90 | 103 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain Bandwidth Product | $R_L$ = 15Ω | | 1.4 | | MHz |
| Slew Rate | 60Vp-p, $R_L$ = 15Ω | 5 | 8 | | V/µs |
| Full-Power Bandwidth | | | See Typical Curve | | |
| Settling Time 0.1% | G = –10, 60V Step | | 25 | | µs |
| Total Harmonic Distortion | | | See Typical Curve | | |
| **OUTPUT** | | | | | |
| Voltage Output, Positive | $I_O$ = 2A | (V+) –5 | (V+) –4.4 | | V |
| Negative | $I_O$ = 2A | (V–) +5 | (V–) +3.8 | | V |
| Positive | $I_O$ = 0.5A | (V+) –4.2 | (V+) –3.8 | | V |
| Negative | $I_O$ = 0.5A | (V–) +4 | (V–) +3.1 | | V |
| Current Output | | | See SOA Curves | | |
| Short-Circuit Current | | | 4 | | A |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±35 | | V |
| Operating Voltage Range | | ±10 | | ±35 | V |
| Quiescent Current | $I_O$ = 0 | | ±12 | ±15 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –40 | | +85 | °C |
| Storage | | –40 | | +125 | °C |
| Thermal Resistance, $\theta_{JC}$ | f > 50Hz | | 2.7 | | °C/W |
| Thermal Resistance, $\theta_{JC}$ | DC | | 3 | | °C/W |
| Thermal Resistance, $\theta_{JA}$ | No Heat Sink | | 65 | | °C/W |

NOTES: (1) High-speed test at $T_J$ = 25°C.

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## CONNECTION DIAGRAMS




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, V+ to V– | 70V |
| Output Current | See SOA Curve |
| Input Voltage | (V–) –0.7V to (V+) +0.7V |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering –10s)[1] | 300°C |

NOTE: (1) Vapor-phase or IR reflow techniques are recommended for soldering the OPA544F surface mount package. Wave soldering is not recommended due to excessive thermal shock and "shadowing" of nearby devices.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| OPA544T | 5-Lead TO-220 | 315 |
| OPA544T-1 | 5-Lead Stagger-Formed TO-220 | 323 |
| OPA544F | 5-Lead Surface-Mount | 325 |

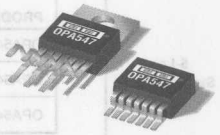
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# OPA547

www.burr-brown.com/databook/OPA547.html

# High-Voltage, High-Current OPERATIONAL AMPLIFIER

## FEATURES

- WIDE SUPPLY RANGE
  Single Supply: +8V to +60V
  Dual Supply: ±4V to ±30V
- HIGH OUTPUT CURRENT:
  500mA Continuous
- WIDE OUTPUT VOLTAGE SWING
- FULLY PROTECTED:
  Thermal Shutdown
  Adjustable Current Limit
- OUTPUT DISABLE CONTROL
- THERMAL SHUTDOWN INDICATOR
- HIGH SLEW RATE: 6V/µs
- LOW QUIESCENT CURRENT
- PACKAGES:
  7-Lead TO-220
  7-Lead DDPAK Surface-Mount

## APPLICATIONS

- VALVE, ACTUATOR DRIVER
- SYNCHRO, SERVO DRIVER
- POWER SUPPLIES
- TEST EQUIPMENT
- TRANSDUCER EXCITATION
- AUDIO AMPLIFIER

## DESCRIPTION

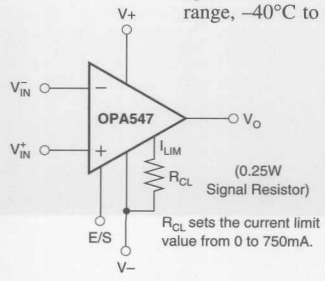
The OPA547 is a low cost, high-voltage/high-current operational amplifier ideal for driving a wide variety of loads. A laser-trimmed monolithic integrated circuit provides excellent low-level signal accuracy and high output voltage and current.

The OPA547 operates from either single or dual supplies for design flexibility. In single supply operation, the input common-mode range extends below ground.

The OPA547 is internally protected against overtemperature conditions and current overloads. In addition, the OPA547 was designed to provide an accurate, user-selected current limit. Unlike other designs which use a "power" resistor in series with the output current path, the OPA547 senses the load indirectly. This allows the current limit to be adjusted from 0 to 750mA with a 0 to 150µA control signal. This is easily done with a resistor/potentiometer or controlled digitally with a voltage-out or current-out DAC.

The Enable/Status (E/S) pin provides two functions. An input on the pin not only disables the output stage to effectively disconnect the load but also reduces the quiescent to conserve power. The E/S pin output can be monitored to determine if the OPA547 is in thermal shutdown.

The OPA547 is available in an industry-standard 7-lead staggered TO-220 package and a 7-lead DDPAK surface-mount plastic power package. The copper tab allows easy mounting to a heat sink or circuit board for excellent thermal performance. It is specified for operation over the extended industrial temperature range, –40°C to +85°C.




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# SPECIFICATIONS

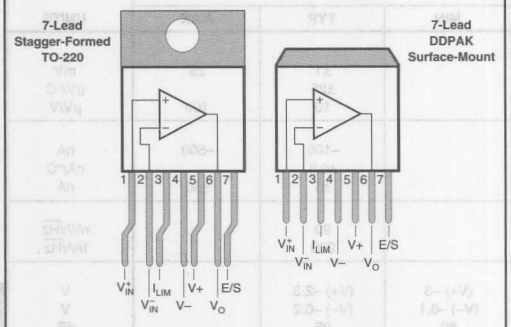
At $T_{CASE}$ = +25°C, $V_S$ = ±30V and E/S pin open, unless otherwise noted.

| PARAMETER | CONDITION | OPA547T, F MIN | OPA547T, F TYP | OPA547T, F MAX | UNITS |
|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0, $I_O$ = 0 | | ±1 | ±5 | mV |
| vs Temperature | $T_A$ = –40°C to +85°C | | ±25 | | µV/°C |
| vs Power Supply | $V_S$ = ±4V to ±30V | | 10 | 100 | µV/V |
| **INPUT BIAS CURRENT**(1) | | | | | |
| Input Bias Current(2) | $V_{CM}$ = 0V | | –100 | –500 | nA |
| vs Temperature | | | ±0.5 | | nA/°C |
| Input Offset Current | $V_{CM}$ = 0V | | ±5 | ±50 | nA |
| **NOISE** | | | | | |
| Input Voltage Noise Density, f = 1kHz | | | 90 | | nV/√Hz |
| Current Noise Density, f = 1kHz | | | 200 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Voltage Range: Positive | Linear Operation | (V+) –3 | (V+) –2.3 | | V |
| Negative | Linear Operation | (V–) –0.1 | (V–) –0.2 | | V |
| Common-Mode Rejection | $V_{CM}$ = (V–) –0.1V to (V+) –3V | 80 | 95 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $10^7$ ll 6 | | Ω ll pF |
| Common-Mode | | | $10^9$ ll 4 | | Ω ll pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain, f = 10Hz | $V_O$ = ±25V, $R_L$ = 1kΩ | 100 | 115 | | dB |
| | $V_O$ = ±25V, $R_L$ = 50Ω | | 110 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product | $R_L$ = 50Ω | | 1 | | MHz |
| Slew Rate | G = 1, 50Vp-p, $R_L$ = 50Ω | | 6 | | V/µs |
| Full Power Bandwidth | | | See Typical Curve | | kHz |
| Settling Time: ±0.1% | G = –10, 50V Step | | 18 | | µs |
| Total Harmonic Distortion + Noise, f = 1kHz | $R_L$ = 50Ω, G = +3V, 1W Power | | 0.004(3) | | % |
| **OUTPUT** | | | | | |
| Voltage Output, Positive | $I_O$ = 0.5A | (V+) –2.2 | (V+) –1.9 | | V |
| Negative | $I_O$ = –0.5A | (V–) +1.6 | (V–) +1.3 | | V |
| Positive | $I_O$ = 0.1A | (V+) –1.8 | (V+) –1.5 | | V |
| Negative | $I_O$ = –0.1A | (V–) +1.2 | (V–) +0.8 | | V |
| Maximum Continuous Current Output: dc | | ±500 | | | mA |
| ac | | 500 | | | mArms |
| Leakage Current, Output Disabled, dc | | | See Typical Curve | | |
| Output Current Limit | | | | | |
| Current Limit Range | | | 0 to ±750 | | mA |
| Current Limit Equation | | | $I_{LIM}$ = (5000)(4.75)/(31600Ω + $R_{CL}$) | | A |
| Current Limit Tolerance(1) | $R_{CL}$ = 31.6kΩ ($I_{LIM}$ = ±375mA), | | ±10 | ±30 | mA |
| | $R_L$ = 50Ω | | | | |
| Capacitive Load Drive | | | See Typical Curve(4) | | |
| **OUTPUT ENABLE /STATUS (E/S) PIN** | | | | | |
| Shutdown Input Mode | | | | | |
| $V_{E/S}$ High (output enabled) | E/S Pin Open or Forced High | (V–) +2.4 | | | V |
| $V_{E/S}$ Low (output disabled) | E/S Pin Forced Low | | | (V–) +0.8 | V |
| $I_{E/S}$ High (output enabled) | E/S Pin High | | –60 | | µA |
| $I_{E/S}$ Low (output disabled) | E/S Pin Low | | –65 | | µA |
| Output Disable Time | | | 1 | | µs |
| Output Enable Time | | | 3 | | ms |
| Thermal Shutdown Status Output | | | | | |
| Normal Operation | Sourcing 20µA | (V–) +2.4 | (V–) +3.5 | | V |
| Thermally Shutdown | Sinking 5µA, $T_J$ > 160°C | | (V–) +0.35 | (V–) +0.8 | V |
| Junction Temperature, Shutdown | | | +160 | | °C |
| Reset from Shutdown | | | +140 | | °C |
| **POWER SUPPLY** | | | | | |
| Specified Voltage | | | ±30 | | V |
| Operating Voltage Range | | ±4 | | ±30 | V |
| Quiescent Current | $I_{LIM}$ Connected to V–, $I_O$ = 0 | | ±10 | ±15 | mA |
| Quiescent Current, Shutdown Mode | $I_{LIM}$ Connected to V– | | ±4 | | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specified Range | | –40 | | +85 | °C |
| Operating Range | | –40 | | +125 | °C |
| Storage Range | | –55 | | +125 | °C |
| Thermal Resistance, $\theta_{JC}$ | | | | | |
| 7-Lead DDPAK, 7-Lead TO-220 | f > 50Hz | | 2 | | °C/W |
| 7-Lead DDPAK, 7-Lead TO-220 | dc | | 3 | | °C/W |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| 7-Lead DDPAK, 7-Lead TO-220 | No Heat Sink | | 65 | | °C/W |

NOTES: (1) High-speed test at $T_J$ = +25°C. (2) Positive conventional current flows into the input terminals. (3) See "Total Harmonic Distortion+Noise" in the Typical Performance Curves section for additional power levels. (4) See "Small-Signal Overshoot vs Load Capacitance" in the Typical Performance Curves section.

## CONNECTION DIAGRAMS

Top Front View




NOTE: Tabs are electrically connected to V– supply.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Output Current | See SOA Curve |
| Supply Voltage, V+ to V– | 60V |
| Input Voltage | (V–)–0.5V to (V+)+0.5V |
| Input Shutdown Voltage | V+ |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering 10s)[2] | 300°C |

NOTE: (1) Stresses above these ratings may cause permanent damage. (2) Vapor-phase or IR reflow techniques are recommended for soldering the OPA547F surface mount package. Wave soldering is not recommended due to excessive thermal shock and "shadowing" of nearby devices.

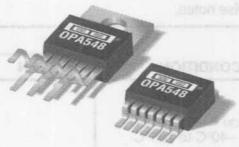
## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| OPA547T | 7-Lead Stagger-Formed TO-220 | 327 | –40°C to +85°C |
| OPA547F[2] | 7-Lead DDPAK Surface-Mount | 328 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet or Appendix C of Burr-Brown IC Data Book. (2) Available on Tape and Reel.

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# OPA548

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# High-Voltage, High-Current OPERATIONAL AMPLIFIER

## FEATURES

- WIDE SUPPLY RANGE
  Single Supply: +8V to +60V
  Dual Supply: ±4V to ±30V
- HIGH OUTPUT CURRENT:
  3A Continuous
  5A Peak
- WIDE OUTPUT VOLTAGE SWING
- FULLY PROTECTED:
  Thermal Shutdown
  Adjustable Current Limit
- OUTPUT DISABLE CONTROL
- THERMAL SHUTDOWN INDICATOR
- HIGH SLEW RATE: 10V/µs
- LOW QUIESCENT CURRENT
- PACKAGES:
  7-Lead TO-220
  7-Lead DDPAK Surface-Mount

## APPLICATIONS

- VALVE, ACTUATOR DRIVER
- SYNCHRO, SERVO DRIVER
- POWER SUPPLIES
- TEST EQUIPMENT
- TRANSDUCER EXCITATION
- AUDIO AMPLIFIER

## DESCRIPTION

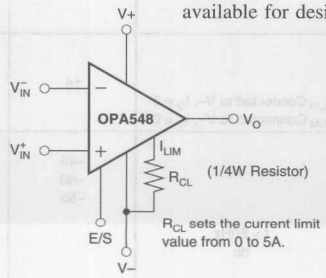
The OPA548 is a low cost, high-voltage/high-current operational amplifier ideal for driving a wide variety of loads. A laser-trimmed monolithic integrated circuit provides excellent low-level signal accuracy and high output voltage and current.

The OPA548 operates from either single or dual supplies for design flexibility. In single supply operation, the input common-mode range extends below ground.

The OPA548 is internally protected against overtemperature conditions and current overloads. In addition, the OPA548 was designed to provide an accurate, user-selected current limit. Unlike other designs which use a "power" resistor in series with the output current path, the OPA548 senses the load indirectly. This allows the current limit to be adjusted from 0 to 5A with a resistor/potentiometer or controlled digitally with a voltage-out or current-out DAC.

The Enable/Status (E/S) pin provides two functions. An input on the pin not only disables the output stage to effectively disconnect the load but also reduces the quiescent current to conserve power. The E/S pin output can be monitored to determine if the OPA548 is in thermal shutdown.

The OPA548 is available in an industry-standard 7-lead staggered TO-220 package and a 7-lead DDPAK surface-mount plastic power package. The copper tab allows easy mounting to a heat sink or circuit board for excellent thermal performance. It is specified for operation over the extended industrial temperature range, –40°C to +85°C. A SPICE macromodel is available for design analysis.




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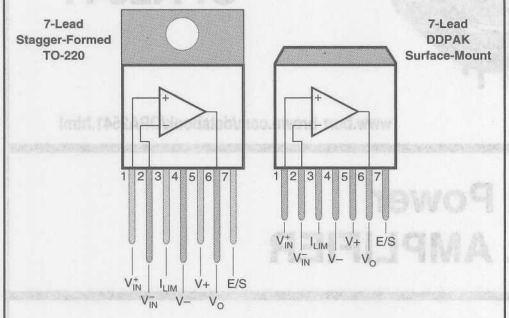
At $T_{CASE}$ = +25°C, $V_S$ = ±30V and E/S pin open, unless otherwise noted.

| PARAMETER | CONDITION | OPA548T, F MIN | OPA548T, F TYP | OPA548T, F MAX | UNITS |
|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0, $I_O$ = 0 | | ±2 | ±10 | mV |
| vs Temperature | $T_A$ = –40°C to +85°C | | ±30 | | µV/°C |
| vs Power Supply | $V_S$ = ±4V to ±30V | | 30 | 100 | µV/V |
| **INPUT BIAS CURRENT**[1] | | | | | |
| Input Bias Current[2] | $V_{CM}$ = 0V | | –100 | –500 | nA |
| vs Temperature | $T_A$ = –40°C to +85°C | | ±0.5 | | nA/°C |
| Input Offset Current | $V_{CM}$ = 0V | | ±5 | ±50 | nA |
| **NOISE** | | | | | |
| Input Voltage Noise Density, f = 1kHz | | | 90 | | nV/√Hz |
| Current Noise Density, f = 1kHz | | | 200 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Voltage Range: Positive | Linear Operation | (V+) –3 | (V+) –2.3 | | V |
| Negative | Linear Operation | (V–) –0.1 | (V–) –0.2 | | V |
| Common-Mode Rejection | $V_{CM}$ = (V–) –0.1V to (V+) –3V | 80 | 95 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $10^7$ ll 6 | | Ω ll pF |
| Common-Mode | | | $10^9$ ll 4 | | Ω ll pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±25V, $R_L$ = 1kΩ | 90 | 98 | | dB |
| | $V_O$ = ±25V, $R_L$ = 8Ω | | 90 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product | $R_L$ = 8Ω | | 1 | | MHz |
| Slew Rate | G = 1, 50Vp-p, $R_L$ = 8Ω | | 10 | | V/µs |
| Full Power Bandwidth | | | See Typical Curve | | kHz |
| Settling Time: ±0.1% | G = –10, 50V Step | | 15 | | µs |
| Total Harmonic Distortion + Noise, f = 1kHz | $R_L$ = 8Ω, G = +3, Power = 10W | | 0.02[3] | | % |
| **OUTPUT** | | | | | |
| Voltage Output, Positive | $I_O$ = 3A | (V+) –4.1 | (V+) –3.7 | | V |
| Negative | $I_O$ = –3A | (V–) +3.7 | (V–) +3.3 | | V |
| Positive | $I_O$ = 0.6A | (V+) –2.4 | (V+) –2.1 | | V |
| Negative | $I_O$ = –0.6A | (V–) +1.3 | (V–) +1.0 | | V |
| Maximum Continuous Current Output: dc | | ±3 | | | A |
| ac | | 3 | | | Arms |
| Leakage Current, Output Disabled, dc | | | See Typical Curve | | |
| Output Current Limit | | | | | |
| Current Limit Range | | | 0 to ±5 | | A |
| Current Limit Equation | | | $I_{LIM} = (15000)(4.75)/(13750Ω + R_{CL})$ | | A |
| Current Limit Tolerance[1] | $R_{CL}$ = 14.8kΩ ($I_{LIM}$ = ±2.5A), $R_L$ = 8Ω | | ±100 | ±250 | mA |
| Capacitive Load Drive | | | See Typical Curve[4] | | |
| **OUTPUT ENABLE /STATUS (E/S) PIN** | | | | | |
| Shutdown Input Mode | | | | | |
| $V_{E/S}$ High (output enabled) | E/S Pin Open or Forced High | (V–) +2.4 | | | V |
| $V_{E/S}$ Low (output disabled) | E/S Pin Forced Low | | | (V–) +0.8 | V |
| $I_{E/S}$ High (output enabled) | E/S Pin High | | –65 | | µA |
| $I_{E/S}$ Low (output disabled) | E/S Pin Low | | –70 | | µA |
| Output Disable Time | | | 1 | | µs |
| Output Enable Time | | | 3 | | µs |
| Thermal Shutdown Status Output | | | | | |
| Normal Operation | Sourcing 20µA | (V–) +2.4 | (V–) +3.5 | | V |
| Thermally Shutdown | Sinking 5µA, $T_J$ > 160°C | | (V–) +0.35 | (V–) +0.8 | V |
| Junction Temperature, Shutdown | | | +160 | | °C |
| Reset from Shutdown | | | +140 | | °C |
| **POWER SUPPLY** | | | | | |
| Specified Voltage | | | ±30 | | V |
| Operating Voltage Range | | ±4 | | ±30 | V |
| Quiescent Current | $I_{LIM}$ Connected to V–, $I_O$ = 0 | | ±17 | ±20 | mA |
| Quiescent Current, Shutdown Mode | $I_{LIM}$ Connected to V–, $I_O$ = 0 | | ±6 | | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specified Range | | –40 | | +85 | °C |
| Operating Range | | –40 | | +125 | °C |
| Storage Range | | –55 | | +125 | °C |
| Thermal Resistance, $\theta_{JC}$ | | | | | |
| 7-Lead DDPAK, 7-Lead TO-220 | f > 50Hz | | 2 | | °C/W |
| 7-Lead DDPAK, 7-Lead TO-220 | dc | | 2.5 | | °C/W |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| 7-Lead DDPAK, 7-Lead TO-220 | No Heat Sink | | 65 | | °C/W |

NOTES: (1) High-speed test at $T_J$ = +25°C. (2) Positive conventional current flows into the input terminals. (3) See "Total Harmonic Distortion+Noise vs Frequency" in the Typical Performance Curves section for additional power levels. (4) See "Small-Signal Overshoot vs Load Capacitance" in the Typical Performance Curves section.

## CONNECTION DIAGRAMS

Top Front View




NOTE: Tabs are electrically connected to V– supply.

## ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|---|
| Output Current | See SOA Curve |
| Supply Voltage, V+ to V– | 60V |
| Input Voltage | (V–)–0.5V to (V+)+0.5V |
| Input Shutdown Voltage | V+ |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering 10s)(2) | 300°C |

NOTE: (1) Stresses above these ratings may cause permanent damage. (2) Vapor-phase or IR reflow techniques are recommended for soldering the OPA548F surface mount package. Wave soldering is not recommended due to excessive thermal shock and "shadowing" of nearby devices.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| OPA548T | 7-Lead Stagger-Formed TO-220 | 327 | –40°C to +85°C |
| OPA548F(2) | 7-Lead DDPAK Surface-Mount | 328 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Available on Tape and Reel.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



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# OPA2541

www.burr-brown.com/databook/OPA2541.html

# Dual High Power OPERATIONAL AMPLIFIER

## FEATURES

- OUTPUT CURRENTS TO 5A
- POWER SUPPLIES TO ±40V
- FET INPUT
- ELECTRICALLY ISOLATED CASE

## APPLICATIONS

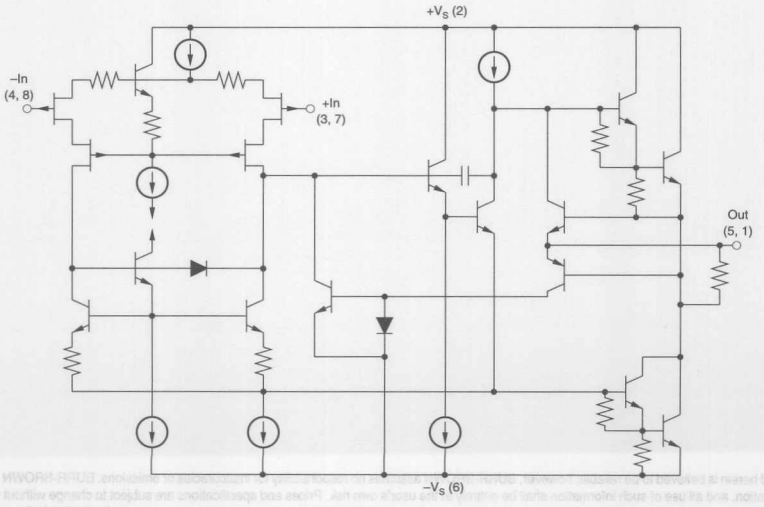
- MOTOR DRIVER
- SERVO AMPLIFIER
- SYNCRO/RESOLVER EXCITATION
- VOICE COIL DRIVER
- BRIDGE AMPLIFIER
- PROGRAMMABLE POWER SUPPLY
- AUDIO AMPLIFIER

## DESCRIPTION

The OPA2541 is a dual power operational amplifier capable of operation from power supplies up to ±40V and output currents of 5A continuous. With two monolithic power amplifiers in a single package it provides unequaled functional density.

The industry-standard 8-pin TO-3 package is isolated from all internal circuitry allowing it to be mounted directly to a heat sink without insulators which degrade thermal performance. Internal circuitry limits output current to approximately 6A.

The OPA2541 is available in both industrial and military temperature range versions.




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# SPECIFICATIONS

## ELECTRICAL

At $T_C$ = +25°C and $V_S$ = ±35VDC, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA2541AM MIN | OPA2541AM TYP | OPA2541AM MAX | OPA2541BM, SM MIN | OPA2541BM, SM TYP | OPA2541BM, SM MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **INPUT OFFSET VOLTAGE** | | | | | | | | |
| $V_{OS}$ | | | ±2 | ±10 | | ±0.25 | ±1 | mV |
| vs Temperature | Specified Temperature Range | | ±20 | ±40 | | ±15 | ±30 | µV/°C |
| vs Supply Voltage | $V_S$ = ±10V to $±V_{MAX}$ | | ±2.5 | ±10 | | * | * | µV/V |
| vs Power | | | ±20 | ±60 | | * | * | µV/W |
| **INPUT BIAS CURRENT** | | | | | | | | |
| $I_B$ | | | 15 | 50 | | * | * | pA |
| | Specified Temperature Range | | Note 1 | | | * | | |
| **INPUT OFFSET CURRENT** | | | | | | | | |
| $I_{OS}$ | | | ±5 | ±30 | | * | * | pA |
| | Specified Temperature Range | | Note 1 | | | * | | |
| **INPUT CHARACTERISTICS** | | | | | | | | |
| Common-Mode Voltage Range | Specified Temperature Range | ±($\|V_S\|$ –6) | ±($\|V_S\|$ –3) | | * | * | | V |
| Common-Mode Rejection | $V_{CM}$ = (±$\|V_S\|$ –6V) | 95 | 106 | | * | * | | dB |
| Input Capacitance | | | 5 | | | * | | pF |
| Input Impedance, DC | | | 1 | | | * | | $10^{12}Ω$ |
| **GAIN CHARACTERISTICS** | | | | | | | | |
| Open Loop Gain at 10Hz | $R_L$ = 6Ω | 90 | 96 | | * | * | | dB |
| Gain-Bandwidth Product | | | 1.6 | | | * | | MHz |
| **OUTPUT** | | | | | | | | |
| Voltage Swing | $I_O$ = 5A | ±($\|V_S\|$ –5.5) | ±($\|V_S\|$ –4.5) | | * | * | | V |
| | $I_O$ = 2A | ±($\|V_S\|$ –4.5) | ±($\|V_S\|$ –3.6) | | * | * | | V |
| | $I_O$ = 0.5A | ±($\|V_S\|$ –4) | ±($\|V_S\|$ –3.2) | | * | * | | V |
| Current, Continuous | +25°C | 5 | 7.0 | | * | * | | A |
| | +85°C | 4 | 5.0 | | * | | | A |
| | +125°C (SM grade only) | | | | 3 | 3.5 | | A |
| **AC PERFORMANCE** | | | | | | | | |
| Slew Rate | | 6 | 8 | | * | * | | V/µs |
| Power Bandwidth | $R_L$ = 8Ω, $V_O$ = 20Vrms | 45 | 55 | | * | * | | kHz |
| Settling Time to 0.1% | 2V Step | | 2 | | | * | | µs |
| Capacitive Load | Specified Temperature Range, G = 1 | | | 3.3 | | | * | nF |
| | Specified Temperature Range, G >10 | | | SOA | | | * | |
| Phase Margin | Specified Temperature Range, $R_L$ = 8Ω | | 40 | | | * | | Degrees |
| Channel Separation | 1kHz, $R_L$ = 6Ω | | 80 | | | * | | dB |
| **POWER SUPPLY** | | | | | | | | |
| Power Supply Voltage, $±V_S$ | Specified Temperature Range | ±10 | ±30 | ±35 | * | ±35 | ±40 | V |
| Current, Quiescent | Total—Both Amplifiers | | 40 | 50 | | * | * | mA |
| **THERMAL RESISTANCE** | | | | | | | | |
| $θ_{JC}$, (Junction-to-Case) | Both Amplifiers(2), AC Output f > 60Hz | | 0.8 | 1.0 | | * | * | °C/W |
| $θ_{JC}$ | Both Amplifiers(2), DC Output | | 0.9 | 1.2 | | * | * | °C/W |
| $θ_{JC}$ | One Amplifier, AC Output f > 60Hz | | 1.25 | 1.5 | | * | * | °C/W |
| $θ_{JC}$ | One Amplifier, DC Output | | 1.4 | 1.9 | | * | * | °C/W |
| $θ_{JA}$, (Junction-to-Ambient) | No Heat Sink | | 30 | | | * | | °C/W |
| **TEMPERATURE RANGE** | | | | | | | | |
| Case | AM, BM | –25 | | +85 | * | | * | °C |
| | SM | | | | –55 | | +125 | °C |

*Specification same as OPA2541AM.

NOTES: (1) Input bias and offset current approximately doubles for every 10°C increase in temperature. (2) Assumes equal dissipation in both amplifiers.

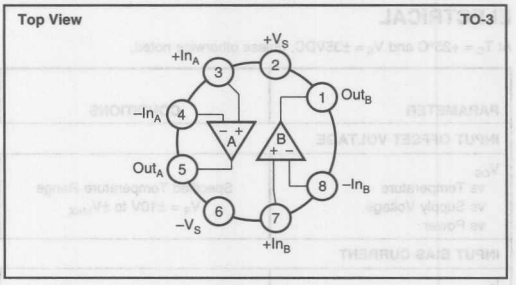
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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, $+V_S$ to $-V_S$ | 80V |
| Output Current | see SOA |
| Power Dissipation, Internal[1] | 125W |
| Input Voltage: Differential | $\pm V_S$ |
| Common-mode | $\pm V_S$ |
| Temperature: Pin Solder, 10s | +300°C |
| Junction[1] | +150°C |
| Temperature Range: | |
| Storage | –65°C to +150°C |
| Operating (Case) | –55°C to +125°C |

NOTE: (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

## CONNECTION DIAGRAM




## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| OPA2541AM | TO-3 | 030 | –25°C to +85°C |
| OPA2541BM | TO-3 | 030 | –25°C to +85°C |
| OPA2541SM | TO-3 | 030 | –55°C to +125°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

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# OPA2544

www.burr-brown.com/databook/OPA2544.html



# High-Voltage, High-Current DUAL OPERATIONAL AMPLIFIER

## FEATURES

- HIGH OUTPUT CURRENT: 2A min
- WIDE POWER SUPPLY RANGE: ±10V to ±35V
- SLEW RATE: 8V/µs
- INTERNAL CURRENT LIMIT
- THERMAL SHUTDOWN PROTECTION
- FET INPUT: $I_B$ = 50pA max
- 11-LEAD PLASTIC PACKAGE

## APPLICATIONS

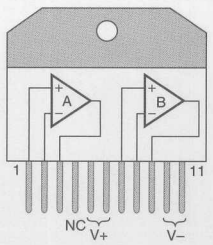
- MOTOR DRIVER
- PROGRAMMABLE POWER SUPPLY
- SERVO AMPLIFIER
- VALVES, ACTUATOR DRIVER
- MAGNETIC DEFLECTION COIL DRIVER
- AUDIO AMPLIFIER

## DESCRIPTION

The OPA2544 is a dual high-voltage/high-current operational amplifier suitable for driving a wide variety of high power loads. It provides 2A output current and power supply voltage range extends to ±35V.

The OPA2544 integrates two high performance FET op amps with high power output stages on a single monolithic chip. Internal current limit and thermal shutdown protect the amplifier and load from damage.

The OPA2544 is available in a 11-lead plastic packages and is specified for the –40°C to +85°C temperature range.




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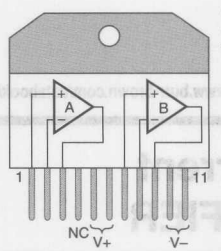
At $T_{CASE}$ = +25°C and $V_S$ = ±35V, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA2544T MIN | OPA2544T TYP | OPA2544T MAX | UNITS |
|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | | | ±1 | ±5 | mV |
| vs Temperature | Specified Temp. Range | | ±10 | | µV/°C |
| vs Power Supply | $V_S$ = ±10V to ±35V | | ±10 | ±100 | µV/V |
| **INPUT BIAS CURRENT**[1] | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | ±15 | ±50 | pA |
| vs Temperature | | | Doubles every 10°C | | |
| Input Offset Current | $V_{CM}$ = 0V | | ±10 | ±50 | pA |
| **NOISE** | | | | | |
| Input Voltage Noise | | | | | |
| Noise Density, f = 1kHz | | | 36 | | nV/√Hz |
| Current Noise Density, f = 1kHz | | | 3 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range | | | | | |
| Positive | Linear Operation | (V+) –6 | (V+) –4 | | V |
| Negative | Linear Operation | (V–) +6 | (V–) +4 | | V |
| Common-Mode Rejection | $V_{CM}$ = ±$V_S$ – 6V | 90 | 106 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $10^{12}$ ‖ 8 | | Ω ‖ pF |
| Common-Mode | | | $10^{12}$ ‖ 10 | | Ω ‖ pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±30V, $R_L$ = 15Ω | 90 | 103 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product | $R_L$ = 15Ω | | 1.4 | | MHz |
| Slew Rate | 60Vp-p, $R_L$ = 15Ω | 5 | 8 | | V/µs |
| Full-Power Bandwidth | | | See Typical Curve | | |
| Settling Time 0.1% | G = –10, 60V Step | | 25 | | µs |
| Total Harmonic Distortion | | | See Typical Curve | | |
| **OUTPUT** | | | | | |
| Voltage Output: Positive | $I_O$ = 2A | (V+) –5 | (V+) –4.4 | | V |
| Negative | $I_O$ = 2A | (V–) +5 | (V–) +3.8 | | V |
| Positive | $I_O$ = 0.5A | (V+) –4.2 | (V+) –3.8 | | V |
| Negative | $I_O$ = 0.5A | (V–) +4 | (V–) +3.1 | | V |
| Current Output | | | See SOA Curves | | |
| Short-Circuit Current | | | ±4 | | A |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±35 | | V |
| Operating Voltage Range | | ±10 | | ±35 | V |
| Quiescent Current (total) | $I_O$ = 0 | | ±22 | ±30 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Operating Range | | –40 | | +85 | °C |
| Storage | | –40 | | +125 | °C |
| Thermal Resistance, $\theta_{JC}$[2] | Both Amplifiers, f > 50Hz | | 2 | | °C/W |
| Thermal Resistance, $\theta_{JC}$[2] | Both Amplifiers, DC | | 2.5 | | °C/W |
| Thermal Resistance, $\theta_{JC}$[2] | One Amplifier, f > 50Hz | | 2.7 | | °C/W |
| Thermal Resistance, $\theta_{JC}$[2] | One Amplifier, DC | | 3 | | °C/W |
| Thermal Resistance, $\theta_{JA}$[2] | No Heat Sink | | 30 | | °C/W |

NOTES: (1) High-speed test at $T_J$ = +25°C. (2) Calculated from total power dissipation of both amplifiers.

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**Front View** **11-Lead Plastic**




| | |
|---|---|
| Supply Voltage, V+ to V– | 70V |
| Output Current | See SOA Curve |
| Input Voltage | (V–) –0.7V to (V+) +0.7V |
| Operating Temperature | –55°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering, –10s) | 300°C |

NOTE: (1) Stresses above these ratings may cause permanent damage.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| OPA2544T | 11-Lead Plastic | 242 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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**3583**

www.burr-brown.com/databook/3583.html

# High Voltage, High Current OPERATIONAL AMPLIFIER

## FEATURES

- WIDE POWER SUPPLY VOLTAGE: ±70V to ±150V
- OUTPUT CURRENT TO 75mA
- SLEW RATE: 30V/µs
- FET INPUT: $I_B$ = 20pA max
- THERMAL SHUT-DOWN PROTECTION
- HERMETIC TO-3 PACKAGE, ISOLATED CASE

## APPLICATIONS

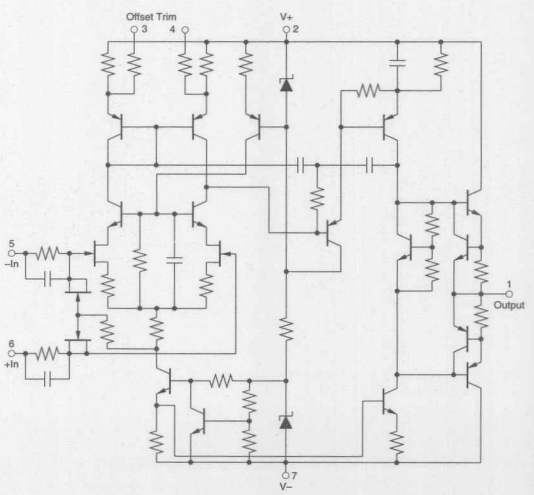
- PROGRAMMABLE POWER SUPPLY
- PIEZO-ELECTRIC TRANSDUCER DRIVER
- HIGH VOLTAGE CURRENT SOURCE

## DESCRIPTION

The 3583 is a high voltage, high speed hybrid operational amplifier designed for a wide variety of programmable power supply and transducer driver applications.

The 3583 operates over a wide power supply range (±50V to ±150V) and provides outputs up to 75mA. Laser-trimmed FET input circuitry provides low offset voltage (3mV max) and low input bias current (20pA max). Thermal shut-down circuitry protects internal circuitry from excessive power dissipation.

Commercial and industrial temperature range models are available. The 3583's hermetic 8-pin TO-3 package is electrically isolated from all internal circuitry.




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# SPECIFICATIONS

At $T_{CASE}$ = +25°C, $V_S$ = ±150V, unless otherwise noted.

| PARAMETER | CONDITIONS | 3583AM MIN | 3583AM TYP | 3583AM MAX | 3583JM MIN | 3583JM TYP | 3583JM MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | | | | ±3 | | | * | mV |
| vs Temperature | Specified Temp. Range | | | ±23 | | | * | µV/°C |
| vs Power Supply | | | 20 | | | * | | µV/V |
| vs Time | | | 50 | | | * | | µV/month |
| **INPUT BIAS CURRENT**[1] | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | | –20 | | | * | pA |
| vs Temperature | | | Doubles Every 10°C | | | * | | |
| vs Power Supply | | | 0.2 | | | * | | pA/V |
| Input Offset Current | $V_{CM}$ = 0V | | | ±20 | | | * | pA |
| vs Temperature | | | Doubles Every 10°C | | | * | | |
| vs Power Supply | | | 0.2 | | | * | | pA/V |
| **NOISE** | | | | | | | | |
| Voltage, 0.01Hz to 10Hz | | | 5 | | | * | | µVp-p |
| 10Hz to 1kHz | | | 1.7 | | | * | | µVrms |
| Current, 0.01Hz to 10Hz | | | 0.3 | | | * | | pAp-p |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Max Safe Differential Input | | | (V+) + \|V–\| | | | * | | |
| Max Safe Common-Mode Input | | | V– to V+ | | | * | | |
| Common-Mode Input Range | Linear Operation | | $V_S$ –10 | | | * | | V |
| Common-Mode Rejection | | | 110 | | | * | | dB |
| **INPUT IMPEDANCE** | | | | | | | | |
| Differential | | | $10^{11}$ \|\| 10 | | | * | | Ω \|\| pF |
| Common-Mode | | | $10^{11}$ | | | * | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | | | | |
| Open-Loop Voltage Gain | No Load, DC | | 118 | | | * | | dB |
| Open-Loop Voltage Gain | Rated Load, DC | 94 | 105 | | * | * | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Unity-Gain Bandwidth | Small-Signal | | 5 | | | * | | MHz |
| Full-Power Bandwidth | $R_L$ = 10kΩ | | 60 | | | * | | kHz |
| Slew Rate | | | 30 | | | * | | V/µs |
| Settling Time: 0.1% | | | 12 | | | * | | µs |
| **OUTPUT** | | | | | | | | |
| Voltage Output | | $V_S$ –10 | | | * | | | V |
| Current Output | | ±75 | | | * | | | mA |
| Short Circuit Current | | | ±100 | | | * | | mA |
| Load Capacitance | | | | 10 | | | * | nF |
| **POWER SUPPLY** | | | | | | | | |
| Operating Voltage Range | | ±50 | | ±150 | * | | * | V |
| Quiescent Current | $I_O$ = 0 | | | ±8.5 | | | * | mA |
| **TEMPERATURE RANGE (CASE)** | | | | | | | | |
| Specification | | –25 | | +85 | 0 | | +70 | °C |
| Operating | | –55 | | +125 | * | | * | °C |
| Storage $\theta_{JC}$ = 4°C/W | | –55 | | +125 | * | | * | °C |

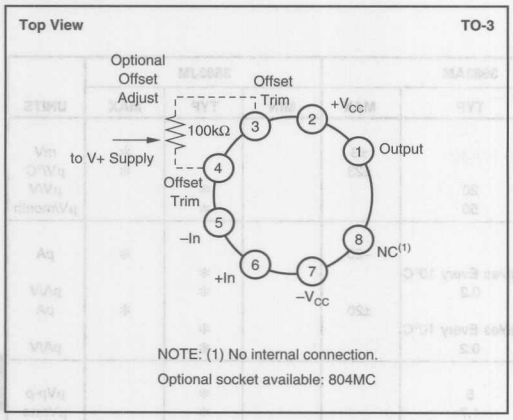
* Specification same as 3583AM.

NOTE: (1) Inputs may be damaged by input slew rates exceeding 1000V/µs. Inputs can be protected from signals exceeding 1000V/µs by limiting input current to 150mA with external series resistors (pins 5 and 6).



The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## CONNECTION DIAGRAM




## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| 3583AM | 8-Pin TO 3 | 030 | –25°C to +85°C |
| 3583JM | 8-Pin TO 3 | 030 | 0°C to +70°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®



**3584**

www.burr-brown.com/databook/3584.html

# High Voltage, High Speed OPERATIONAL AMPLIFIER



## FEATURES

- WIDE POWER SUPPLY VOLTAGE: ±70V to ±150V
- GAIN-BANDWIDTH PRODUCT: 50MHz
- SLEW RATE: 150V/μs
- FET INPUT: $I_B$ = 20pA max
- THERMAL SHUT-DOWN PROTECTION
- HERMETIC TO-3 PACKAGE, ISOLATED CASE

## APPLICATIONS

- PROGRAMABLE POWER SUPPLY
- PIEZO-ELECTRIC TRANSDUCER DRIVER
- ELECTROSTATIC TRANSDUCER DRIVER
- CRT DEFLECTION

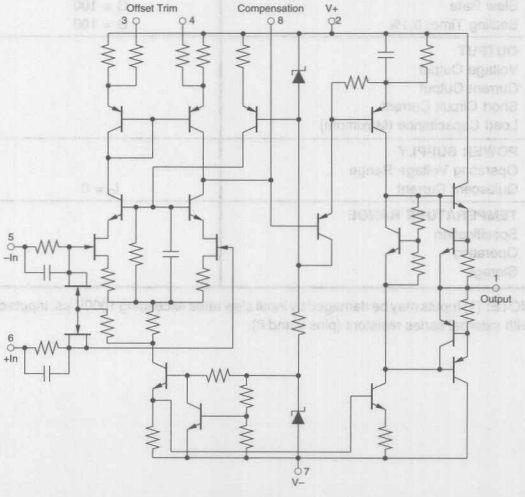
## DESCRIPTION

The 3584 is a high voltage, high speed hybrid operational amplifier designed for a wide variety of programmable power supply and transducer driver applications.

The 3584 operates over a wide power supply range (±70V to ±150V) and provides outputs up to 15mA. Laser-trimmed FET input circuitry provides low offset voltage (3mV max) and low input bias current (20pA max). Thermal shut-down circuitry protects internal circuitry from excessive power dissipation.

The 3584 provides a gain-bandwidth product of 20MHz min (50MHz typical). External frequency compensation (series R/C) allows the user to optimize the bandwidth and slew rate for a particular application.

Specified temperature range is 0°C to +70°C. The 3584's hermetic 8-pin TO-3 package is electrically isolated from all internal circuitry.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_{CASE}$ = +25°C, $V_S$ = ±150V, unless otherwise noted.

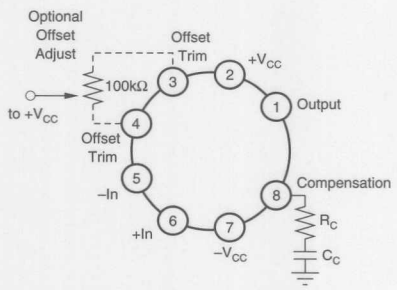
| PARAMETER | CONDITIONS | 3584JM MIN | 3584JM TYP | 3584JM MAX | UNITS |
|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | | | | ±3 | mV |
| vs Temperature | Specified Temperature Range | | | ±25 | µV/°C |
| vs Power Supply | | | 20 | | µV/V |
| vs Time | | | 50 | | µV/month |
| **INPUT BIAS CURRENT**(1) | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | | –20 | pA |
| vs Temperature | | | Doubles Every 10°C | | |
| vs Power Supply | | | 0.2 | | pA/V |
| Input Offset Current | $V_{CM}$ = 0V | | | ±20 | pA |
| vs Temperature | | | Doubles Every 10°C | | |
| vs Power Supply | | | 0.2 | | pA/V |
| **NOISE** | | | | | |
| Voltage, 0.01Hz to 10Hz | | | 5 | | µVp-p |
| 10Hz to 1kHz | | | 1.7 | | µVrms |
| Current, 0.01Hz to 10Hz | | | 0.3 | | pAp-p |
| **INPUT VOLTAGE RANGE** | | | | | |
| Maximum Safe Differential Input | | | (V+) + \|V–\| | | |
| Maximum Safe Common-Mode Input | | | V– to V+ | | |
| Common-Mode Input Range | Linear Operation | | $V_S$ – 10 | | V |
| Common-Mode Rejection | | | 110 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $10^{11}$\|\|10 | | Ω \|\| pF |
| Common-Mode | | | $10^{11}$ | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | No Load, DC | | 120 | | dB |
| Open-Loop Voltage Gain | Rated Load, DC | 100 | | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Unity-Gain Bandwidth | Small-Signal | | 7 | | MHz |
| Gain-Bandwidth Product | f = 1kHz, G = 100 | 20 | | | MHz |
| Full-Power Bandwidth | G = 100 | | 135 | | kHz |
| Slew Rate | G = 100 | | 150 | | V/µs |
| Settling Time: 0.1% | G = 100 | | 12 | | µs |
| **OUTPUT** | | | | | |
| Voltage Output | | $V_S$ - 5 | | | V |
| Current Output | | ±15 | | | mA |
| Short Circuit Current | | | ±25 | | mA |
| Load Capacitance (Maximum) | | | 10 | | nF |
| **POWER SUPPLY** | | | | | |
| Operating Voltage Range | | ±70 | | ±150 | V |
| Quiescent Current | $I_O$ = 0 | | | ±6.5 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | 0 | | +70 | °C |
| Operating | | –55 | | +125 | °C |
| Storage | | –55 | | +150 | °C |

NOTE: (1) Inputs may be damaged by input slew rates exceeding 1000V/µs. Inputs can be protected from signals exceeding 1000V/µs by limiting input current to 150mA with external series resistors (pins 5 and 6).

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## CONNECTION DIAGRAM

Top View




Optional Socket: Burr-Brown Model 0804MC

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| 3584JM | 8-Pin TO-3 | 030 | 0°C to +70°C |

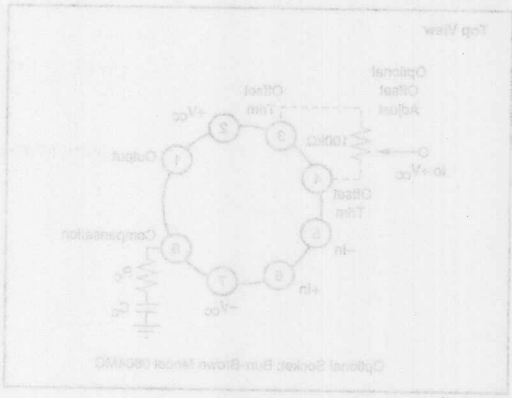
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## CONNECTION DIAGRAM




Optional Socket Burr-Brown Model 08DIP/C

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| 3629/1JM | 8-Pin TO-3 | 029 | 0°C to +70°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# 4 Instrumentation Amplifiers

Instrumentation amplifiers (IAs) are much more than just precise op amps. They are closed loop amplifiers with built-in precision feedback components. Knowledgeable designers use IAs to extract low-level signals from system errors and noise.

Instrumentation amplifiers can amplify signals in the presence of large common-mode signals. They are ideal for use with all sensor types such as strain gages, load cells, thermocouples, RTDs, current shunts, chemical sensors, and physiological probes. They also make excellent universal input amplifiers for data acquisition systems.

Programmable gain amplifiers are ideal for systems that must connect to a variety of sources with varying signal levels. Products include programmable-gain IAs and op amps.

Choose from the industry's widest selection, including:

**INA105, INA106, INA132**—Simple G=1 and G=10 difference amplifiers... incredibly versatile circuit elements.

**INA114, INA118**—The industry's most versatile and accurate 8-pin IAs. INA118 features low-power operation.

**INA111**—High-speed, FET-input IAs using a current-feedback architecture.

**INA116**—Electrometer IA with ultra-low 3fA input bias current. Its 3-op amp design provides an ultra-high impedance differential input, and allows gain setting from 1 to 1000 by connecting a single external resistor.

**INA103**—Ultra-low 1nV/$\sqrt{\text{Hz}}$ noise makes this IA ideal for microphones, bridges or other low impedance sources.

**INA117**—A difference amplifier with ±200V common-mode voltage range.

**INA122**—A micropower instrumentation amplifier for accurate, low noise differential signal acquisition. Its two-op-amp design provides excellent performance with very low (60µA) quiescent current, and is ideal for portable instrumentation and data acquisition systems.

**INA125**—A low power, high accuracy instrumentation amplifier with a precision voltage reference. It provides complete bridge excitation and precision differential-input amplification on a single integrated circuit.

**INA126, INA2126**—The INA126 and INA2126 (dual) are precision instrumentation amplifiers for accurate, low noise differential signal acquisition. Their two-op-amp design provides excellent performance with very low quiescent current (175µA/chan.). This, combined with wide operating voltage range of ±1.35V to ±18V, makes them ideal for portable instrumentation and data acquisition systems.

**INA128, INA141**—Low power, general purpose IAs offering excellent accuracy and wide bandwidth, even at high gain (200kHz at G=100). INA128 gain can be set from 1 to 10,000 using a single external resistor. INA141, a fixed-gain version, uses simple pin connections to set an accurate gain of 10 or 100V/V without external resistors.

**INA134, INA2134, INA137, INA2137**—A family of audio balanced line receivers for professional audio equipment. These G = 1 and G = 0.5 or G = 2 difference amps provide excellent sound quality. Industry-first dual versions save space and lower cost.

**INA2128, INA2141**—Industry's first dual instrumentation amplifiers—two complete IAs on a single monolithic chip. Both provide excellent accuracy and wide bandwidth at high gain (200kHz at G=100).

**PGA204, PGA205**—Programmable gain IAs great for data acquisition systems that connect to a variety of sources or needing exceptional dynamic range.

**PGA206, PGA207**—These are complete 3-op amp IAs with digitally selected gains. PGA206 provides gains of 1, 2, 4 and 8V/V, while PGA207 has gains of 1, 2, 5 and 10V/V. Fast settling time of 3.5µs to 0.01% (all gains) allows fast polling of many channels.

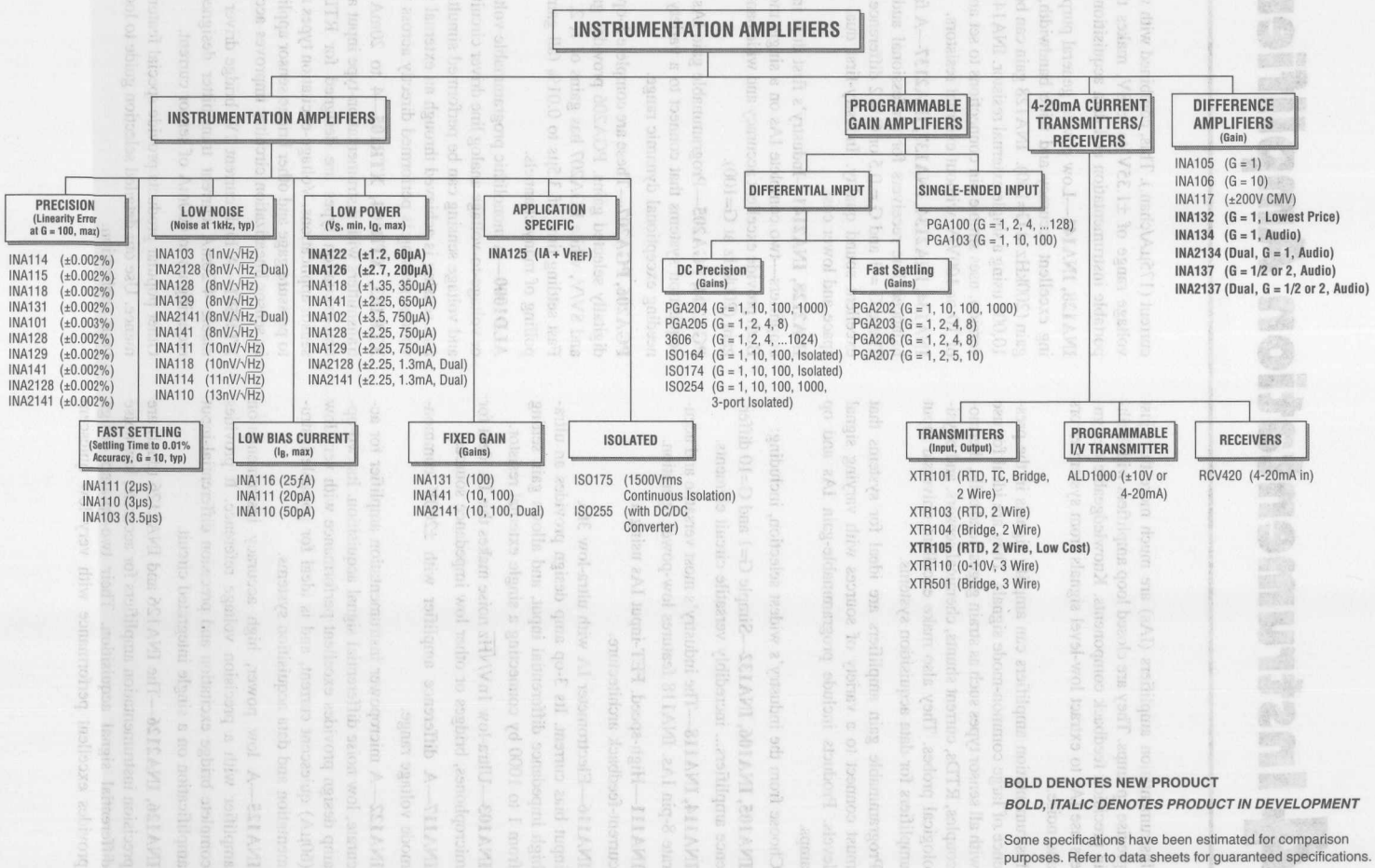
**ALD1000**—A monolithic programmable voltage-to-current or voltage-to-voltage analog line driver circuit. Both current and voltage sensing can be performed simultaneously: current sensing is achieved through an external resistor, while voltage sensing is performed directly across the load.

**XTR103, XTR104, XTR105**—4 to 20mA current loop transmitters with instrumentation-type input amplifier. Current-excitation types are designed for RTD temperature sensor applications. Voltage-excitation types are well-suited to pressure gage and other bridge sensor applications. Built-in sensor linearization circuitry improves accuracy.

**XTR501**—A high current 1W bridge driver and programmable 4-20mA current transmitter designed for sensors requiring up to 600mA of sensor current.

Other popular products provide special features and performance. Use our detailed selection guide to locate the IA for your application.

# Instrumentation Amplifiers




**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

*For Immediate Assistance, Contact Your Local Salesperson*

# INSTRUMENTATION AMPLIFIERS

| Product | Gains Available | Gain Error[2] max (%) | Gain Drift[2] max ±(ppm/°C) | Non Linearity[2] max (%) | CMR[1,2] min (dB) | Offset Voltage Drift max (µV/°C) | Small Signal Bandwidth[2] typ (kHz) | Package | Description |
|---|---|---|---|---|---|---|---|---|---|
| INA101 | 1-1k[3] | 0.1 | 110 | ±0.003 | 106 | ±0.25+10/G | 25 | CDIP, PDIP, SOIC, TO-100 | 25µV Offset, 13nV/√Hz, High CMR |
| INA102 | 1, 10, 100, 1000 | 0.15 | 15 | ±0.020 | 90 | ±0.25+5/G | 3 | CDIP, PDIP, SOIC | Low Power: 7V, 750µA |
| INA103 | 1-1k[3] | 0.25 | 25 | ±0.01 | 100 | ±1+20/G* | 800 | PDIP, SOIC | 1nV/√Hz Noise, 0.0009% THD+N |
| INA110 | 1, 10, 100, 200, 500 | 0.1 | 20 | ±0.010 | 106 | ±0.25+5/G | 450 | CDIP, PDIP, SOIC | FET-Input, 3µs $t_S$, 50pA $I_B$ |
| INA111 | 1-10k[3] | 0.5 | 110 | ±0.005 | 106 | ±5±100/G | 450 | PDIP, SOIC | FET-Input, 4µs $t_S$, 20pA $I_B$, 8-pin DIP |
| INA114 | 1-10k[3] | 0.5 | 110 | ±0.002 | 110 | ±0.25+5/G | 10 | PDIP, SOIC | Accurate, Low cost, 8-pin DIP |
| INA115 | 1-10k[3] | 0.5 | 110 | ±0.002 | 110 | ±0.25+5/G | 10 | SOIC | INA114 with additional pin-outs. |
| INA116 | 1-1000[3] | 0.5 | 110 | ±0.005 | 86 | ±0.25+20/G* | 70 | PDIP, SOIC | Electrometer input (10fA), Guard Drive |
| INA118 | 1-10k[3] | 0.5 | 110 | ±0.002 | 107 | ±0.25+5/G | 100 | PDIP, SOIC | Low Power: ±1.35V, 350µA, 8-pin DIP |
| INA120 | 1, 10, 100, 1000 | 0.2 | 30 | ±0.010 | 106 | ±0.25+10/G | 20 | PDIP | Low Offset and Drift, High CMR |
| **INA122** | **1-10k[3]** | **0.5[2]** | **100[2]** | **0.012[2]** | **86[1, 2]** | **3** | **10[2]** | **PDIP, SO** | **MicroPower, Single Supply, Rail-to-Rail** |
| **INA125** | **1-10k[3]** | **0.5[2]** | **100[2]** | **±0.01[2]** | **100[1, 2]** | **2** | **4.5[2]** | **PDIP, SO** | **MicroPower, IA with on board ref** |
| **INA126** | **1-10k[3]** | **0.5[2]** | **100[2]** | **±0.012[2]** | **83[1, 2]** | **3** | **9[2]** | **PDIP, SO, MSOP** | **MicroPower, Lowest cost, tiny MSOP-8 package** |
| INA128 | 1-10k[3] | 0.5 | 100 | ±0.002 | 120 | ±0.5±20/G | 200 | PDIP, SOIC | Low Power, 700µA, 8-pin DIP, SO-8 |
| INA129 | 1-10k[3] | 0.5 | 100 | ±0.002 | 120 | ±0.5±20/G | 200 | PDIP, SOIC | Low Power, 700µA, 8-pin DIP, SO-8 |
| INA131 | 100 | 0.024 | 10 | ±0.002 | 110 | ±0.25 | 70 | PDIP | G = 100, 8 pin DIP, Ultra Low Gain Error |
| INA141 | 10,100 | 0.075 | 10 | ±0.002 | 117 | ±0.5 | 200 | PDIP, SOIC | Low Power, 600µA |
| INA2128 | 1-10k[3] | 0.5 | 100 | ±0.002 | 120 | ±0.5+20/G | 200 | PDIP, SOIC | Worlds first Dual IA, High Accuracy |
| INA2141 | 10, 100 | 0.075 | 10 | ±0.002 | 117 | ±0.5 | 200 | PDIP, SOIC | Dual IA, 2 Fixed Gains, Low gain error |
| ISO175 | 1-10k[3] | 0.95* | 11[6]* | ±0.04 | — | ±(1+520/G)* | 50 | PDIP | Isolated, Unpowered |
| ISO255 | 1-10k[3] | 0.95 | 50* | ±0.104 | 90 | ±(1+520/G)* | 45 | DIP | Three-port Isolated with DC/DC Converter |

NOTES: (1) DC to 60Hz, balanced source impedance. (2) G = 100. (3) Set with external resistor. (4) G = 50. (5) G = 0.5. (6) G = 1.

* DENOTES TYPICAL

**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

# DIGITALLY PROGRAMMABLE GAIN AMPLIFIERS

| Product | Digitally Selected Gains[2] | Gain Error[2] max (%) | Gain Drift[2] max (ppm/°C) | Non Linearity Error[2] max (%) | CMR[1,2] min (dB) | Offset Voltage Drift ±max (µV/°C) | Small Signal Bandwidth[2] typ (kHz) | Package | Description |
|---|---|---|---|---|---|---|---|---|---|
| ISO164 | *1*, 10, 100 | 0.3 | 12.5* | 0.01 | 90* | 155* | 6 | PDIP | Isolated, Unpowered |
| ISO174 | *1*, 10, 100 | 0.3 | 42.5* | 0.04 | 90* | 505* | 60 | PDIP | Isolated, Unpowered |
| ISO254 | 1, 10, *100*, 1000 | 0.3 | 15* | 0.104 | 90* | (1+510/G)* | 10 | PDIP | Three-port Isolated with DC/DC Converter. |
| PGA100 | 1, 2, 4, ... *128* | 0.02 | 10 | 0.005 | — | 6* | 40 | CDIP | 8 Multiplexed S-E[3] inputs, 8 Binary gains, still available. |
| PGA102 | 1, 10, *100* | 0.025 | 20 | 0.01 | — | 3 | 250 | CDIP, PDIP | 3 S-E[3] inputs, Gain control per channel. |
| PGA103 | 1, 10, *100* | 0.2 | 30* | 0.01 | — | 2* | 250 | PDIP, SOIC | 8-pin, low cost, 1 S-E input, < 3 mA Iq |
| PGA202 | 1, 10, *100*, 1000 | 0.15 | 60 | 0.012 | 92 | 13 | 1000 | CDIP, PDIP | FET IA[3] Input, 3µs $t_S$, constant GBW |
| PGA203 | 1, 2, 4, *8* | 0.25 | 25 | 0.015 | 86 | 9* | 1000 | PDIP | FET IA[3] Input, 3µs $t_S$, constant GBW |
| PGA204 | 1, 10, *100*, 1000 | 0.024 | 10 | 0.002 | 110 | 0.25 | 10 | PDIP, SOIC | IA[3] Input, DC precision, ±40V protection |
| PGA205 | 1, 2, 4, *8* | 0.024 | 10 | 0.002 | 96 | 0.26 | 80 | PDIP, SOIC | IA[3] Input, DC precision, ±40V protection |
| PGA206 | 1, 2, 4, *8* | 0.05 | 10 | 0.002 | 95 | 2* | 600 | PDIP, SOIC | IA[3] Input, Fast: $t_S$ = 3.5µs, SR = 25V/µs |
| PGA207 | 1, 2, 5, *10* | 0.05 | 10 | 0.002 | 95 | 2* | 600 | PDIP, SOIC | IA[3] Input, Fast: $t_S$ = 3.5µs, SR = 25V/µs |
| 3606 | 1, 2, 4, ... *1024* | 0.02 | 10 | 0.01 | 110 | 5 | 10 | CDIP | Precision Hybrid, $2^9$ Binary Gains |

NOTES: (1) DC to 60Hz, balanced source impedance. (2) Listed specifications apply for gain values in italics from "Digitally Selected Gains" column. (3) S-E: Single-Ended input. IA: Instrumentation Amplifier inputs (differential, high impedance).

# 4-20mA TRANSMITTERS/RECEIVERS

| Product | Supply Voltage Range (V) | Span Error (Unadj) max (%) | Non-Linearity max (%) | CMR 60Hz typ (dB) | Offset Voltage Drift max (µV/°C) | Output Zero Error ±max | Full Scale Output Error max | Package | Description |
|---|---|---|---|---|---|---|---|---|---|
| RCV420 | –5/11.4 to ±18 | — | 0.002 | 94 | — | 1.25mV | 2.5mV | CDIP, PDIP | Precision 4-20mA current loop receiver. |
| XTR101 | 11.6 to 40 | 5 | 0.01 | 100 | 0.75 | 6µA | 30µA | CDIP, PDIP, SOIC | 2 Wire transmitter, selectable in/out ranges. |
| XTR103 | 9 to 40 | 1 | 0.01 | 100 | 2.5 | 50µA | 50µA | PDIP, SOIC | 2 Wire, RTD excitation/linearization |
| XTR104 | 9 to 40 | 1 | 0.01 | 100 | 2.5 | 50µA | 50µA | PDIP, SOIC | 2 Wire, Bridge excitation/linearization |
| **XTR105** | **7.5 to 36** | **0.2** | **0.01** | **100** | **1.5** | **25µA** | **—** | **PDIP, SOIC** | **2 Wire, RTD excitation/linearization, $V_{REG}$, lowest cost** |
| XTR110 | 13.5 to 40 | 0.2 | 0.005 | — | — | 16µA | 32µA | CDIP, PDIP, SOIC | 3 Wire transmitter, selectable in/out ranges. |
| XTR501 | 11.4 to 30 | 2.5[1] | 0.025 | 85 | 50* | 100µA | — | DIP | 1W bridge excitation for low Z sensors. |

NOTE: (1) Gain = 1.

* DENOTES TYPICAL

**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

For Immediate Assistance, Contact Your Local Salesperson

## PROGRAMMABLE I/V TRANSMITTERS

| Product | Current Output | Span Error max (5) | Voltage Output | Non Linearity max (%) | Voltage Frequency Response G = 1 (kHz) | Supply Voltage | Package | Description |
|---|---|---|---|---|---|---|---|---|
| ALD1000 | 4-20mA | 1 | ±10V | 0.05 | 100* | $V_S-$ = –15V<br>$V_S+$ = +24V | SOIC | Programmable voltage-to-current or voltage-to-voltage analog driver circuit. |

## DIFFERENCE AMPLIFIERS

| Product | Gain (V/V) | Gain Error max (%) | Gain Drift* max (ppm/°C) | Non Linearity max (%) | CMR(1) DC min (dB) | Offset Voltage Drift max (µV/°C) | Small Signal Bandwidth typ (kHz) | Package | Description |
|---|---|---|---|---|---|---|---|---|---|
| INA105 | 1 | 0.010 | 5 | ±0.001 | 86 | 10 | 1000 | TO-99, DIP, SOIC | High Accuracy, Cost Effective |
| INA106 | 10 | 0.025 | 4* | ±0.001 | 86 | 0.2* | 5000 | DIP, SOIC | High Accuracy, Cost Effective |
| INA117 | 1 | 0.020 | 10 | ±0.001 | 86 | 20 | 200 | TO-99, DIP | ±200VDC Common Mode, ±500VDC ($V_{CM}$ and $V_{DIFF}$) Protected Input |
| **INA132** | **1** | **0.075** | **10** | **±0.001** | **76** | **5** | **300** | **PDIP, SOIC** | **Accurate, Lowest Cost** |
| **INA134** | **1** | **0.1** | **10** | **±0.0001*** | **74** | **2*** | **3100** | **DIP, SO-8** | **Audio Line Receiver** |
| **INA137** | **1/2, 2** | **0.1** | **10** | **±0.0001*** | **74** | **2*** | **4000** | **DIP, SO-8** | **Audio Line Receiver** |
| **INA2134** | **1** | **0.1** | **10** | **±0.0001*** | **74** | **2*** | **3100** | **DIP, SO-14** | **Audio Line Receiver, Dual** |
| **INA2137** | **1/2, 2** | **0.1** | **10** | **±0.0001*** | **74** | **2*** | **4000** | **DIP, SO-14** | **Audio Line Receiver, Dual** |

NOTE: (1) DC to 60Hz, balanced source impedance.

* DENOTES TYPICAL

**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

BURR-BROWN®




# ALD1000

www.burr-brown.com/databook/ALD1000.html

# Precision Programmable CURRENT/VOLTAGE TRANSMITTER

## FEATURES

- SWITCHABLE OUTPUT ±10V OR 4-20mA
- DRIVES 1000Ω || 1µF AT 20mA
- VOLTAGE AND CURRENT SENSE
- GROUND NOISE SUPPRESSION
- ERROR DETECTION FLAG
- OUTPUT DISABLE
- ACCURACY: 0.05% max
- WIDE SUPPLY RANGE: ±11V TO +24/–15V

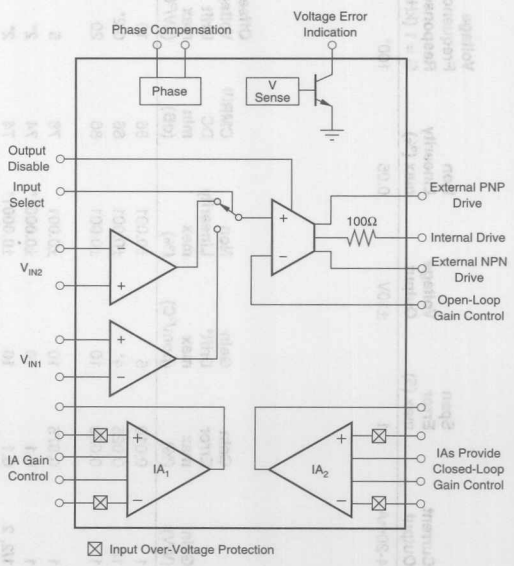
## APPLICATIONS

- PROGRAMMABLE CONTROLLERS
- STANDARDIZED OUTPUTS FOR TERMINATION PANELS
- INDUSTRIAL PROCESS CONTROL
- PROGRAMMABLE CURRENT SOURCE
- MOTOR CONTROL SYSTEMS
- PC AND VME BASED INSTRUMENTATION
- CONDITIONER FOR STANDARD SENSOR OUTPUTS
- TEST EQUIPMENT PIN DRIVER

## DESCRIPTION

This product is a monolithic programmable voltage-to-current or voltage-to-voltage analog line driver circuit. It can convert a ±10V input into either an output voltage or current with remote sensing. It provides drive for external transistors to boost output current to greater than ±25mA levels.

Current and voltage sensing can be performed simultaneously. Current sensing is achieved through a single external sense resistor. Voltage sensing is performed directly across the load. The logic inputs provide for both output disable and switching between constant current or constant voltage output functions. An open collector output provides an error flag for open circuit loads. The output disable function allows full control of the output even during power-on and power-off sequencing. The instrumentation amplifiers are designed to insure that load noise is not circulated within the control loop.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $+V_S$ = 24V, $-V_S$ = 15V, $T_{AMB}$ = 25°C, and 2N2222, 2N2907 external transistors, unless otherwise noted.

| PARAMETER | CONDITIONS | ALD1000U MIN | ALD1000U TYP | ALD1000U MAX | UNITS |
|---|---|---|---|---|---|
| **TRANSMITTER** | | | | | |
| **SWOP INPUTS** | | | | | |
| Linear Range Min | Internal Drive Transistors | | | –10 | V |
| Linear Range Max | 5mA Load | 10 | | | V |
| Input Bias Current | | | 50 | | pA |
| **XTR OUTPUT** | | | | | |
| Positive Overvoltage Sense | | | 19.5 | | V |
| Negative Overvoltage Sense | Internal Drive Transistors | | –10.5 | | V |
| Positive Overcurrent Sense | | | +25 | | mA |
| Negative Overcurrent Sense | | | –15 | | mA |
| **LOGIC INPUTS** | | | | | |
| Logic Low | | | | 0.8 | V |
| Logic High | | 4.0 | 2.6 | | V |
| **LOGIC OUTPUTS** | | | | | |
| Logic High | 5V Logic Supply | 4.0 | | | V |
| Logic Low | with 10k pull-up resistor | | | 0.8 | V |
| **OUTPUT—VOLTAGE MODE** (Gain = 1 unless otherwise specified) | | | | | |
| Span Error | | | 0.5 | 1 | % |
| Span Drift | | | 50 | | ppm/°C of FS |
| Linear Range Min | 0.1% of FS | | | –10 | |
| Linear Range Max | 0.1% of FS | 10 | | | |
| Output Current Min | Internal Drive Transistors | | | –5 | mA |
| Output Current Max | Internal Drive Transistors | 5 | | | mA |
| Short-Circuit Current | Internal Drive Transistors | | 25 | | mA |
| Short-Circuit Current | Internal Drive Transistors | | –15 | | mA |
| Non-Linearity | | | 0.005 | 0.05 | % |
| Initial Offset Voltage—RTI | | | 2 | | mV |
| Offset Voltage vs Temperature | | | 20 | | µV/°C |
| **OUTPUT—CURRENT MODE** (Gain = 5 with 50Ω shunt resistor unless otherwise specified) | | | | | |
| Span Error | | | 5 | | % |
| Span Drift | Gain = 1[1] | | 50 | | ppm/°C of FS |
| Output Current Min | Internal Drive Transistors[2] | | | –5 | mA |
| Output Current Max | Internal Drive Transistors[2] | 5 | | | mA |
| Compliance Min | | –10 | | | V |
| Compliance Max | | | | 15 | V |
| Offset Current Min | | | | –25 | µA |
| Offset Current Min | | 25 | | | µA |
| **INSTRUMENTATION AMPLIFIERS $R_{LOAD}$ = 10k** | | | | | |
| **IA INPUTS** | | | | | |
| Linear Input Voltage Min | | | | –10 | V |
| Linear Input Voltage Max | | 20 | | | V |
| Common-Mode Input Voltage Min | $V_{IN}$ = 0 | | | –10 | V |
| Common-Mode Input Voltage Max | $V_{IN}$ = 0 | 20 | | | V |
| Input Bias Current | | | 100 | | nA |
| Initial Offset Voltage | G = 1 | –1 | | 1 | mV |
| CMRR | G = 10 | 80 | 100 | | |
| **IA OUTPUTS (with 10k Load)** | | | | | |
| Output Voltage Max | | 20 | | | V |
| Output Voltage Min | | | | –10 | V |
| + Short Circuit Current | | | 5 | | mA |
| – Short Circuit Current | | | –12 | | mA |
| **GAIN EQUATION (gain = 1+50k/$R_G$)** | | | | | |
| Gain Error, G = 1 | | | | 0.3 | %±FS |
| G = 5 | | | | 0.6 | %±FS |
| G = 100 | | | | 0.8 | %±FS |
| Non-Linearity, G = 1 | | | | 0.004 | %±FS |
| G = 5 | | | | 0.008 | %±FS |
| G = 100 | | | | 0.02 | %±FS |

## SPECIFICATIONS (CONT)

At $+V_S$ = 24V, $-V_S$ = 15V, $T_{AMB}$ = 25°C, and 2N2222, 2N2907 external transistors, unless otherwise noted.

| PARAMETER | CONDITIONS | ALD1000U MIN | ALD1000U TYP | ALD1000U MAX | UNITS |
|---|---|---|---|---|---|
| **FREQUENCY RESPONSE** | | | | | |
| G = 1 | | | 700 | | kHz |
| G = 5 | | | 400 | | kHz |
| G = 100 | | | 50 | | kHz |
| Slew Rate | $V_O$ = ±10V, G = 10 | | 4 | | V/µS |
| **SETTLING TIME, 0.01%** | | | | | |
| G = 1 | | | 20 | | µS |
| G = 5 | | | 20 | | µS |
| G = 100 | | | 30 | | µS |
| **POWER SUPPLY** | | | | | |
| Quiescent Current | Internal Drive Transistors | | 5 | | mA |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –40 | | +85 | °C |
| Storage | | –65 | | +150 | °C |

NOTES: (1) Gain drift depends on tempco of 50K factor on gain equation when gain is greater than 1. (2) External Drive capacity varies with configuration. See Application Note.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage (±$V_S$) | +25V, –18V |
| IA Inputs | ±40V |
| SWOP Inputs | ±$V_S$ |
| Logic Inputs | +$V_S$, –$V_S$ + 0.5V |
| Junction Temperature | 150°C |
| Storage Temperature | –65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short-to-Ground at 25°C | Continuous |

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ALD1000U | 28-Pin SOIC | 217 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### ELECTROSTATIC DISCHARGE SENSITIVITY

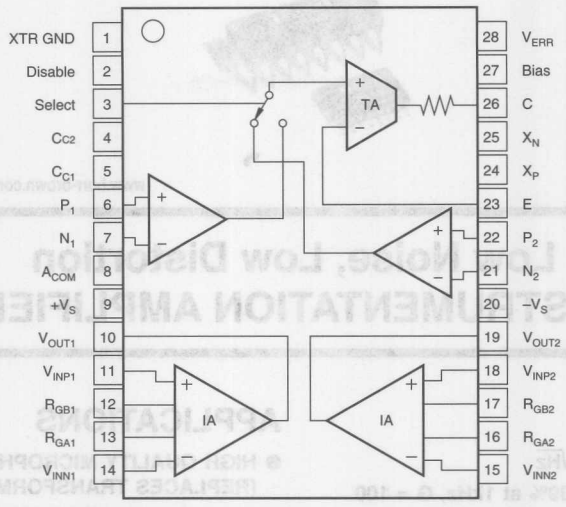
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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## PIN CONFIGURATION

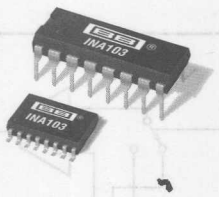
Top View — 28-Lead SOIC




## PIN ASSIGNMENTS

| PIN # | NAME | DESCRIPTION |
|---|---|---|
| 1 | XTR GND | Power ground pin. |
| 2 | Disable | A 5V signal puts the internal drive in a high impedance state and limits the external drive capacity. |
| 3 | Select | Selects the SWOP amp input. A 5V signal selects inputs N1 and P1. |
| 4 | $C_{C2}$ | $C_{C1}$ and $C_{C2}$ are for the external compensation capacitor. |
| 5 | $C_{C1}$ | $C_{C1}$ and $C_{C2}$ are for the external compensation capacitor. |
| 6 | $P_1$ | Non-inverting input to the XTR SWOP amp 1. |
| 7 | $N_1$ | Inverting input to the XTR SWOP amp 1. |
| 8 | $A_{COM}$ | Signal ground for the instrumentation amplifiers. |
| 9 | $+V_S$ | Positive power supply voltage. |
| 10 | $V_{OUT1}$ | Output of the instrumentation amplifier 1. |
| 11 | $V_{INP1}$ | Non-inverting input to instrumentation amplifier 1. |
| 12 | $R_{GB1}$ | Gain set resistor for instrumentation amplifier 1. |
| 13 | $R_{GA1}$ | Gain set resistor for instrumentation amplifier 1. |
| 14 | $V_{INN1}$ | Inverting input of instrumentation amplifier 1. |
| 15 | $V_{INN2}$ | Inverting input of instrumentation amplifier 2. |
| 16 | $R_{GA2}$ | Gain set resistor for instrumentation amplifier 2. |
| 17 | $R_{GB2}$ | Gain set resistor for instrumentation amplifier 2. |
| 18 | $V_{INP2}$ | Non-inverting input to instrumentation amplifier 2. |
| 19 | $V_{OUT2}$ | Output of the instrumentation amplifier 2. |
| 20 | $-V_S$ | Negative power supply voltage. |
| 21 | $N_2$ | Inverting input to the XTR SWOP amp 2. |
| 22 | $P_2$ | Non-inverting input to the XTR SWOP amp 2. |
| 23 | E | Inverting input (emitter) of the output transconductance amplifier. |
| 24 | $X_P$ | Base drive for an external, PNP, driver transistor (optional). |
| 25 | $X_N$ | Base drive for an external, NPN, driver transistor (optional). |
| 26 | C | Output (collector) of the output transconductance amplifier. |
| 27 | Bias | Open collector output indicating an internal overcurrent condition. |
| 28 | $V_{ERR}$ | Open collector output indicating an overvoltage condition. |

BURR-BROWN®



# INA103

www.burr-brown.com/databook/INA103.html

# Low Noise, Low Distortion INSTRUMENTATION AMPLIFIER

## FEATURES

- LOW NOISE: 1nV/√Hz
- LOW THD+N: 0.0009% at 1kHz, G = 100
- HIGH GBW: 100MHz at G = 1000
- WIDE SUPPLY RANGE: ±9V to ±25V
- HIGH CMRR: >100dB
- BUILT-IN GAIN SETTING RESISTORS: G = 1, 100
- UPGRADES AD625

## APPLICATIONS

- HIGH QUALITY MICROPHONE PREAMPS (REPLACES TRANSFORMERS)
- MOVING-COIL PREAMPLIFIERS
- DIFFERENTIAL RECEIVERS
- AMPLIFICATION OF SIGNALS FROM:
  Strain Gages (Weigh Scale Applications)
  Thermocouples
  Bridge Transducers

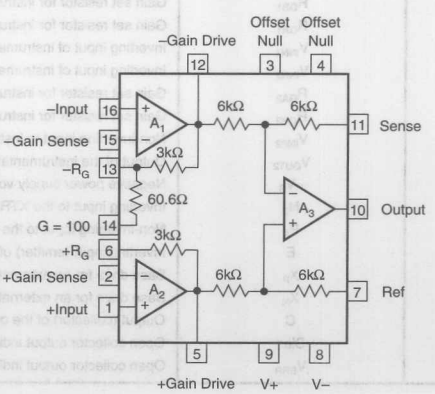
## DESCRIPTION

The INA103 is a very low noise, low distortion monolithic instrumentation amplifier. Its current-feedback circuitry achieves very wide bandwidth and excellent dynamic response. It is ideal for low-level audio signals such as balanced low-impedance microphones. The INA103 provides near-theoretical limit noise performance for 200Ω source impedances. Many industrial applications also benefit from its low noise and wide bandwidth.

Unique distortion cancellation circuitry reduces distortion to extremely low levels, even in high gain. Its balanced input, low noise and low distortion provide superior performance compared to transformer-coupled microphone amplifiers used in professional audio equipment.

The INA103's wide supply voltage (±9 to ±25V) and high output current drive allow its use in high-level audio stages as well. A copper lead frame in the plastic DIP assures excellent thermal performance.

The INA103 is available in 16-pin plastic DIP and SOL-16 surface-mount packages. Commercial and Industrial temperature range models are available.




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# SPECIFICATIONS

All specifications at $T_A$ = +25°C, $V_S$ = ±15V and $R_L$ = 2kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | INA103KP, KU MIN | INA103KP, KU TYP | INA103KP, KU MAX | UNITS |
|---|---|---|---|---|---|
| **GAIN** | | | | | |
| Range of Gain | | 1 | | 1000 | V/V |
| Gain Equation (1) | | | G = 1 + 6kΩ/$R_G$ | | V/V |
| Gain Error, DC G = 1 | ±10V Output | | 0.005 | 0.05 | % |
| G = 100 | | | 0.07 | 0.25 | % |
| Equation | | | 0.05 | | % |
| Gain Temp. Co. G = 1 | ±10V Output | | 10 | | ppm/°C |
| G = 100 | | | 25 | | ppm/°C |
| Equation | | | 25 | | ppm/°C |
| Nonlinearity, DC G = 1 | ±10V Output | | 0.0003 | 0.01 | % of FS(2) |
| G = 100 | | | 0.0006 | 0.01 | % of FS |
| **OUTPUT** | | | | | |
| Voltage, $R_L$ = 600Ω | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | ±11.5 | ±12 | | V |
| $R_L$ = 600Ω | $V_S$ = ±25, $T_A$ = 25°C | ±20 | ±21 | | V |
| Current | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | ±40 | | | mA |
| Short Circuit Current | | | ±70 | | mA |
| Capacitive Load Stability | | | 10 | | nF |
| **INPUT OFFSET VOLTAGE** | | | | | |
| Initial Offset RTI(3) | | | (30 + 1200/G) | | µV |
| (KU Grade) | | | | (250+ 5000/G) | µV |
| vs Temp G = 1 to 1000 | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | 1 + 20/G | | µV/°C |
| G = 1000 | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | | µV/°C |
| vs Supply | ±9V to ±25V | | 0.2 + 8/G | 4 + 60/G | µV/V |
| **INPUT BIAS CURRENT** | | | | | |
| Initial Bias Current | | | 2.5 | 12 | µA |
| vs Temp | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | 15 | | nA/°C |
| Initial Offset Current | | | 0.04 | 1 | µA |
| vs Temp | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | 0.5 | | nA/°C |
| **INPUT IMPEDANCE** | | | | | |
| Differential Mode | | | 60 ‖ 2 | | MΩ ‖ pF |
| Common-Mode | | | 60 ‖ 5 | | MΩ ‖ pF |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Range(4) | | ±11 | ±12 | | V |
| CMR | | | | | |
| G = 1 | DC to 60Hz | 72 | 86 | | dB |
| G = 100 | DC to 60Hz | 100 | 125 | | dB |
| **INPUT NOISE** | | | | | |
| Voltage(5) | $R_S$ = 0Ω | | | | |
| 10Hz | | | 2 | | nV/√Hz |
| 100Hz | | | 1.2 | | nV/√Hz |
| 1kHz | | | 1 | | nV/√Hz |
| Current, 1kHz | | | 2 | | pA/√Hz |
| **OUTPUT NOISE** | | | | | |
| Voltage | 1kHz | | 65 | | nV/√Hz |
| A Weighted, 20Hz-20kHz | 20Hz-20kHz | | –100 | | dBu |
| **DYNAMIC RESPONSE** | | | | | |
| –3dB Bandwidth: G = 1 | Small Signal | | 6 | | MHz |
| G = 100 | Small Signal | | 800 | | kHz |
| Full Power Bandwidth | G = 1 | | | | |
| $V_{OUT}$ = ±10V, $R_L$ = 600Ω | | | 240 | | kHz |
| Slew Rate | G = 1 to 500 | | 15 | | V/µs |
| THD + Noise | G = 100, f = 1kHz | | 0.0009 | | % |
| Settling Time 0.1% | | | | | |
| G = 1 | $V_O$ = 20V Step | | 1.7 | | µs |
| G = 100 | | | 1.5 | | µs |
| Settling Time 0.01% | | | | | |
| G = 1 | $V_O$ = 20V Step | | 2 | | µs |
| G = 100 | | | 3.5 | | µs |
| Overload Recovery(6) | 50% Overdrive | | 1 | | µs |

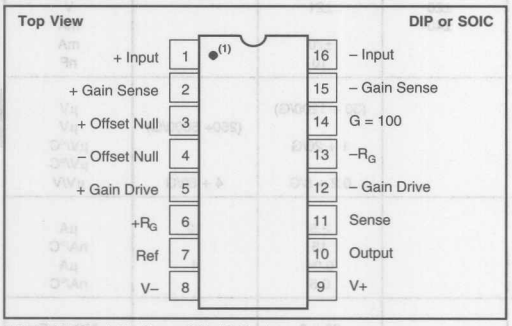
NOTES: (1) Gains other than 1 and 100 can be set by adding an external resistor, $R_G$ between pins 2 and 15. Gain accuracy is a function of $R_G$. (2) FS = Full Scale. (3) Adjustable to zero. (4) $V_O$ = 0V, see Typical Curves for $V_{CM}$ vs $V_O$. (5) $V_{NOISE\ RTI} = \sqrt{V^2_{N\ INPUT} + (V_{N\ OUTPUT}/Gain)^2 + 4KTR_G}$. See Typical Curves. (6) Time required for output to return from saturation to linear operation following the removal of an input overdrive voltage.

## SPECIFICATIONS (CONT)

All specifications at $T_A$ = +25°C, $V_S$ = ±15V and $R_L$ = 2kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | INA103KP, KU MIN | INA103KP, KU TYP | INA103KP, KU MAX | UNITS |
|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | |
| Rated Voltage | | | ±15 | | V |
| Voltage Range | | ±9 | | ±25 | V |
| Quiescent Current | | | 9 | 12.5 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | 0 | | +70 | °C |
| Operation | | –40 | | +85 | °C |
| Storage | | –40 | | +100 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | 100 | | °C/W |

### PIN CONFIGURATION




NOTE: (1) Pin 1 Marking—SOL-16 Package

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| INA103KP | Plastic DIP | 180 | 0°C to +70°C |
| INA103KU | SOL-16 | 211 | 0°C to +70°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

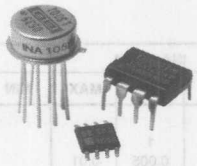
### ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|---|
| Power Supply Voltage | ±25V |
| Input Voltage Range, Continuous | $\pm V_S$ |
| Operating Temperature Range: | –40°C to +85°C |
| Storage Temperature Range: | –40°C to +85°C |
| Junction Temperature: | |
| P, U Package | +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short Circuit to Common | Continuous |

NOTE: (1) Stresses above these ratings may cause permanent damage.

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# INA105

www.burr-brown.com/databook/INA105.html

# Precision Unity Gain DIFFERENTIAL AMPLIFIER

## FEATURES

- CMR 86dB min OVER TEMPERATURE
- GAIN ERROR: 0.01% max
- NONLINEARITY: 0.001% max
- NO EXTERNAL ADJUSTMENTS REQUIRED
- EASY TO USE
- COMPLETE SOLUTION
- HIGHLY VERSATILE
- LOW COST
- PLASTIC DIP, TO-99 HERMETIC METAL, AND SO-8 SOIC PACKAGES

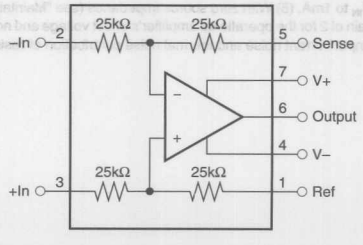
## APPLICATIONS

- DIFFERENTIAL AMPLIFIER
- INSTRUMENTATION AMPLIFIER BUILDING BLOCK
- UNITY-GAIN INVERTING AMPLIFIER
- GAIN-OF-1/2 AMPLIFIER
- NONINVERTING GAIN-OF-2 AMPLIFIER
- AVERAGE VALUE AMPLIFIER
- ABSOLUTE VALUE AMPLIFIER
- SUMMING AMPLIFIER
- SYNCHRONOUS DEMODULATOR
- CURRENT RECEIVER WITH COMPLIANCE TO RAILS
- 4mA TO 20mA TRANSMITTER
- VOLTAGE-CONTROLLED CURRENT SOURCE
- ALL-PASS FILTERS

## DESCRIPTION

The INA105 is a monolithic Gain = 1 differential amplifier consisting of a precision op amp and on-chip metal film resistors. The resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature.

The differential amplifier is the foundation of many commonly used circuits. The INA105 provides this precision circuit function without using an expensive precision resistor network. The INA105 is available in 8-pin plastic DIP, SO-8 surface-mount and TO-99 metal packages.






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# SPECIFICATIONS

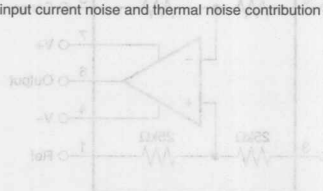
## ELECTRICAL

At +25°C, $V_{CC}$ = ±15V, unless otherwise noted.

| PARAMETER | CONDITIONS | INA105AM | | | INA105BM | | | INA105KP, KU | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **GAIN** | | | | | | | | | | | |
| Initial[1] | | | 1 | | | * | | | * | | V/V |
| Error | | | 0.005 | 0.01 | | * | * | | 0.01 | 0.025 | % |
| vs Temperature | | | 1 | 5 | | * | * | | * | * | ppm/°C |
| Nonlinearity[2] | | | 0.0002 | 0.001 | | * | * | | * | * | % |
| **OUTPUT** | | | | | | | | | | | |
| Rated Voltage | $I_O$ = +20mA, –5mA | 10 | 12 | | * | * | | * | * | | V |
| Rated Current | $V_O$ = 10V | +20, –5 | | | * | | | * | | | mA |
| Impedance | | | 0.01 | | | * | | | * | | Ω |
| Current Limit | To Common | | +40/–10 | | | * | | | * | | mA |
| Capacitive Load | Stable Operation | | 1000 | | | * | | | * | | pF |
| **INPUT** | | | | | | | | | | | |
| Impedance[3] | Differential | | 50 | | | * | | | * | | kΩ |
| | Common-Mode | | 50 | | | * | | | * | | kΩ |
| Voltage Range[4] | Differential | ±10 | | | * | | | * | | | V |
| | Common-Mode | ±20 | | | * | | | * | | | V |
| Common-Mode Rejection[5] | $T_A = T_{MIN}$ to $T_{MAX}$ | 80 | 90 | | 86 | 100 | | 72 | * | | dB |
| **OFFSET VOLTAGE** | RTO[6], [7] | | | | | | | | | | |
| Initial | | | 50 | 250 | | * | * | | * | 500 | µV |
| vs Temperature | | | 5 | 20 | | 5 | 10 | | * | * | µV/°C |
| vs Supply | $\pm V_S$ = 6V to 18V | | 1 | 25 | | * | 15 | | * | * | µV/V |
| vs Time | | | 20 | | | * | | | * | | µV/mo |
| **OUTPUT NOISE VOLTAGE** | RTO[6], [8] | | | | | | | | | | |
| $f_B$ = 0.01Hz to 10Hz | | | 2.4 | | | * | | | * | | $\mu V_{p-p}$ |
| $f_O$ = 10kHz | | | 60 | | | * | | | * | | $nV/\sqrt{Hz}$ |
| **DYNAMIC RESPONSE** | | | | | | | | | | | |
| Small Signal Bandwidth | –3dB | | 1 | | | * | | | * | | MHz |
| Full Power Bandwidth | $V_O$ = 20Vp-p | 30 | 50 | | * | * | | * | * | | kHz |
| Slew Rate | | 2 | 3 | | * | * | | * | * | | V/µs |
| Settling Time: 0.1% | $V_O$ = 10V Step | | 4 | | | * | | | * | | µs |
| 0.01% | $V_O$ = 10V Step | | 5 | | | * | | | * | | µs |
| 0.01% | $V_{CM}$ = 10V Step, $V_{DIFF}$ = 0V | | 1.5 | | | * | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | | | | |
| Rated | | | ±15 | | | * | | | * | | V |
| Voltage Range | Derated Performance | ±5 | | ±18 | * | | * | * | | * | V |
| Quiescent Current | $V_O$ = 0V | | ±1.5 | ±2 | | * | * | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification | | –40 | | +85 | * | | * | * | | * | °C |
| Operation | | –55 | | +125 | * | | * | –40 | | +85 | °C |
| Storage | | –65 | | +150 | * | | * | –40 | | +125 | °C |

* Specification same as for INA105AM.

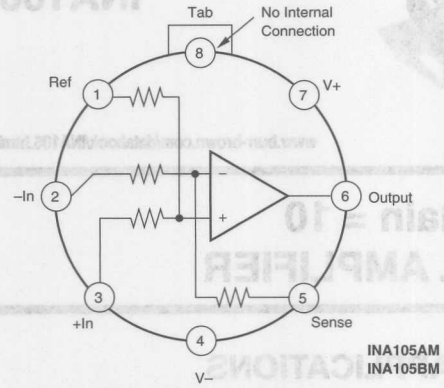
NOTES: (1) Connected as difference amplifier (see Figure 4). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output. (3) 25kΩ resistors are ratio matched but have ±20% absolute value. (4) Maximum input voltage without protection is 10V more than either ±15V supply (±25V). Limit $I_{IN}$ to 1mA. (5) With zero source impedance (see "Maintaining CMR" section). (6) Referred to output in unity-gain difference configuration. Note that this circuit has a gain of 2 for the operational amplifier's offset voltage and noise voltage. (7) Includes effects of amplifier's input bias and offset currents. (8) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.



The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN CONFIGURATIONS

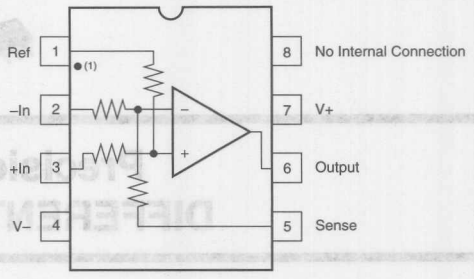
Top View — TO-99




INA105AM
INA105BM

Case internally connected to V–. Make no connection.

Top View — DIP/SOIC




NOTE: (1) Performance grade identifier box for small outline surface mount. Blank indicates K grade. Part is marked INA105U.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply | ±18V |
| Input Voltage Range | $\pm V_S$ |
| Operating Temperature Range: M | –55°C to +125°C |
| P, U | –40°C to +85°C |
| Storage Temperature Range: M | –65°C to +150°C |
| P, U | –40°C to +125°C |
| Lead Temperature (soldering, 10s) M, P | +300°C |
| Wave Soldering (3s, max) U | +260°C |
| Output Short Circuit to Common | Continuous |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| INA105AM | TO-99 Metal | 001 | –40°C to +85°C |
| INA105BM | TO-99 Metal | 001 | –40°C to +85°C |
| INA105KP | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| INA105KU | 8-Pin SOIC | 182 | –40°C to +85°C |

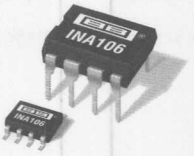
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# INA106

www.burr-brown.com/databook/INA106.html

# Precision Gain = 10 DIFFERENTIAL AMPLIFIER

## FEATURES

- ACCURATE GAIN: ±0.025% max
- HIGH COMMON-MODE REJECTION: 86dB min
- NONLINEARITY: 0.001% max
- EASY TO USE
- PLASTIC 8-PIN DIP, SO-8 SOIC PACKAGES

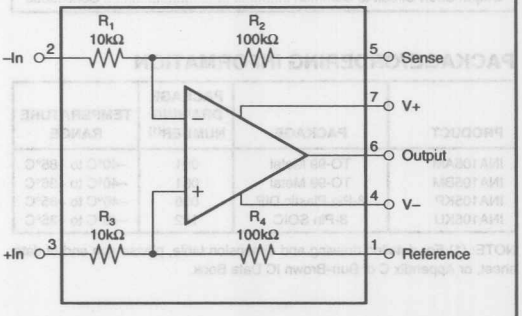
## APPLICATIONS

- G = 10 DIFFERENTIAL AMPLIFIER
- G = +10 AMPLIFIER
- G = –10 AMPLIFIER
- G = +11 AMPLIFIER
- INSTRUMENTATION AMPLIFIER

## DESCRIPTION

The INA106 is a monolithic Gain = 10 differential amplifier consisting of a precision op amp and on-chip metal film resistors. The resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature.

The differential amplifier is the foundation of many commonly used circuits. The INA106 provides this precision circuit function without using an expensive resistor network. The INA106 is available in 8-pin plastic DIP and SO-8 surface-mount packages.




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# SPECIFICATIONS

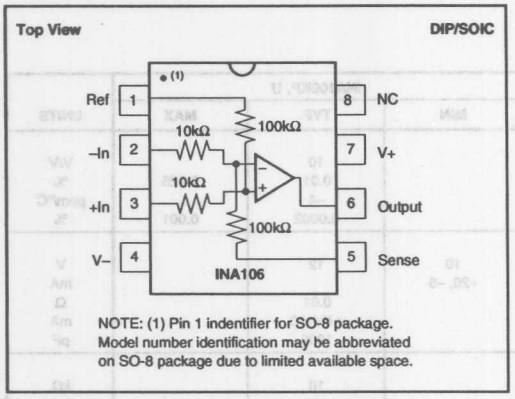
## ELECTRICAL

At +25°C, $V_S$ = ±15V, unless otherwise specified.

| PARAMETER | CONDITIONS | INA106KP, U MIN | INA106KP, U TYP | INA106KP, U MAX | UNITS |
|---|---|---|---|---|---|
| **GAIN** | | | | | |
| Initial[1] | | | 10 | | V/V |
| Error | | | 0.01 | 0.025 | % |
| vs Temperature | | | –4 | | ppm/°C |
| Nonlinearity[2] | | | 0.0002 | 0.001 | % |
| **OUTPUT** | | | | | |
| Related Voltage | $I_O$ = +20mA, –5mA | 10 | 12 | | V |
| Rated Current | $V_O$ = 10V | +20, –5 | | | mA |
| Impedance | | | 0.01 | | Ω |
| Current Limit | To Common | | +40/–10 | | mA |
| Capacitive Load | Stable Operation | | 1000 | | pF |
| **INPUT** | | | | | |
| Impedance | Differential | | 10 | | kΩ |
| | Common-Mode | | 110 | | kΩ |
| Voltage Range | Differential | ±1 | | | V |
| | Common-Mode | ±11 | | | V |
| Common-Mode Rejection[3] | $T_A = T_{MIN}$ to $T_{MAX}$ | 86 | 100 | | dB |
| **OFFSET VOLTAGE** | RTI[4] | | | | |
| Initial | | | 50 | 200 | µV |
| vs Temperature | | | 0.2 | | µV/°C |
| vs Supply | ±$V_S$ = 6V to 18V | | 1 | 10 | µV/V |
| vs Time | | | 10 | | µV/mo |
| **NOISE VOLTAGE** | RTI[5] | | | | |
| $f_B$ = 0.01Hz to 10Hz | | | 1 | | µVp-p |
| $f_O$ = 10kHz | | | 30 | | nV/√Hz |
| **DYNAMIC RESPONSE** | | | | | |
| Small Signal | –3dB | | 5 | | MHz |
| Full Power BW | $V_O$ = 20Vp-p | 30 | 50 | | kHz |
| Slew Rate | | 2 | 3 | | V/µs |
| Settling Time: 0.1% | $V_O$ = 10V Step | | 5 | | µs |
| 0.01% | $V_O$ = 10V Step | | 10 | | µs |
| 0.01% | $V_{CM}$ = 10V Step, $V_{DIFF}$ = 0V | | 5 | | µs |
| **POWER SUPPLY** | | | | | |
| Rated | | | 5 | | V |
| Voltage Range | Derated Performance | ±5 | | ±18 | V |
| Quiescent Current | $V_O$ = 0V | | ±1.5 | ±2 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | 0 | | +70 | °C |
| Operation | | –40 | | +85 | °C |
| Storage | | –65 | | +150 | °C |

NOTES: (1) Connected as difference amplifier (see Figure 1). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output. (3) With zero source impedance (see "Maintaining CMR" section). (4) Includes effects of amplifiers's input bias and offset currents. (5) Includes effect of amplifier's input current noise and thermal noise contribution of resistor network.

## PIN CONFIGURATION




NOTE: (1) Pin 1 indentifier for SO-8 package. Model number identification may be abbreviated on SO-8 package due to limited available space.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | ±18V |
| Input Voltage Range | $\pm V_S$ |
| Operating Temperature Range: P, U | –40°C to +85°C |
| Storage Temperature Range | –40°C to +85°C |
| Lead Temperature (soldering, 10s): P | +300°C |
| Wave Soldering (3s, max) U | +260°C |
| Output Short Circuit to Common | Continuous |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integral circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

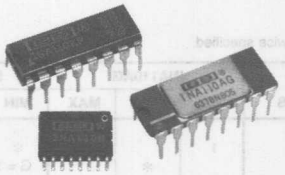
## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| INA106KP | 8-Pin Plastic DIP | 006 | 0°C to +70°C |
| INA106U | SO-8 Surface Mount | 182 | 0°C to +70°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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# INA110

www.burr-brown.com/databook/INA110.html

# Fast-Settling FET-Input INSTRUMENTATION AMPLIFIER



## FEATURES

- LOW BIAS CURRENT: 50pA max
- FAST SETTLING: 4µs to 0.01%
- HIGH CMR: 106dB min; 90dB at 10kHz
- INTERNAL GAINS: 1, 10, 100, 200, 500
- VERY LOW GAIN DRIFT: 10 to 50ppm/°C
- LOW OFFSET DRIFT: 2µV/°C
- LOW COST
- PINOUT SIMILAR TO AD524 AND AD624

## APPLICATIONS

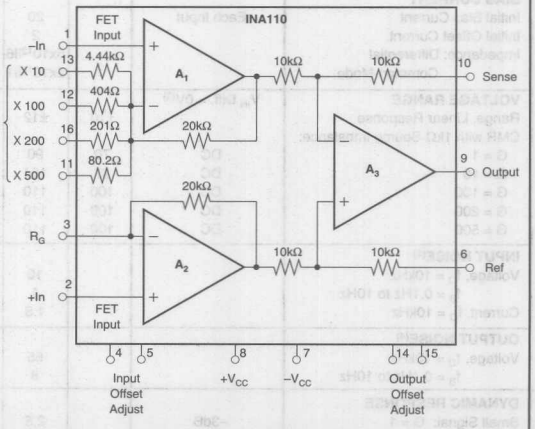
- MULTIPLEXED INPUT DATA ACQUISITION SYSTEM
- FAST DIFFERENTIAL PULSE AMPLIFIER
- HIGH SPEED GAIN BLOCK
- AMPLIFICATION OF HIGH IMPEDANCE SOURCES

## DESCRIPTION

The INA110 is a versatile monolithic FET-input instrumentation amplifier. Its current-feedback circuit topology and laser trimmed input stage provide excellent dynamic performance and accuracy. The INA110 settles in 4µs to 0.01%, making it ideal for high speed or multiplexed-input data acquisition systems.

Internal gain-set resistors are provided for gains of 1, 10, 100, 200, and 500V/V. Inputs are protected for differential and common-mode voltages up to $\pm V_{CC}$. Its very high input impedance and low input bias current make the INA110 ideal for applications requiring input filters or input protection circuitry.

The INA110 is available in 16-pin plastic and ceramic DIPs, and in the SOL-16 surface-mount package. Military, industrial and commercial temperature range grades are available.




NOTE: (1) Connect to $R_G$ for desired gain.

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# SPECIFICATIONS

## ELECTRICAL

At +25°C, $\pm V_{CC}$ = 15VDC, and $R_L$ = 2kΩ, unless otherwise specified.

| PARAMETER | CONDITIONS | INA110AG | | | INA110BG, SG | | | INA110KP, KU | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **GAIN** | | | | | | | | | | | |
| Range of Gain | | 1 | | 800 | * | | * | * | | * | V/V |
| Gain Equation[1] | | | * | | | G = 1 + [40k/($R_G$ + 50Ω)] | | | * | | V/V |
| Gain Error, DC: G = 1 | | | 0.002 | 0.04 | | * | 0.02 | | * | * | % |
| G = 10 | | | 0.01 | 0.1 | | 0.005 | 0.05 | | * | * | % |
| G = 100 | | | 0.02 | 0.2 | | 0.01 | 0.1 | | * | * | % |
| G = 200 | | | 0.04 | 0.4 | | 0.02 | 0.2 | | * | * | % |
| G = 500 | | | 0.1 | 1 | | 0.05 | 0.5 | | * | * | % |
| Gain Temp. Coefficient: G = 1 | | | ±3 | ±20 | | * | ±10 | | * | | ppm/°C |
| G = 10 | | | ±4 | ±20 | | ±2 | ±10 | | * | | ppm/°C |
| G = 100 | | | ±6 | ±40 | | ±3 | ±20 | | * | | ppm/°C |
| G = 200 | | | ±10 | ±60 | | ±5 | ±30 | | * | | ppm/°C |
| G = 500 | | | ±25 | ±100 | | ±10 | ±50 | | * | | ppm/°C |
| Nonlinearity, DC: G = 1 | | | ±0.001 | ±0.01 | | ±0.0005 | ±0.005 | | * | * | % of FS |
| G = 10 | | | ±0.002 | ±0.01 | | ±0.001 | ±0.005 | | * | * | % of FS |
| G = 100 | | | ±0.004 | ±0.02 | | ±0.002 | ±0.01 | | * | * | % of FS |
| G = 200 | | | ±0.006 | ±0.02 | | ±0.003 | ±0.01 | | * | * | % of FS |
| G = 500 | | | ±0.01 | ±0.04 | | ±0.005 | ±0.02 | | * | * | % of FS |
| **OUTPUT** | | | | | | | | | | | |
| Voltage, $R_L$ = 2kΩ | Over Temperature | ±10 | ±12.7 | | * | * | | * | * | | V |
| Current | Over Temperature | ±5 | ±25 | | * | * | | * | * | | mA |
| Short-Circuit Current | | | ±25 | | | * | | | * | | mA |
| Capacitive Load | Stability | | 5000 | | | * | | | * | | pF |
| **INPUT OFFSET VOLTAGE[2]** | | | | | | | | | | | |
| Initial Offset: G, P | | | ±(100 + 1000/G) | ±(500 + 5000/G) | | ±(50 + 600/G) | ±(250 + 3000/G) | | * | * | µV |
| U | | | | | | | | | ±(200 + 2000/G) | ±(1000 + 5000/G) | µV |
| vs Temperature | | | ±(2 + 20/G) | ±(5 + 100/G) | | ±(1 + 10/G) | ±(2 + 50/G) | | * | | µV/°C |
| vs Supply | $V_{CC}$ = ±6V to ±18V | | ±(4 + 60/G) | ±(30 + 300/G) | | ±(2 + 30/G) | ±(10 + 180/G) | | * | * | µV/V |
| **BIAS CURRENT** | | | | | | | | | | | |
| Initial Bias Current | Each Input | | 20 | 100 | | 10 | 50 | | * | * | pA |
| Initial Offset Current | | | 2 | 50 | | 1 | 25 | | * | * | pA |
| Impedance: Differential | | | $5x10^{12}$\|\|6 | | | * | | | * | | Ω \|\| pF |
| Common-Mode | | | $2x10^{12}$\|\|1 | | | * | | | * | | Ω \|\| pF |
| **VOLTAGE RANGE** | $V_{IN}$ Diff. = 0V[3] | | | | | | | | | | |
| Range, Linear Response | | ±10 | ±12 | | | | | * | * | | V |
| CMR with 1kΩ Source Imbalance: | | | | | | | | | | | |
| G = 1 | DC | 70 | 90 | | 80 | 100 | | * | * | | dB |
| G = 10 | DC | 87 | 104 | | 96 | 112 | | * | * | | dB |
| G = 100 | DC | 100 | 110 | | 106 | 116 | | * | * | | dB |
| G = 200 | DC | 100 | 110 | | 106 | 116 | | * | * | | dB |
| G = 500 | DC | 100 | 110 | | 106 | 116 | | * | * | | dB |
| **INPUT NOISE[4]** | | | | | | | | | | | |
| Voltage, $f_O$ = 10kHz | | | 10 | | | * | | | * | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 1 | | | * | | | * | | µVp-p |
| Current, $f_O$ = 10kHz | | | 1.8 | | | * | | | * | | fA/√Hz |
| **OUTPUT NOISE[4]** | | | | | | | | | | | |
| Voltage, $f_O$ = 10kHz | | | 65 | | | * | | | * | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 8 | | | * | | | * | | µVp-p |
| **DYNAMIC RESPONSE** | | | | | | | | | | | |
| Small Signal: G = 1 | –3dB | | 2.5 | | | * | | | * | | MHz |
| G = 10 | | | 2.5 | | | * | | | * | | MHz |
| G = 100 | | | 470 | | | * | | | * | | kHz |
| G = 200 | | | 240 | | | * | | | * | | kHz |
| G = 500 | | | 100 | | | * | | | * | | kHz |
| Full Power | $V_{OUT}$ = ±10V, G = 2 to 100 | 190 | 270 | | * | * | | | * | * | kHz |
| Slew Rate | G = 2 to 100 | 12 | 17 | | * | * | | | * | * | V/µs |
| Settling Time: | | | | | | | | | | | |
| 0.1%, G = 1 | $V_O$ = 20V Step | | 4 | | | * | | | * | | µs |
| G = 10 | | | 2 | | | * | | | * | | µs |
| G = 100 | | | 3 | | | * | | | * | | µs |
| G = 200 | | | 5 | | | * | | | * | | µs |
| G = 500 | | | 11 | | | * | | | * | | µs |

## SPECIFICATIONS (CONT)

### ELECTRICAL

At +25°C, $\pm V_{CC}$ 15VDC, and $R_L$ = 2KΩ, unless otherwise specified.

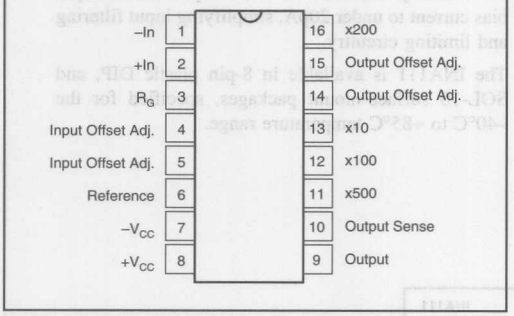
| PARAMETER | CONDITIONS | INA110AG | | | INA110BG, SG | | | INA110KP, KU | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **DYNAMIC RESPONSE (CONT)** | | | | | | | | | | | |
| Settling Time: | | | | | | | | | | | |
| 0.01%,G = 1 | $V_O$ = 20V Step | | 5 | 12.5 | | * | * | | * | | µs |
| G = 10 | | | 3 | 7.5 | | * | * | | * | | µs |
| G = 100 | | | 4 | 7.5 | | * | * | | * | | µs |
| G = 200 | | | 7 | 12.5 | | * | * | | * | | µs |
| G = 500 | | | 16 | 25 | | * | * | | * | | µs |
| Recovery[5] | 50% Overdrive | | 1 | | | * | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | | | | |
| Rated Voltage | | | ±15 | | | * | | | * | | V |
| Voltage Range | | ±6 | | ±18 | * | | * | * | | * | V |
| Quiescent Current | $V_O$ = 0V | | ±3 | ±4.5 | | * | * | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification: A, B, K | | –25 | | +85 | * | | * | 0 | | +70 | °C |
| S | | | | | –55 | | +125 | | | | °C |
| Operation | | –55 | | +125 | * | | * | –25 | | +85 | °C |
| Storage | | –65 | | +150 | * | | * | –40 | | +85 | °C |
| $\theta_{JA}$ | | | 100 | | | * | | | * | | °C/W |

* Same as INA110AG.

NOTES: (1) Gains other than 1, 10, 100, 200, and 500 can be set by adding an external resistor, $R_G$, between pin 3 and pins 11, 12 and 16. Gain accuracy is a function of $R_G$ and the internal resistors which have a ±20% tolerance with 20ppm/°C drift. (2) Adjustable to zero. (3) For differential input voltage other than zero, see Typical Performance Curves. (4) $V_{NOISE\ RTI} = \sqrt{V_N{}^2_{\ INPUT} + (V_{N\ OUTPUT}/Gain)^2}$. (5) Time required for output to return from saturation to linear operation following the removal of an input overdrive voltage.

### PIN CONFIGURATION

Top View — DIP/SOIC




### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Input Voltage Range | $\pm V_{CC}$ |
| Operating Temperature Range: G | –55°C to +125°C |
| P, U | –25°C to +85°C |
| Storage Temperature Range: G | –65°C to +150°C |
| P, U | –40°C to +85°C |
| Lead Temperature (soldering, 10s): G, P | +300°C |
| (soldering, 3s): U | +260°C |
| Output Short Circuit Duration | Continuous to Common |

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| INA110AG | 16-Pin Ceramic DIP | 109 | –25°C to +85°C |
| INA110BG | 16-Pin Ceramic DIP | 109 | –25°C to +85°C |
| INA110SG | 16-Pin Ceramic DIP | 109 | –55°C to +125°C |
| INA110KP | 16-Pin Plastic DIP | 180 | 0°C to +70°C |
| INA110KU | SOL-16 SOIC | 211 | 0°C to +70°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

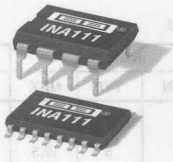
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# INA111

www.burr-brown.com/databook/INA111.html

# High Speed FET-Input INSTRUMENTATION AMPLIFIER

## FEATURES

- FET INPUT: $I_B$ = 20pA max
- HIGH SPEED: $T_S$ = 4µs (G = 100, 0.01%)
- LOW OFFSET VOLTAGE: 500µV max
- LOW OFFSET VOLTAGE DRIFT: 5µV/°C max
- HIGH COMMON-MODE REJECTION: 106dB min
- 8-PIN PLASTIC DIP, SOL-16 SOIC

## APPLICATIONS

- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

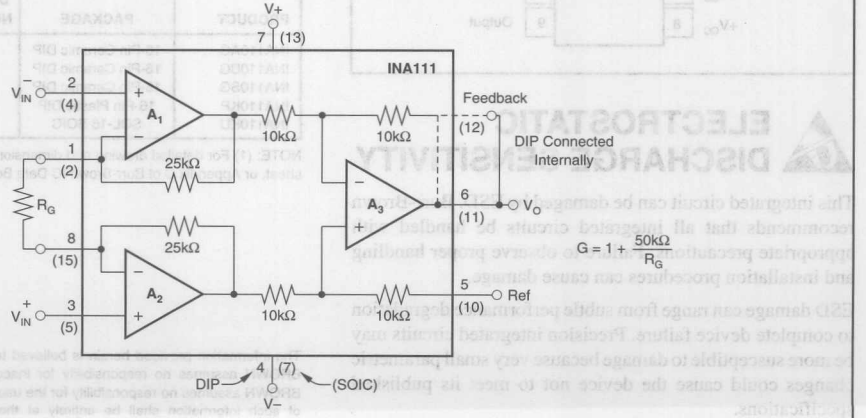
## DESCRIPTION

The INA111 is a high speed, FET-input instrumentation amplifier offering excellent performance.

The INA111 uses a current-feedback topology providing extended bandwidth (2MHz at G = 10) and fast settling time (4µs to 0.01% at G = 100). A single external resistor sets any gain from 1 to over 1000.

Offset voltage and drift are laser trimmed for excellent DC accuracy. The INA111's FET inputs reduce input bias current to under 20pA, simplifying input filtering and limiting circuitry.

The INA111 is available in 8-pin plastic DIP, and SOL-16 surface-mount packages, specified for the –40°C to +85°C temperature range.




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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 2kΩ, unless otherwise noted.

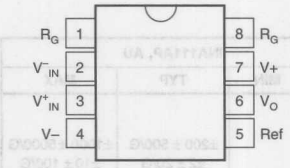
| | | INA111BP, BU | | | INA111AP, AU | | | |
|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **CONDITIONS** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **INPUT** | | | | | | | | |
| Offset Voltage, RTI | | | | | | | | |
| Initial | $T_A$ = +25°C | | ±100 ± 500/G | ±500 ±2000/G | | ±200 ± 500/G | ±1000 ±5000/G | µV |
| vs Temperature | $T_A = T_{MIN}$ to $T_{MAX}$ | | ±2 ± 10/G | ±5 ± 100/G | | ±2 ± 20/G | ±10 ± 100/G | µV/°C |
| vs Power Supply | $V_S$ = ±6V to ±18V | | 2 +10/G | 30 + 100/G | | * | * | µV/V |
| Impedance, Differential | | | $10^{12}$ \|\| 6 | | | * | | Ω \|\| pF |
| Common-Mode | | | $10^{12}$ \|\| 3 | | | * | | Ω \|\| pF |
| Input Common-Mode Range | $V_{DIFF}$ = 0V | ±10 | ±12 | | * | * | | V |
| Common-Mode Rejection | $V_{CM}$ = ±10V, $\Delta R_S$ = 1kΩ | | | | | | | |
| | G = 1 | 80 | 90 | | 75 | * | | dB |
| | G = 10 | 96 | 110 | | 90 | * | | dB |
| | G = 100 | 106 | 115 | | 100 | * | | dB |
| | G = 1000 | 106 | 115 | | 100 | * | | dB |
| **BIAS CURRENT** | | | ±2 | ±20 | | * | * | pA |
| **OFFSET CURRENT** | | | ±0.1 | ±10 | | * | * | pA |
| **NOISE VOLTAGE, RTI** | G = 1000, $R_S$ = 0Ω | | | | | | | |
| f = 100Hz | | | 13 | | | * | | nV/√Hz |
| f = 1kHz | | | 10 | | | * | | nV/√Hz |
| f = 10kHz | | | 10 | | | * | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 1 | | | * | | µVp-p |
| Noise Current | | | | | | | | |
| f = 10kHz | | | 0.8 | | | * | | fA/√Hz |
| **GAIN** | | | | | | | | |
| Gain Equation | | | 1 + (50kΩ/$R_G$) | | | * | | V/V |
| Range of Gain | | 1 | | 10000 | * | | * | V/V |
| Gain Error | G = 1, $R_L$ = 10kΩ | | ±0.01 | ±0.02 | | * | 0.05 | % |
| | G = 10, $R_L$ = 10kΩ | | ±0.1 | ±0.5 | | * | * | % |
| | G = 100, $R_L$ = 10kΩ | | ±0.15 | ±0.5 | | * | ±0.7 | % |
| | G = 1000, $R_L$ = 10kΩ | | ±0.25 | ±1 | | * | ±2 | % |
| Gain vs Temperature | G = 1 | | ±1 | ±10 | | * | * | ppm/°C |
| 50kΩ Resistance[1] | | | ±25 | ±100 | | * | * | ppm/°C |
| Nonlinearity | G = 1 | | ±0.0005 | ±0.005 | | * | * | % of FSR |
| | G = 10 | | ±0.001 | ±0.005 | | * | ±0.01 | % of FSR |
| | G = 100 | | ±0.001 | ±0.005 | | * | ±0.01 | % of FSR |
| | G = 1000 | | ±0.005 | ±0.02 | | * | ±0.04 | % of FSR |
| **OUTPUT** | | | | | | | | |
| Voltage | $I_O$ = 5mA, $T_{MIN}$ to $T_{MAX}$ | ±11 | ±12.7 | | * | * | | V |
| Load Capacitance Stability | | | 1000 | | | * | | pF |
| Short Circuit Current | | | +30/–25 | | | * | | mA |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Bandwidth, –3dB | G = 1 | | 2 | | | * | | MHz |
| | G = 10 | | 2 | | | * | | MHz |
| | G = 100 | | 450 | | | * | | kHz |
| | G = 1000 | | 50 | | | * | | kHz |
| Slew Rate | $V_O$ = ±10V, G = 2 to 100 | | 17 | | | * | | V/µs |
| Settling Time, 0.01% | G = 1 | | 2 | | | * | | µs |
| | G = 10 | | 2 | | | * | | µs |
| | G = 100 | | 4 | | | * | | µs |
| | G = 1000 | | 30 | | | * | | µs |
| Overload Recovery | 50% Overdrive | | 1 | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | |
| Voltage Range | | ±6 | ±15 | ±18 | * | * | * | V |
| Current | $V_{IN}$ = 0V | | ±3.3 | ±4.5 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –40 | | 85 | * | | * | °C |
| Operating | | –40 | | 125 | * | | * | °C |
| $\theta_{JA}$ | | | 100 | | | * | | °C/W |

* Specification same as INA111BP.

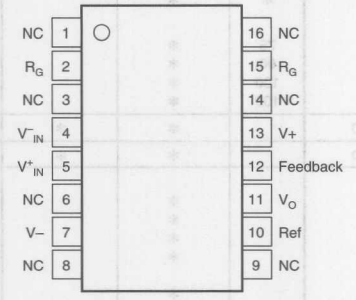
NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation.

## PIN CONFIGURATIONS

**Top View** **DIP**




**Top View** **SOL-16 Surface Mount**




## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Supply Voltage | ±18V |
| Input Voltage Range | (V–) –0.7V to (V+) +15V |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: Stresses above these ratings may cause permanent damage.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

| PRODUCT | PACKAGE | TEMPERATURE RANGE |
|---|---|---|
| INA111AP | 8-Pin Plastic DIP | –40°C to +85°C |
| INA111BP | 8-Pin Plastic DIP | –40°C to +85°C |
| INA111AU | SOL-16 Surface-Mount | –40°C to +85°C |
| INA111BU | SOL-16 Surface-Mount | –40°C to +85°C |

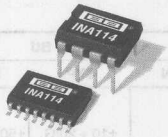
## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| INA111AP | 8-Pin Plastic DIP | 006 |
| INA111BP | 8-Pin Plastic DIP | 006 |
| INA111AU | 16-Pin Surface Mount | 211 |
| INA111BU | 16-Pin Surface Mount | 211 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# INA114

www.burr-brown.com/databook/INA114.html

# Precision INSTRUMENTATION AMPLIFIER



## FEATURES

- LOW OFFSET VOLTAGE: 50μV max
- LOW DRIFT: 0.25μV/°C max
- LOW INPUT BIAS CURRENT: 2nA max
- HIGH COMMON-MODE REJECTION: 115dB min
- INPUT OVER-VOLTAGE PROTECTION: ±40V
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 3mA max
- 8-PIN PLASTIC AND SOL-16

## APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

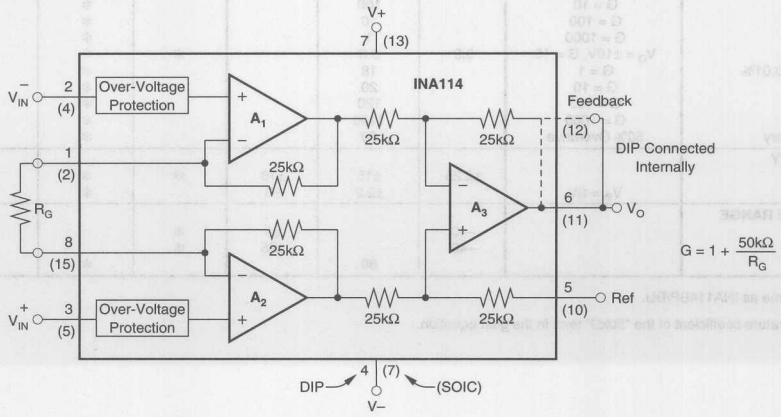
## DESCRIPTION

The INA114 is a low cost, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications.

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA114 is laser trimmed for very low offset voltage (50μV), drift (0.25μV/°C) and high common-mode rejection (115dB at G = 1000). It operates with power supplies as low as ±2.25V, allowing use in battery operated and single 5V supply systems. Quiescent current is 3mA maximum.

The INA114 is available in 8-pin plastic and SOL-16 surface-mount packages. Both are specified for the –40°C to +85°C temperature range.




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# SPECIFICATIONS

## ELECTRICAL

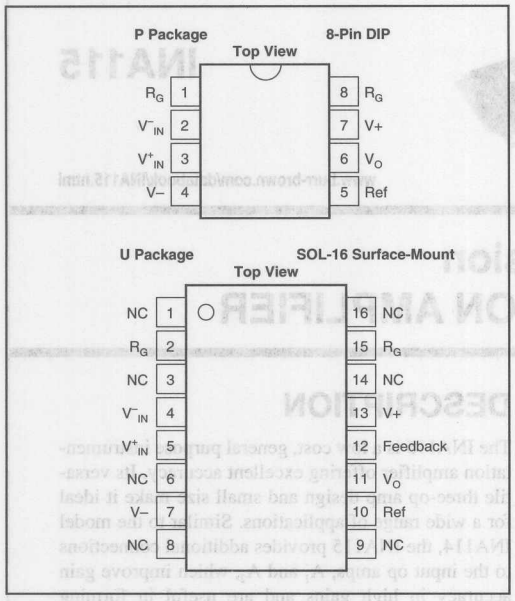
At $T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 2kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | INA114BP, BU | | | INA114AP, AU | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT** | | | | | | | | |
| Offset Voltage, RTI | | | | | | | | |
| Initial | $T_A$ = +25°C | | ±10 + 20/G | ±50 + 100/G | | ±25 + 30/G | ±125 + 500/G | µV |
| vs Temperature | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | ±0.1 + 0.5/G | ±0.25 + 5/G | | ±0.25 + 5/G | ±1 + 10/G | µV/°C |
| vs Power Supply | $V_S$ = ±2.25V to ±18V | | 0.5 + 2/G | 3 + 10/G | | * | * | µV/V |
| Long-Term Stability | | | ±0.2 + 0.5/G | | | * | | µV/mo |
| Impedance, Differential | | | $10^{10}$ \|\| 6 | | | * | | Ω \|\| pF |
| Common-Mode | | | $10^{10}$ \|\| 6 | | | * | | Ω \|\| pF |
| Input Common-Mode Range | | ±11 | ±13.5 | | * | * | | V |
| Safe Input Voltage | | | | ±40 | | | * | V |
| Common-Mode Rejection | $V_{CM}$ = ±10V, $\Delta R_S$ = 1kΩ | | | | | | | |
| | G = 1 | 80 | 96 | | 75 | 90 | | dB |
| | G = 10 | 96 | 115 | | 90 | 106 | | dB |
| | G = 100 | 110 | 120 | | 106 | 110 | | dB |
| | G = 1000 | 115 | 120 | | 106 | 110 | | dB |
| **BIAS CURRENT** | | | ±0.5 | ±2 | | * | ±5 | nA |
| vs Temperature | | | ±8 | | | * | | pA/°C |
| **OFFSET CURRENT** | | | ±0.5 | ±2 | | * | ±5 | nA |
| vs Temperature | | | ±8 | | | * | | pA/°C |
| **NOISE VOLTAGE, RTI** | G = 1000, $R_S$ = 0Ω | | | | | | | |
| f = 10Hz | | | 15 | | | * | | nV/√Hz |
| f = 100Hz | | | 11 | | | * | | nV/√Hz |
| f = 1kHz | | | 11 | | | * | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 0.4 | | | * | | µVp-p |
| Noise Current | | | | | | | | |
| f=10Hz | | | 0.4 | | | * | | pA/√Hz |
| f=1kHz | | | 0.2 | | | * | | pA/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 18 | | | * | | pAp-p |
| **GAIN** | | | | | | | | |
| Gain Equation | | | 1 + (50kΩ/$R_G$) | | | * | | V/V |
| Range of Gain | | 1 | | 10000 | * | * | * | V/V |
| Gain Error | G = 1 | | ±0.01 | ±0.05 | | * | * | % |
| | G = 10 | | ±0.02 | ±0.4 | | * | ±0.5 | % |
| | G = 100 | | ±0.05 | ±0.5 | | * | ±0.7 | % |
| | G = 1000 | | ±0.5 | ±1 | | * | ±2 | % |
| Gain vs Temperature | G = 1 | | ±2 | ±10 | | * | ±10 | ppm/°C |
| 50kΩ Resistance[1] | | | ±25 | ±100 | | * | * | ppm/°C |
| Nonlinearity | G = 1 | | ±0.0001 | ±0.001 | | * | ±0.002 | % of FSR |
| | G = 10 | | ±0.0005 | ±0.002 | | * | ±0.004 | % of FSR |
| | G = 100 | | ±0.0005 | ±0.002 | | * | ±0.004 | % of FSR |
| | G = 1000 | | ±0.002 | ±0.01 | | * | ±0.02 | % of FSR |
| **OUTPUT** | | | | | | | | |
| Voltage | $I_O$ = 5mA, $T_{MIN}$ to $T_{MAX}$ | ±13.5 | ±13.7 | | * | * | | V |
| | $V_S$ = ±11.4V, $R_L$ = 2kΩ | ±10 | ±10.5 | | * | * | | V |
| | $V_S$ = ±2.25V, $R_L$ = 2kΩ | ±1 | ±1.5 | | * | * | | V |
| Load Capacitance Stability | | | 1000 | | | * | | pF |
| Short Circuit Current | | | +20/–15 | | | * | | mA |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Bandwidth, –3dB | G = 1 | | 1 | | | * | | MHz |
| | G = 10 | | 100 | | | * | | kHz |
| | G = 100 | | 10 | | | * | | kHz |
| | G = 1000 | | 1 | | | * | | kHz |
| Slew Rate | $V_O$ = ±10V, G = 10 | 0.3 | 0.6 | | * | * | | V/µs |
| Settling Time, 0.01% | G = 1 | | 18 | | | * | | µs |
| | G = 10 | | 20 | | | * | | µs |
| | G = 100 | | 120 | | | * | | µs |
| | G = 1000 | | 1100 | | | * | | µs |
| Overload Recovery | 50% Overdrive | | 20 | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | |
| Voltage Range | | ±2.25 | ±15 | ±18 | * | * | * | V |
| Current | $V_{IN}$ = 0V | | ±2.2 | ±3 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –40 | | 85 | * | | * | °C |
| Operating | | –40 | | 125 | * | | * | °C |
| $\theta_{JA}$ | | | 80 | | | * | | °C/W |

* Specification same as INA114BP/BU.

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation.

## PIN CONFIGURATIONS




## ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|---|
| Supply Voltage | ±18V |
| Input Voltage Range | ±40V |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above these ratings may cause permanent damage.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| INA114AP | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| INA114BP | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| INA114AU | SOL-16 Surface-Mount | 211 | –40°C to +85°C |
| INA114BU | SOL-16 Surface-Mount | 211 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



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# INA115

www.burr-brown.com/databook/INA115.html

# Precision INSTRUMENTATION AMPLIFIER

## FEATURES

- LOW OFFSET VOLTAGE: 50μV max
- LOW DRIFT: 0.25μV/°C max
- LOW INPUT BIAS CURRENT: 2nA max
- HIGH COMMON-MODE REJECTION: 115dB min
- INPUT OVER-VOLTAGE PROTECTION: ±40V
- WIDE SUPPLY RANGE: ±2.25 TO ±18V
- LOW QUIESCENT CURRENT: 3mA max
- SOL-16 SURFACE-MOUNT PACKAGE

## APPLICATIONS

- SWITCHED-GAIN AMPLIFIER
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

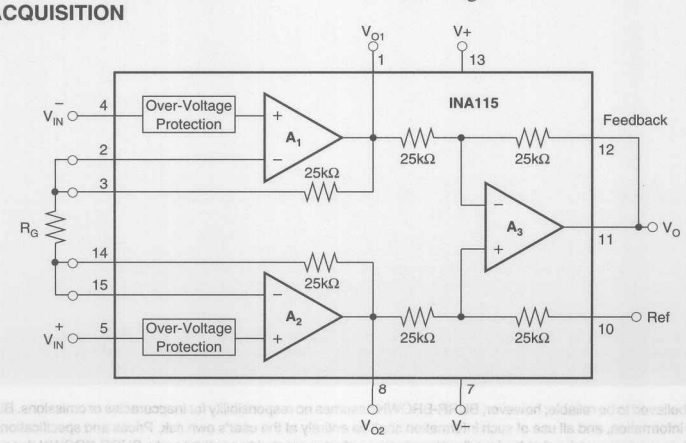
## DESCRIPTION

The INA115 is a low cost, general purpose instrumentation amplifier offering excellent accuracy. Its versatile three-op amp design and small size make it ideal for a wide range of applications. Similar to the model INA114, the INA115 provides additional connections to the input op amps, $A_1$ and $A_2$, which improve gain accuracy in high gains and are useful in forming switched-gain amplifiers.

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA115 is laser trimmed for very low offset voltage (50μV), drift (0.25μV/°C) and high common-mode rejection (115dB at G=1000). It operates with power supplies as low as ±2.25V, allowing use in battery operated and single 5V supply systems. Quiescent current is 3mA maximum.

The INA115 is available in the SOL-16 surface-mount package, specified for the –40°C to +85°C temperature range.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

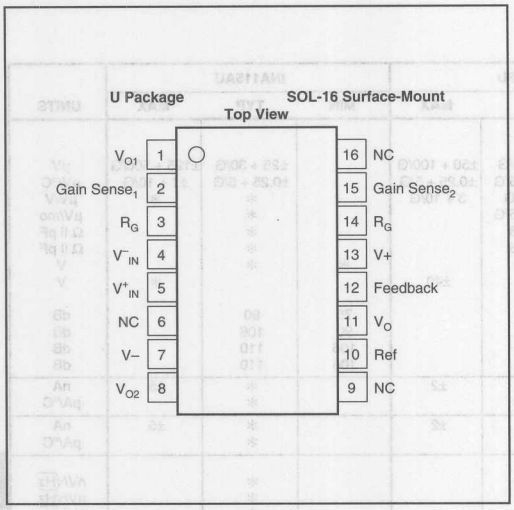
At $T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 2kΩ unless otherwise noted.

| PARAMETER | CONDITIONS | INA115BU MIN | INA115BU TYP | INA115BU MAX | INA115AU MIN | INA115AU TYP | INA115AU MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | | |
| Offset Voltage, RTI | | | | | | | | |
| Initial | $T_A$ = +25°C | | ±10 + 20/G | ±50 + 100/G | | ±25 + 30/G | ±125 + 500/G | µV |
| vs Temperature | $T_A = T_{MIN}$ to $T_{MAX}$ | | ±0.1 + 0.5/G | ±0.25 + 5/G | | ±0.25 + 5/G | ±1 + 10/G | µV/°C |
| vs Power Supply | $V_S$ = ±2.25V to ±18V | | 0.5 + 2/G | 3 + 10/G | | * | * | µV/V |
| Long-Term Stability | | | ±0.2 + 0.5/G | | | * | | µV/mo |
| Impedance, Differential | | | $10^{10}$ \|\| 6 | | | * | | Ω \|\| pF |
| Common-Mode | | | $10^{10}$ \|\| 6 | | | * | | Ω \|\| pF |
| Input Common-Mode Range | | ±11 | ±13.5 | | * | * | | V |
| Safe Input Voltage | | | | ±40 | | | * | V |
| Common-Mode Rejection | $V_{CM}$ = ±10V, $\Delta R_S$ = 1kΩ | | | | | | | |
| | G = 1 | 80 | 96 | | 75 | 90 | | dB |
| | G = 10 | 96 | 115 | | 90 | 106 | | dB |
| | G = 100 | 110 | 120 | | 106 | 110 | | dB |
| | G = 1000 | 115 | 120 | | 106 | 110 | | dB |
| **BIAS CURRENT** | | | ±0.5 | ±2 | | * | ±5 | nA |
| vs Temperature | | | ±8 | | | * | | pA/°C |
| **OFFSET CURRENT** | | | ±0.5 | ±2 | | * | ±5 | nA |
| vs Temperature | | | ±8 | | | * | | pA/°C |
| **NOISE VOLTAGE, RTI** | G = 1000, $R_S$ = 0Ω | | | | | | | |
| f = 10Hz | | | 15 | | | * | | nV/√Hz |
| f = 100Hz | | | 11 | | | * | | nV/√Hz |
| f = 1kHz | | | 11 | | | * | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 0.4 | | | * | | µVp-p |
| Noise Current | | | | | | | | |
| f=10Hz | | | 0.4 | | | * | | pA/√Hz |
| f=1kHz | | | 0.2 | | | * | | pA/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 18 | | | * | | pAp-p |
| **GAIN** | | | | | | | | |
| Gain Equation | | | 1 + (50kΩ/$R_G$) | | | * | | V/V |
| Range of Gain | | 1 | | 10000 | * | | * | V/V |
| Gain Error | G = 1 | | ±0.01 | ±0.05 | | * | * | % |
| | G = 10 | | ±0.02 | ±0.4 | | * | ±0.5 | % |
| | G = 100 | | ±0.05 | ±0.5 | | * | ±0.7 | % |
| | G = 1000 | | ±0.5 | ±1 | | * | ±2 | % |
| Gain vs Temperature | G = 1 | | ±2 | ±10 | | * | ±10 | ppm/°C |
| 50kΩ Resistance[1] | | | ±25 | ±100 | | * | * | ppm/°C |
| Nonlinearity | G = 1 | | ±0.0001 | ±0.001 | | * | ±0.002 | % of FSR |
| | G = 10 | | ±0.0005 | ±0.002 | | * | ±0.004 | % of FSR |
| | G = 100 | | ±0.0005 | ±0.002 | | * | ±0.004 | % of FSR |
| | G = 1000 | | ±0.002 | ±0.01 | | * | ±0.02 | % of FSR |
| **OUTPUT**[2] | | | | | | | | |
| Voltage | $I_O$ = 5mA, $T_{MIN}$ to $T_{MAX}$ | ±13.5 | ±13.7 | | * | * | | V |
| | $V_S$ = ±11.4V, $R_L$ = 2kΩ | ±10 | ±10.5 | | * | * | | V |
| | $V_S$ = ±2.25V, $R_L$ = 2kΩ | ±1 | ±1.5 | | * | * | | V |
| Load Capacitance Stability | | | 1000 | | | * | | pF |
| Short Circuit Current | | | +20/–15 | | | * | | mA |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Bandwidth, –3dB | G = 1 | | 1 | | | * | | MHz |
| | G = 10 | | 100 | | | * | | kHz |
| | G = 100 | | 10 | | | * | | kHz |
| | G = 1000 | | 1 | | | * | | kHz |
| Slew Rate | $V_O$ = ±10V, G = 10 | 0.3 | 0.6 | | * | * | | V/µs |
| Settling Time, 0.01% | G = 1 | | 18 | | | * | | µs |
| | G = 10 | | 20 | | | * | | µs |
| | G = 100 | | 120 | | | * | | µs |
| | G = 1000 | | 1100 | | | * | | µs |
| Overload Recovery | 50% Overdrive | | 20 | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | |
| Voltage Range | | ±2.25 | ±15 | ±18 | * | * | * | V |
| Current | $V_{IN}$ = 0V | | ±2.2 | ±3 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –40 | | +85 | * | | * | °C |
| Operating | | –40 | | +125 | * | | * | °C |
| $\theta_{JA}$ | | | 80 | | | * | | °C/W |

* Specification same as INA115BU.

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation. (2) Output specifications are for output amplifier, $A_3$. $A_1$ and $A_2$ provide the same output voltage swing but have less output current drive. $A_1$ and $A_2$ can drive external loads of 25kΩ || 200pF.

## PIN CONFIGURATIONS




## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| INA115AU | SOL-16 Surface-Mount | 211 | –40°C to +85°C |
| INA115BU | SOL-16 Surface-Mount | 211 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

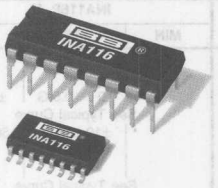
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Input Voltage Range | ±40V |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

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# INA116

www.burr-brown.com/databook/INA116.html

# Ultra Low Input Bias Current INSTRUMENTATION AMPLIFIER



## FEATURES

- LOW INPUT BIAS CURRENT: 3fA typ
- BUFFERED GUARD DRIVE PINS
- LOW OFFSET VOLTAGE: 2mV max
- HIGH COMMON-MODE REJECTION: 84dB (G = 10)
- LOW QUIESCENT CURRENT: 1mA
- INPUT OVER-VOLTAGE PROTECTION: ±40V

## APPLICATIONS

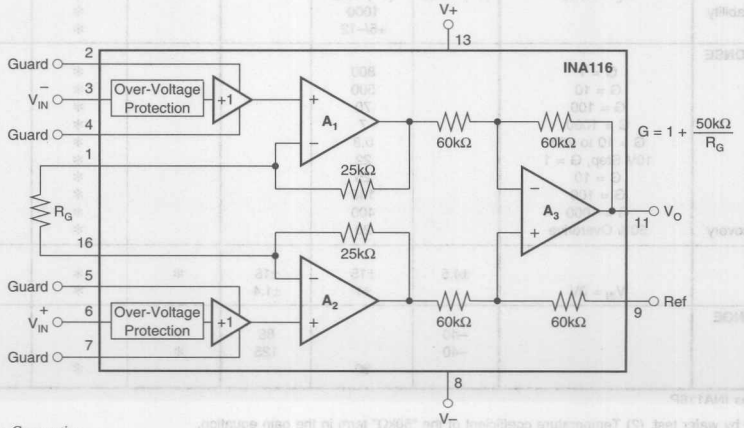
- LABORATORY INSTRUMENTATION
- pH MEASUREMENT
- ION–SPECIFIC PROBES
- LEAKAGE CURRENT MEASUREMENT

## DESCRIPTION

The INA116 is a complete monolithic FET-input instrumentation amplifier with extremely low input bias current. ***Difet***® inputs and special guarding techniques yield input bias currents of 3fA at 25°C, and only 25fA at 85°C. Its 3-op amp topology allows gains to be set from 1 to 1000 by connecting a single external resistor.

Guard pins adjacent to both input connections can be used to drive circuit board and input cable guards to maintain extremely low input bias current.

The INA116 is available in 16-pin plastic DIP and SOL-16 surface-mount packages, specified for the –40°C to +85°C temperature range.




*Difet*®, Burr-Brown Corporation

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

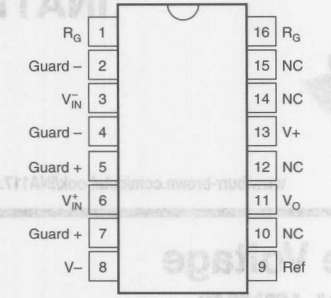
AT $T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 10kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | INA116P, U | | | INA116PA, UA | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT** | | | | | | | | |
| Offset Voltage, RTI | | | | | | | | |
| Initial | $T_A$ = +25°C | | ±0.5 ±0.5/G | ±2 ±2/G | | * | ±5 ±5/G | mV |
| vs Temperature | $T_A = T_{MIN}$ to $T_{MAX}$ | | See Typical Curve | | | * | | |
| vs Power Supply | $V_S$ = ±4.5V to ±18V | | ±10 ±15/G | ±50 ±100/G | | * | ±100 ±200/G | µV/V |
| Long-Term Stability | | | ±1 ±5/G | | | * | | µV/mo |
| Bias Current | | | ±3 | ±25 | | * | ±100 | fA |
| vs Temperature | | | See Typical Curve | | | * | | |
| Offset Current | | | ±1 | ±25 | | * | ±100 | fA |
| vs Temperature | | | See Typical Curve | | | * | | |
| Impedance, Differential | | | $>10^{15}$/0.2 | | | * | | Ω/pF |
| Common-Mode | | | $>10^{15}$/7 | | | * | | Ω/pF |
| Common-Mode Voltage Range | | (V+)–4 | (V+)–2 | | * | * | | V |
| | | (V–)+4 | (V–)+2.4 | | * | * | | V |
| Safe Input Voltage | | ±40 | | | * | | | V |
| Common-Mode Rejection | $V_{CM}$ = ±11V, $\Delta R_S$ = 1kΩ | | | | | | | |
| | G = 1 | 80 | 89 | | 73 | * | | dB |
| | G = 10 | 84 | 92 | | 78 | * | | dB |
| | G = 100 | 86 | 94 | | 80 | * | | dB |
| | $V_{CM}$ = ±5V, G = 1000 | 86 | 94 | | 80 | * | | dB |
| **NOISE** | | | | | | | | |
| Voltage Noise, RTI | G = 1000, $R_S$ = 0Ω | | | | | | | |
| f = 1kHz | | | 28 | | | * | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 2 | | | * | | µVp-p |
| Current Noise | | | | | | | | |
| f = 1kHz | | | 0.1 | | | * | | fA/√Hz |
| **GAIN** | | | | | | | | |
| Gain Equation | | | 1+(50kΩ/$R_G$) | | | * | | V/V |
| Range of Gain | | 1 | | 1000 | * | | * | V/V |
| Gain Error | G = 1 | | ±0.01 | ±0.05 | | * | 0.1 | % |
| | G = 10 | | ±0.25 | ±0.4 | | * | ±0.5 | % |
| | G = 100 | | ±0.35 | ±0.5 | | * | ±0.7 | % |
| | G = 1000 | | ±1.25 | | | * | | % |
| Gain vs Temperature[1] | G = 1 | | ±5 | ±10 | | * | ±20 | ppm/°C |
| 50kΩ Resistance[1][2] | | | ±25 | ±100 | | * | ±100 | ppm/°C |
| Nonlinearity | G = 1 | | ±0.0005 | ±0.005 | | * | ±0.01 | % of FSR |
| | G = 10 | | ±0.001 | ±0.005 | | * | ±0.01 | % of FSR |
| | G = 100 | | ±0.001 | ±0.005 | | * | ±0.01 | % of FSR |
| | G = 1000 | | ±0.005 | | | * | | % of FSR |
| **GUARD OUTPUTS** | | | | | | | | |
| Offset Voltage | | | ±15 | ±50 | | * | * | mV |
| Output Impedance | | | 650 | | | * | | Ω |
| Current Drive | | | +2/–0.05 | | | * | | mA |
| **OUTPUT** | | | | | | | | |
| Voltage Positive | $R_L$ = 10kΩ | (V+) –1 | (V+) –0.7 | | * | * | | V |
| Negative | $R_L$ = 10kΩ | (V–) +0.35 | (V–) +0.2 | | * | * | | V |
| Load Capacitance Stability | | | 1000 | | | * | | pF |
| Short-Circuit Current | | | +5/–12 | | | * | | mA |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Bandwidth, –3dB | G = 1 | | 800 | | | * | | kHz |
| | G = 10 | | 500 | | | * | | kHz |
| | G = 100 | | 70 | | | * | | kHz |
| | G = 1000 | | 7 | | | * | | kHz |
| Slew Rate | G = 10 to 200 | | 0.8 | | | * | | V/µs |
| Settling Time, 0.01% | 10V Step, G = 1 | | 22 | | | * | | µs |
| | G = 10 | | 25 | | | * | | µs |
| | G = 100 | | 145 | | | * | | µs |
| | G = 1000 | | 400 | | | * | | µs |
| Output Overload Recovery | 50% Overdrive | | 20 | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | |
| Voltage Range | | ±4.5 | ±15 | ±18 | * | * | * | V |
| Current | $V_{IN}$ = 0V | | ±1 | ±1.4 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –40 | | 85 | * | | * | °C |
| Operating | | –40 | | 125 | * | | * | °C |
| $\theta_{JA}$ | | | 80 | | | * | | °C/W |

* Specification same as INA116P

NOTE: (1) Guaranteed by wafer test. (2) Temperature coefficient of the "50kΩ" term in the gain equation.

Top View — DIP SOL-16




NC: No Internal Connection.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Input Voltage Range | ±40V |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

## DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

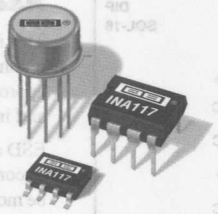
## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| INA116PA | 16-Pin Plastic DIP | 180 |
| INA116P | 16-Pin Plastic DIP | 180 |
| INA116UA | SOL-16 Surface-Mount | 211 |
| INA116U | SOL-16 Surface-Mount | 211 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# INA117

www.burr-brown.com/databook/INA117.html

# High Common-Mode Voltage DIFFERENCE AMPLIFIER

## FEATURES

- COMMON-MODE INPUT RANGE: ±200V ($V_S$ = ±15V)
- PROTECTED INPUTS: ±500V Common-Mode ±500V Differential
- UNITY GAIN: 0.02% Gain Error max
- NONLINEARITY: 0.001% max
- CMRR: 86dB min

## APPLICATIONS

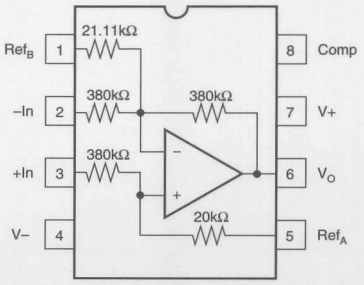
- CURRENT MONITOR
- BATTERY CELL-VOLTAGE MONITOR
- GROUND BREAKER
- INPUT PROTECTION
- SIGNAL ACQUISITION IN NOISY ENVIRONMENTS
- FACTORY AUTOMATION

## DESCRIPTION

The INA117 is a precision unity-gain difference amplifier with very high common-mode input voltage range. It is a single monolithic IC consisting of a precision op amp and integrated thin-film resistor network. It can accurately measure small differential voltages in the presence of common-mode signals up to ±200V. The INA117 inputs are protected from momentary common-mode or differential overloads up to ±500V.

In many applications, where galvanic isolation is not essential, the INA117 can replace isolation amplifiers. This can eliminate costly isolated input-side power supplies and their associated ripple, noise and quiescent current. The INA117's 0.001% nonlinearity and 200kHz bandwidth are superior to those of conventional isolation amplifiers.

The INA117 is available in 8-pin plastic mini-DIP and SO-8 surface-mount packages, specified for the 0°C to +70°C temperature range. The metal TO-99 models are available specified for the –25°C to +85°C and –55°C to +125°C temperature range.




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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

| PARAMETER | CONDITIONS | INA117AM, SM | | | INA117BM | | | INA117P, KU | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **GAIN** | | | | | | | | | | | |
| Initial [1] | | | 1 | | | * | | | * | | V/V |
| Error | | | 0.01 | 0.05 | | * | 0.02 | | * | * | % |
| vs Temperature | | | 2 | 10 | | | * | | * | | ppm/°C |
| Nonlinearity [2] | | | 0.0002 | 0.001 | | * | * | | * | * | % |
| **OUTPUT** | | | | | | | | | | | |
| Rated Voltage | $I_O$ = +20mA, –5mA | 10 | 12 | | * | * | | * | * | | V |
| Rated Current | $V_O$ = 10V | +20, –5 | | | * | | | * | | | mA |
| Impedance | | | 0.01 | | | * | | | * | | Ω |
| Current Limit | To Common | | +49, –13 | | | * | | | * | | mA |
| Capacitive Load | Stable Operation | | 1000 | | | * | | | * | | pF |
| **INPUT** | | | | | | | | | | | |
| Impedance | Differential | | 800 | | | * | | | * | | kΩ |
| | Common-Mode | | 400 | | | * | | | * | | kΩ |
| Voltage Range | Differential | ±10 | | | | * | | | * | | V |
| | Common-Mode, Continuous | ±200 | | | * | | | * | | | V |
| Common-Mode Rejection [3] | | | | | | | | | | | |
| DC | | 70 | 80 | | 86 | 94 | | * | * | | dB |
| AC, 60Hz | $V_{CM}$ = 400Vp-p | 66 | 80 | | 66 | 94 | | * | * | | dB |
| vs Temperature, DC | $T_A = T_{MIN}$ to $T_{MAX}$ | | | | | | | | | | |
| AM, BM, P, KU | | 66 | 75 | | 80 | 90 | | | * | | dB |
| SM | | 60 | 75 | | | | | | | | dB |
| **OFFSET VOLTAGE** | RTO [4] | | | | | | | | | | |
| Initial | | | 120 | 1000 | | * | 1000 | | * | * | µV |
| KU Grade (SO-8 Package) | | | | | | | | | 600 | 2000 | µV |
| vs Temperature | $T_A = T_{MIN}$ to $T_{MAX}$ | | 8.5 | 40 | | * | 20 | | * | | µV/°C |
| vs Supply | $V_S$ = ±5V to ±18V | 74 | 90 | | 80 | * | | * | * | | dB |
| vs Time | | | 200 | | | * | | | * | | µV/mo |
| **OUTPUT NOISE VOLTAGE** | RTO [5] | | | | | | | | | | |
| $f_B$ = 0.01Hz to 10Hz | | | 25 | | | * | | | * | | µVp-p |
| $f_B$ = 10kHz | | | 550 | | | * | | | * | | nV/√Hz |
| **DYNAMIC RESPONSE** | | | | | | | | | | | |
| Gain Bandwidth, –3dB | | | 200 | | | * | | | * | | kHz |
| Full Power Bandwidth | $V_O$ = 20Vp-p | 30 | | | * | | | * | | | kHz |
| Slew Rate | | 2 | 2.6 | | * | * | | * | * | | V/µs |
| Settling Time: 0.1% | $V_O$ = 10V Step | | 6.5 | | | * | | | * | | µs |
| 0.01% | $V_O$ = 10V Step | | 10 | | | * | | | * | | µs |
| 0.01% | $V_{CM}$ = 10V Step, $V_{DIFF}$ = 0V | | 4.5 | | | * | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | | | | |
| Rated | | | ±15 | | | * | | | * | | V |
| Voltage Range | Derated Performance | ±5 | | ±18 | * | | * | * | | * | V |
| Quiescent Current | $V_O$ = 0V | | 1.5 | 2 | * | * | | * | * | | mA |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification: AM, BM, P, KU | | –25 | | +85 | * | | * | 0 | | +70 | °C |
| SM | | –55 | | +125 | | | | | | | °C |
| Operation | | –55 | | +125 | * | | * | –25 | | +85 | °C |
| Storage | | –65 | | +150 | * | | * | –40 | | +85 | °C |

* Specification same as for INA117AM.

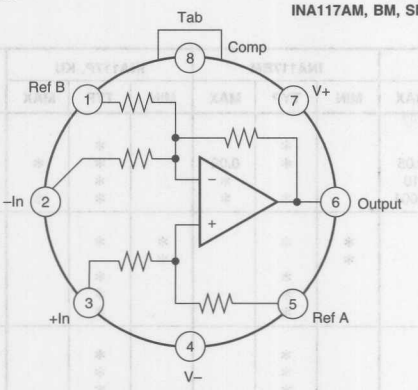
NOTES: (1) Connected as difference amplifier (see Figure 1). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output. (3) With zero source impedance (see discussion of common-mode rejection in Application Information section). (4) Includes effects of amplifier's input bias and offset currents. (5) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.



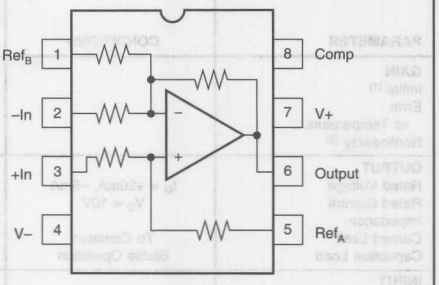
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## PIN CONFIGURATION

**Top View** — **TO-99** — **INA117AM, BM, SM**




**Top View** — **DIP/SOIC** — **INA117P, KU**




Case internally connected to V–. Make no connection.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±22V |
| Input Voltage Range, Continuous | ±200V |
| Common-Mode and Differential, 10s | ±500V |
| Operating Temperature | |
| M Metal TO-99 | –55 to +125°C |
| P Plastic DIP and U SO-8 | –40 to +85°C |
| Storage Temperature | |
| M Package | –65 to +150°C |
| P Plastic DIP and U SO-8 | –40 to +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short Circuit to Common | Continuous |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| INA117P | 8-Pin Plastic DIP | 006 | 0°C to +70°C |
| INA117KU | SO-8 Surface-Mount | 182 | 0°C to +70°C |
| INA117AM | TO-99 Metal | 001 | –25°C to +85°C |
| INA117BM | TO-99 Metal | 001 | –25°C to +85°C |
| INA117SM | TO-99 Metal | 001 | –55°C to +125°C |

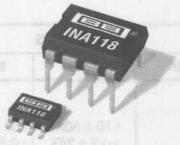
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# INA118

www.burr-brown.com/databook/INA118.html

# Precision, Low Power INSTRUMENTATION AMPLIFIER

## FEATURES

- LOW OFFSET VOLTAGE: 50μV max
- LOW DRIFT: 0.5μV/°C max
- LOW INPUT BIAS CURRENT: 5nA max
- HIGH CMR: 110dB min
- INPUTS PROTECTED TO ±40V
- WIDE SUPPLY RANGE: ±1.35 to ±18V
- LOW QUIESCENT CURRENT: 350μA
- 8-PIN PLASTIC DIP, SO-8

## APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

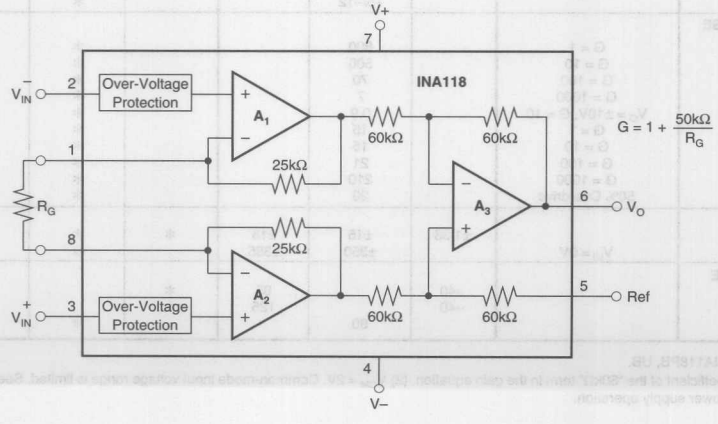
## DESCRIPTION

The INA118 is a low power, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (70kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA118 is laser trimmed for very low offset voltage (50μV), drift (0.5μV/°C) and high common-mode rejection (110dB at G = 1000). It operates with power supplies as low as ±1.35V, and quiescent current is only 350μA—ideal for battery operated systems.

The INA118 is available in 8-pin plastic DIP, and SO-8 surface-mount packages, specified for the –40°C to +85°C temperature range.




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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 10kΩ unless otherwise noted.

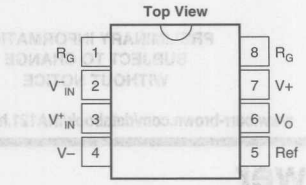
| PARAMETER | CONDITIONS | INA118PB, UB | | | INA118P, U | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT** | | | | | | | | |
| Offset Voltage, RTI | | | | | | | | |
| Initial | $T_A$ = +25°C | | ±10 ± 50/G | ±50 ± 500/G | | ±25 ±100/G | ±125±1000/G | µV |
| vs Temperature | $T_A = T_{MIN}$ to $T_{MAX}$ | | ±0.2 ± 2/G | ±0.5 ± 20/G | | ±0.2 ± 5/G | ±1 ± 20/G | µV/°C |
| vs Power Supply | $V_S$ = ±1.35V to ±18V | | ±1 ±10/G | ±5 ± 100/G | | * | ±10 ±100/G | µV/V |
| Long-Term Stability | | | ±0.4 ±5/G | | | * | | µV/mo |
| Impedance, Differential | | | $10^{10}$ \|\| 1 | | | * | | Ω \|\| pF |
| Common-Mode | | | $10^{10}$ \|\| 4 | | | * | | Ω \|\| pF |
| Linear Input Voltage Range | | (V+) – 1 | (V+) – 0.65 | | * | * | | V |
| | | (V–) + 1.1 | (V–) + 0.95 | | * | * | | V |
| Safe Input Voltage | | | | ±40 | | | * | V |
| Common-Mode Rejection | $V_{CM}$ = ±10V, $\Delta R_S$ = 1kΩ | | | | | | | |
| | G = 1 | 80 | 90 | | 73 | * | | dB |
| | G = 10 | 97 | 110 | | 89 | * | | dB |
| | G = 100 | 107 | 120 | | 98 | * | | dB |
| | G = 1000 | 110 | 125 | | 100 | * | | dB |
| **BIAS CURRENT** | | | ±1 | ±5 | | * | ±10 | nA |
| vs Temperature | | | ±40 | | | * | | pA/°C |
| **OFFSET CURRENT** | | | ±1 | ±5 | | * | ±10 | nA |
| vs Temperature | | | ±40 | | | * | | pA/°C |
| **NOISE VOLTAGE, RTI** | G = 1000, $R_S$ = 0Ω | | | | | | | |
| f = 10Hz | | | 11 | | | * | | nV/√Hz |
| f = 100Hz | | | 10 | | | * | | nV/√Hz |
| f = 1kHz | | | 10 | | | * | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 0.28 | | | * | | µVp-p |
| Noise Current | | | | | | | | |
| f=10Hz | | | 2.0 | | | * | | pA/√Hz |
| f=1kHz | | | 0.3 | | | * | | pA/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 80 | | | * | | pAp-p |
| **GAIN** | | | | | | | | |
| Gain Equation | | | 1 + (50kΩ/$R_G$) | | | * | | V/V |
| Range of Gain | | 1 | | 10000 | * | | * | V/V |
| Gain Error | G = 1 | | ±0.01 | ±0.024 | | * | ±0.1 | % |
| | G = 10 | | ±0.02 | ±0.4 | | * | ±0.5 | % |
| | G = 100 | | ±0.05 | ±0.5 | | * | ±0.7 | % |
| | G = 1000 | | ±0.5 | ±1 | | * | ±2 | % |
| Gain vs Temperature | G = 1 | | ±1 | ±10 | | * | ±10 | ppm/°C |
| 50kΩ Resistance[1] | | | ±25 | ±100 | | * | * | ppm/°C |
| Nonlinearity | G = 1 | | ±0.0003 | ±0.001 | | * | ±0.002 | % of FSR |
| | G = 10 | | ±0.0005 | ±0.002 | | * | ±0.004 | % of FSR |
| | G = 100 | | ±0.0005 | ±0.002 | | * | ±0.004 | % of FSR |
| | G = 1000 | | ±0.002 | ±0.01 | | * | ±0.02 | % of FSR |
| **OUTPUT** | | | | | | | | |
| Voltage: Positive | $R_L$ = 10kΩ | (V+) – 1 | (V+) – 0.8 | | * | * | | V |
| Negative | $R_L$ = 10kΩ | (V–) + 0.35 | (V–) + 0.2 | | * | * | | V |
| Single Supply High | $V_S$ = +2.7V/0V[2], $R_L$ = 10kΩ | 1.8 | 2.0 | | * | * | | V |
| Single Supply Low | $V_S$ = +2.7V/0V[2], $R_L$ = 10kΩ | 60 | 35 | | * | * | | mV |
| Load Capacitance Stability | | | 1000 | | | * | | pF |
| Short Circuit Current | | | +5/–12 | | | * | | mA |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Bandwidth, –3dB | G = 1 | | 800 | | | * | | kHz |
| | G = 10 | | 500 | | | * | | kHz |
| | G = 100 | | 70 | | | * | | kHz |
| | G = 1000 | | 7 | | | * | | kHz |
| Slew Rate | $V_O$ = ±10V, G = 10 | | 0.9 | | | * | | V/µs |
| Settling Time, 0.01% | G = 1 | | 15 | | | * | | µs |
| | G = 10 | | 15 | | | * | | µs |
| | G = 100 | | 21 | | | * | | µs |
| | G = 1000 | | 210 | | | * | | µs |
| Overload Recovery | 50% Overdrive | | 20 | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | |
| Voltage Range | | ±1.35 | ±15 | ±18 | * | * | * | V |
| Current | $V_{IN}$ = 0V | | ±350 | ±385 | | * | * | µA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –40 | | 85 | * | | * | °C |
| Operating | | –40 | | 125 | * | | * | °C |
| $\theta_{JA}$ | | | 80 | | | * | | °C/W |

* Specification same as INA118PB, UB.

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation. (2) $V_{CM}$ = 2V. Common-mode input voltage range is limited. See text for discussion of low power supply and single power supply operation.

## PIN CONFIGURATION

8-Pin DIP and SO-8




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

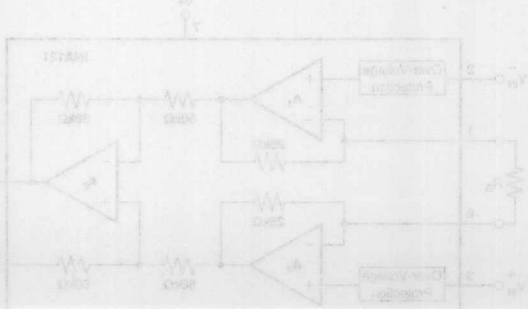
| | |
|---|---|
| Supply Voltage | ±18V |
| Analog Input Voltage Range | ±40V |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

## ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| INA118P | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| INA118PB | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| INA118U | SO-8 Surface-Mount | 182 | –40°C to +85°C |
| INA118UB | SO-8 Surface-Mount | 182 | –40°C to +85°C |

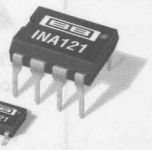
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.





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# INA121

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www.burr-brown.com/databook/INA121.html

# FET-Input, Low Power INSTRUMENTATION AMPLIFIER

## FEATURES

- LOW BIAS CURRENT: 2pA
- LOW QUIESCENT CURRENT: ±450µA
- LOW OFFSET VOLTAGE: ±100µV
- LOW OFFSET DRIFT: +2µV/°C
- LOW NOISE: 20nV/√Hz at f = 1kHz (G =1000)
- HIGH CMR: 120dB
- WIDE SUPPLY RANGE: ±2.25V to ±18V
- LOW NONLINEARITY ERROR: 0.001% max
- INPUT PROTECTION TO ±40V
- 8-PIN DIP AND SO-8 SURFACE MOUNT

## APPLICATIONS

- LOW-LEVEL TRANSDUCER AMPLIFIER
  Bridge, RTD, Thermocouple
- PHYSIOLOGICAL AMPLIFIER
  ECG, EEG, EMG, Respiratory
- HIGH IMPEDANCE TRANSDUCERS
- MULTI-CHANNEL DATA ACQUISITION
- PORTABLE, BATTERY OPERATED SYSTEMS
- GENERAL PURPOSE INSTRUMENTATION

## DESCRIPTION

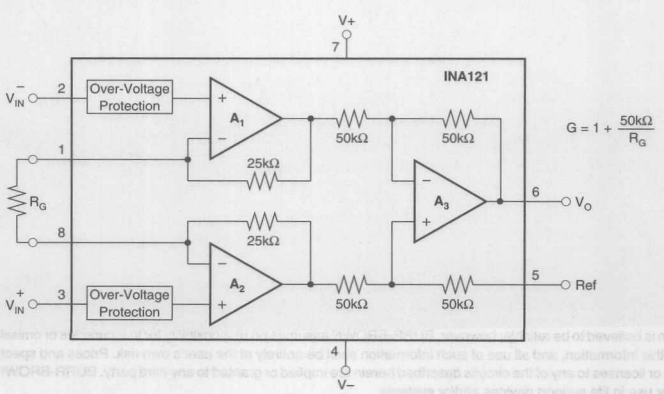
The INA121 is a FET-input, low power instrumentation amplifier offering excellent accuracy. Its versatile three-op amp design and very small size make it ideal for a variety of general purpose applications. Low bias current (2pA) allows use with high impedance sources.

Gain can be set from 1V to 10000V/V with a single external resistor. Internal input protection can withstand up to ±40V without damage.

The INA121 is laser-trimmed for very low offset voltage (±100µV), low offset drift (+2µV/°C), and high common-mode rejection (120dB at G = 1000). It operates on power supplies as low as ±2.25V (+4.5V), allowing use in battery operated and single 5V systems. Quiescent current is only 450µA.

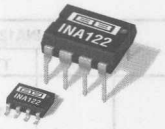
Package options include 8-pin plastic DIP and SO-8 surface mount. All are specified for the –40°C to +85°C industrial temperature range.

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# INA122

www.burr-brown.com/databook/INA122.html

# Single Supply, *Micro*Power INSTRUMENTATION AMPLIFIER

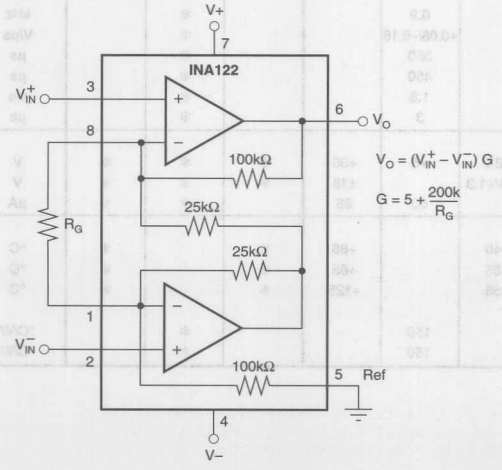


## FEATURES

- LOW QUIESCENT CURRENT: 60µA
- WIDE POWER SUPPLY RANGE
  Single Supply: 2.2V to 36V
  Dual Supply: –0.9/+1.3V to ±18V
- COMMON-MODE RANGE TO (V–)–0.1V
- RAIL-TO-RAIL OUTPUT SWING
- LOW OFFSET VOLTAGE: 250µV max
- LOW OFFSET DRIFT: 3µV/°C max
- LOW NOISE: 60nV/√Hz
- LOW INPUT BIAS CURRENT: 25nA max
- 8-PIN DIP AND SO-8 SURFACE-MOUNT

## APPLICATIONS

- PORTABLE, BATTERY OPERATED SYSTEMS
- INDUSTRIAL SENSOR AMPLIFIER:
  Bridge, RTD, Thermocouple
- PHYSIOLOGICAL AMPLIFIER:
  ECG, EEG, EMG
- MULTI-CHANNEL DATA ACQUISITION




## DESCRIPTION

The INA122 is a precision instrumentation amplifier for accurate, low noise differential signal acquisition. Its two-op-amp design provides excellent performance with very low quiescent current, and is ideal for portable instrumentation and data acquisition systems.

The INA122 can be operated with single power supplies from 2.2V to 36V and quiescent current is a mere 60µA. It can also be operated from dual supplies. By utilizing an input level-shift network, input common-mode range extends to 0.1V below negative rail (single supply ground).

A single external resistor sets gain from 5V/V to 10000V/V. Laser trimming provides very low offset voltage (250µV max), offset voltage drift (3µV/°C max) and excellent common-mode rejection.

Package options include 8-pin plastic DIP and SO-8 surface-mount packages. Both are specified for the –40°C to +85°C extended industrial temperature range.

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

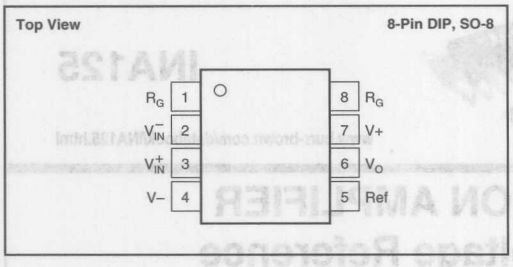
At $T_A$ = +25°C, $V_S$ = +5V, $R_L$ = 20kΩ connected to $V_S$/2, unless otherwise noted.

| PARAMETER | CONDITIONS | INA122P, U | | | INA122PA, UA | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT** | | | | | | | | |
| Offset Voltage, RTI | | | ±100 | ±250 | | ±150 | ±500 | µV |
| vs Temperature | | | ±1 | ±3 | | * | ±5 | µV/°C |
| vs Power Supply (PSRR) | $V_S$ = +2.2V to +36V | | 10 | 30 | | * | 100 | µV/V |
| Input Impedance | | | $10^{10}$ ‖ 3 | | | * | | Ω ‖ pF |
| Safe Input Voltage | $R_S$ = 0 | (V–)–0.3 | | (V+)+0.3 | * | | * | V |
| | $R_S$ = 10kΩ | (V–)–40 | | (V+)+40 | * | | * | V |
| Common-Mode Voltage Range | | 0 | | 3.4 | * | | * | V |
| Common-Mode Rejection | $V_{CM}$ = 0V to 3.4V | 83 | 96 | | 76 | 90 | | dB |
| **INPUT BIAS CURRENT** | | | –10 | –25 | | * | –50 | nA |
| vs Temperature | | | ±40 | | | * | | pA/°C |
| Offset Current | | | ±1 | ±2 | | * | ±5 | nA |
| vs Temperature | | | ±40 | | | * | | pA/°C |
| **GAIN** | | | G = 5 to 10k | | | * | | V/V |
| Gain Equation | | | G = 5 + 200kΩ/$R_G$ | | | * | | V/V |
| Gain Error | G = 5 | | ±0.05 | ±0.1 | | * | ±0.15 | % |
| vs Temperature | G = 5 | | 5 | 10 | | * | * | ppm/°C |
| Gain Error | G = 100 | | ±0.3 | ±0.5 | | * | ±1 | % |
| vs Temperature | G = 100 | | ±25 | ±100 | | * | * | ppm/°C |
| Nonlinearity | G = 100, $V_O$ = –14.85V to +14.9V | | ±0.005 | ±0.012 | | * | ±0.024 | % |
| **NOISE (RTI)** | | | | | | | | |
| Voltage Noise, f = 1kHz | | | 60 | | | * | | nV/√Hz |
| f = 100Hz | | | 100 | | | * | | nV/√Hz |
| f = 10Hz | | | 110 | | | * | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 2 | | | * | | µVp-p |
| Current Noise, f = 1kHz | | | 80 | | | * | | fA/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 2 | | | * | | pAp-p |
| **OUTPUT** | | | | | | | | |
| Voltage, Positive | $V_S$ = ±15V | (V+)–0.1 | (V+)–0.05 | | * | * | | V |
| Negative | $V_S$ = ±15V | (V–)+0.15 | (V–)+0.1 | | * | * | | V |
| Short-Circuit Current | Short-Circuit to Ground | | +3/–30 | | | * | | mA |
| Capacitive Load Drive | | | 1 | | | * | | nF |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Bandwidth, –3dB | G = 5 | | 120 | | | * | | kHz |
| | G = 100 | | 5 | | | * | | kHz |
| | G = 500 | | 0.9 | | | * | | kHz |
| Slew Rate | | | +0.08/–0.16 | | | * | | V/µs |
| Settling Time, 0.01% | G = 5 | | 350 | | | * | | µs |
| | G = 100 | | 450 | | | * | | µs |
| | G = 500 | | 1.8 | | | * | | ms |
| Overload Recovery | 50% Input Overload | | 3 | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | |
| Voltage Range, Single Supply | | +2.2 | +5 | +36 | * | * | * | V |
| Dual Supplies | | –0.9/+1.3 | | ±18 | * | * | * | V |
| Current | $I_O$ = 0 | | 60 | 85 | | * | * | µA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –40 | | +85 | * | | * | °C |
| Operation | | –55 | | +85 | * | | * | °C |
| Storage | | –55 | | +125 | * | | * | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| 8-Pin DIP | | | 150 | | | * | | °C/W |
| SO-8 Surface-Mount | | | 150 | | | * | | °C/W |

* Specification same as INA122P, INA122U.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN CONFIGURATION




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Supply Voltage, V+ to V– | 36V |
| Signal Input Terminals, Voltage[2] | (V–)–0.3V to (V+)+0.3V |
| Current[2] | 5mA |
| Output Short Circuit | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |

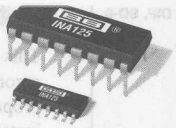
NOTES: (1) Stresses above these ratings may cause permanent damage. (2) Input terminals are internally diode-clamped to the power supply rails. Input signals that can exceed the supply rails by more than 0.3V should be current-limited to 5mA or less.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| INA122PA | 8-Pin DIP | 006 |
| INA122P | 8-Pin DIP | 006 |
| INA122UA | SO-8 Surface Mount | 182 |
| INA122U | SO-8 Surface Mount | 182 |

NOTE: (1) For detailed drawing and dimension table, see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# INA125

www.burr-brown.com/databook/INA125.html

# INSTRUMENTATION AMPLIFIER
## With Precision Voltage Reference

## FEATURES

- LOW QUIESCENT CURRENT: 460µA
- PRECISION VOLTAGE REFERENCE: 1.24V, 2.5V, 5V or 10V
- SLEEP MODE
- LOW OFFSET VOLTAGE: 250µV max
- LOW OFFSET DRIFT: 2µV/°C max
- LOW INPUT BIAS CURRENT: 20nA max
- HIGH CMR: 100dB min
- LOW NOISE: 38nV/√Hz at f = 1kHz
- INPUT PROTECTION TO ±40V
- WIDE SUPPLY RANGE
  Single Supply: 2.7V to 36V
  Dual Supply: ±1.35V to ±18V
- 16-PIN DIP AND SO-16 SOIC PACKAGES

## APPLICATIONS

- PRESSURE AND TEMPERATURE BRIDGE AMPLIFIERS
- INDUSTRIAL PROCESS CONTROL
- FACTORY AUTOMATION
- MULTI-CHANNEL DATA ACQUISITION
- BATTERY OPERATED SYSTEMS
- GENERAL PURPOSE INSTRUMENTATION

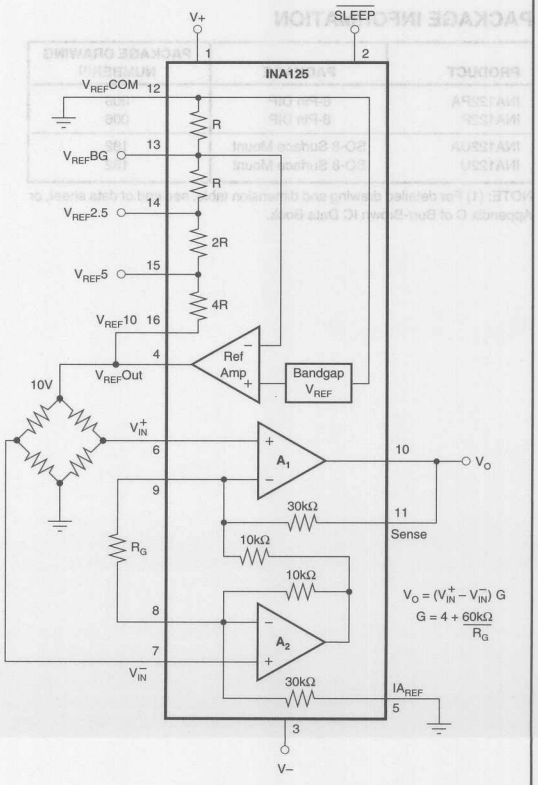
## DESCRIPTION

The INA125 is a low power, high accuracy instrumentation amplifier with a precision voltage reference. It provides complete bridge excitation and precision differential-input amplification on a single integrated circuit.

A single external resistor sets any gain from 4 to 10,000. The INA125 is laser-trimmed for low offset voltage (250µV), low offset drift (2µV/°C), and high common-mode rejection (100dB at G = 100). It operates on single (+2.7V to +36V) or dual (±1.35V to ±18V) supplies.

The voltage reference is externally adjustable with pin-selectable voltages of 2.5V, 5V, or 10V, allowing use with a variety of transducers. The reference voltage is accurate to ±0.5% (max) with ±35ppm/°C drift (max). Sleep mode allows shutdown and duty cycle operation to save power.

The INA125 is available in 16-pin plastic DIP and SO-16 surface-mount packages and is specified for the –40°C to +85°C industrial temperature range.




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# SPECIFICATIONS: $V_S = \pm 15V$

At $T_A = +25°C$, $V_S = \pm 15V$, IA common = 0V, $V_{REF}$ common = 0V, and $R_L = 10k\Omega$, unless otherwise noted.

| PARAMETER | CONDITIONS | INA125P, U MIN | INA125P, U TYP | INA125P, U MAX | INA125PA, UA MIN | INA125PA, UA TYP | INA125PA, UA MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | | |
| Offset Voltage, RTI | | | | | | | | |
| Initial | | | ±50 | ±250 | | * | ±500 | µV |
| vs Temperature | | | ±0.25 | ±2 | | * | ±5 | µV/°C |
| vs Power Supply | $V_S$ = ±1.35V to ±18V, G = 4 | | ±3 | ±20 | | * | ±50 | µV/V |
| Long-Term Stability | | | ±0.2 | | | * | | µV/mo |
| Impedance, Differential | | | $10^{11}$ \|\| 2 | | | * | | Ω \|\| pF |
| Common-Mode | | | $10^{11}$ \|\| 9 | | | * | | Ω \|\| pF |
| Safe Input Voltage | | | | ±40 | | | * | V |
| Input Voltage Range | | | See Text | | | * | | |
| Common-Mode Rejection | $V_{CM}$ = −10.7V to +10.2V | | | | | | | |
| | G = 4 | 78 | 84 | | 72 | * | | dB |
| | G = 10 | 86 | 94 | | 80 | * | | dB |
| | G = 100 | 100 | 114 | | 90 | * | | dB |
| | G = 500 | 100 | 114 | | 90 | * | | dB |
| **BIAS CURRENT** | $V_{CM}$ = 0V | | 10 | 25 | | * | 50 | nA |
| vs Temperature | | | ±60 | | | * | | pA/°C |
| Offset Current | | | ±0.5 | ±2.5 | | * | ±5 | nA |
| vs Temperature | | | ±0.5 | | | * | | pA/°C |
| **NOISE, RTI** | $R_S = 0\Omega$ | | | | | | | |
| Voltage Noise, f = 10Hz | | | 40 | | | * | | nV/√Hz |
| f = 100Hz | | | 38 | | | * | | nV/√Hz |
| f = 1kHz | | | 38 | | | * | | nV/√Hz |
| f = 0.1Hz to 10Hz | | | 0.8 | | | * | | µVp-p |
| Current Noise, f = 10Hz | | | 170 | | | * | | fA/√Hz |
| f = 1kHz | | | 56 | | | * | | fA/√Hz |
| f = 0.1Hz to 10Hz | | | 5 | | | * | | pAp-p |
| **GAIN** | | | | | | | | |
| Gain Equation | | | 4 + 60kΩ/$R_G$ | | | * | | V/V |
| Range of Gain | | 4 | | 10,000 | * | | * | V/V |
| Gain Error | $V_O$ = −14V to +13.3V | | | | | | | |
| | G = 4 | | ±0.01 | ±0.075 | | * | ±0.1 | % |
| | G = 10 | | ±0.03 | ±0.3 | | * | ±0.5 | % |
| | G = 100 | | ±0.05 | ±0.5 | | * | ±1 | % |
| | G = 500 | | ±0.1 | | | * | | % |
| Gain vs Temperature | | | | | | | | |
| | G = 4 | | ±1 | ±15 | | * | * | ppm/°C |
| | G > 4[1] | | ±25 | ±100 | | * | * | ppm/°C |
| Nonlinearity | $V_O$ = −14V to +13.3V | | | | | | | |
| | G = 4 | | ±0.0004 | ±0.002 | | * | ±0.004 | % of FS |
| | G = 10 | | ±0.0004 | ±0.002 | | * | ±0.004 | % of FS |
| | G = 100 | | ±0.001 | ±0.01 | | * | * | % of FS |
| | G = 500 | | ±0.002 | | | * | | % of FS |
| **OUTPUT** | | | | | | | | |
| Voltage: Positive | | (V+)–1.7 | (V+)–0.9 | | * | * | | V |
| Negative | | (V–)+1 | (V–)+0.4 | | * | * | | V |
| Load Capacitance Stability | | | 1000 | | | * | | pF |
| Short-Circuit Current | | | –9/+12 | | | * | | mA |
| **VOLTAGE REFERENCE** | $V_{REF}$ = +2.5V, +5V, +10V | | | | | | | |
| Accuracy | $I_L = 0$ | | ±0.15 | ±0.5 | | * | ±1 | % |
| vs Temperature | $I_L = 0$ | | ±18 | ±35 | | * | ±100 | ppm/°C |
| vs Power Supply, V+ | V+ = ($V_{REF}$ + 1.25V) to +36V | | ±20 | ±50 | | * | ±100 | ppm/V |
| vs Load | $I_L$ = 0 to 5mA | | 3 | 75 | | * | * | ppm/mA |
| Dropout Voltage, (V+) – $V_{REF}$[2] | Ref Load = 2kΩ | 1.25 | 1 | | * | * | | V |
| Bandgap Voltage Reference | | | 1.24 | | | * | | V |
| Accuracy | $I_L = 0$ | | ±0.5 | | | * | | % |
| vs Temperature | $I_L = 0$ | | ±18 | | | * | | ppm/°C |



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## SPECIFICATIONS: $V_S$ = ±15V (CONT)

At $T_A$ = +25°C, $V_S$ = ±15V, IA common = 0V, $V_{REF}$ common = 0V, and $R_L$ = 10kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | INA125P, U | | | INA125PA, UA | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Bandwidth, –3dB | G = 4 | | 150 | | | * | | kHz |
| | G = 10 | | 45 | | | * | | kHz |
| | G = 100 | | 4.5 | | | * | | kHz |
| | G = 500 | | 0.9 | | | * | | kHz |
| Slew Rate | G = 4, 10V Step | | 0.2 | | | * | | V/µs |
| Settling Time, 0.01% | G = 4, 10V Step | | 60 | | | * | | µs |
| | G = 10, 10V Step | | 83 | | | * | | µs |
| | G = 100, 10V Step | | 375 | | | * | | µs |
| | G = 500, 10V Step | | 1700 | | | * | | µs |
| Overload Recovery | 50% Overdrive | | 5 | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | | ±15 | | | * | | V |
| Specified Voltage Range | | ±1.35 | | ±18 | * | | * | V |
| Quiescent Current, Positive | $I_O = I_{REF}$ = 0mA | | 460 | 525 | | * | * | µA |
| Negative | $I_O = I_{REF}$ = 0mA | | –280 | –325 | | * | * | µA |
| Reference Ground Current[3] | | | 180 | | | * | | µA |
| Sleep Current ($V_{SLEEP} \leq$ 100mV) | $R_L$ = 10kΩ, Ref Load = 2kΩ | | ±1 | ±25 | | * | * | µA |
| **SLEEP MODE PIN[4]** | | | | | | | | |
| $V_{IH}$ (Logic high input voltage) | | +2.7 | | V+ | * | | * | V |
| $V_{IL}$ (Logic low input voltage) | | 0 | | +0.1 | * | | * | V |
| $I_{IH}$ (Logic high input current) | | | 15 | | | * | | µA |
| $I_{IL}$ (Logic low input current) | | | 0 | | | * | | µA |
| Wake-up Time[5] | | | 150 | | | * | | µs |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification Range | | –40 | | +85 | * | | * | °C |
| Operation Range | | –55 | | +125 | * | | * | °C |
| Storage Range | | –55 | | +125 | * | | * | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| 16-Pin DIP | | | 80 | | | * | | °C/W |
| SO-16 Surface-Mount | | | 100 | | | * | | °C/W |

* Specification same as INA125P, U.

NOTES: (1) Temperature coefficient of the "Internal Resistor" in the gain equation. Does not include TCR of gain-setting resistor, $R_G$. (2) Dropout voltage is the positive supply voltage minus the reference voltage that produces a 1% decrease in reference voltage. (3) $V_{REF}$COM pin. (4) Voltage measured with respect to Reference Common. Logic low input selects Sleep mode. (5) IA and Reference, see Typical Performance Curves.

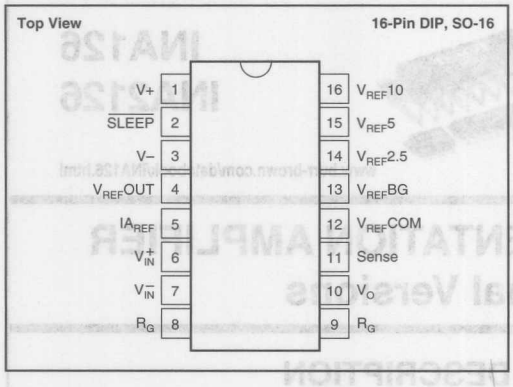
## SPECIFICATIONS: $V_S$ = +5V

At $T_A$ = +25°C, $V_S$ = +5V, IA common at $V_S$/2, $V_{REF}$ common = $V_S$/2, $V_{CM}$ = $V_S$/2, and $R_L$ = 10kΩ to $V_S$/2, unless otherwise noted.

| PARAMETER | CONDITIONS | INA125P, U | | | INA125PA, UA | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT** | | | | | | | | |
| Offset Voltage, RTI | | | | | | | | |
| Initial | | | ±75 | ±500 | | * | ±750 | µV |
| vs Temperature | | | ±0.25 | | | * | | µV/°C |
| vs Power Supply | $V_S$ = +2.7V to +36V | | 3 | 20 | | * | 50 | µV/V |
| Input Voltage Range | | | See Text | | | * | | |
| Common-Mode Rejection | $V_{CM}$ = +1.1V to +3.6V | | | | | | | |
| | G = 4 | 78 | 84 | | 72 | * | | dB |
| | G = 10 | 86 | 94 | | 80 | * | | dB |
| | G = 100 | 100 | 114 | | 90 | * | | dB |
| | G = 500 | 100 | 114 | | 90 | * | | dB |
| **GAIN** | | | | | | | | |
| Gain Error | $V_O$ = +0.3V to +3.8V | | | | | | | |
| | G = 4 | | ±0.01 | | | * | | % |
| **OUTPUT** | | | | | | | | |
| Voltage, Positive | | (V+)–1.2 | (V+)–0.8 | | * | * | | V |
| Negative | | (V–)+0.3 | (V–)+0.15 | | * | * | | V |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | | +5 | | | * | | V |
| Operating Voltage Range | | +2.7 | | +36 | * | | * | V |
| Quiescent Current | $I_O = I_{REF}$ = 0mA | | 460 | 525 | | * | * | µA |
| Sleep Current ($V_{SLEEP} \leq$ 100mV) | $R_L$ = 10kΩ, Ref Load = 2kΩ | | ±1 | ±25 | | * | * | µA |

* Specification same as INA125P, U.

## PIN CONFIGURATION




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|---|
| Power Supply Voltage, V+ to V– | 36V |
| Input Signal Voltage | ±40V |
| Output Short Circuit | Continuous |
| Operating Temperature | –55°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |

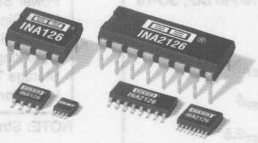
NOTE: Stresses above these ratings may cause permanent damage.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| INA125PA | 16-Pin Plastic DIP | 180 |
| INA125P | 16-Pin Plastic DIP | 180 |
| INA125UA | SO-16 Surface-Mount | 265 |
| INA125U | SO-16 Surface-Mount | 265 |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# INA126
# INA2126

www.burr-brown.com/databook/INA126.html

# *Micro*POWER INSTRUMENTATION AMPLIFIER
## Single and Dual Versions

## FEATURES

- LOW QUIESCENT CURRENT: 175µA/chan.
- WIDE SUPPLY RANGE: ±1.35V to ±18V
- LOW OFFSET VOLTAGE: 250µV max
- LOW OFFSET DRIFT: 3µV/°C max
- LOW NOISE: 35nV/√Hz
- LOW INPUT BIAS CURRENT: 25nA max
- 8-PIN DIP, SO-8, MSOP-8 SURFACE- MOUNT
  DUAL: 16-Pin DIP, SO-16, SSOP-16

## APPLICATIONS

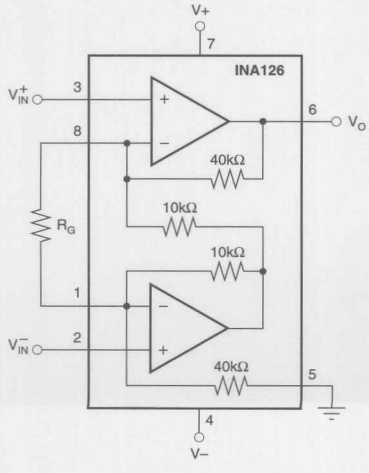
- INDUSTRIAL SENSOR AMPLIFIER:
  Bridge, RTD, Thermocouple
- PHYSIOLOGICAL AMPLIFIER:
  ECG, EEG, EMG
- MULTI-CHANNEL DATA ACQUISITION
- PORTABLE, BATTERY OPERATED SYSTEMS

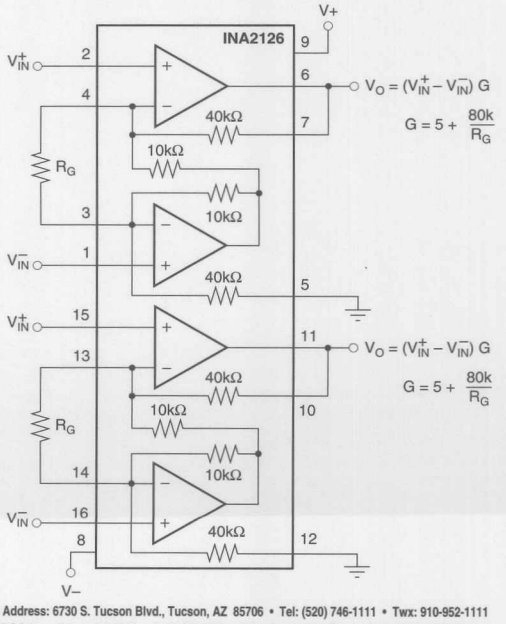
## DESCRIPTION

The INA126 and INA2126 are precision instrumentation amplifiers for accurate, low noise differential signal acquisition. Their two-op-amp design provides excellent performance with very low quiescent current (175µA/chan.). This, combined with wide operating voltage range of ±1.35V to ±18V, makes them ideal for portable instrumentation and data acquisition systems.

Gain can be set from 5V/V to 10000V/V with a single external resistor. Laser trimmed input circuitry provides low offset voltage (250µV max), low offset voltage drift (3µV/°C max) and excellent common-mode rejection.

Single version package options include 8-pin plastic DIP, SO-8 surface mount, and fine-pitch MSOP-8 surface-mount. Dual version is available in the space-saving SSOP-16 fine-pitch surface mount, SO-16, and 16-pin DIP. All are specified for the –40°C to +85°C industrial temperature range.




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# SPECIFICATIONS

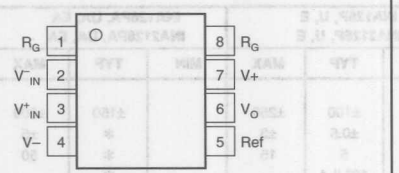
At $T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 25kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | INA126P, U, E INA2126P, U, E MIN | TYP | MAX | INA126PA, UA, EA INA2126PA, UA, EA MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | | |
| Offset Voltage, RTI | | | ±100 | ±250 | | ±150 | ±500 | µV |
| vs Temperature | | | ±0.5 | ±3 | | * | ±5 | µV/°C |
| vs Power Supply (PSRR) | $V_S$ = ±1.35V to ±18V | | 5 | 15 | | * | 50 | µV/V |
| Input Impedance | | | $10^9$ ‖ 4 | | | * | | Ω ‖ pF |
| Safe Input Voltage | $R_S$ = 0 | (V–)–0.5 | | (V+)+0.5 | * | | * | V |
| | $R_S$ = 1kΩ | (V–)–10 | | (V+)+10 | * | | * | V |
| Common-Mode Voltage Range | $V_O$ = 0V | ±11.25 | ±11.5 | | * | * | | V |
| Channel Separation (dual) | G = 5, dc | | 130 | | | | | dB |
| Common-Mode Rejection | $R_S$ = 0, $V_{CM}$ = ±11.25V | 83 | 94 | | 74 | 90 | | dB |
| INA2126U (dual SO-16) | | 80 | 94 | | | | | dB |
| **INPUT BIAS CURRENT** | | | –10 | –25 | | * | –50 | nA |
| vs Temperature | | | ±30 | | | * | | pA/°C |
| Offset Current | | | ±0.5 | ±2 | | * | ±5 | nA |
| vs Temperature | | | ±10 | | | * | | pA/°C |
| **GAIN** | G = 5 to 10k | | | | | * | | V/V |
| Gain Equation | G = 5 + 80kΩ/$R_G$ | | | | | * | | V/V |
| Gain Error | $V_O$ = ±14V, G = 5 | | ±0.02 | ±0.1 | | * | ±0.18 | % |
| vs Temperature | G = 5 | | ±2 | ±10 | | * | * | ppm/°C |
| Gain Error | $V_O$ = ±12V, G = 100 | | ±0.2 | ±0.5 | | * | ±1 | % |
| vs Temperature | G = 100 | | ±25 | ±100 | | * | * | ppm/°C |
| Nonlinearity | G = 100, $V_O$ = ±14V | | ±0.002 | ±0.012 | | * | * | % |
| **NOISE** | | | | | | | | |
| Voltage Noise, f = 1kHz | | | 35 | | | * | | nV/√Hz |
| f = 100Hz | | | 35 | | | * | | nV/√Hz |
| f = 10Hz | | | 45 | | | * | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 0.7 | | | * | | µVp-p |
| Current Noise, f = 1kHz | | | 60 | | | * | | fA/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 2 | | | * | | pAp-p |
| **OUTPUT** | | | | | | | | |
| Voltage, Positive | $R_L$ = 25kΩ | (V+)–0.9 | (V+)–0.75 | | * | * | | V |
| Negative | $R_L$ = 25kΩ | (V–)+0.95 | (V–)+0.8 | | * | * | | V |
| Short-Circuit Current | Short-Circuit to Ground | | +10/–5 | | | * | | mA |
| Capacitive Load Drive | | | 1000 | | | * | | pF |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Bandwidth, –3dB | G = 5 | | 200 | | | * | | kHz |
| | G = 100 | | 9 | | | * | | kHz |
| | G = 500 | | 1.8 | | | * | | kHz |
| Slew Rate | $V_O$ = ±10V, G = 5 | | 0.4 | | | * | | V/µs |
| Settling Time, 0.01% | 10V Step, G = 5 | | 30 | | | * | | µs |
| | 10V Step, G = 100 | | 160 | | | * | | µs |
| | 10V Step, G = 500 | | 1500 | | | * | | µs |
| Overload Recovery | 50% Input Overload | | 4 | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | |
| Voltage Range | | ±1.35 | ±15 | ±18 | * | * | * | V |
| Current (per channel) | $I_O$ = 0 | | ±175 | ±200 | | * | * | µA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification Range | | –40 | | +85 | * | | * | °C |
| Operation Range | | –55 | | +125 | * | | * | °C |
| Storage Range | | –55 | | +125 | * | | * | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| 8-Pin DIP | | | 100 | | | * | | °C/W |
| SO-8 Surface-Mount | | | 150 | | | * | | °C/W |
| MSOP-8 Surface-Mount | | | 200 | | | * | | °C/W |
| 16-Pin DIP (dual) | | | 80 | | | * | | °C/W |
| SO-16 (dual) | | | 100 | | | * | | °C/W |
| SSOP-16 (dual) | | | 100 | | | * | | °C/W |

* Specification same as INA126P, INA126U, INA126E; INA2126P, INA2126U, INA2126E.

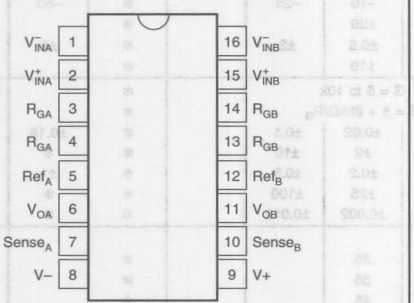
## PIN CONFIGURATION (Single)

Top View — 8-Pin DIP, SO-8, MSOP-8




## PIN CONFIGURATION (Dual)

Top View — 16-Pin DIP, SO-16, SSOP-16




## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Power Supply Voltage, V+ to V– | 36V |
| Input Signal Voltage[2] | (V–)–0.7 to (V+)+0.7V |
| Input Signal Current[2] | 10mA |
| Output Short Circuit | Continuous |
| Operating Temperature | –55°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTES: (1) Stresses above these ratings may cause permanent damage. (2) Input signal voltage is limited by internal diodes connected to power supplies. See text.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

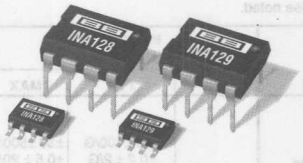
## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA |
|---|---|---|---|---|---|
| **Single** | | | | | |
| INA126PA | 8-Pin DIP | 006 | INA126PA | INA126PA | Rails |
| INA126P | 8-Pin DIP | 006 | INA126P | INA126P | Rails |
| INA126UA | SO-8 | 182 | INA126UA | INA126UA | Rails or Reel |
| INA126U | SO-8 | 182 | INA126U | INA126U | Rails or Reel |
| INA126EA[2] | MSOP-8 | 337 | A26[3] | INA126EA-250 | Reel Only |
| " | " | " | " | INA126EA-2500 | " |
| INA126E[2] | MSOP-8 | 337 | A26[3] | INA126E-250 | Reel Only |
| " | " | " | " | INA126E-2500 | " |
| **Dual** | | | | | |
| INA2126PA | 16-Pin DIP | 180 | INA2126PA | INA2126PA | Rails |
| INA2126P | 16-Pin DIP | 180 | INA2126P | INA2126P | Rails |
| INA2126UA | SO-16 | 265 | INA2126UA | INA2126UA | Rails |
| INA2126U | SO-16 | 265 | INA2126U | INA2126U | Rails |
| INA2126EA[2] | SSOP-16 | 322 | INA2126EA | INA2126EA-250 | Reel Only |
| " | " | " | " | INA2126EA-2500 | " |
| INA2126E[2] | SSOP-16 | 322 | INA2126E | INA2126E-250 | Reel Only |
| " | " | " | " | INA2126E-2500 | " |

NOTES: (1) For detailed drawing and dimension table, see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) MSOP-8 and SSOP-16 packages are available only on 250 or 2500 piece reels. (3) Grade designation is marked on reel.

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# INA128
# INA129

www.burr-brown.com/databook/INA128.html

# Precision, Low Power INSTRUMENTATION AMPLIFIERS

## FEATURES

- LOW OFFSET VOLTAGE: 50μV max
- LOW DRIFT: 0.5μV/°C max
- LOW INPUT BIAS CURRENT: 5nA max
- HIGH CMR: 120dB min
- INPUTS PROTECTED TO ±40V
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 700μA
- 8-PIN PLASTIC DIP, SO-8

## APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

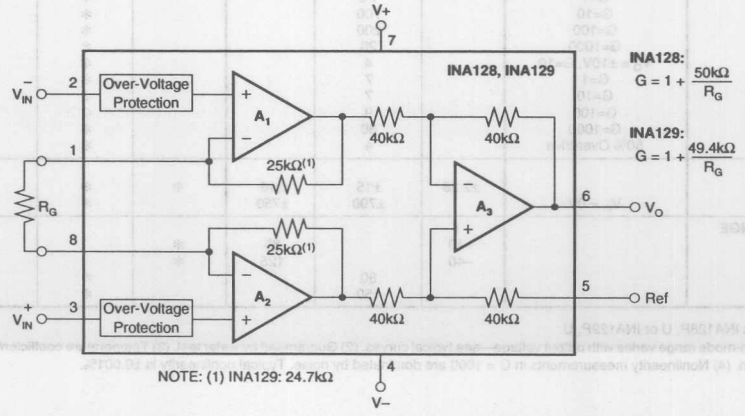
## DESCRIPTION

The INA128 and INA129 are low power, general purpose instrumentation amplifiers offering excellent accuracy. Their versatile 3-op amp design and small size make them ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. INA128 provides an industry standard gain equation; INA129's gain equation is compatible with the AD620.

The INA128/INA129 is laser trimmed for very low offset voltage (50μV), drift (0.5μV/°C) and high common-mode rejection (120dB at G ≥ 100). It operates with power supplies as low as ±2.25V, and quiescent current is only 700μA—ideal for battery operated systems. Internal input protection can withstand up to ±40V without damage.

The INA128/INA129 is available in 8-pin plastic DIP, and SO-8 surface-mount packages, specified for the –40°C to +85°C temperature range. The INA128 is also available in dual configuration, the INA2128.




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# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 10kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | INA128P, U INA129P, U MIN | INA128P, U INA129P, U TYP | INA128P, U INA129P, U MAX | INA128PA, UA INA129PA, UA MIN | INA128PA, UA INA129PA, UA TYP | INA128PA, UA INA129PA, UA MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | | |
| Offset Voltage, RTI | | | | | | | | |
| Initial | $T_A$ = +25°C | | ±10 ±100/G | ±50 ±500/G | | ±25 ±100/G | ±125 ±1000/G | µV |
| vs Temperature | $T_A = T_{MIN}$ to $T_{MAX}$ | | ±0.2 ± 2/G | ±0.5 ± 20/G | | ±0.2 ± 5/G | ±1 ± 20/G | µV/°C |
| vs Power Supply | $V_S$ = ±2.25V to ±18V | | ±0.2 ±20/G | ±1 ±100/G | | * | ±2 ±200/G | µV/V |
| Long-Term Stability | | | ±0.1 ±3/G | | | * | | µV/mo |
| Impedance, Differential | | | $10^{10}$ \|\| 2 | | | * | | Ω \|\| pF |
| Common-Mode | | | $10^{11}$ \|\| 9 | | | * | | Ω \|\| pF |
| Common-Mode Voltage Range[1] | $V_O$ = 0V | (V+) – 2 | (V+) – 1.4 | | * | * | | V |
| | | (V–) + 2 | (V–) + 1.7 | | * | * | | V |
| Safe Input Voltage | | | | ±40 | | | * | V |
| Common-Mode Rejection | $V_{CM}$ = ±13V, $\Delta R_S$ = 1kΩ | | | | | | | |
| | G=1 | 80 | 86 | | 73 | * | | dB |
| | G=10 | 100 | 106 | | 93 | * | | dB |
| | G=100 | 120 | 125 | | 110 | * | | dB |
| | G=1000 | 120 | 130 | | 110 | * | | dB |
| **BIAS CURRENT** | | | ±2 | ±5 | | * | ±10 | nA |
| vs Temperature | | | ±30 | | | * | | pA/°C |
| Offset Current | | | ±1 | ±5 | | * | ±10 | nA |
| vs Temperature | | | ±30 | | | * | | pA/°C |
| **NOISE VOLTAGE, RTI** | G = 1000, $R_S$ = 0Ω | | | | | | | |
| f = 10Hz | | | 10 | | | * | | nV/√Hz |
| f = 100Hz | | | 8 | | | * | | nV/√Hz |
| f = 1kHz | | | 8 | | | * | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 0.2 | | | * | | µVp-p |
| Noise Current | | | | | | | | |
| f=10Hz | | | 0.9 | | | * | | pA/√Hz |
| f=1kHz | | | 0.3 | | | * | | pA/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 30 | | | * | | pAp-p |
| **GAIN** | | | | | | | | |
| Gain Equation, INA128 | | | 1 + (50kΩ/$R_G$) | | | * | | V/V |
| INA129 | | | 1 + (49.4kΩ/$R_G$) | | | * | | V/V |
| Range of Gain | | 1 | | 10000 | * | | * | V/V |
| Gain Error | G=1 | | ±0.01 | ±0.024 | | * | ±0.1 | % |
| | G=10 | | ±0.02 | ±0.4 | | * | ±0.5 | % |
| | G=100 | | ±0.05 | ±0.5 | | * | ±0.7 | % |
| | G=1000 | | ±0.5 | ±1 | | * | ±2 | % |
| Gain vs Temperature[2] | G=1 | | ±1 | ±10 | | * | * | ppm/°C |
| 50kΩ (or 49.4kΩ) Resistance[2, 3] | | | ±25 | ±100 | | * | * | ppm/°C |
| Nonlinearity | $V_O$ = ±13.6V, G=1 | | ±0.0001 | ±0.001 | | * | ±0.002 | % of FSR |
| | G=10 | | ±0.0003 | ±0.002 | | * | ±0.004 | % of FSR |
| | G=100 | | ±0.0005 | ±0.002 | | * | ±0.004 | % of FSR |
| | G=1000 | | ±0.001 | (Note 4) | | * | * | % of FSR |
| **OUTPUT** | | | | | | | | |
| Voltage: Positive | $R_L$ = 10kΩ | (V+) – 1.4 | (V+) – 0.9 | | * | * | | V |
| Negative | $R_L$ = 10kΩ | (V–) + 1.4 | (V–) + 0.8 | | * | * | | V |
| Load Capacitance Stability | | | 1000 | | | * | | pF |
| Short-Circuit Current | | | +6/–15 | | | * | | mA |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Bandwidth, –3dB | G=1 | | 1.3 | | | * | | MHz |
| | G=10 | | 700 | | | * | | kHz |
| | G=100 | | 200 | | | * | | kHz |
| | G=1000 | | 20 | | | * | | kHz |
| Slew Rate | $V_O$ = ±10V, G=10 | | 4 | | | * | | V/µs |
| Settling Time, 0.01% | G=1 | | 7 | | | * | | µs |
| | G=10 | | 7 | | | * | | µs |
| | G=100 | | 9 | | | * | | µs |
| | G=1000 | | 80 | | | * | | µs |
| Overload Recovery | 50% Overdrive | | 4 | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | |
| Voltage Range | | ±2.25 | ±15 | ±18 | * | * | * | V |
| Current, Total | $V_{IN}$ = 0V | | ±700 | ±750 | | * | * | µA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –40 | | 85 | * | | * | °C |
| Operating | | –40 | | 125 | * | | * | °C |
| $\theta_{JA}$ 8-Pin Dip | | | 80 | | | * | | °C/W |
| SO-8 SOIC | | | 150 | | | * | | °C/W |

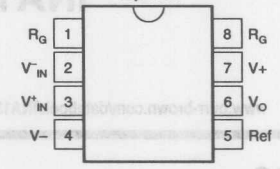
* Specification same as INA128P, U or INA129P, U.

NOTE: (1) Input common-mode range varies with output voltage—see typical curves. (2) Guaranteed by wafer test. (3) Temperature coefficient of the 50kΩ (or 49.4kΩ) term in the gain equation. (4) Nonlinearity measurements in G = 1000 are dominated by noise. Typical nonlinearity is ±0.001%.

## PIN CONFIGURATION

8-Pin DIP and SO-8

Top View




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Analog Input Voltage Range | ±40V |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

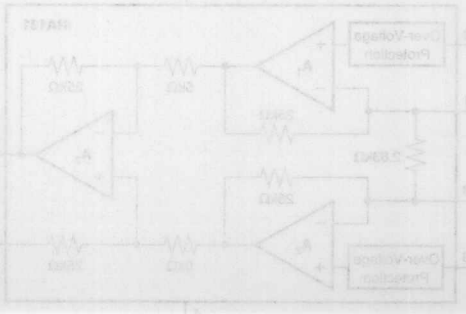
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| INA128PA | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| INA128P | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| INA128UA | SO-8 Surface-Mount | 182 | –40°C to +85°C |
| INA128U | SO-8 Surface-Mount | 182 | –40°C to +85°C |
| INA129PA | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| INA129P | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| INA129UA | SO-8 Surface-Mount | 182 | –40°C to +85°C |
| INA129U | SO-8 Surface-Mount | 182 | –40°C to +85°C |

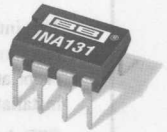
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.





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# INA131

www.burr-brown.com/databook/INA131.html

# Precision G = 100 INSTRUMENTATION AMPLIFIER

## FEATURES

- LOW OFFSET VOLTAGE: 50μV max
- LOW DRIFT: 0.25μV/°C max
- LOW INPUT BIAS CURRENT: 2nA max
- HIGH COMMON-MODE REJECTION: 110dB min
- INPUT OVERVOLTAGE PROTECTION: ±40V
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 3mA
- 8-PIN PLASTIC DIP

## APPLICATIONS

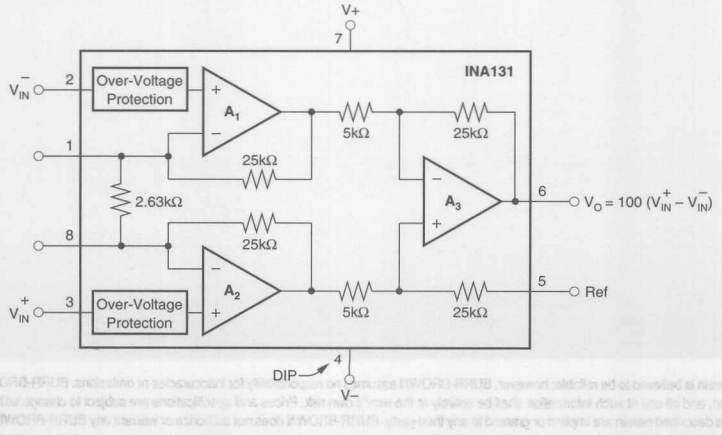
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

## DESCRIPTION

The INA131 is a low cost, general purpose G = 100 instrumentation amplifier offering excellent accuracy. Its 3-op amp design and small size make it ideal for a wide range of applications.

On-chip laser trimmed resistors accurately set a fixed gain of 100. The INA131 is laser trimmed to achieve very low offset voltage (50μV max), drift (0.25μV/°C max), and high CMR (110dB min). Internal input protection can withstand up to ±40V inputs without damage.

The INA131 is available in a 8-pin plastic DIP. They are specified over the –40°C to +85°C temperature range.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 2kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | INA131BP MIN | INA131BP TYP | INA131BP MAX | INA131AP MIN | INA131AP TYP | INA131AP MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | | |
| Offset Voltage, RTI | | | | | | | | |
| Initial | $T_A$ = +25°C | | ±10 | ±50 | | ±25 | ±125 | µV |
| vs Temperature | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | ±0.1 | ±0.25 | | ±0.25 | ±1 | µV/°C |
| vs Power Supply | $V_S$ = ±2.25V to ±18V | | 0.5 | 3 | | * | * | µV/V |
| Long-Term Stability | | | 0.2 | | | * | | µV/mo |
| Impedance, Differential | | | $10^{10}$ \|\| 6 | | | * | | Ω \|\| pF |
| Common-Mode | | | $10^{10}$ \|\| 6 | | | * | | Ω \|\| pF |
| Input Common-Mode Range | | ±11 | ±13.5 | | * | * | | V |
| Safe Input Voltage | | | | ±40 | | | * | V |
| Common-Mode Rejection | $V_{CM}$ = ±10V, $\Delta R_S$ = 1kΩ | 110 | 120 | | 106 | 110 | | dB |
| **BIAS CURRENT** | | | ±0.5 | ±2 | | * | ±5 | nA |
| vs Temperature | | | ±8 | | | * | | pA/°C |
| **OFFSET CURRENT** | | | ±0.5 | ±2 | | * | ±5 | nA |
| vs Temperature | | | ±8 | | | * | | pA/°C |
| **NOISE VOLTAGE, RTI** | $R_S$ = 0Ω | | | | | | | |
| f = 10Hz | | | 16 | | | * | | nV/√Hz |
| f = 100Hz | | | 12 | | | * | | nV/√Hz |
| f = 1kHz | | | 12 | | | * | | nV/√Hz |
| f = 10kHz | | | 12 | | | * | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 0.4 | | | * | | µVp-p |
| Noise Current | | | | | | | | |
| f = 10Hz | | | 0.4 | | | * | | pA/√Hz |
| f= 1kHz | | | 0.2 | | | * | | pA/√Hz |
| $f_B$ = 0.1Hz to 100Hz | | | 18 | | | * | | pAp-p |
| **GAIN** | | | | | | | | |
| Gain Error[1] | | | ±0.01 | ±0.024 | | * | ±0.1 | % |
| Resistor Value[2] | | | ±10 | ±40 | | * | * | % |
| Gain vs Temperature | | | ±5 | ±10 | | * | ±20 | ppm/°C |
| Nonlinearity | | | ±0.0003 | ±0.002 | | * | ±0.004 | % of FSR |
| **OUTPUT** | | | | | | | | |
| Voltage | $I_O$ = 5mA, $T_{MIN}$ to $T_{MAX}$ | ±13.5 | ±13.7 | | * | * | | V |
| | $V_S$ = ±11.4V, $R_L$ = 2kΩ | ±10 | 10.5 | | * | * | | V |
| | $V_S$ = ±2.25V, $R_L$ = 2kΩ | ±1 | 1.5 | | * | * | | V |
| Load Capacitance, max | Stable Operation | | 1000 | | | * | | pF |
| Short Circuit Current | | | +20/–15 | | | * | | mA |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Bandwidth, –3dB | | | 70 | | | * | | kHz |
| Slew Rate | $V_O$ = ±10V | 0.3 | 0.7 | | * | * | | V/µs |
| Settling Time, 0.01% | | | 100 | | | * | | µs |
| Overload Recovery | 50% Overdrive | | 20 | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | |
| Voltage Range | | ±2.25 | ±15 | ±18 | * | * | * | V |
| Current | $V_{IN}$ = 0V | | ±2.2 | ±3 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –40 | | 85 | * | | * | °C |
| Operating | | –40 | | 125 | * | | * | °C |
| $\theta_{JA}$ | | | 100 | | | * | | °C/W |

* Specification same as INA131BP.

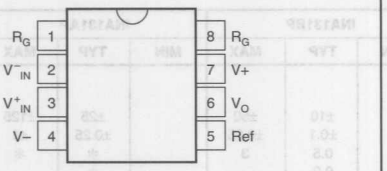
NOTES: (1) $R_L$ = 10kΩ. (2) Absolute value of internal gain-setting resistors. (Gain depends on resistor ratios.)



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## PIN CONFIGURATION

Top View — P-Package/8-Pin DIP




## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| INA131AP | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| INA131BP | 8-Pin Plastic DIP | 006 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Supply Voltage | ±18V |
| Input Voltage Range | ±40V |
| Output Short Circuit (to ground) | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering –10s) | +300°C |

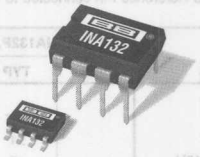
NOTE: (1) Stresses above these ratings may cause permanent damage.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®




# INA132

www.burr-brown.com/databook/INA132.html

# Low Power, Single-Supply DIFFERENCE AMPLIFIER



## FEATURES

- LOW QUIESCENT CURRENT: 160μA
- WIDE SUPPLY RANGE
  Single Supply: 2.7V to 36V
  Dual Supplies: ±1.35V to ±18V
- LOW GAIN ERROR: ±0.075% max
- LOW NONLINEARITY: 0.001% max
- HIGH CMR: 90dB
- HIGHLY VERSATILE CIRCUIT
- EASY TO USE
- LOW COST
- 8-PIN DIP AND SO-8 PACKAGES

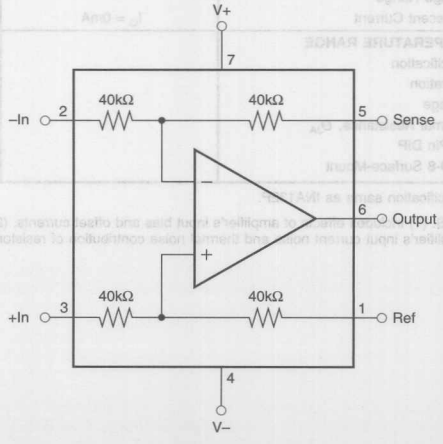
## APPLICATIONS

- DIFFERENTIAL INPUT AMPLIFIER
- INSTRUMENTATION AMPLIFIER BUILDING BLOCK
- UNITY-GAIN INVERTING AMPLIFIER
- G = 1/2 AMPLIFIER
- G = 2 AMPLIFIER
- SUMMING AMPLIFIER
- DIFFERENTIAL CURRENT RECEIVER
- VOLTAGE-CONTROLLED CURRENT SOURCE
- BATTERY-POWERED SYSTEMS
- GROUND LOOP ELIMINATOR

## DESCRIPTION

The INA132 is a low power, unity-gain differential amplifier consisting of a precision op amp with a precision resistor network. The on-chip resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. The internal op amp's common-mode range extends to the negative supply—ideal for single-supply applications. It operates on single (2.7V to 36V) or dual supplies (±1.35V to ±18V).

The differential amplifier is the foundation of many commonly used circuits. The INA132 provides this circuit function without using an expensive precision resistor network. The INA132 is available in 8-pin DIP and SO-8 surface-mount packages and is specified for operation over the extended industrial temperature range, –40°C to +85°C.




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At $T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 10kΩ connected to Ground, and Reference Pin connected to Ground, unless otherwise noted.

| PARAMETER | CONDITIONS | INA132P, U | | | INA132PA, UA | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OFFSET VOLTAGE**[1] | RTO | | | | | | | |
| Initial | | | ±75 | ±250 | | * | ±500 | µV |
| vs Temperature | | | ±1 | ±5 | | * | ±10[4] | µV/°C |
| vs Power Supply | $V_S$ = ±1.35V to ±18V | | ±5 | ±30 | | * | * | µV/V |
| vs Time | | | 0.3 | | | * | | µV/mo |
| **INPUT IMPEDANCE**[2] | | | | | | | | |
| Differential | | | 80 | | | * | | kΩ |
| Common-Mode | | | 80 | | | * | | kΩ |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Voltage Range | $V_O$ = 0V | (V–) | | 2(V+)–2 | * | | * | V |
| Common-Mode Rejection | $V_{CM}$ = –15V to 28V, $R_S$ = 0Ω | 76 | 90 | | 70 | * | | dB |
| **OUTPUT VOLTAGE NOISE**[3] | RTO | | | | | | | |
| f = 0.1Hz to 10Hz | | | 1.6 | | | * | | µVp-p |
| f = 1kHz | | | 65 | | | * | | nV/√Hz |
| **GAIN** | | | | | | | | |
| Initial | | | 1 | | | * | | V/V |
| Error | $V_O$ = –14V to 13.5V | | ±0.01 | ±0.075 | | * | ±0.1 | % |
| vs Temperature[4] | | | ±1 | ±10 | | * | * | ppm/°C |
| vs Nonlinearity | $V_O$ = –14V to 13.5V | | ±0.0001 | ±0.001 | | * | ±0.002 | % of FS |
| **OUTPUT** | | | | | | | | |
| Voltage, Positive | $R_L$ = 100kΩ to Ground | (V+)–1 | (V+)–0.8 | | | * | | V |
| Negative | $R_L$ = 100kΩ to Ground | (V–)+0.5 | (V–)+0.15 | | | * | | V |
| Positive | $R_L$ = 10kΩ to Ground | (V+)–1.5 | (V+)–0.8 | | | * | | V |
| Negative | $R_L$ = 10kΩ to Ground | (V–)+1 | (V–)+0.25 | | | * | | V |
| Current Limit, Continuous to Common | | | ±12 | | | * | | mA |
| Capacitive Load (Stable Operation) | | | 10,000 | | | * | | pF |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Small Signal Bandwidth | –3dB | | 300 | | | * | | kHz |
| Slew Rate | | | 0.1 | | | * | | V/µs |
| Settling Time: 0.1% | $V_O$ = 10V Step | | 85 | | | * | | µs |
| 0.01% | $V_O$ = 10V Step | | 88 | | | * | | µs |
| Overload Recovery Time | 50% Overdrive | | 7 | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | |
| Rated Voltage | | | ±15 | | | * | | V |
| Voltage Range | | ±1.35 | | ±18 | * | | * | V |
| Quiescent Current | $I_O$ = 0mA | | ±160 | ±185 | | * | * | µA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –40 | | +85 | * | | * | °C |
| Operation | | –55 | | +125 | * | | * | °C |
| Storage | | –55 | | +125 | * | | * | °C |
| Thermal Resistance, $\Theta_{JA}$ | | | | | | | | |
| 8-Pin DIP | | | 100 | | | * | | °C/W |
| SO-8 Surface-Mount | | | 150 | | | * | | °C/W |

* Specification same as INA132P.

NOTES: (1) Includes effects of amplifier's input bias and offset currents. (2) 40kΩ resistors are ratio matched but have ±20% absolute value. (3) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network. (4) Guaranteed by wafer test to 95% confidence level.

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# SPECIFICATIONS: $V_S$ = +5V

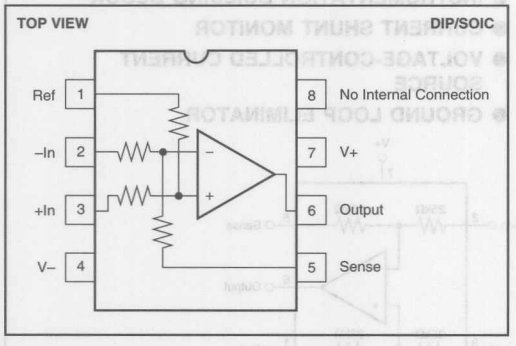
At $T_A$ = +25°C, $V_S$ = +5V, $R_L$ = 10kΩ connected to $V_S$/2, and Reference Pin connected to $V_S$/2, unless otherwise noted.

| PARAMETER | CONDITIONS | INA132P, U | | | INA132PA, UA | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OFFSET VOLTAGE**(1) | RTO | | | | | | | |
| Initial | | | ±150 | ±500 | | * | ±750 | µV |
| vs Temperature | | | ±2 | | | * | | µV/°C |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Voltage Range | | 0 | | 2(V+)–2 | * | | * | V |
| Common-Mode Rejection | $V_{CM}$ = 0V to 8V, $R_S$ = 0Ω | 76 | 90 | | 70 | * | | dB |
| **OUTPUT** | | | | | | | | |
| Voltage, Positive | $R_L$ = 100kΩ | (V+)–1 | (V+)–0.75 | | * | * | | V |
| Negative | $R_L$ = 100kΩ | +0.25 | +0.06 | | * | * | | V |
| Positive | $R_L$ = 10kΩ | (V+)–1 | (V+)–0.8 | | * | * | | V |
| Negative | $R_L$ = 10kΩ | +0.25 | +0.12 | | * | * | | V |
| **POWER SUPPLY** | | | | | | | | |
| Rated Voltage | | | +5 | | | * | | V |
| Voltage Range | | +2.7 | | +36 | * | | * | V |
| Quiescent Current | $I_O$ = 0mA | | ±155 | ±185 | | * | * | µA |

* Specification same as INA132P.

NOTE: (1) Include effects of amplifier's input bias and offset currents.

## PIN CONFIGURATION




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, V+ to V– | 36V |
| Input Voltage Range | ±80V |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | –55°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| INA132PA | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| INA132P | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| INA132UA | SO-8 Surface-Mount | 182 | –40°C to +85°C |
| INA132U | SO-8 Surface-Mount | 182 | –40°C to +85°C |

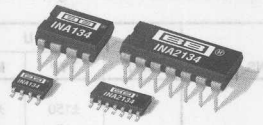
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# INA134
# INA2134

www.burr-brown.com/databook/INA134.html

# AUDIO DIFFERENTIAL LINE RECEIVERS
# 0dB (G = 1)

## FEATURES

- SINGLE AND DUAL VERSIONS
- LOW DISTORTION: 0.0005% at f = 1kHz
- HIGH SLEW RATE: 14V/µs
- FAST SETTLING TIME: 3µs to 0.01%
- WIDE SUPPLY RANGE: ±4V to ±18V
- LOW QUIESCENT CURRENT: 2.9mA max
- HIGH CMRR: 90dB
- FIXED GAIN = 0dB (1V/V)
- PACKAGES—SINGLE: 8-PIN DIP, SO-8
  DUAL: 14-PIN DIP, SO-14

## APPLICATIONS

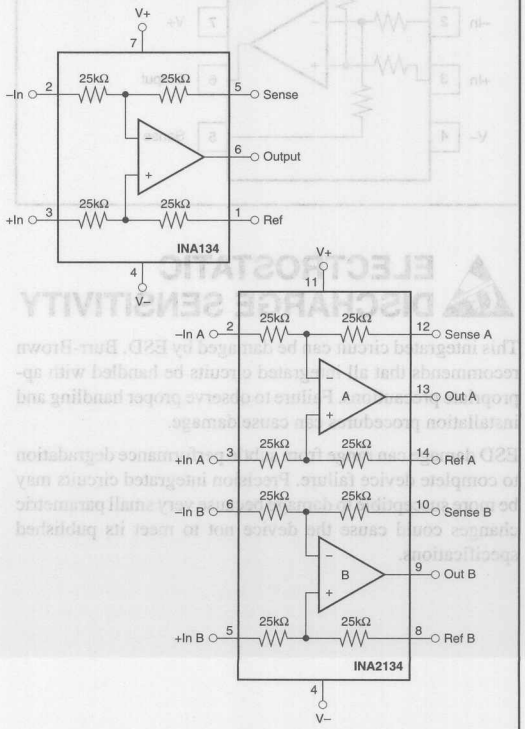
- AUDIO DIFFERENTIAL LINE RECEIVER
- SUMMING AMPLIFIER
- UNITY-GAIN INVERTING AMPLIFIER
- PSEUDOGROUND GENERATOR
- INSTRUMENTATION BUILDING BLOCK
- CURRENT SHUNT MONITOR
- VOLTAGE-CONTROLLED CURRENT SOURCE
- GROUND LOOP ELIMINATOR

## DESCRIPTION

The INA134 and INA2134 are differential line receivers consisting of high performance op amps with on-chip precision resistors. They are fully specified for high performance audio applications and have excellent ac specifications, including low distortion (0.0005% at 1kHz) and high slew rate (14V/µs), assuring good dynamic response. In addition, wide output voltage swing and high output drive capability allow use in a wide variety of demanding applications. The dual version features completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

The INA134 and INA2134 on-chip resistors are laser trimmed for accurate gain and optimum common-mode rejection. Furthermore, excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. Operation is guaranteed from ±4V to ±18V (8V to 36V total supply).

The INA134 is available in 8-pin DIP and SO-8 surface-mount packages. The INA2134 comes in 14-pin DIP and SO-14 surface-mount packages. Both are specified for operation over the extended industrial temperature range, –40°C to +85°C.




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# SPECIFICATIONS: $V_S = \pm 18V$

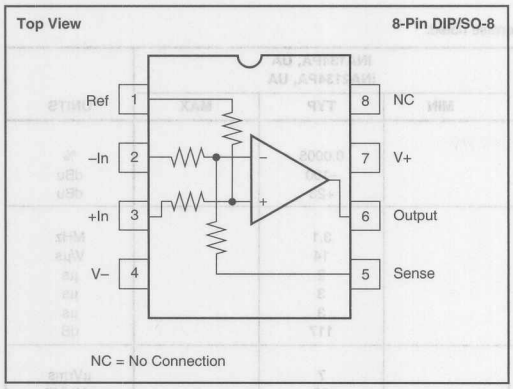
At $T_A = +25°C$, $V_S = \pm 18V$, $R_L = 2k\Omega$, and Ref Pin connected to Ground, unless otherwise noted.

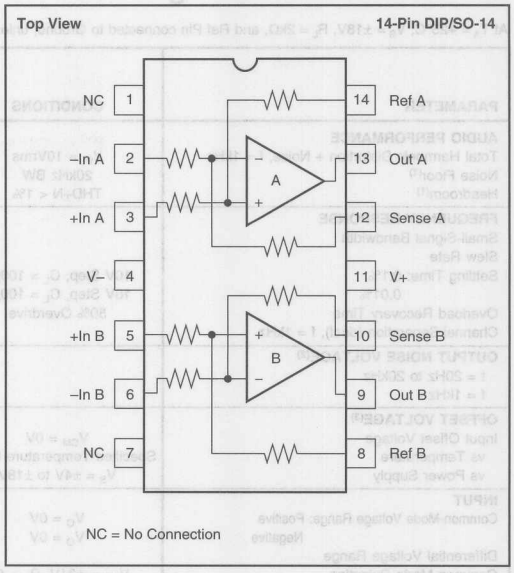
| PARAMETER | CONDITIONS | INA134PA, UA INA2134PA, UA MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **AUDIO PERFORMANCE** | | | | | |
| Total Harmonic Distortion + Noise, f = 1kHz | $V_{IN}$ = 10Vrms | | 0.0005 | | % |
| Noise Floor[1] | 20kHz BW | | –100 | | dBu |
| Headroom[1] | THD+N < 1% | | +23 | | dBu |
| **FREQUENCY RESPONSE** | | | | | |
| Small-Signal Bandwidth | | | 3.1 | | MHz |
| Slew Rate | | | 14 | | V/µs |
| Settling Time: 0.1% | 10V Step, $C_L$ = 100pF | | 2 | | µs |
| 0.01% | 10V Step, $C_L$ = 100pF | | 3 | | µs |
| Overload Recovery Time | 50% Overdrive | | 3 | | µs |
| Channel Separation (dual), f = 1kHz | | | 117 | | dB |
| **OUTPUT NOISE VOLTAGE[2]** | | | | | |
| f = 20Hz to 20kHz | | | 7 | | µVrms |
| f = 1kHz | | | 52 | | nV/√HZ |
| **OFFSET VOLTAGE[3]** | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0V | | ±100 | ±1000 | µV |
| vs Temperature | Specified Temperature Range | | ±2 | | µV/°C |
| vs Power Supply | $V_S$ = ±4V to ±18V | | ±5 | ±60 | µV/V |
| **INPUT** | | | | | |
| Common-Mode Voltage Range: Positive | $V_O$ = 0V | 2(V+)–5 | 2(V+)–4 | | V |
| Negative | $V_O$ = 0V | 2(V–)+5 | 2(V–)+2 | | V |
| Differential Voltage Range | | | See Typical Curve | | |
| Common-Mode Rejection | $V_{CM}$ = ±31V, $R_S$ = 0Ω | 74 | 90 | | dB |
| Impedance[4] | | | | | |
| Differential | | | 50 | | kΩ |
| Common-Mode | | | 50 | | kΩ |
| **GAIN** | | | | | |
| Initial | | | 1 | | V/V |
| Error | $V_O$ = –16V to 16V | | ±0.02 | ±0.1 | % |
| vs Temperature | | | ±1 | ±10 | ppm/°C |
| Nonlinearity | $V_O$ = –16V to 16V | | 0.0001 | | % |
| **OUTPUT** | | | | | |
| Voltage Output, Positive | | (V+)–2 | (V+)–1.8 | | V |
| Negative | | (V–)+2 | (V–)+1.6 | | V |
| Current Limit, Continuous to Common | | | ±60 | | mA |
| Capacitive Load (Stable Operation) | | | 500 | | pF |
| **POWER SUPPLY** | | | | | |
| Rated Voltage | | | ±18 | | V |
| Voltage Range | | ±4 | | ±18 | V |
| Quiescent Current (per Amplifier) | $I_O$ = 0 | | ±2.4 | ±2.9 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification Range | | –40 | | 85 | °C |
| Operation Range | | –55 | | 125 | °C |
| Storage Range | | –55 | | 125 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| 8-Pin DIP | | | 100 | | °C/W |
| SO-8 Surface-Mount | | | 150 | | °C/W |
| 14-Pin DIP | | | 80 | | °C/W |
| SO-14 Surface-Mount | | | 100 | | °C/W |

NOTES: (1) dBu = 20log (Vrms/0.7746). (2) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network. (3) Includes effects of amplifier's input bias and offset currents. (4) 25kΩ resistors are ratio matched but have ±25% absolute value.



The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.




## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Supply Voltage, V+ to V– | 40V |
| Input Voltage Range | ±80V |
| Output Short-Circuit (to ground)[2] | Continuous |
| Operating Temperature | –55°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above these ratings may cause permanent damage. (2) One channel per package.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | SPECIFICATION TEMPERATURE RANGE |
|---|---|---|---|
| **Single** | | | |
| INA134PA | 8-Pin DIP | 006 | –40°C to +85°C |
| INA134UA | SO-8 Surface-Mount | 182 | –40°C to +85°C |
| **Dual** | | | |
| INA2134PA | 14-Pin DIP | 010 | –40°C to +85°C |
| INA2134UA | SO-14 Surface-Mount | 235 | –40°C to +85°C |

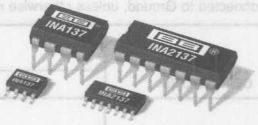
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®



# INA137
# INA2137

www.burr-brown.com/databook/INA137.html



# AUDIO DIFFERENTIAL LINE RECEIVERS
# ±6dB (G = 1/2 or 2)

## FEATURES

- SINGLE AND DUAL VERSIONS
- LOW DISTORTION: 0.0005% at f = 1kHz
- HIGH SLEW RATE: 14V/µs
- FAST SETTLING TIME: 3µs to 0.01%
- WIDE SUPPLY RANGE: ±4V to ±18V
- LOW QUIESCENT CURRENT: 2.9mA max
- HIGH CMRR: 90dB
- FIXED GAIN = ±6dB
- PACKAGES—SINGLE: 8-PIN DIP, SO-8
  DUAL: 14-PIN DIP, SO-14

## APPLICATIONS

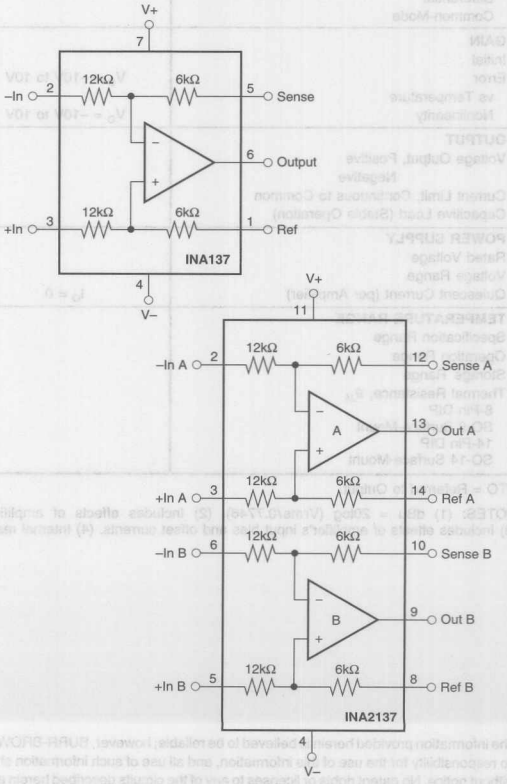
- AUDIO DIFFERENTIAL LINE RECEIVER
- G = 1/2 OR G = 2 AMPLIFIER
- INSTRUMENTATION BUILDING BLOCK
- CURRENT SHUNT MONITOR
- VOLTAGE-CONTROLLED CURRENT SOURCE
- GROUND LOOP ELIMINATOR

## DESCRIPTION

The INA137 and INA2137 are differential line receivers consisting of high performance op amps with on-chip precision resistors. They are fully specified for high performance audio applications and have excellent ac specifications, including low distortion (0.0005% at 1kHz) and high slew rate (14V/µs), assuring good dynamic response. In addition, wide output voltage swing and high output drive capability allow use in a wide variety of demanding applications. The dual version features completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

The INA137 and INA2137 on-chip resistors are laser trimmed for accurate gain and optimum common-mode rejection. Furthermore, excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. Operation is guaranteed from ±4V to ±18V (8V to 36V total supply).

The INA137 is available in 8-pin DIP and SO-8 surface-mount packages. The INA2137 comes in 14-pin DIP and SO-14 surface-mount packages. Both are specified for operation over the extended industrial temperature range, –40°C to +85°C.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS: $V_S = \pm 18V$

At $T_A = +25°C$, $V_S = \pm 18V$, $R_L = 2k\Omega$, G = 1/2, and Ref Pin connected to Ground, unless otherwise noted.

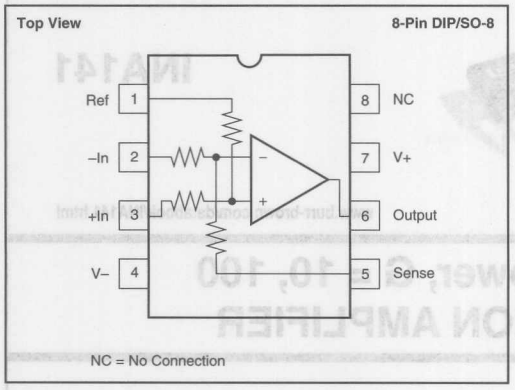
| PARAMETER | CONDITIONS | INA137PA, UA<br>INA2137PA, UA<br>MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **AUDIO PERFORMANCE** | | | | | |
| Total Harmonic Distortion + Noise, f = 1kHz | $V_{IN}$ = 10Vrms | | 0.0005 | | % |
| Noise Floor, RTO[1] | 20kHz BW | | –106 | | dBu |
| Headroom, RTO[1] | THD+N < 1% | | +23 | | dBu |
| **FREQUENCY RESPONSE** | | | | | |
| Small-Signal Bandwidth | | | 4.0 | | MHz |
| Slew Rate | | | 14 | | V/µs |
| Settling Time: 0.1% | 10V Step, $C_L$ = 100pF | | 2 | | µs |
| 0.01% | 10V Step, $C_L$ = 100pF | | 3 | | µs |
| Overload Recovery Time | 50% Overdrive | | 3 | | µs |
| Channel Separation (dual), f = 1kHz | | | 123 | | dB |
| **OUTPUT NOISE VOLTAGE[2]** | | | | | |
| f = 20Hz to 20kHz | | | 3.5 | | µVrms |
| f = 1kHz | | | 26 | | $nV/\sqrt{Hz}$ |
| **OFFSET VOLTAGE[3]** | RTO | | | | |
| Input Offset Voltage | $V_{CM}$ = 0V | | ±100 | ±1000 | µV |
| vs Temperature | Specified Temperature Range | | ±2 | | µV/°C |
| vs Power Supply | $V_S$ = ±4V to ±18V | | ±5 | ±60 | µV/V |
| **INPUT** | | | | | |
| Common-Mode Voltage Range: Positive | $V_O$ = 0V | 3(V+)–7.5 | 3(V+)–6 | | V |
| Negative | $V_O$ = 0V | 3(V–)+7.5 | 3(V–)+3 | | V |
| Differential Voltage Range | | | See Typical Curve | | |
| Common-Mode Rejection | $V_{CM}$ = ±46.5V, $R_S$ = 0Ω | 74 | 90 | | dB |
| Impedance[4] | | | | | |
| Differential | | | 24 | | kΩ |
| Common-Mode | | | 18 | | kΩ |
| **GAIN** | | | | | |
| Initial | | | 0.5 | | V/V |
| Error | $V_O$ = –10V to 10V | | ±0.01 | ±0.1 | % |
| vs Temperature | | | ±1 | ±10 | ppm/°C |
| Nonlinearity | $V_O$ = –10V to 10V | | 0.0001 | | % |
| **OUTPUT** | | | | | |
| Voltage Output, Positive | | (V+)–2 | (V+)–1.8 | | V |
| Negative | | (V–)+2 | (V–)+1.6 | | V |
| Current Limit, Continuous to Common | | | ±60 | | mA |
| Capacitive Load (Stable Operation) | | | 500 | | pF |
| **POWER SUPPLY** | | | | | |
| Rated Voltage | | | ±18 | | V |
| Voltage Range | | ±4 | | ±18 | V |
| Quiescent Current (per Amplifier) | $I_O$ = 0 | | ±2.4 | ±2.9 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification Range | | –40 | | 85 | °C |
| Operation Range | | –55 | | 125 | °C |
| Storage Range | | –55 | | 125 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| 8-Pin DIP | | | 100 | | °C/W |
| SO-8 Surface-Mount | | | 150 | | °C/W |
| 14-Pin DIP | | | 80 | | °C/W |
| SO-14 Surface-Mount | | | 100 | | °C/W |

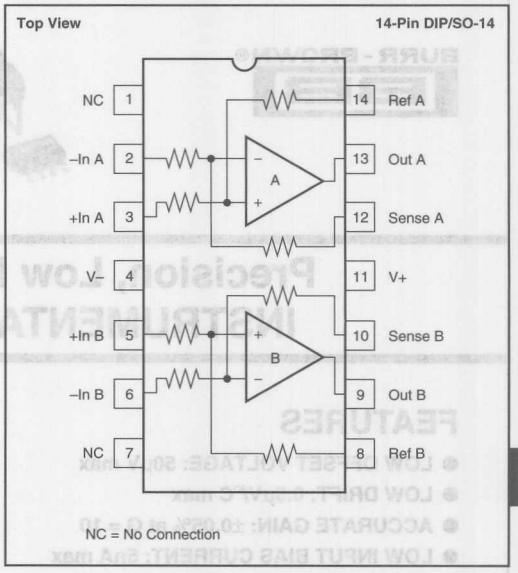
RTO = Referred to Output.

NOTES: (1) dBu = 20log (Vrms/0.7746). (2) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network. (3) Includes effects of amplifier's input bias and offset currents. (4) Internal resistors are ratio matched but have ±25% absolute value.

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## PIN CONFIGURATIONS




## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Supply Voltage, V+ to V– | 40V |
| Input Voltage Range | ±80V |
| Output Short-Circuit (to ground)[2] | Continuous |
| Operating Temperature | –55°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above these ratings may cause permanent damage. (2) One channel per package.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | SPECIFICATION TEMPERATURE RANGE |
|---|---|---|---|
| **Single** | | | |
| INA137PA | 8-Pin DIP | 006 | –40°C to +85°C |
| INA137UA | SO-8 Surface-Mount | 182 | –40°C to +85°C |
| **Dual** | | | |
| INA2137PA | 14-Pin DIP | 010 | –40°C to +85°C |
| INA2137UA | SO-14 Surface-Mount | 235 | –40°C to +85°C |

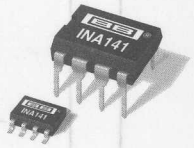
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

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# INA141

www.burr-brown.com/databook/INA141.html

# Precision, Low Power, G = 10, 100 INSTRUMENTATION AMPLIFIER

## FEATURES

- LOW OFFSET VOLTAGE: 50μV max
- LOW DRIFT: 0.5μV/°C max
- ACCURATE GAIN: ±0.05% at G = 10
- LOW INPUT BIAS CURRENT: 5nA max
- HIGH CMR: 117dB min
- INPUTS PROTECTED TO ±40V
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 750μA
- 8-PIN PLASTIC DIP, SO-8

## APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

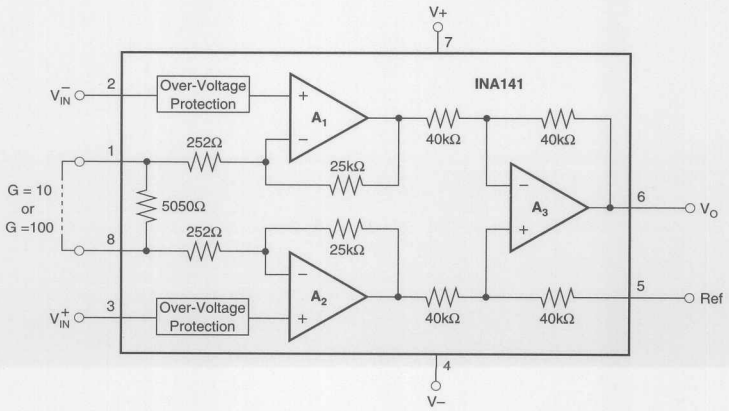
## DESCRIPTION

The INA141 is a low power, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200kHz at G = 100).

Simple pin connections set an accurate gain of 10 or 100V/V without external resistors. Internal input protection can withstand up to ±40V without damage.

The INA141 is laser trimmed for very low offset voltage (50μV), drift (0.5μV/°C) and high common-mode rejection (117dB at G = 100). It operates with power supplies as low as ±2.25V, and quiescent current is only 750μA—ideal for battery operated systems.

The INA141 is available in 8-pin plastic DIP, and SO-8 surface-mount packages, specified for the –40°C to +85°C temperature range.




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# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = ±15V, and $R_L$ = 10kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | INA141P, U MIN | INA141P, U TYP | INA141P, U MAX | INA141PA, UA MIN | INA141PA, UA TYP | INA141PA, UA MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | | |
| Offset Voltage, RTI | G = 100 | | ±20 | ±50 | | * | ±125 | µV |
| | G = 10 | | ±50 | ±100 | | * | ±250 | µV |
| vs Temperature | G = 100 | | ±0.2 | ±0.5 | | * | ±1.5 | µV/°C |
| | G = 10[2] | | ±0.5 | ±2 | | * | ±2.5 | µV/°C |
| vs Power Supply | $V_S$ = ±2.25 to ±18V, G = 100 | | ±0.4 | ±1 | | * | ±3 | µV/V |
| | G = 10 | | ±2 | ±10 | | * | ±20 | µV/V |
| Long-Term Stability | G = 100 | | 0.2 | | | * | | µV/mo |
| | G = 10 | | 0.5 | | | * | | µV/mo |
| Impedance, Differential | | | $10^{10}$ \|\| 2 | | | * | | Ω \|\| pF |
| Common-Mode | | | $10^{10}$ \|\| 9 | | | * | | Ω \|\| pF |
| Common-Mode Voltage Range[1] | $V_O$ = 0V | (V+) – 2 | (V+) – 1.4 | | * | * | | V |
| | | (V–) + 2 | (V–) + 1.7 | | * | * | | V |
| Safe Input Voltage | | | | ±40 | | | * | V |
| Common-Mode Rejection | $V_{CM}$ = ±13V, $\Delta R_S$ = 1kΩ | | | | | | | |
| | G = 100 | 117 | 125 | | 110 | 120 | | dB |
| | G = 10 | 100 | 106 | | 93 | 100 | | dB |
| **BIAS CURRENT** | | | ±2 | ±5 | | * | ±10 | nA |
| vs Temperature | | | ±30 | | | * | | pA/°C |
| Offset Current | | | ±1 | ±5 | | * | ±10 | nA |
| vs Temperature | | | ±30 | | | * | | pA/°C |
| **NOISE VOLTAGE, RTI** | | | | | | | | |
| f = 10Hz | G = 100, $R_S$ = 0Ω | | 10 | | | * | | nV/√Hz |
| f = 100Hz | | | 8 | | | * | | nV/√Hz |
| f = 1kHz | | | 8 | | | * | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 0.2 | | | * | | µVp-p |
| f = 10Hz | G = 10, $R_S$ = 0Ω | | 22 | | | * | | nV/√Hz |
| f = 100Hz | | | 13 | | | * | | nV/√Hz |
| f = 1kHz | | | 12 | | | * | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 0.6 | | | * | | µVp-p |
| Noise Current | | | | | | | | |
| f = 10Hz | | | 0.9 | | | * | | pA/√Hz |
| f = 1kHz | | | 0.3 | | | * | | pA/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 30 | | | * | | pAp-p |
| **GAIN** | | | | | | | | |
| Gain Error | $V_O$ = ±13.6V, G = 100 | | ±0.03 | ±0.075 | | * | ±0.15 | % |
| | G = 10 | | ±0.01 | ±0.05 | | * | ±0.15 | % |
| Gain vs Temperature[2] | G = 10, 100 | | ±2 | ±10 | | * | * | ppm/°C |
| Nonlinearity | G = 100 | | ±0.0005 | ±0.002 | | * | ±0.004 | % of FSR |
| | G = 10 | | ±0.0003 | ±0.001 | | * | ±0.002 | % of FSR |
| **OUTPUT** | | | | | | | | |
| Voltage: Positive | $R_L$ = 10kΩ | (V+) – 1.4 | (V+) – 0.9 | | * | * | | V |
| Negative | $R_L$ = 10kΩ | (V–) + 1.4 | (V–) + 0.9 | | * | * | | V |
| Load Capacitance Stability | | | 1000 | | | * | | pF |
| Short-Circuit Current | | | +6/–15 | | | * | | mA |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Bandwidth, –3dB | G = 100 | | 200 | | | * | | kHz |
| | G = 10 | | 1 | | | * | | MHz |
| Slew Rate | $V_O$ = ±10V, G = 10 | | 4 | | | * | | V/µs |
| Settling Time, 0.01% | $V_O$ = ±5V, G = 100 | | 9 | | | * | | µs |
| | G = 10 | | 7 | | | * | | µs |
| Overload Recovery | 50% Overdrive | | 4 | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | |
| Voltage Range | | ±2.25 | ±15 | ±18 | * | * | * | V |
| Current, Total | $V_{IN}$ = 0V | | ±750 | ±800 | | * | * | µA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –40 | | 85 | * | | * | °C |
| Operating | | –40 | | 125 | * | | * | °C |
| $\theta_{JA}$ 8-Pin DIP | | | 80 | | | * | | °C/W |
| SO-8 SOIC | | | 150 | | | * | | °C/W |

* Specification same as INA141P, U.

NOTE: (1) Input common-mode range varies with output voltage—see typical curves. (2) Guaranteed by wafer test.

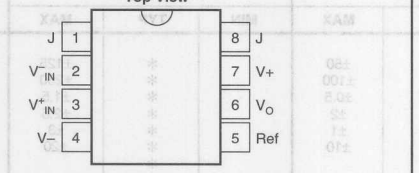


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## PIN CONFIGURATION

8-Pin DIP and SO-8

Top View




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Analog Input Voltage Range | ±40V |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

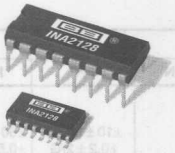
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| INA141PA | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| INA141P | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| INA141UA | SO-8 Surface-Mount | 182 | –40°C to +85°C |
| INA141U | SO-8 Surface-Mount | 182 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR-BROWN®



# INA2128

www.burr-brown.com/databook/INA2128.html

# Dual, Low Power INSTRUMENTATION AMPLIFIER



## FEATURES

- LOW OFFSET VOLTAGE: 50μV max
- LOW DRIFT: 0.5μV/°C max
- LOW INPUT BIAS CURRENT: 5nA max
- HIGH CMR: 120dB min
- INPUTS PROTECTED TO ±40V
- WIDE SUPPLY RANGE: ±2.25V to ±18V
- LOW QUIESCENT CURRENT: 700μA / IA
- 16-PIN PLASTIC DIP, SOL-16

## APPLICATIONS

- SENSOR AMPLIFIER THERMOCOUPLE, RTD, BRIDGE
- MEDICAL INSTRUMENTATION
- MULTIPLE-CHANNEL SYSTEMS
- BATTERY OPERATED EQUIPMENT

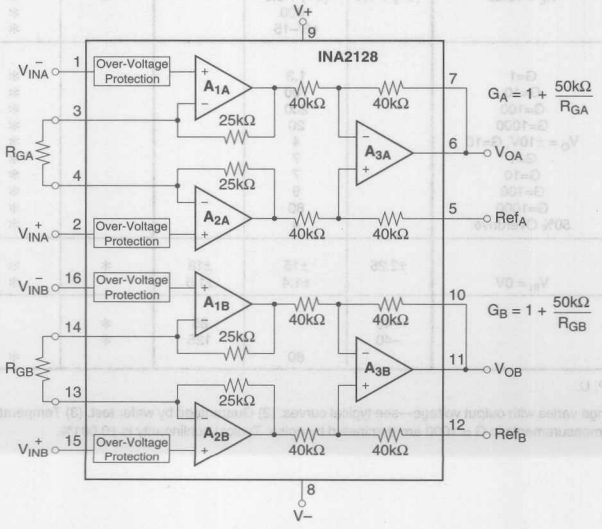
## DESCRIPTION

The INA2128 is a dual, low power, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA2128 is laser trimmed for very low offset voltage (50μV), drift (0.5μV/°C) and high common-mode rejection (120dB at G ≥ 100). It operates with power supplies as low as ±2.25V, and quiescent current is only 700μA per IA—ideal for battery operated and multiple-channel systems.

The INA2128 is available in 16-pin plastic DIP, and SOL-16 surface-mount packages, specified for the –40°C to +85°C temperature range.




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## SPECIFICATIONS

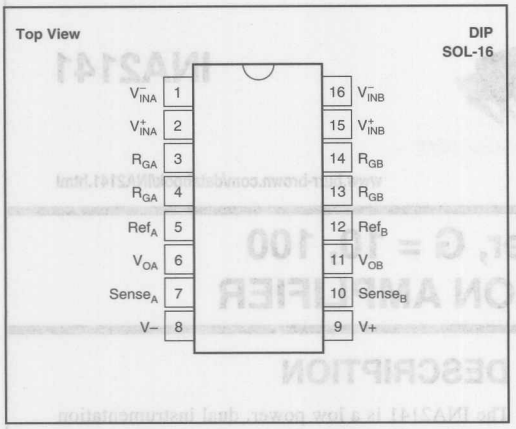
At $T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 10kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | INA2128P, U | | | INA2128PA, UA | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT** | | | | | | | | |
| Offset Voltage, RTI | | | | | | | | |
| Initial | $T_A$ = +25°C | | ±10 ±100/G | ±50 ±500/G | | ±25 ±100/G | ±125 ±1000/G | µV |
| vs Temperature | $T_A = T_{MIN}$ to $T_{MAX}$ | | ±0.2 ± 2/G | ±0.5 ± 20/G | | ±0.2 ± 5/G | ±1 ± 20/G | µV/°C |
| vs Power Supply | $V_S$ = ±2.25V to ±18V | | ±0.2 ±20/G | ±1 ±100/G | | * | ±2 ±200/G | µV/V |
| Long-Term Stability | | | ±0.1 ±3/G | | | * | | µV/mo |
| Impedance, Differential | | | $10^{10}$ \|\| 2 | | | * | | Ω \|\| pF |
| Common-Mode | | | $10^{11}$ \|\| 9 | | | * | | Ω \|\| pF |
| Common-Mode Voltage Range[1] | $V_O$ = 0V | (V+) – 2 | (V+) – 1.4 | | * | * | | V |
| | | (V–) + 2 | (V–) + 1.7 | | * | * | | V |
| Safe Input Voltage | | | | ±40 | | | * | V |
| Common-Mode Rejection | $V_{CM}$ = ±13V, $\Delta R_S$ = 1kΩ | | | | | | | |
| | G=1 | 80 | 86 | | 73 | * | | dB |
| | G=10 | 100 | 106 | | 93 | * | | dB |
| | G=100 | 120 | 125 | | 110 | * | | dB |
| | G=1000 | 120 | 130 | | 110 | * | | dB |
| **BIAS CURRENT** | | | ±2 | ±5 | | * | ±10 | nA |
| vs Temperature | | | ±30 | | | * | | pA/°C |
| Offset Current | | | ±1 | ±5 | | * | ±10 | nA |
| vs Temperature | | | ±30 | | | * | | pA/°C |
| **NOISE VOLTAGE, RTI** | G = 1000, $R_S$ = 0Ω | | | | | | | |
| f = 10Hz | | | 10 | | | * | | nV/√Hz |
| f = 100Hz | | | 8 | | | * | | nV/√Hz |
| f = 1kHz | | | 8 | | | * | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 0.2 | | | * | | µVp-p |
| Noise Current | | | | | | | | |
| f=10Hz | | | 0.9 | | | * | | pA/√Hz |
| f=1kHz | | | 0.3 | | | * | | pA/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 30 | | | * | | pAp-p |
| **GAIN** | | | | | | | | |
| Gain Equation | | | 1 + (50kΩ/$R_G$) | | | * | | V/V |
| Range of Gain | | 1 | | 10000 | * | | * | V/V |
| Gain Error | G=1 | | ±0.01 | ±0.024 | | * | ±0.1 | % |
| | G=10 | | ±0.02 | ±0.4 | | * | ±0.5 | % |
| | G=100 | | ±0.05 | ±0.5 | | * | ±0.7 | % |
| | G=1000 | | ±0.5 | ±1 | | * | ±2 | % |
| Gain vs Temperature[2] | G=1 | | ±1 | ±10 | | * | * | ppm/°C |
| 50kΩ Resistance[2, 3] | | | ±25 | ±100 | | * | * | ppm/°C |
| Nonlinearity | $V_O$ = ±13.6V, G=1 | | ±0.0001 | ±0.001 | | * | ±0.002 | % of FSR |
| | G=10 | | ±0.0003 | ±0.002 | | * | ±0.004 | % of FSR |
| | G=100 | | ±0.0005 | ±0.002 | | * | ±0.004 | % of FSR |
| | G=1000 | | ±0.001 | (Note 4) | | * | * | % of FSR |
| **OUTPUT** | | | | | | | | |
| Voltage: Positive | $R_L$ = 10kΩ | (V+) – 1.4 | (V+) – 0.9 | | * | * | | V |
| Negative | $R_L$ = 10kΩ | (V–) + 1.4 | (V–) + 0.8 | | * | * | | V |
| Load Capacitance Stability | | | 1000 | | | * | | pF |
| Short-Circuit Current | | | +6/–15 | | | * | | mA |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Bandwidth, –3dB | G=1 | | 1.3 | | | * | | MHz |
| | G=10 | | 700 | | | * | | kHz |
| | G=100 | | 200 | | | * | | kHz |
| | G=1000 | | 20 | | | * | | kHz |
| Slew Rate | $V_O$ = ±10V, G=10 | | 4 | | | * | | V/µs |
| Settling Time, 0.01% | G=1 | | 7 | | | * | | µs |
| | G=10 | | 7 | | | * | | µs |
| | G=100 | | 9 | | | * | | µs |
| | G=1000 | | 80 | | | * | | µs |
| Overload Recovery | 50% Overdrive | | 4 | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | |
| Voltage Range | | ±2.25 | ±15 | ±18 | * | * | * | V |
| Current, Total | $V_{IN}$ = 0V | | ±1.4 | ±1.5 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –40 | | 85 | * | | * | °C |
| Operating | | –40 | | 125 | * | | * | °C |
| $\theta_{JA}$ | | | 80 | | | * | | °C/W |

* Specification same as INA2128P, U.

NOTE: (1) Input common-mode range varies with output voltage—see typical curves. (2) Guaranteed by wafer test. (3) Temperature coefficient of the "50kΩ" term in the gain equation. (4) Nonlinearity measurements in G = 1000 are dominated by noise. Typical nonlinearity is ±0.001%.

## PIN CONFIGURATION




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Analog Input Voltage Range | ±40V |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

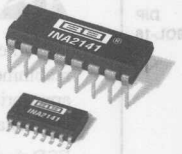
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| INA2128PA | 16-Pin Plastic DIP | 180 | –40°C to +85°C |
| INA2128P | 16-Pin Plastic DIP | 180 | –40°C to +85°C |
| INA2128UA | SOL-16 Surface-Mount | 211 | –40°C to +85°C |
| INA2128U | SOL-16 Surface-Mount | 211 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



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# INA2141

www.burr-brown.com/databook/INA2141.html

# Dual, Low Power, G = 10, 100 INSTRUMENTATION AMPLIFIER

## FEATURES

- LOW OFFSET VOLTAGE: 50µV max
- LOW DRIFT: 0.5µV/°C max
- EXCELLENT GAIN ACCURACY: ±0.05% max at G = 10
- LOW INPUT BIAS CURRENT: 5nA max
- HIGH CMR: 117dB min (G = 100)
- INPUTS PROTECTED TO ±40V
- WIDE SUPPLY RANGE: ±2.25V to ±18V
- LOW QUIESCENT CURRENT: 750µA/IA
- 16-PIN PLASTIC DIP, SOL-16

## APPLICATIONS

- SENSOR AMPLIFIER THERMOCOUPLE, RTD, BRIDGE
- MEDICAL INSTRUMENTATION
- MULTIPLE CHANNEL SYSTEMS

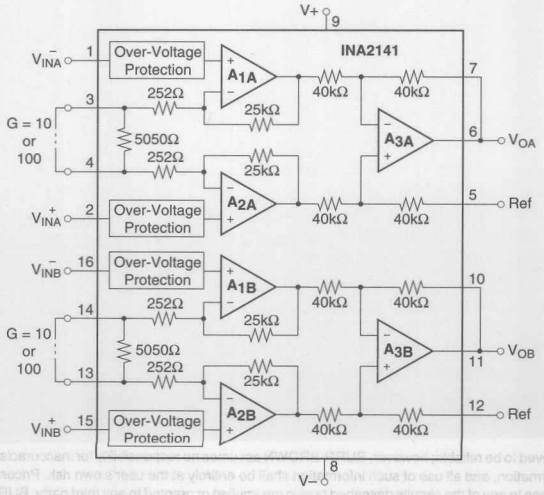
## DESCRIPTION

The INA2141 is a low power, dual instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200kHz at G = 100).

Simple pin connections set an accurate gain of 10 or 100V/V without external resistors. Internal input protection can withstand up to ±40V without damage.

The INA2141 is laser trimmed for very low offset voltage (50µV), drift (0.5µV/°C) and high common-mode rejection (117dB at G = 100). It operates with power supplies as low as ±2.25V, and quiescent current is only 750µA per amplifier—ideal for battery operated systems.

Packages are 16-pin plastic DIP, and SOL-16 surface-mount, specified for the –40°C to +85°C temperature range.




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# SPECIFICATIONS

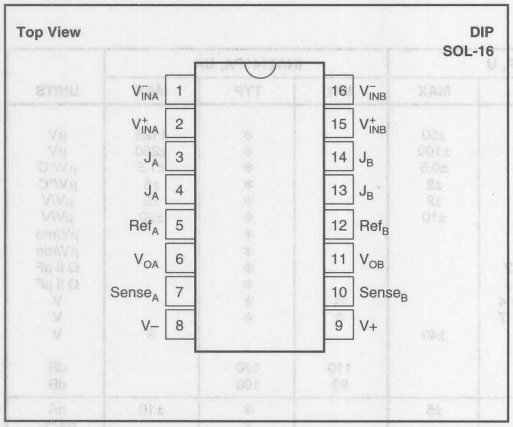
At $T_A$ = +25°C, $V_S$ = ±15V, and $R_L$ = 10kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | INA2141P, U MIN | INA2141P, U TYP | INA2141P, U MAX | INA2141PA, UA MIN | INA2141PA, UA TYP | INA2141PA, UA MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | | |
| Offset Voltage, RTI | G = 100 | | ±20 | ±50 | | * | ±125 | µV |
| | G = 10 | | ±50 | ±100 | | * | ±250 | µV |
| vs Temperature | G = 100 | | ±0.2 | ±0.5 | | * | ±1.5 | µV/°C |
| | G = 10[2] | | ±0.5 | ±2 | | * | ±5 | µV/°C |
| vs Power Supply | $V_S$ = ±2.25 to ±18V, G = 100 | | ±1 | ±2 | | * | ±5 | µV/V |
| | G = 10 | | ±2 | ±10 | | * | ±20 | µV/V |
| Long-Term Stability | G = 100 | | 0.2 | | | * | | µV/mo |
| | G = 10 | | 0.5 | | | * | | µV/mo |
| Impedance, Differential | | | $10^{10}$ II 2 | | | * | | Ω II pF |
| Common-Mode | | | $10^{10}$ II 9 | | | * | | Ω II pF |
| Common-Mode Voltage Range[1] | $V_O$ = 0V | (V+) – 2 | (V+) – 1.4 | | * | * | | V |
| | | (V–) + 2 | (V–) + 1.7 | | * | * | | V |
| Safe Input Voltage | | | | ±40 | | | * | V |
| Common-Mode Rejection | $V_{CM}$ = ±13V, $\Delta R_S$ = 1kΩ | | | | | | | |
| | G = 100 | 117 | 125 | | 110 | 120 | | dB |
| | G = 10 | 97 | 106 | | 93 | 100 | | dB |
| **BIAS CURRENT** | | | ±2 | ±5 | | * | ±10 | nA |
| vs Temperature | | | ±30 | | | * | | pA/°C |
| Offset Current | | | ±1 | ±5 | | * | ±10 | nA |
| vs Temperature | | | ±30 | | | * | | pA/°C |
| **NOISE VOLTAGE, RTI** | | | | | | | | |
| f = 10Hz | G = 100, $R_S$ = 0Ω | | 10 | | | * | | nV/√Hz |
| f = 100Hz | | | 8 | | | * | | nV/√Hz |
| f = 1kHz | | | 8 | | | * | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 0.2 | | | * | | µVp-p |
| f = 10Hz | G = 10, $R_S$ = 0Ω | | 22 | | | * | | nV/√Hz |
| f = 100Hz | | | 13 | | | * | | nV/√Hz |
| f = 1kHz | | | 12 | | | * | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 0.6 | | | * | | µVp-p |
| Noise Current | | | | | | | | |
| f = 10Hz | | | 0.9 | | | * | | pA/√Hz |
| f = 1kHz | | | 0.3 | | | * | | pA/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 30 | | | * | | pAp-p |
| **GAIN** | | | | | | | | |
| Gain Error | $V_O$ = ±13.6V, G = 100 | | ±0.03 | ±0.075 | | * | ±0.15 | % |
| | G = 10 | | ±0.01 | ±0.05 | | * | ±0.15 | % |
| Gain vs Temperature[2] | G = 10, 100 | | ±2 | ±10 | | * | * | ppm/°C |
| Nonlinearity | G = 100 | | ±0.0005 | ±0.002 | | * | ±0.004 | % of FSR |
| | G = 10 | | ±0.0003 | ±0.001 | | * | ±0.002 | % of FSR |
| **OUTPUT** | | | | | | | | |
| Voltage: Positive | $R_L$ = 10kΩ | (V+) – 1.4 | (V+) – 0.9 | | * | * | | V |
| Negative | $R_L$ = 10kΩ | (V–) + 1.4 | (V–) + 0.9 | | * | * | | V |
| Load Capacitance Stability | | | 1000 | | | * | | pF |
| Short-Circuit Current | | | +6/–15 | | | * | | mA |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Bandwidth, –3dB | G = 100 | | 200 | | | * | | kHz |
| | G = 10 | | 1 | | | * | | MHz |
| Slew Rate | $V_O$ = ±10V, G = 10 | | 4 | | | * | | V/µs |
| Settling Time, 0.01% | $V_O$ = ±5V, G = 100 | | 9 | | | * | | µs |
| | G = 10 | | 7 | | | * | | µs |
| Overload Recovery | 50% Overdrive | | 4 | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | |
| Voltage Range | | ±2.25 | ±15 | ±18 | * | * | * | V |
| Current, Total | $V_{IN}$ = 0V | | ±1.5 | ±1.6 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –40 | | 85 | * | | * | °C |
| Operating | | –40 | | 125 | * | | * | °C |
| $\theta_{JA}$ | | | 80 | | | * | | °C/W |

* Specification same as INA2141P, U.

NOTE: (1) Input common-mode range varies with output voltage—see typical curves. (2) Guaranteed by wafer test.

## PIN CONFIGURATION




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Analog Input Voltage Range | ±40V |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

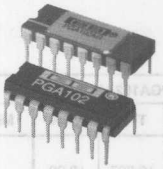
## ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| INA2141PA | 16-Pin Plastic DIP | 180 | –40°C to +85°C |
| INA2141P | 16-Pin Plastic DIP | 180 | –40°C to +85°C |
| INA2141UA | SOL-16 Surface-Mount | 211 | –40°C to +85°C |
| INA2141U | SOL-16 Surface-Mount | 211 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# PGA102

www.burr-brown.com/databook/PGA102.html

# High Speed PROGRAMMABLE GAIN AMPLIFIER



## FEATURES

- DIGITALLY PROGRAMMABLE GAIN: G = 1, 10, 100
- LOW GAIN ERROR: 0.025% max
- FAST SETTLING: 2.8µs to 0.01%
- 16-PIN PLASTIC AND CERAMIC DIP

## APPLICATIONS

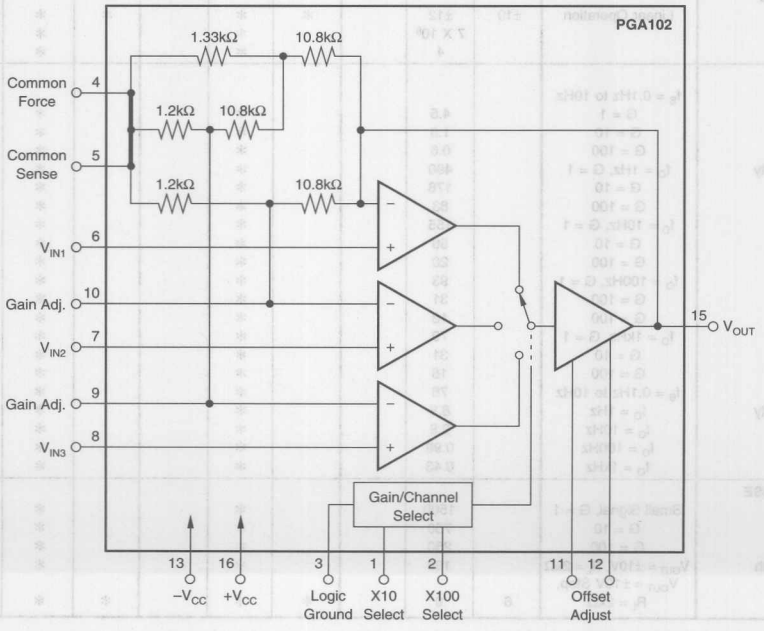
- DATA ACQUISITION AMPLIFIER
- FIXED-GAIN AMPLIFIER
- AUTOMATIC GAIN SCALING

## DESCRIPTION

The PGA102 is a high speed, digitally programmable-gain amplifier. CMOS/TTL-compatible inputs select gains of 1, 10 or 100V/V. Each gain has an independent input terminal, providing an input multiplexer function.

On-chip metal film gain-set resistors are laser-trimmed to provide excellent gain accuracy. High speed input circuitry allows multiplexing of high speed signals.

The PGA102 is available in 16-pin plastic and ceramic DIP packages. Commercial, industrial and military temperature range models are available.




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# SPECIFICATIONS

## ELECTRICAL

At +25°C, $\pm V_{CC}$ = 15VDC, unless otherwise specified.

| PARAMETER | CONDITIONS | PGA102AG | | | PGA102BG, SG | | | PGA102KP | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **GAIN** | | | | | | | | | | | |
| Inaccuracy[1] | $R_L$ = 2kΩ, G = 1 | | ±0.007 | ±0.02 | | ±0.003 | ±0.01 | | * | * | % |
| | G = 10 | | ±0.015 | ±0.03 | | ±0.01 | ±0.02 | | * | ±0.05 | % |
| | G = 100 | | ±0.02 | ±0.05 | | ±0.015 | ±0.025 | | * | ±0.06 | % |
| vs Temperature | G = 1 | | ±0.4 | ±5 | | * | * | | * | * | ppm/°C |
| | G = 10 | | ±2 | ±7 | | * | * | | * | * | ppm/°C |
| | G = 100 | | ±7 | ±20 | | * | * | | ±9 | * | ppm/°C |
| Nonlinearity | $R_L$ = 2kΩ, G = 1 | | 0.001 | 0.003 | | * | * | | * | * | % of FS |
| | G = 10 | | 0.002 | 0.005 | | * | * | | * | * | % of FS |
| | G = 100 | | 0.003 | 0.01 | | * | * | | * | * | % of FS |
| **RATED OUTPUT** | | | | | | | | | | | |
| Voltage | $R_L$ = 2kΩ | ±10 | ±12.5 | | * | * | | * | * | | V |
| Current | $V_{OUT}$ = 10V | ±5 | ±10 | | * | * | | * | * | | mA |
| Short Circuit Current | | ±10 | ±25 | | * | * | | * | * | | mA |
| Output Resistance | | | 0.01 | | | * | | | * | | Ω |
| Load Capacitance | For Stable Operation | | 2000 | | | * | | | * | | pF |
| **INPUT OFFSET VOLTAGE** | | | | | | | | | | | |
| Initial[2] | G = 1 | | ±200 | ±500 | | ±100 | ±250 | | * | ±1500 | µV |
| | G = 10 | | ±70 | ±200 | | ±50 | ±100 | | * | ±600 | µV |
| | G = 100 | | ±70 | ±200 | | ±50 | ±100 | | * | ±600 | µV |
| vs Temperature | G = 1 | | ±5 | ±20 | | * | * | | ±7 | ±50 | µV/°C |
| | G = 10 | | ±1 | ±7 | | * | * | | ±3 | ±10 | µV/°C |
| | G = 100 | | ±0.5 | ±3 | | * | * | | ±2 | ±7 | µV/°C |
| vs Supply Voltage | ±5 < $V_{CC}$ < ±18V | | | | | | | | | | |
| | G = 1 | | ±30 | ±70 | | * | * | | * | * | µV/V |
| | G = 10 | | ±8 | ±30 | | * | * | | * | * | µV/V |
| | G = 100 | | ±8 | ±30 | | * | * | | * | * | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | | | | | |
| Initial | $T_A$ = +25°C | | ±20 | ±50 | | * | * | | * | * | nA |
| Over Temperature | $T_{A\,MIN}$ to $T_{A\,MAX}$ | | ±25 | ±60 | | * | * | | * | * | nA |
| **ANALOG INPUT CHARACTERISTICS** | | | | | | | | | | | |
| Voltage Range | Linear Operation | ±10 | ±12 | | * | * | | * | * | | V |
| Resistance | | | 7 X $10^8$ | | | * | | | * | | Ω |
| Capacitance | | | 4 | | | * | | | * | | pF |
| **INPUT NOISE** | | | | | | | | | | | |
| Voltage Noise | $f_B$ = 0.1Hz to 10Hz | | | | | | | | | | |
| | G = 1 | | 4.5 | | | * | | | * | | µVp-p |
| | G = 10 | | 1.5 | | | * | | | * | | µVp-p |
| | G = 100 | | 0.6 | | | * | | | * | | µVp-p |
| Voltage Noise Density | $f_O$ = 1Hz, G = 1 | | 490 | | | * | | | * | | nV/√Hz |
| | G = 10 | | 178 | | | * | | | * | | nV/√Hz |
| | G = 100 | | 83 | | | * | | | * | | nV/√Hz |
| | $f_O$ = 10Hz, G = 1 | | 155 | | | * | | | * | | nV/√Hz |
| | G = 10 | | 56 | | | * | | | * | | nV/√Hz |
| | G = 100 | | 20 | | | * | | | * | | nV/√Hz |
| | $f_O$ = 100Hz, G = 1 | | 93 | | | * | | | * | | nV/√Hz |
| | G = 100 | | 31 | | | * | | | * | | nV/√Hz |
| | G = 100 | | 18 | | | * | | | * | | nV/√Hz |
| | $f_O$ = 1kHz, G = 1 | | 79 | | | * | | | * | | nV/√Hz |
| | G = 10 | | 31 | | | * | | | * | | nV/√Hz |
| | G = 100 | | 18 | | | * | | | * | | nV/√Hz |
| Current Noise | $f_B$ = 0.1Hz to 10Hz | | 76 | | | * | | | * | | pAp-p |
| Current Noise Density | $f_O$ = 1Hz | | 8.8 | | | * | | | * | | pA/√Hz |
| | $f_O$ = 10Hz | | 2.8 | | | * | | | * | | pA/√Hz |
| | $f_O$ = 100Hz | | 0.99 | | | * | | | * | | pA/√Hz |
| | $f_O$ = 1kHz | | 0.43 | | | * | | | * | | pA/√Hz |
| **DYNAMIC RESPONSE** | | | | | | | | | | | |
| ±3dB Bandwidth | Small Signal, G = 1 | | 1500 | | | * | | | * | | kHz |
| | G = 10 | | 750 | | | * | | | * | | kHz |
| | G = 100 | | 250 | | | * | | | * | | kHz |
| Full Power Bandwidth | $V_{OUT}$ = ±10V, $R_L$ = 2kΩ | | 160 | | | * | | | * | | kHz |
| Slew Rate | $V_{OUT}$ = ±10V Step, $R_L$ = 2kΩ | 6 | 9 | | * | * | | * | * | | V/µs |

# SPECIFICATIONS (CONT)

## ELECTRICAL

At +25°C, $\pm V_{CC}$ = 15VDC, unless otherwise specified.

| PARAMETER | CONDITIONS | PGA102AG | | | PGA102BG | | | PGA102KP | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **DYNAMIC RESPONSE (CONT)** | | | | | | | | | | | |
| Settling Time (0.1%) | $V_{OUT}$ = 10V Step, G = 1 | | 1.6 | | | * | | | * | | µs |
| | G = 10 | | 2.2 | | | * | | | * | | µs |
| | G = 100 | | 5.2 | | | * | | | * | | µs |
| Settling Time (0.01%) | $V_{OUT}$ = 10V Step, G = 1 | | 2.8 | | | * | | | * | | µs |
| | G = 10 | | 2.8 | | | * | | | * | | µs |
| | G = 100 | | 8.2 | | | * | | | * | | µs |
| Overload Recovery Time, 0.1% | 50% Overdrive, G = 1 (see Performance Curve) | | 2.5 | | | * | | | * | | µs |
| **CROSSTALK** | | | | | | | | | | | |
| DC | ±10V to Both Off Channels | | –155 | | | * | | | * | | dB |
| 60Hz | ±10V to Both Off Channels | | –144 | | | * | | | * | | dB |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | | | | | | | |
| Input "Low" Threshold | $V_{IL}$[3] on Pin 1 or 2 | | | VLTC+0.8 | | | * | | | * | V |
| Input "Low" Current | | | | 1 | | | * | | | * | µA |
| Input "High" Threshold | $V_{IH}$[3] on Pin 1 or 2 | VLTC+2 | | 1 | * | | * | * | | * | V |
| Input "High" Current | | | 0.1 | 1 | | * | * | | * | * | µA |
| Logic Threshold Control | VLTC on Pin 3 | $-V_{CC}$ | | $V_{CC}$ – 4 | * | | * | * | | * | V |
| Switching Time[4] | Between Channels | | 1 | | | * | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | | | | |
| Rated Voltage | | | ±15 | | | * | | | * | | VDC |
| Voltage Range | | ±5 | | ±18 | * | | * | * | | * | VDC |
| Quiescent Current | $V_{OUT}$ = 0V | | ±2.4 | ±3.3 | | * | * | | * | * | mA |
| | No External Load, $V_{OUT}$ = ±10V | | | ±5.3 | | | * | | | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification, KP Grade | $T_{A\ MIN}$ to $T_{A\ MAX}$ | | | | | | | 0 | | +70 | °C |
| AG and BG Grades | | –25 | | +85 | * | | * | | | | °C |
| SG Grade | | | | | –55 | | +125 | | | | °C |
| Operating | | –55 | | +125 | * | | * | –25 | | +85 | °C |
| Storage | | –65 | | +150 | * | | * | –55 | | +125 | °C |
| Thermal Resistance | $\theta_{JA}$ | | 100 | | | * | | | * | | °C/W |

* Specification same as AG grade.

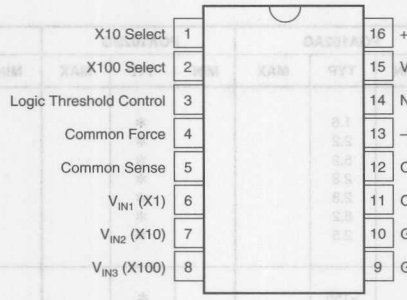
NOTES: (1) Gain inaccuracy is the percent error between the actual and ideal gain selected. It may be externally adjusted to zero for gains of 10 and 100. (2) Offset voltage can be adjusted for any one channel. Adjustment affects temperature drift by approximately ±0.3µV/°C for each 100µV of offset adjusted. (3) Voltage on the logic threshold control pin, VLTC, adjusts the threshold for "Low" and "High" logic levels. (4) Total time to settle equals switching time plus settling time of the newly selected gain.



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## PIN CONFIGURATION

Top View — DIP




NOTE: (1) No Internal Connection.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply | ±18V |
| Input Voltage Range: Analog | $\pm V_{CC}$ |
| Digital | $(V_{PIN\ 3} - 5.6V)$ to $+V_{CC}$ |
| Storage Temperature Range: G Package | –65°C to +150°C |
| P Package | –55°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short Circuit Duration | Continuous to Common |
| Junction Temperature: G Package | +175°C |
| P Package | +110°C |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| PGA102AG | 16-Pin Hermetic DIP | 109 | –25°C to +85°C |
| PGA102BG | 16-Pin Hermetic DIP | 109 | –25°C to +85°C |
| PGA102SG | 16-Pin Hermetic DIP | 109 | –55°C to +125°C |
| PGA102KP | 16-Pin Plastic DIP | 180 | 0°C to +70°C |

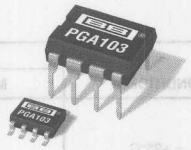
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# PGA103

www.burr-brown.com/databook/PGA103.html

# Programmable Gain AMPLIFIER



## FEATURES

- DIGITALLY PROGRAMABLE GAINS: G=1, 10, 100V/V
- CMOS/TTL-COMPATIBLE INPUTS
- LOW GAIN ERROR: ±0.05% max, G=10
- LOW OFFSET VOLTAGE DRIFT: 2µV/°C
- LOW QUIESCENT CURRENT: 2.6mA
- LOW COST
- 8-PIN PLASTIC DIP, SO-8 PACKAGES

## APPLICATIONS

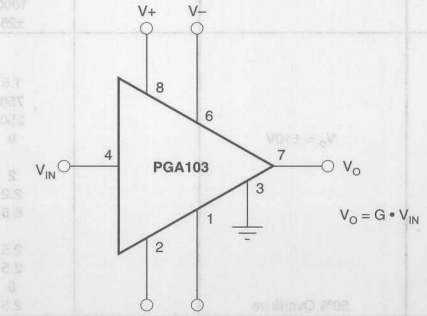
- DATA ACQUISITION SYSTEMS
- GENERAL PURPOSE ANALOG BOARDS
- MEDICAL INSTRUMENTATION

## DESCRIPTION

The PGA103 is a programmable-gain amplifier for general purpose applications. Gains of 1, 10, or 100 are digitally selected by two CMOS/TTL-compatible inputs. The PGA103 is ideal for systems that must handle wide dynamic range signals.

The PGA103's high speed circuitry provides fast settling time, even at G=100 (8µs to 0.01%). Bandwidth is 250kHz at G=100, yet quiescent current is only 2.6mA. It operates from ±4.5V to ±18V power supplies.

The PGA103 is available in 8-pin plastic DIP and SO-8 surface-mount packages, specified for the –40°C to +85°C temperature range.




| GAIN | $A_1$ | $A_0$ |
|---|---|---|
| 1 | 0 | 0 |
| 10 | 0 | 1 |
| 100 | 1 | 0 |

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# SPECIFICATIONS

## ELECTRICAL

AT $T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 2kΩ, unless otherwise specified.

| PARAMETER | CONDITIONS | PGA103P, U | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **INPUT** | | | | | |
| Offset Voltage, RTI | | | | | |
| G = 1 | $T_A$ = +25°C | | ±200 | ±1500 | µV |
| G = 10 | | | ±100 | ±500 | µV |
| G = 100 | | | ±100 | ±500 | µV |
| vs Temperature | $T_A = T_{MIN}$ to $T_{MAX}$ | | | | |
| G = 1 | | | ±5 | | µV/°C |
| G = 10 | | | ±2 | | µV/°C |
| G = 100 | | | ±2 | | µV/°C |
| vs Power Supply | $V_S$ = ±4.5V to ±18V | | | | |
| G = 1 | | | 30 | 70 | µV/V |
| G = 10 | | | 10 | 35 | µV/V |
| G = 100 | | | 10 | 35 | µV/V |
| Impedance | | | $10^8$ \|\| 2 | | Ω \|\| pF |
| **INPUT BIAS CURRENT** | | | | | |
| Initial Bias Current | | | ±50 | ±150 | nA |
| vs Temperature | | | ±100 | | pA/°C |
| **NOISE VOLTAGE, RTI** | G = 100, $R_S$ = 0Ω | | | | |
| f = 10Hz | | | 16 | | nV/√Hz |
| f = 100Hz | | | 11 | | nV/√Hz |
| f = 1kHz | | | 11 | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 0.6 | | µVp-p |
| **NOISE CURRENT** | | | | | |
| f = 10Hz | | | 2.8 | | pA/√Hz |
| f = 1kHz | | | 0.3 | | pA/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 76 | | pAp-p |
| **GAIN** | | | | | |
| Gain Error | | | | | |
| G = 1 | | | ±0.005 | ±0.02 | % |
| G = 10 | | | ±0.02 | ±0.05 | % |
| G = 100 | | | ±0.04 | ±0.2 | % |
| Gain vs Temperature | | | | | |
| G = 1 | | | ±2 | | ppm/°C |
| G = 10 | | | ±10 | | ppm/°C |
| G = 100 | | | ±30 | | ppm/°C |
| Nonlinearity | | | | | |
| G = 1 | | | ±0.001 | ±0.003 | % of FSR |
| G = 10 | | | ±0.002 | ±0.005 | % of FSR |
| G = 100 | | | ±0.004 | ±0.01 | % of FSR |
| **OUTPUT** | | | | | |
| Voltage, Positive | | (V+) –3.5 | (V+) –2.5 | | V |
| Negative | | (V–) +3.5 | (V–) +2.5 | | V |
| Load Capacitance, max | | | 1000 | | pF |
| Short-Circuit Current | | | ±25 | | mA |
| **FREQUENCY RESPONSE** | | | | | |
| Bandwidth, –3dB | | | | | |
| G = 1 | | | 1.5 | | MHz |
| G = 10 | | | 750 | | kHz |
| G = 100 | | | 250 | | kHz |
| Slew Rate | $V_O$ = ±10V | | 9 | | V/µs |
| Settling Time, 0.1% | | | | | |
| G = 1 | | | 2 | | µs |
| G = 10 | | | 2.2 | | µs |
| G = 100 | | | 6.5 | | µs |
| Settling Time, 0.01% | | | | | |
| G = 1 | | | 2.5 | | µs |
| G = 10 | | | 2.5 | | µs |
| G = 100 | | | 8 | | µs |
| Overload Recovery | 50% Overdrive | | 2.5 | | µs |
| **DIGITAL LOGIC INPUTS** | | | | | |
| Digital Low Voltage | | –5.6 | | 0.8 | V |
| Digital Low or High Current | | | 1 | | µA |
| Digital High Voltage | | 2 | | V+ | V |

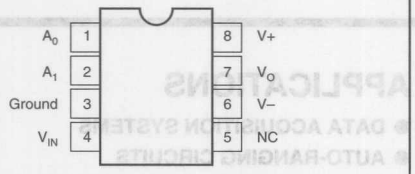
## ELECTRICAL

At $T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 2kΩ, unless otherwise specified.

| PARAMETER | CONDITIONS | PGA103P, U | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **POWER SUPPLY** | | | | | |
| Voltage Range | | ±4.5 | ±15 | ±18 | V |
| Current | $V_{IN}$ = 0V | | ±2.6 | ±3.5 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –40 | | +85 | °C |
| Operating | | –40 | | +125 | °C |
| $\theta_{JA}$: P or U Package | | | 100 | | °C/W |

## PIN CONFIGURATION

Top View — DIP/SO-8




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Analog Input Voltage Range | V– to V+ |
| Logic Input Voltage Range | V– to V+ |
| Output Short Circuit (to ground) | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering,10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

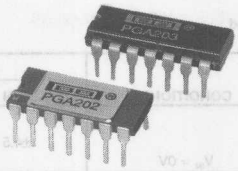
## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| PGA103P | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| PGA103U | SO-8 Surface-Mount | 182 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# PGA202
# PGA203

www.burr-brown.com/databook/PGA202.html

# Digitally Controlled Programmable-Gain INSTRUMENTATION AMPLIFIER

## FEATURES

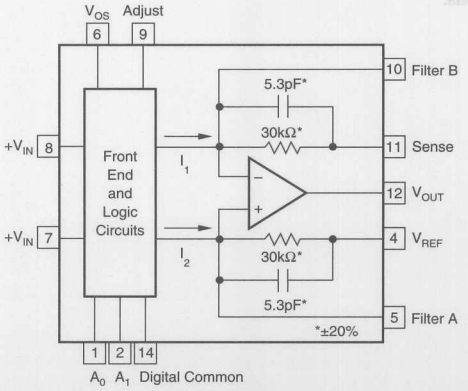
- DIGITALLY PROGRAMMABLE GAINS:
  DECADE MODEL—PGA202
  GAINS OF 1, 10, 100, 1000
  BINARY MODEL—PGA203
  GAINS OF 1, 2, 4, 8
- LOW BIAS CURRENT: 50pA max
- FAST SETTLING: 2µs to 0.01%
- LOW NON-LINEARITY: 0.012% max
- HIGH CMRR: 80dB min
- NEW TRANSCONDUCTANCE CIRCUITRY
- LOW COST

## APPLICATIONS

- DATA ACQUISITION SYSTEMS
- AUTO-RANGING CIRCUITS
- DYNAMIC RANGE EXPANSION
- REMOTE INSTRUMENTATION
- TEST EQUIPMENT

## DESCRIPTION

The PGA202 is a monolithic instrumentation amplifier with digitally controlled gains of 1, 10, 100, and 1000. The PGA203 provides gains of 1, 2, 4, and 8. Both have TTL or CMOS-compatible inputs for easy microprocessor interface. Both have FET inputs and a new transconductance circuitry that keeps the bandwidth nearly constant with gain. Gain and offsets are laser trimmed to allow use without any external components. Both amplifiers are available in ceramic or plastic packages. The ceramic package is specified over the full industrial temperature range while the plastic package covers the commercial range.




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# SPECIFICATIONS

## ELECTRICAL

At +25°C, $V_{CC}$ = ±15V unless otherwise noted.

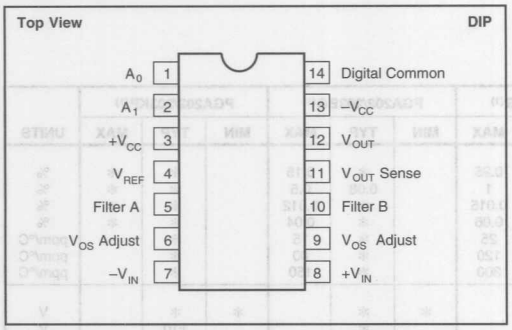
| PARAMETER | CONDITION | PGA202/203AG[1] MIN | PGA202/203AG[1] TYP | PGA202/203AG[1] MAX | PGA202/203BG[1] MIN | PGA202/203BG[1] TYP | PGA202/203BG[1] MAX | PGA202/203KP[1] MIN | PGA202/203KP[1] TYP | PGA202/203KP[1] MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **GAIN** | | | | | | | | | | | |
| Error[2] | G < 1000 | | 0.05 | 0.25 | | * | 0.15 | | * | * | % |
| | G = 1000 | | 0.1 | 1 | | 0.08 | 0.5 | | * | * | % |
| Nonlinearity | G < 1000 | | 0.002 | 0.015 | | * | 0.012 | | * | * | % |
| | G = 1000 | | 0.02 | 0.06 | | * | 0.04 | | * | * | % |
| Gain vs Temperature | G < 100 | | 3 | 25 | | * | 15 | | * | | ppm/°C |
| | G = 100 | | 40 | 120 | | * | 60 | | * | | ppm/°C |
| | G = 1000 | | 100 | 300 | | * | 150 | | * | | ppm/°C |
| **RATED OUTPUT** | | | | | | | | | | | |
| Voltage | $\|I_{OUT}\| \leq 5mA$ | ±10 | ±12 | | * | * | | * | * | | V |
| Over Specified Temperature | See Typical Perf. Curve | | ±9 | | | * | | | ±10 | | V |
| Current | $\|V_{OUT}\| \leq 10V$ | ±5 | ±10 | | * | * | | * | * | | mA |
| Impedance | | | 0.5 | | | * | | | * | | Ω |
| **ANALOG INPUTS** | | | | | | | | | | | |
| Common-Mode Range | | ±10 | ±13 | | * | * | | * | * | | V |
| Absolute Max Voltage[3] | No Damage | | | $\pm V_{CC}$ | | * | | | | * | V |
| Impedance, Differential | | | 10 \|\| 3 | | | * | | | * | | GΩ \|\| pF |
| Common-Mode | | | 10 \|\| 1 | | | * | | | * | | GΩ \|\| pF |
| **OFFSET VOLTAGE (RTI)** | | | | | | | | | | | |
| Initial Offset at 25°C[4] | | | ±(0.5 + 5/G) | ±(2 + 24/G) | | * | ±(1 + 12/G) | | * | * | mV |
| vs Temperature | | | ±(3 + 50/G) | ±(24 + 240/G) | | * | ±(12 + 120/G) | | * | | µV/°C |
| Offset vs Time | | | 50 | | | * | | | * | | µV/Month |
| Offset vs Supply | $10 \leq V_{CC} \leq 15$ | | 10 + 250/G | 100 + 900/G | | * | 50 + 450/G | | * | * | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | | | | | |
| Initial Bias Current: at 25°C | | | 10 | 50 | | * | * | | * | * | pA |
| at 85°C | | | 640 | 3200 | | * | * | | * | * | pA |
| Initial Offset Current: at 25°C | | | 5 | 25 | | * | * | | * | * | pA |
| at 85°C | | | 320 | 1600 | | * | * | | * | * | pA |
| **COMMON-MODE REJECTION RATIO** | | | | | | | | | | | |
| | G = 1 | 80 | 100 | | * | * | | * | * | | dB |
| | G = 10 | 86 | 110 | | * | * | | * | * | | dB |
| | G = 100 | 92 | 120 | | * | * | | * | * | | dB |
| | G = 1000 | 94 | 120 | | * | * | | * | * | | dB |
| **INPUT NOISE** | | | | | | | | | | | |
| Noise Voltage 0.1 to 10Hz | | | 1.7 | | | * | | | * | | µVp-p |
| Noise Density at 10kHz[5] | | | 12 | | | * | | | * | | nV/√Hz |
| **OUTPUT NOISE** | | | | | | | | | | | |
| Noise Voltage 0.1 to 10Hz | | | 32 | | | * | | | * | | µVp-p |
| Density at 1kHz[5] | | | 400 | | | * | | | * | | nV/√Hz |
| **DYNAMIC RESPONSE** | | | | | | | | | | | |
| Frequency Response | G < 1000 | | 1000 | | | * | | | * | | kHz |
| | G = 1000 | | 250 | | | * | | | * | | kHz |
| Full Power Bandwidth | G < 1000 | | 400 | | | * | | | * | | kHz |
| | G = 1000 | | 100 | | | * | | | * | | kHz |
| Slew Rate | | 10 | 20 | | 15 | * | | * | * | | V/µs |
| Settling Time (0.01%)[7] | G < 1000 | | 2 | | | * | | | * | | µs |
| | G = 1000 | | 10 | | | * | | | * | | µs |
| Overload Recovery Time[7] | G < 1000 | | 5 | | | * | | | * | | µs |
| | G = 1000 | | 10 | | | * | | | * | | µs |
| **DIGITAL INPUTS** | | | | | | | | | | | |
| Digital Common Range | | $-V_{CC}$ | | $V_{CC} - 8$ | * | | * | * | | * | V |
| Input Low Threshold[6] | | | | 0.8 | | | * | | | * | V |
| Input Low Current | | | | 10 | | | * | | | * | µA |
| Input High Voltage | | 2.4 | | | * | | | * | | | V |
| Input High Current | | | | 10 | | | * | | | * | µA |
| **POWER SUPPLY** | | | | | | | | | | | |
| Rated Voltage | | | ±15 | | | * | | | * | | V |
| Voltage Range | | ±6 | | ±18 | * | | * | * | | * | V |
| Quiescent Current | | | 6.5 | | | * | | | * | | mA |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification | | –25 | | 85 | * | | * | 0 | | 70 | °C |
| Operating | | –55 | | 125 | * | | * | –25 | | 85 | °C |
| Storage | | –65 | | 150 | * | | * | –40 | | 100 | °C |
| $\theta_{JA}$ | | | 100 | | | * | | | * | | °C/W |

* Specification same as PGA202/203AG.

NOTES: (1) All specifications apply to both the PGA202 and the PGA203. Values given for a gain of 10 are the same for a gain of 8 and other values may be interpolated. (2) Measured with a 10k load. (3) The analog inputs are internally diode clamped. (4) Adjustable to zero. (5) $V_{NOISE\ (RTI)} = \sqrt{(V_{N\ INPUT})^2 + (V_{N\ OUTPUT}/Gain)^2}$. (6) Threshold voltages are referenced to Digital Common. (7) From input change or gain change.

## PIN CONFIGURATION

Top View — DIP




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Internal Power Dissipation | 750mW |
| Analog and Digital Inputs | ±($V_{CC}$ + 0.5V) |
| Operating Temperature Range: | |
| G Package | –55°C to +125°C |
| P Package | –40°C to +100°C |
| Lead Temperature (soldering, 10s) | 300°C |
| Output Short Circuit Duration | Continuous |
| Junction Temperature | 175°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| PGA202KP | 14-Pin Plastic DIP | 010 |
| PGA202AG | 14-Pin Ceramic DIP | 169 |
| PGA202BG | 14-Pin Ceramic DIP | 169 |
| PGA203KP | 14-Pin Plastic DIP | 010 |
| PGA203AG | 14-Pin Ceramic DIP | 169 |
| PGA203BG | 14-Pin Ceramic DIP | 169 |

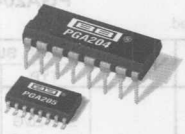
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

| PRODUCT | GAINS | PACKAGE | TEMPERATURE RANGE | OFFSET VOLTAGE MAX (mV) |
|---|---|---|---|---|
| PGA202KP | 1, 10, 100, 1000 | Plastic DIP | 0°C to +70°C | ±(2 + 24/G) |
| PGA202AG | 1, 10, 100, 1000 | Ceramic DIP | –25°C to +85°C | ±(2 + 24/G) |
| PGA202BG | 1, 10, 100, 1000 | Ceramic DIP | –25°C to +85°C | ±(1 + 12/G) |
| PGA203KP | 1, 2, 4, 8 | Plastic DIP | 0°C to +70°C | ±(2 + 24/G) |
| PGA203AG | 1, 2, 4, 8 | Ceramic DIP | –25°C to +85°C | ±(2 + 24/G) |
| PGA203BG | 1, 2, 4, 8 | Ceramic DIP | –25°C to +85°C | ±(1 + 12/G) |

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

BURR - BROWN®



# PGA204
# PGA205

www.burr-brown.com/databook/PGA204.html



# Programmable Gain INSTRUMENTATION AMPLIFIER

## FEATURES

- DIGITALLY PROGRAMMABLE GAIN:
  PGA204: G=1, 10, 100, 1000V/V
  PGA205: G=1, 2, 4, 8V/V
- LOW OFFSET VOLTAGE: 50μV max
- LOW OFFSET VOLTAGE DRIFT: 0.25μV/°C
- LOW INPUT BIAS CURRENT: 2nA max
- LOW QUIESCENT CURRENT: 5.2mA typ
- NO LOGIC SUPPLY REQUIRED
- 16-PIN PLASTIC DIP, SOL-16 PACKAGES

## APPLICATIONS

- DATA ACQUISITION SYSTEM
- GENERAL PURPOSE ANALOG BOARDS
- MEDICAL INSTRUMENTATION

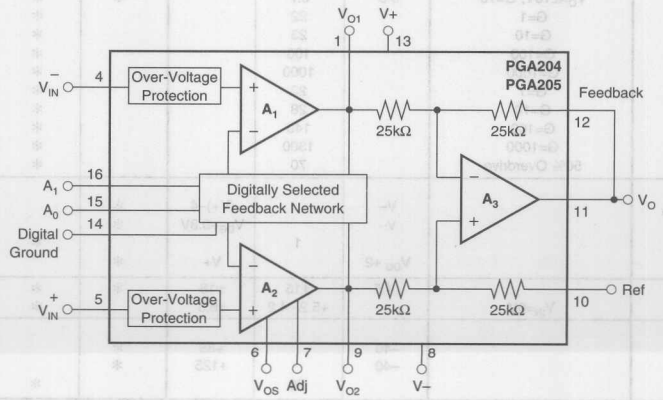
## DESCRIPTION

The PGA204 and PGA205 are low cost, general purpose programmable-gain instrumentation amplifiers offering excellent accuracy. Gains are digitally selected: PGA204—1, 10, 100, 1000, and PGA205—1, 2, 4, 8V/V. The precision and versatility, and low cost of the PGA204 and PGA205 make them ideal for a wide range of applications.

Gain is selected by two TTL or CMOS-compatible address lines, $A_0$ and $A_1$. Internal input protection can withstand up to ±40V on the analog inputs without damage.

The PGA204 and PGA205 are laser trimmed for very low offset voltage (50μV), drift (0.25μV/°C) and high common-mode rejection (115dB at G=1000). They operate with power supplies as low as ±4.5V, allowing use in battery operated systems. Quiescent current is 5mA.

The PGA204 and PGA205 are available in 16-pin plastic DIP, and SOL-16 surface-mount packages, specified for the –40°C to +85°C temperature range.




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# SPECIFICATIONS

## ELECTRICAL

**PGA204 G=1, 10, 100, 1000V/V**

At $T_A$ = +25°C, $V_S$ = ±15V, and $R_L$ = 2kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | PGA204BP, BU MIN | PGA204BP, BU TYP | PGA204BP, BU MAX | PGA204AP, AU MIN | PGA204AP, AU TYP | PGA204AP, AU MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | | |
| Offset Voltage, RTI | $T_A$=+25°C | | ±10+20/G | ±50+100/G | | ±25+30/G | ±125+500/G | µV |
| vs Temperature | $T_A$=$T_{MIN}$ to $T_{MAX}$ | | ±0.1+0.5/G | ±0.25+5/G | | ±0.25+5/G | ±1+10/G | µV/°C |
| vs Power Supply | $V_S$=±4.5V to ±18V | | 0.5+2/G | 3+10/G | | * | * | µV/V |
| Long-Term Stability | | | ±0.2+0.5/G | | | * | | µV/mo |
| Impedance, Differential | | | $10^{10}$\|\|6 | | | * | | Ω \|\| pF |
| Common-Mode | | | $10^{10}$\|\|6 | | | * | | Ω \|\| pF |
| Input Common-Mode Range | $V_O$=0V (see text) | ±10.5 | ±12.7 | | * | * | | V |
| Safe Input Voltage | | | | ±40 | | | * | V |
| Common-Mode Rejection | $V_{CM}$=±10V, $\Delta R_S$=1kΩ | | | | | | | |
| | G=1 | 80 | 99 | | 75 | 90 | | dB |
| | G=10 | 96 | 114 | | 90 | 106 | | dB |
| | G=100 | 110 | 123 | | 106 | 110 | | dB |
| | G=1000 | 115 | 123 | | 106 | 110 | | dB |
| **BIAS CURRENT** | | | ±0.5 | ±2 | | * | ±5 | nA |
| vs Temperature | | | ±8 | | | * | | pA/°C |
| Offset Current | | | ±0.5 | ±2 | | * | * | nA |
| vs Temperature | | | ±8 | | | * | | pA/°C |
| **NOISE**, Voltage, RTI[1]: f=10Hz | G≥100, $R_S$=0Ω | | 16 | | | * | | nV/√Hz |
| f=100Hz | G≥100, $R_S$=0Ω | | 13 | | | * | | nV/√Hz |
| f=1kHz | G≥100, $R_S$=0Ω | | 13 | | | * | | nV/√Hz |
| $f_B$=0.1Hz to 10Hz | G≥100, $R_S$=0Ω | | 0.4 | | | * | | µVp-p |
| Noise Current | | | | | | | | |
| f=10Hz | | | 0.4 | | | * | | pA/√Hz |
| f=1kHz | | | 0.2 | | | * | | pA/√Hz |
| $f_B$=0.1Hz to 10Hz | | | 18 | | | * | | pAp-p |
| **GAIN**, Error | G=1 | | ±0.005 | ±0.024 | | * | ±0.05 | % |
| | G=10 | | ±0.01 | ±0.024 | | * | ±0.05 | % |
| | G=100 | | ±0.01 | ±0.024 | | * | ±0.05 | % |
| | G=1000 | | ±0.02 | ±0.05 | | * | ±0.1 | % |
| Gain vs Temperature | G=1 to 1000 | | ±2.5 | ±10 | | * | * | ppm/°C |
| Nonlinearity | G=1 | | ±0.0004 | ±0.001 | | * | ±0.002 | % of FSR |
| | G=10 | | ±0.0004 | ±0.002 | | * | ±0.004 | % of FSR |
| | G=100 | | ±0.0004 | ±0.002 | | * | ±0.004 | % of FSR |
| | G=1000 | | ±0.0008 | ±0.01 | | * | ±0.02 | % of FSR |
| **OUTPUT** | | | | | | | | |
| Voltage, Positive[2] | $I_O$=5mA, $T_{MIN}$ to $T_{MAX}$ | (V+)–1.5 | (V+)–1.3 | | * | * | | V |
| Negative[2] | $I_O$=–5mA, $T_{MIN}$ to $T_{MAX}$ | (V–)+1.5 | (V–)+1.3 | | * | * | | V |
| Load Capacitance Stability | | | 1000 | | | * | | pF |
| Short Circuit Current | | | +23/–17 | | | * | | mA |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Bandwidth, –3dB | G=1 | | 1 | | | * | | MHz |
| | G=10 | | 80 | | | * | | kHz |
| | G=100 | | 10 | | | * | | kHz |
| | G=1000 | | 1 | | | * | | kHz |
| Slew Rate | $V_O$=±10V, G=10 | 0.3 | 0.7 | | * | * | | V/µs |
| Settling Time[3], 0.1% | G=1 | | 22 | | | * | | µs |
| | G=10 | | 23 | | | * | | µs |
| | G=100 | | 100 | | | * | | µs |
| | G=1000 | | 1000 | | | * | | µs |
| 0.01% | G=1 | | 23 | | | * | | µs |
| | G=10 | | 28 | | | * | | µs |
| | G=100 | | 140 | | | * | | µs |
| | G=1000 | | 1300 | | | * | | µs |
| Overload Recovery | 50% Overdrive | | 70 | | | * | | µs |
| **DIGITAL LOGIC** | | | | | | | | |
| Digital Ground Voltage, $V_{DG}$ | | V– | | (V+)–4 | * | | * | V |
| Digital Low Voltage | | V– | | $V_{DG}$+0.8V | * | | * | V |
| Digital Input Current | | | 1 | | | * | | µA |
| Digital High Voltage | | $V_{DG}$ +2 | | V+ | * | | * | V |
| **POWER SUPPLY**, Voltage | | ±4.5 | ±15 | ±18 | * | * | * | V |
| Current | $V_{IN}$=0V | | +5.2/–4.2 | ±6.5 | | * | ±7.5 | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –40 | | +85 | * | | * | °C |
| Operating | | –40 | | +125 | * | | * | °C |
| $\theta_{JA}$ | | | 80 | | | * | | °C/W |

* Specification same as PGA204BP.

NOTES: (1) Input-referred noise voltage varies with gain. See typical curves. (2) Output voltage swing is tested for ±10V min on ±11.4V power supplies. (3) Includes time to switch to a new gain.

# SPECIFICATIONS

## ELECTRICAL

**PGA205 G=1, 2, 4, 8V/V**

At $T_A$ = +25°C, $V_S$ = ±15V, and $R_L$ = 2kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | PGA205BP, BU MIN | PGA205BP, BU TYP | PGA205BP, BU MAX | PGA205AP, AU MIN | PGA205AP, AU TYP | PGA205AP, AU MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | | |
| Offset Voltage, RTI | $T_A$=+25°C | | ±10+20/G | ±50+100/G | | ±25+30/G | ±125+500/G | µV |
| vs Temperature | $T_A$=$T_{MIN}$ to $T_{MAX}$ | | ±0.1+0.5/G | ±0.25+5/G | | ±0.25+5/G | ±1+10/G | µV/°C |
| vs Power Supply | $V_S$=±4.5V to ±18V | | 0.5+2/G | 3+10/G | | * | * | µV/V |
| Long-Term Stability | | | ±0.2+0.5/G | | | * | | µV/mo |
| Impedance, Differential | | | $10^{10}$\|\|6 | | | * | | Ω\|\|pF |
| Common-Mode | | | $10^{10}$\|\|6 | | | * | | Ω\|\|pF |
| Input Common-Mode Range | $V_O$=0V (see text) | ±10.5 | ±12.7 | | * | * | | V |
| Safe Input Voltage | | | | ±40 | | | * | V |
| Common-Mode Rejection | $V_{CM}$=±10V, $\Delta R_S$=1kΩ | | | | | | | |
| | G=1 | 80 | 94 | | 75 | 88 | | dB |
| | G=2 | 85 | 100 | | 80 | 94 | | dB |
| | G=4 | 90 | 106 | | 85 | 100 | | dB |
| | G=8 | 95 | 112 | | 89 | 106 | | dB |
| **BIAS CURRENT** | | | ±0.5 | ±2 | | * | ±5 | nA |
| vs Temperature | | | ±8 | | | * | | pA/°C |
| Offset Current | | | ±0.5 | ±2 | | * | * | nA |
| vs Temperature | | | ±8 | | | * | | pA/°C |
| Noise Voltage, RTI[1]: f=10Hz | G=8, $R_S$=0Ω | | 19 | | | * | | nV/√Hz |
| f=100Hz | G=8, $R_S$=0Ω | | 15 | | | * | | nV/√Hz |
| f=1kHz | G=8, $R_S$=0Ω | | 15 | | | * | | nV/√Hz |
| $f_B$=0.1Hz to 10Hz | G=8, $R_S$=0Ω | | 0.5 | | | * | | µVp-p |
| Noise Current | | | | | | | | |
| f=10Hz | | | 0.4 | | | * | | pA/√Hz |
| f=1kHz | | | 0.2 | | | * | | pA/√Hz |
| $f_B$=0.1Hz to 10Hz | | | 18 | | | * | | pAp-p |
| **GAIN**, Error | G=1 | | ±0.005 | ±0.024 | | * | ±0.05 | % |
| | G=2 | | ±0.01 | ±0.024 | | * | ±0.05 | % |
| | G=4 | | ±0.01 | ±0.024 | | * | ±0.05 | % |
| | G=8 | | ±0.01 | ±0.024 | | * | ±0.05 | % |
| Gain vs Temperature | G=1 to 8 | | ±2.5 | ±10 | | * | * | ppm/°C |
| Nonlinearity | G=1 | | ±0.00024 | ±0.001 | | * | ±0.002 | % of FSR |
| | G=2 | | ±0.00024 | ±0.002 | | * | ±0.004 | % of FSR |
| | G=4 | | ±0.00024 | ±0.002 | | * | ±0.004 | % of FSR |
| | G=8 | | ±0.00024 | ±0.002 | | * | ±0.004 | % of FSR |
| **OUTPUT** | | | | | | | | |
| Voltage, Positive[2] | $I_O$=5mA, $T_{MIN}$ to $T_{MAX}$ | (V+)–1.5 | (V+)–1.3 | | * | * | | V |
| Negative[2] | $I_O$=–5mA, $T_{MIN}$ to $T_{MAX}$ | (V–)+1.5 | (V–)+1.3 | | * | * | | V |
| Load Capacitance Stability | | | 1000 | | | * | | pF |
| Short Circuit Current | | | +23/–17 | | | * | | mA |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Bandwidth, –3dB | G=1 | | 1 | | | * | | MHz |
| | G=2 | | 400 | | | * | | kHz |
| | G=4 | | 200 | | | * | | kHz |
| | G=8 | | 100 | | | * | | kHz |
| Slew Rate | $V_O$=±10V, G=8 | 0.3 | 0.7 | | * | * | | V/µs |
| Settling Time[3], 0.1% | G=1 | | 22 | | | * | | µs |
| | G=2 | | 22 | | | * | | µs |
| | G=4 | | 23 | | | * | | µs |
| | G=8 | | 23 | | | * | | µs |
| 0.01% | G=1 | | 23 | | | * | | µs |
| | G=2 | | 23 | | | * | | µs |
| | G=4 | | 25 | | | * | | µs |
| | G=8 | | 28 | | | * | | µs |
| Overload Recovery | 50% overdrive | | 70 | | | * | | µs |
| **DIGITAL LOGIC INPUTS** | | | | | | | | |
| Digital Ground Voltage, $V_{DG}$ | | V– | | (V+)–4 | * | | * | V |
| Digital Low Voltage | | V– | | $V_{DG}$+0.8V | * | | * | V |
| Digital Low Current | | | 1 | | | * | | µA |
| Digital High Voltage | | $V_{DG}$+2 | | V+ | * | | * | V |
| **POWER SUPPLY**, Voltage | | ±4.5 | ±15 | ±18 | * | * | * | V |
| Current | $V_{IN}$=0V | | +5.2/–4.2 | ±6.5 | | * | ±7.5 | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –40 | | +85 | * | | * | °C |
| Operating | | –40 | | +125 | * | | * | °C |
| $\theta_{JA}$ | | | 80 | | | * | | °C/W |

* Specification same as PGA204BP.

NOTES: (1) Input-referred noise voltage varies with gain. See typical curves. (2) Output voltage swing is tested for ±10V min on ±11.4V power supplies. (3) Includes time to switch to a new gain.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| PGA204AP | 16-Pin Plastic DIP | 180 |
| PGA204BP | 16-Pin Plastic DIP | 180 |
| PGA204AU | SOL-16 Surface Mount | 211 |
| PGA204BU | SOL-16 Surface Mount | 211 |
| PGA205AP | 16-Pin Plaseic DIP | 180 |
| PGA205BP | 16-Pin Plastic DIP | 180 |
| PGA205AU | SOL-16 Surface Mount | 211 |
| PGA205BU | SOL-16 Surface Mount | 211 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

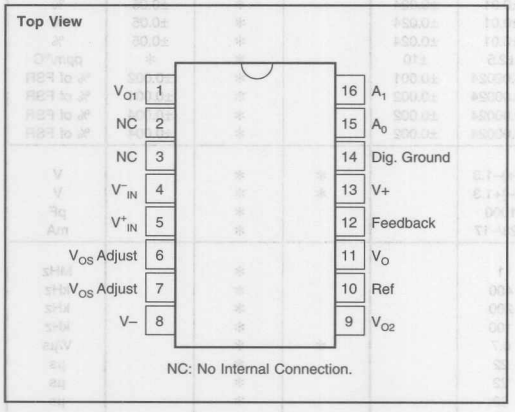
| | |
|---|---|
| Supply Voltage | ±18V |
| Analog Input Voltage Range | ±40V |
| Logic Input Voltage Range | $\pm V_S$ |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering –10s) | +300°C |

## ORDERING INFORMATION

| PRODUCT | GAINS | PACKAGE | TEMPERATURE RANGE |
|---|---|---|---|
| PGA204AP | 1, 10, 100, 1000V/V | 16-Pin Plastic DIP | –40 to +85°C |
| PGA204BP | 1, 10, 100, 1000V/V | 16-Pin Plastic DIP | –40 to +85°C |
| PGA204AU | 1, 10, 100, 1000V/V | SOL-16 Surface-Mount | –40 to +85°C |
| PGA204BU | 1, 10, 100, 1000V/V | SOL-16 Surface-Mount | –40 to +85°C |
| PGA205AP | 1, 2, 4, 8V/V | 16-Pin Plastic DIP | –40 to +85°C |
| PGA205BP | 1, 2, 4, 8V/V | 16-Pin Plastic DIP | –40 to +85°C |
| PGA205AU | 1, 2, 4, 8V/V | SOL-16 Surface-Mount | –40 to +85°C |
| PGA205BU | 1, 2, 4, 8V/V | SOL-16 Surface-Mount | –40 to +85°C |

## PIN CONFIGURATION

Top View




NC: No Internal Connection.

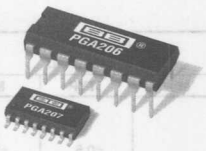
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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BURR - BROWN®



# PGA206
# PGA207

www.burr-brown.com/databook/PGA206.html



# High-Speed Programmable Gain INSTRUMENTATION AMPLIFIER

## FEATURES

- DIGITALLY PROGRAMMABLE GAINS:
  PGA206: G=1, 2, 4, 8V/V
  PGA207: G=1, 2, 5, 10V/V
- TRUE INSTRUMENTATION AMP INPUT
- FAST SETTLING: 3.5µs to 0.01%
- FET INPUT: $I_B$ = 100pA max
- INPUT PROTECTION: ±40V
- LOW OFFSET VOLTAGE: 1.5mV max
- 16-PIN DIP, SOL-16 SOIC PACKAGES

## APPLICATIONS

- MULTIPLE-CHANNEL DATA ACQUISITION
- MEDICAL, PHYSIOLOGICAL AMPLIFIER
- PC-CONTROLLED ANALOG INPUT BOARDS

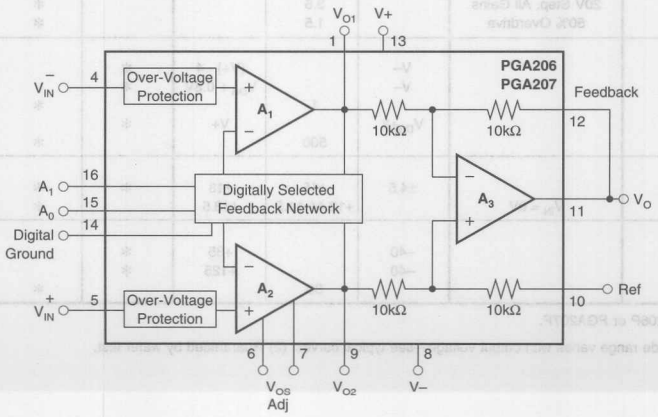
## DESCRIPTION

The PGA206 and PGA207 are digitally programmable gain instrumentation amplifiers that are ideally suited for data acquisition systems.

The PGA206 and PGA207's fast settling time allows multiplexed input channels for excellent system efficiency. FET inputs eliminate $I_B$ errors due to analog multiplexer series resistance.

Gains are selected by two CMOS/TTL-compatible address lines. Analog inputs are internally protected for overloads up to ±40V, even with the power supplies off. The PGA206 and PGA207 are laser-trimmed for low offset voltage and low drift.

The PGA206 and PGA207 are available in 16-pin plastic DIP and SOL-16 surface-mount packages. Both are specified for –40°C to +85°C operation.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 2kΩ unless otherwise noted.

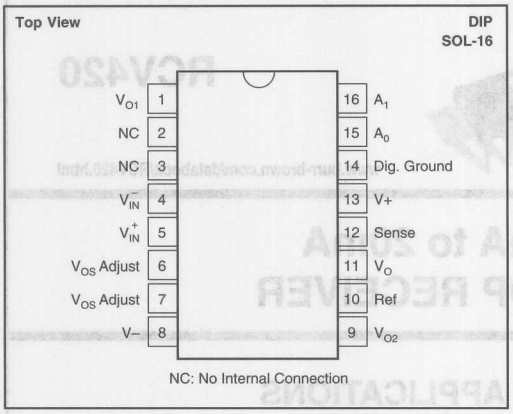
| PARAMETER | CONDITIONS | PGA206P, U PGA207P, U MIN | PGA206P, U PGA207P, U TYP | PGA206P, U PGA207P, U MAX | PGA206PA, UA PGA207PA, UA MIN | PGA206PA, UA PGA207PA, UA TYP | PGA206PA, UA PGA207PA, UA MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | | |
| Offset Voltage, RTI | All Gains | | | | | | | |
| Initial | $T_A$ = +25°C | | ±0.5 | ±1.5 | | ±1 | ±2.5 | mV |
| vs Temperature | $T_A = T_{MIN}$ to $T_{MAX}$, G = 8, 10 | | ±2 | | | * | | µV/°C |
| vs Power Supply | $V_S$ = ±4.5V to ±18V | | ±5 | ±20 | | ±10 | ±40 | µV/V |
| Long-Term Stability | | | 4.5 | | | * | | µV/mo |
| Impedance, Differential | | | $10^{13}$ \|\| 1 | | | * | | Ω \|\| pF |
| Common-Mode | | | $10^{12}$ \|\| 4 | | | * | | Ω \|\| pF |
| Common-Mode Voltage Range[1] | $V_O$ = 0V | ±($IV_S$I–4) | ±($IV_S$I –2.5) | | * | * | | V |
| Safe Input Voltage | | | | ±40 | | | * | V |
| Common-Mode Rejection | $V_{CM}$ = ±11V, $\Delta R_S$ = 1kΩ | | | | | | | |
| | G = 1 | 80 | 92 | | 75 | 86 | | dB |
| | G = 2 | 85 | 96 | | 80 | 90 | | dB |
| | G = 4 or 5 | 90 | 100 | | 84 | 94 | | dB |
| | G = 8 or 10 | 95 | 100 | | 84 | 94 | | dB |
| **INPUT BIAS CURRENT** | $V_{IN}$ = 0 | | 2 | 100 | | * | * | pA |
| vs Temperature | | | See Typical Curve | | | * | | |
| Offset Current | | | 1 | 100 | | * | * | pA |
| vs Temperature | | | See Typical Curve | | | * | | |
| **NOISE VOLTAGE, RTI** | G = 8,10; $R_S$ = 0Ω | | | | | | | |
| f = 10Hz | | | 30 | | | * | | nV/√Hz |
| f = 100Hz | | | 20 | | | * | | nV/√Hz |
| f = 1kHz | | | 18 | | | * | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 1 | | | * | | µVp-p |
| Noise Current | | | | | | | | |
| f = 1kHz | | | 1.5 | | | * | | fA/√Hz |
| **GAIN** | All Gains, $V_O$ = ±11V | | | | | | | |
| Gain Error | | | ±0.01 | ±0.05 | | * | ±0.1 | % |
| Gain vs Temperature[2] | | | ±1 | ±10 | | * | * | ppm/°C |
| Nonlinearity | | | ±0.0003 | ±0.002 | | * | ±0.005 | % of FSR |
| **OUTPUT** | | | | | | | | |
| Voltage, Positive | | (V+) –4 | (V+) –2.3 | | * | * | | V |
| Negative | | (V–) +4 | (V–) +1.5 | | * | * | | V |
| Load Capacitance Stability | | | 1000 | | | * | | pF |
| Short-Circuit Current | | | ±17 | | | * | | mA |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Bandwidth, –3dB | G = 1 | | 5 | | | * | | MHz |
| | G = 2 | | 4 | | | * | | MHz |
| | G = 4, 5 | | 1.3 | | | * | | MHz |
| | G = 8, 10 | | 600 | | | * | | kHz |
| Slew Rate | $V_O$ = ±10V, G = 1 to 10 | | 25 | | | * | | V/µs |
| Settling Time, 0.1% | 20V Step, All Gains | | 2 | | | * | | µs |
| 0.01% | 20V Step, All Gains | | 3.5 | | | * | | µs |
| Output Overload Recovery | 50% Overdrive | | 1.5 | | | * | | µs |
| **DIGITAL LOGIC INPUTS** | | | | | | | | |
| Digital Ground Voltage, $V_{DG}$ | | V– | | (V+) –4 | * | | * | V |
| Digital Low Voltage | | V– | | $V_{DG}$ + 0.8V | * | | * | V |
| Digital Input Current | | | 1 | | | * | | pA |
| Digital High Voltage | | $V_{DG}$+2 | | V+ | * | | * | V |
| Gain Switching Time | | | 500 | | | * | | ns |
| **POWER SUPPLY** | | | | | | | | |
| Voltage Range | | ±4.5 | ±15 | ±18 | * | * | * | V |
| Current | $V_{IN}$ = 0V | | +12.4/–11.2 | ±13.5 | | * | | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –40 | | +85 | * | | * | °C |
| Operating | | –40 | | +125 | * | | * | °C |
| Thermal Resistance, $\theta_{JA}$ | | | 80 | | | * | | °C/W |

* Specification same as PGA206P or PGA207P.

NOTES: (1) Input common-mode range varies with output voltage—see typical curves. (2) Guaranteed by wafer test.

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## PIN CONFIGURATION




NC: No Internal Connection

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Analog Input Voltage Range | ±40V |
| Logic Input Voltage Range | $\pm V_S$ |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering –10s) | +300°C |

## ORDERING INFORMATION

| PRODUCT | GAINS | PACKAGE | TEMPERATURE RANGE |
|---|---|---|---|
| PGA206PA | 1, 2, 4, 8V/V | 16-Pin Plastic DIP | –40°C to +85°C |
| PGA206P | 1, 2, 4, 8V/V | 16-Pin Plastic DIP | –40°C to +85°C |
| PGA206UA | 1, 2, 4, 8V/V | SOL-16 Surface-Mount | –40°C to +85°C |
| PGA206U | 1, 2, 4, 8V/V | SOL-16 Surface-Mount | –40°C to +85°C |
| PGA207PA | 1, 2, 5, 10V/V | 16-Pin Plastic DIP | –40°C to +85°C |
| PGA207P | 1, 2, 5, 10V/V | 16-Pin Plastic DIP | –40°C to +85°C |
| PGA207UA | 1, 2, 5, 10V/V | SOL-16 Surface-Mount | –40°C to +85°C |
| PGA207U | 1, 2, 5, 10V/V | SOL-16 Surface-Mount | –40°C to +85°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| PGA206PA | 16-Pin Plastic DIP | 180 |
| PGA206P | 16-Pin Plastic DIP | 180 |
| PGA206UA | SOL-16 Surface Mount | 211 |
| PGA206U | SOL-16 Surface Mount | 211 |
| PGA207PA | 16-Pin Plastic DIP | 180 |
| PGA207P | 16-Pin Plastic DIP | 180 |
| PGA207UA | SOL-16 Surface Mount | 211 |
| PGA207U | SOL-16 Surface Mount | 211 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®




# RCV420

www.burr-brown.com/databook/RCV420.html

# Precision 4mA to 20mA CURRENT LOOP RECEIVER

## FEATURES

- COMPLETE 4-20mA TO 0-5V CONVERSION
- INTERNAL SENSE RESISTORS
- PRECISION 10V REFERENCE
- BUILT-IN LEVEL-SHIFTING
- ±40V COMMON-MODE INPUT RANGE
- 0.1% OVERALL CONVERSION ACCURACY
- HIGH NOISE IMMUNITY: 86dB CMR

## APPLICATIONS

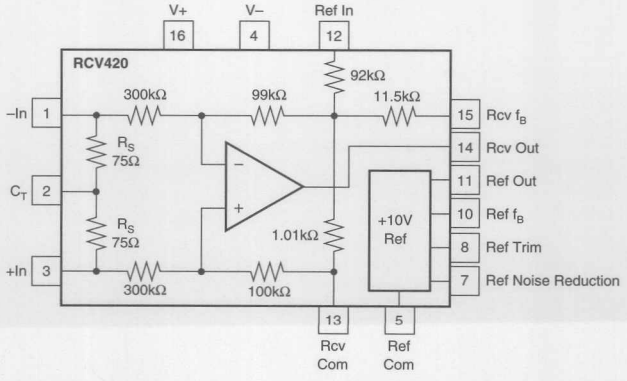
- PROCESS CONTROL
- INDUSTRIAL CONTROL
- FACTORY AUTOMATION
- DATA ACQUISITION
- SCADA
- RTUs
- ESD
- MACHINE MONITORING

## DESCRIPTION

The RCV420 is a precision current-loop receiver designed to convert a 4–20mA input signal into a 0–5V output signal. As a monolithic circuit, it offers high reliability at low cost. The circuit consists of a premium grade operational amplifier, an on-chip precision resistor network, and a precision 10V reference. The RCV420 features 0.1% overall conversion accuracy, 86dB CMR, and ±40V common-mode input range.

The circuit introduces only a 1.5V drop at full scale, which is useful in loops containing extra instrument burdens or in intrinsically safe applications where transmitter compliance voltage is at a premium. The 10V reference provides a precise 10V output with a typical drift of 5ppm/°C.

The RCV420 is completely self-contained and offers a highly versatile function. No adjustments are needed for gain, offset, or CMR. This provides three important advantages over discrete, board-level designs: 1) lower initial design cost, 2) lower manufacturing cost, and 3) easy, cost-effective field repair of a precision circuit.




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# SPECIFICATIONS

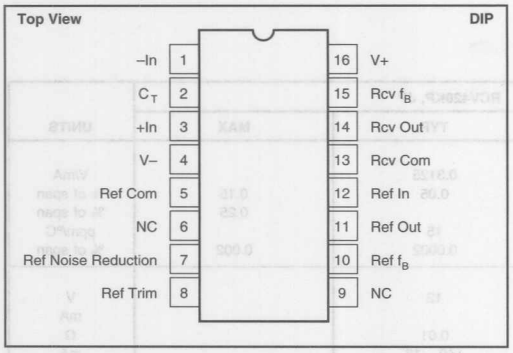
## ELECTRICAL

At T = +25°C and $V_S$ = ±15V, unless otherwise noted.

| CHARACTERISTICS | RCV420KP, JP MIN | RCV420KP, JP TYP | RCV420KP, JP MAX | UNITS |
|---|---|---|---|---|
| **GAIN** | | | | |
| Initial | | 0.3125 | | V/mA |
| Error | | 0.05 | 0.15 | % of span |
| Error—JP Grade | | | 0.25 | % of span |
| vs Temp | | 15 | | ppm/°C |
| Nonlinearity[1] | | 0.0002 | 0.002 | % of span |
| **OUTPUT** | | | | |
| Rated Voltage ($I_O$ = +10mA, –5mA) | 10 | 12 | | V |
| Rated Current ($E_O$ = 10V) | +10, –5 | | | mA |
| Impedance (Differential) | | 0.01 | | Ω |
| Current Limit (To Common) | | +49, –13 | | mA |
| Capacitive Load (Stable Operation) | | 1000 | | pF |
| **INPUT** | | | | |
| Sense Resistance | 74.25 | 75 | 75.75 | Ω |
| Input Impedance (Common-Mode) | | 200 | | kΩ |
| Common-Mode Voltage | | | ±40 | V |
| CMR[2] | 70 | 80 | | dB |
| vs Temp (DC) ($T_A$ = $T_{MIN}$ to $T_{MAX}$) | | 76 | | dB |
| AC 60Hz | | 80 | | dB |
| **OFFSET VOLTAGE (RTO)[3]** | | | | |
| Initial | | | 1 | mV |
| vs Temp | | 10 | | µV/°C |
| vs Supply (±11.4V to ±18V) | 74 | 90 | | dB |
| vs Time | | 200 | | µV/mo |
| **ZERO ERROR[4]** | | | | |
| Initial | | 0.025 | 0.075 | % of span |
| Initial—JP Grade | | | 0.15 | % of span |
| vs Temp | | 10 | | ppm of span/°C |
| **OUTPUT NOISE VOLTAGE** | | | | |
| $f_B$ = 0.1Hz to 10Hz | | 50 | | µVp-p |
| $f_O$ = 10kHz | | 800 | | nV/√Hz |
| **DYNAMIC RESPONSE** | | | | |
| Gain Bandwidth | | 150 | | kHz |
| Full Power Bandwidth | | 30 | | kHz |
| Slew Rate | | 1.5 | | V/µs |
| Settling Time (0.01%) | | 10 | | µs |
| **VOLTAGE REFERENCE** | | | | |
| Initial | 9.99 | | 10.01 | V |
| Trim Range[5] | | ±4 | | % |
| vs Temp | | 5 | | ppm/°C |
| vs Supply (±11.4V to ±18V) | | 0.0002 | | %/V |
| vs Output Current ($I_O$ = 0 to +10mA) | | 0.0002 | | %/mA |
| vs Time | | 15 | | ppm/kHz |
| Noise (0.1Hz to 10Hz) | | 5 | | µVp-p |
| Output Current | +10, –2 | | | mA |
| **POWER SUPPLY** | | | | |
| Rated | | ±15 | | V |
| Voltage Range[6] | –5, +11.4 | | ±18 | V |
| Quiescent Current ($V_O$ = 0V) | | 3 | 4 | mA |
| **TEMPERATURE RANGE** | | | | |
| Specification | 0 | | +70 | °C |
| Operation | –25 | | +85 | °C |
| Storage | –40 | | +85 | °C |
| Thermal Resistance, $\theta_{JA}$ | | 80 | | °C/W |

NOTES: (1) Nonlinearity is the max peak deviation from best fit straight line. (2) With 0 source impedance on Rcv Com pin. (3) Referred to output with all inputs grounded including Ref In. (4) With 4mA input signal and Voltage Reference connected (includes $V_{OS}$, Gain Error, and Voltage Reference Errors). (5) External trim slightly affects drift. (6) $I_O$ Ref = 5mA, $I_O$ Rcv = 2mA.

## PIN CONFIGURATION




## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Supply | ±22V |
| Input Current, Continuous | 40mA |
| Input Current Momentary, 0.1s | 250mA, 1% Duty Cycle |
| Common-Mode Input Voltage, Continuous | ±40V |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short Circuit to Common (Rcv and Ref) | Continuous |

NOTE: (1) Stresses above these ratings may cause permanent damage.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| RCV420KP | 16-Pin Plastic DIP | 180 |
| RCV420JP | 16-Pin Plastic DIP | 180 |

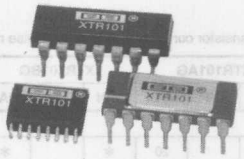
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

| PRODUCT | PERFORMANCE GRADE | PACKAGE |
|---|---|---|
| RCV420KP | 0°C to +70°C | 16-Pin Plastic DIP |
| RCV420JP | 0°C to +70°C | 16-Pin Plastic DIP |

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# XTR101

www.burr-brown.com/databook/XTR101.html

# Precision, Low Drift 4-20mA TWO-WIRE TRANSMITTER



## FEATURES

- INSTRUMENTATION AMPLIFIER INPUT
  - Low Offset Voltage, 30µV max
  - Low Voltage Drift, 0.75µV/°C max
  - Low Nonlinearity, 0.01% max
- TRUE TWO-WIRE OPERATION
  - Power and Signal on One Wire Pair
  - Current Mode Signal Transmission
  - High Noise Immunity
- DUAL MATCHED CURRENT SOURCES
- WIDE SUPPLY RANGE: 11.6V to 40V
- –40°C to +85°C SPECIFICATION RANGE
- SMALL 14-PIN DIP PACKAGE, CERAMIC AND PLASTIC

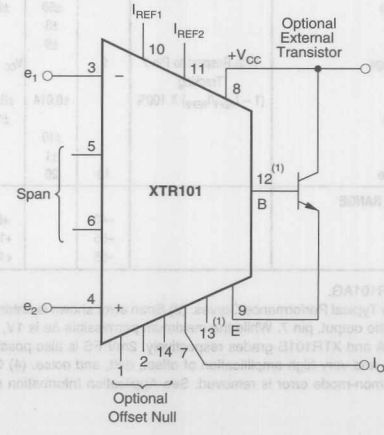
## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  - Pressure Transmitters
  - Temperature Transmitters
  - Millivolt Transmitters
- RESISTANCE BRIDGE INPUTS
- THERMOCOUPLE INPUTS
- RTD INPUTS
- CURRENT SHUNT (mV) INPUTS
- PRECISION DUAL CURRENT SOURCES
- AUTOMATED MANUFACTURING
- POWER/PLANT ENERGY SYSTEM MONITORING

## DESCRIPTION

The XTR101 is a microcircuit, 4-20mA, two-wire transmitter containing a high accuracy instrumentation amplifier (IA), a voltage-controlled output current source, and dual-matched precision current reference. This combination is ideally suited for remote signal conditioning of a wide variety of transducers such as thermocouples, RTDs, thermistors, and strain gauge bridges. State-of-the-art design and laser-trimming, wide temperature range operation and small size make it very suitable for industrial process control applications. In addition, the optional external transistor allows even higher precision.

The two-wire transmitter allows signal and power to be supplied on a single wire-pair by modulating the power supply current with the input signal source. The transmitter is immune to voltage drops from long runs and noise from motors, relays, actuators, switches, transformers, and industrial equipment. It can be used by OEMs producing transmitter modules or by data acquisition system manufacturers.




NOTE: (1) Pins 12 and 13 are used for optional BW control.

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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, +$V_{CC}$ = 24VDC, and $R_L$ = 100Ω with external transistor connected, unless otherwise noted

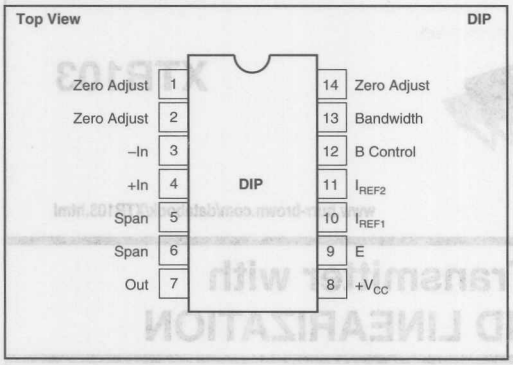
| PARAMETER | CONDITIONS | XTR101AG | | | XTR101BG | | | XTR101AP | | | XTR101AU | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OUTPUT AND LOAD CHARACTERISTICS** | | | | | | | | | | | | | | |
| Current | Linear Operating Region | 4 | | 20 | * | | * | * | | * | * | | * | mA |
| | Derated Performance | 3.8 | | 22 | * | | * | * | | * | * | | * | mA |
| Current Limit | | | 28 | 38 | | * | * | | 31 | * | | 31 | * | mA |
| Offset Current Error | $I_{OS}$, $I_O$ = 4mA | | ±3.9 | ±10 | | ±2.5 | ±6 | | ±8.5 | ±19 | | ±8.5 | ±19 | µA |
| vs Temperature | $\Delta I_{OS}/\Delta T$ | | ±10.5 | ±20 | | ±8 | ±15 | | ±10.5 | ±20 | | * | | ppm, FS/°C |
| Full Scale Output Current Error | Full Scale = 20mA | | ±20 | ±40 | | ±15 | ±30 | | ±30 | ±60 | | ±30 | ±60 | µA |
| Power Supply Voltage | $V_{CC}$, Pins 7 and 8, Compliance[1] | +11.6 | | ±40 | * | | * | * | | * | * | | * | VDC |
| Load Resistance | At $V_{CC}$ = +24V, $I_O$ = 20mA | | | 600 | | | * | | | 600 | | | * | Ω |
| | At $V_{CC}$ = +40V, $I_O$ = 20mA | | | 1400 | | | * | | | 1400 | | | * | Ω |
| **SPAN** | | | | | | | | | | | | | | |
| Output Current Equation | $R_S$ in Ω, $e_1$ and $e_2$ in V | | | | | $i_O = 4mA + [0.016Ω + (40/R_S)] (e_2 - e_1)$ | | | | | | | | |
| Span Equation | $R_S$ in Ω | | | | | $S = [0.016Ω + (40/R_S)]$ | | | | | | | | A/V |
| vs Temperature | Excluding TCR of $R_S$ | | ±30 | ±100 | | * | * | | * | * | | * | * | ppm/°C |
| Untrimmed Error[2] | $\varepsilon_{SPAN}$ | –5 | –2.5 | 0 | * | * | * | * | * | * | * | * | * | % |
| Nonlinearity | $\varepsilon_{NONLINEARITY}$ | | | 0.01 | | | * | | | * | | | * | % |
| Hysteresis | | | 0 | | | * | | | * | | | * | | % |
| Dead Band | | | 0 | | | * | | | * | | | * | | % |
| **INPUT CHARACTERISTICS** | | | | | | | | | | | | | | |
| Impedance: Differential | | | 0.4 ll 3 | | | * | | | * | | | * | | GΩ ll pF |
| Common-Mode | | | 10 ll 3 | | | * | | | * | | | * | | GΩ ll pF |
| Voltage Range, Full Scale | $\Delta e = (e_2 - e_1)$[3] | 0 | | 1 | * | | * | * | | * | * | | * | V |
| Offset Voltage | $V_{OS}$ | | ±30 | ±60 | | ±20 | ±30 | | * | ±100 | | * | ±100 | µV |
| vs Temperature | $\Delta V_{OS}/\Delta T$ | | ±0.75 | ±1.5 | | ±0.35 | ±0.75 | | * | * | | * | * | µV/°C |
| Power Supply Rejection | $\Delta V_{CC}/PSRR = V_{OS}$ Error | 110 | 125 | | * | * | | * | 122 | | 110 | 122 | | dB |
| Bias Current | $I_B$ | | 60 | 150 | | * | * | | * | * | | * | * | nA |
| vs Temperature | $\Delta I_B/\Delta T$ | | 0.30 | 1 | | * | * | | * | * | | * | * | nA/°C |
| Offset Current | $I_{OSI}$ | | 10 | ±30 | | * | ±20 | | * | * | | * | * | nA |
| vs Temperature | $\Delta I_{OS}/\Delta T$ | | 0.1 | 0.3 | | * | * | | * | * | | * | * | nA/°C |
| Common-Mode Rejection[4] | DC | 90 | 100 | | * | * | | * | * | | * | * | | dB |
| Common-Mode Range | $e_1$ and $e_2$ with Respect to Pin 7 | 4 | | 6 | * | | * | * | | * | * | | * | V |
| **CURRENT SOURCES** | | | | | | | | | | | | | | |
| Magnitude | | | 1 | | | * | | | * | | | * | | mA |
| Accuracy | $V_{CC}$ = 24V, $V_{PIN\ 8} - V_{PIN\ 10,11}$ = 19V | | | | | | | | | | | | | |
| | $R_2$ = 5kΩ, Fig. 5 | | ±0.06 | ±0.17 | | ±0.025 | ±0.075 | | ±0.2 | ±0.37 | | ±0.2 | ±0.37 | % |
| vs Temperature | | | ±50 | ±80 | | ±30 | ±50 | | * | * | | * | * | ppm/°C |
| vs $V_{CC}$ | | | ±3 | | | * | | | * | | | * | | ppm/V |
| vs Time | | | ±8 | | | * | | | * | | | * | | ppm/month |
| Compliance Voltage | With Respect to Pin 7 | 0 | | $V_{CC}$ – 3.5 | * | * | * | * | | * | * | | * | V |
| Ratio Match | Tracking | | | | | | | | | | | | | |
| Accuracy | $(1 - I_{REF1}/I_{REF2})$ X 100% | | ±0.014 | ±0.06 | | ±0.009 | ±0.04 | | ±0.031 | ±0.088 | | ±0.031 | ±0.088 | % |
| vs Tempeature | | | | ±15 | | | 10 | | | * | | | * | ppm/°C |
| vs $V_{CC}$ | | | ±10 | | | * | | | * | | | * | | ppm/V |
| vs Time | | | ±1 | | | * | | | * | | | * | | ppm/month |
| Output Impedance | | 10 | 20 | | * | * | | * | 15 | | * | 15 | | MΩ |
| **TEMPERATURE RANGE** | | | | | | | | | | | | | | |
| Specification | | –40 | | +85 | * | | * | –40 | | +85 | * | | * | °C |
| Operating | | –55 | | +125 | * | | * | –40 | | +85 | –40 | | +85 | °C |
| Storage | | –55 | | +165 | * | | * | –55 | | +125 | –55 | | +125 | °C |

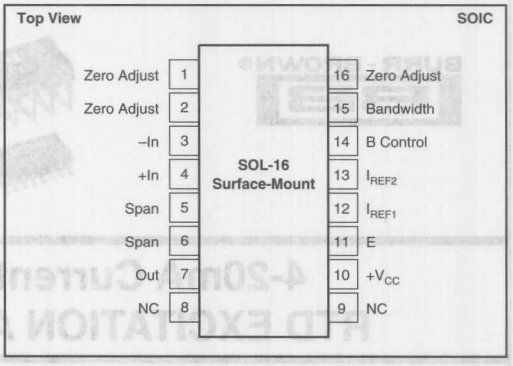
* Same as XTR101AG.

NOTES: (1) See Typical Performance Curves. (2) Span error shown is untrimmed and may be adjusted to zero. (3) $e_1$ and $e_2$ are signals on the –In and +In terminals with respect to the output, pin 7. While the maximum permissible Δe is 1V, it is primarily intended for much lower input signal levels, e.g., 10mV or 50mV full scale for the XTR101A and XTR101B grades respectively. 2mV FS is also possible with the B grade, but accuracy will degrade due to possible errors in the low value span resistance and very high amplification of offset, drift, and noise. (4) Offset voltage is trimmed with the application of a 5V common-mode voltage. Thus the associated common-mode error is removed. See Application Information section.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN CONFIGURATION




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply, $+V_{CC}$ | 40V |
| Input Voltage, $e_1$ or $e_2$ | $\geq V_{OUT}$, $\leq +V_{CC}$ |
| Storage Temperature Range, Ceramic | –55°C to +165°C |
| Plastic | –55°C to +125°C |
| Lead Temperature (soldering 10s) G, P | +300°C |
| (wave soldering, 3s) U | +260°C |
| Output Short-Circuit Duration | Continuous $+V_{CC}$ to $I_{OUT}$ |
| Junction Temperature | +165°C |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| XTR101AG | 14-Pin Ceramic DIP | 169 | –40°C to +85°C |
| XTR101BG | 14-Pin Ceramic DIP | 169 | –40°C to +85°C |
| XTR101AP | 14-Pin Plastic DIP | 010 | –40°C to +85°C |
| XTR101AU | 16-Lead SOIC | 211 | –40°C to +85°C |

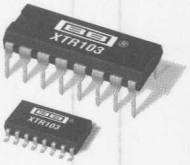
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# XTR103

www.burr-brown.com/databook/XTR103.html

# 4-20mA Current Transmitter with RTD EXCITATION AND LINEARIZATION

## FEATURES

- LESS THAN ±1% TOTAL ADJUSTED ERROR, –40°C TO +85°C
- RTD EXCITATION AND LINEARIZATION
- TWO OR THREE-WIRE RTD OPERATION
- WIDE SUPPLY RANGE: 9V to 40V
- HIGH PSR: 110dB min
- HIGH CMR: 80dB min

## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- FACTORY AUTOMATION
- SCADA

## DESCRIPTION

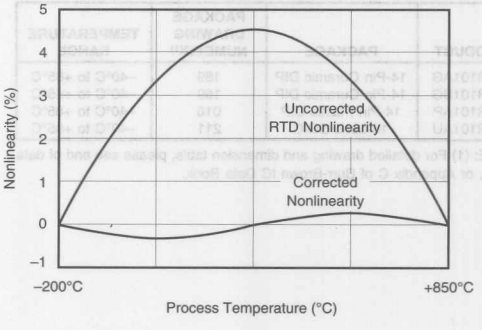
The XTR103 is a monolithic 4-20mA, two-wire current transmitter designed for Platinum RTD temperature sensors. It provides complete RTD current excitation, instrumentation amplifier, linearization, and current output circuitry on a single integrated circuit.

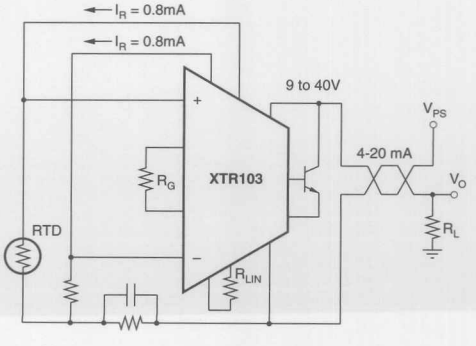
Versatile linearization circuitry provides a 2nd-order correction to the RTD, typically achieving a 40:1 improvement in linearity.

Instrumentation amplifier gain can be configured for a wide range of temperature measurements. Total adjusted error of the complete current transmitter, including the linearized RTD is less than ±1% over the full –40 to +85°C operating temperature range. This includes zero drift, span drift and nonlinearity. The XTR103 operates on loop power supply voltages down to 9V.

The XTR103 is available in 16-pin plastic DIP and SOL-16 surface-mount packages specified for the –40°C to +85°C temperature range.

Pt100 NONLINEARITY CORRECTION
USING XTR103




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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, V+ = 24V, and 2N6121 external transistor, unless otherwise noted.

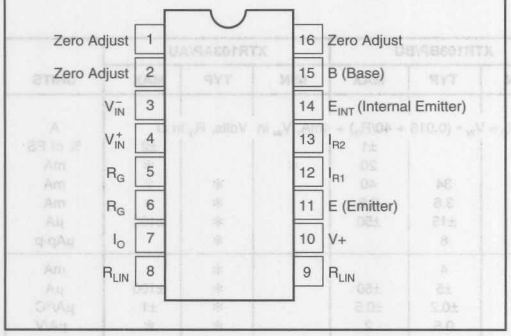
| PARAMETER | CONDITIONS | XTR103BP/BU MIN | XTR103BP/BU TYP | XTR103BP/BU MAX | XTR103AP/AU MIN | XTR103AP/AU TYP | XTR103AP/AU MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | | | |
| Output Current Equation | | | $I_O = V_{IN} \bullet (0.016 + 40/R_G) + 4mA$, $V_{IN}$ in Volts, $R_G$ in Ω | | | | | A |
| Total Adjusted Error[1] | $T_{MIN}$ to $T_{MAX}$ | | | ±1 | | | ±2 | % of FS |
| Output Current, Specified Range | | 4 | | 20 | * | | * | mA |
| Over-Scale Limit | | | 34 | 40 | | * | * | mA |
| Under Scale-Limit | | | 3.6 | 3.8 | | * | * | mA |
| Full Scale Output Error | $V_{IN}$ = 1V, $R_G$ = ∞ | | ±15 | ±50 | | * | ±100 | µA |
| Noise: 0.1Hz to 1kHz | $R_G$ = 40Ω | | 8 | | | * | | µAp-p |
| **ZERO OUTPUT**[2] | $V_{IN}$ = 0, $R_G$ = ∞ | | 4 | | | * | | mA |
| Initial Error | | | ±5 | ±50 | | * | ±100 | µA |
| vs Temperature | | | ±0.2 | ±0.5 | | * | ±1 | µA/°C |
| vs Supply Voltage, V+ | V+ = 9V to 40V[3] | | 0.5 | 2 | | * | * | µA/V |
| vs Common-Mode Voltage | $V_{CM}$ = 2V to 4V[3] | | 0.1 | 2 | | * | * | µA/V |
| **SPAN** | | | | | | | | |
| Span Equation (Transconductance) | | | $S = 0.016 + 40/R_G$ | | | * | | A/V |
| Untrimmed Error | $R_G \geq 75Ω$ | | ±0.1 | ±1 | | * | * | % |
| vs Temperature[4] | | | ±20 | ±50 | | * | ±100 | ppm/°C |
| Nonlinearity: Ideal Input | | | | 0.01 | | | * | % |
| RTD Input | Pt100: –200°C to +850°C<br>$R_{LIN}$ = 1127Ω | | 0.1 | | | | * | % |
| **INPUT** | | | | | | | | |
| Differential Range | $R_G$ = ∞ | | | 1 | | | * | V |
| Input Voltage Range[3] | | 2 | | 4 | * | | * | V |
| Common-Mode Rejection | $V_{IN}$ = 2V to 4V[3] | 80 | 100 | | * | * | | dB |
| Impedance: Differential | | | 3 | | | * | | GΩ |
| Common-Mode | | | 0.5 | | | * | | GΩ |
| Offset Voltage | | | ±0.5 | ±2.5 | | * | * | mV |
| vs Temperature | | | ±1 | ±2.5 | | ±2 | ±5 | µV/°C |
| vs Supply Voltage, V+ | V+ = 9V to 40V[3] | 110 | 130 | | * | * | | dB |
| Input Bias Current | | | 100 | 250 | | * | * | nA |
| vs Temperature | | | 0.1 | 2 | | * | * | nA/°C |
| Input Offset Current | | | 2 | 20 | | * | * | nA |
| vs Temperature | | | 0.01 | 0.25 | | * | * | nA/°C |
| **CURRENT SOURCES**[5] | | | | | | | | |
| Current | | | 0.8 | | | * | | mA |
| Accuracy | | | ±0.25 | ±0.5 | | * | ±1 | % |
| vs Temperature | | | ±25 | ±50 | | ±50 | ±100 | ppm/°C |
| vs Power Supply, V+ | V+ = 9V to 40V[3] | | 50 | | | * | | ppm/V |
| Compliance Voltage[3] | | $(V^-_{IN})$ – 0.2 | | (V+) – 5 | * | | * | V |
| Matching | | | | ±0.5 | | | * | % |
| vs Temperature | | | ±10 | ±25 | | * | ±50 | ppm/°C |
| vs Power Supply, V+ | V+ = 9V to 40V[3] | | 10 | | | * | | ppm/V |
| **POWER SUPPLY** | | | | | | | | |
| Voltage Range[3], V+ | | 9 | | 40 | * | | * | V |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification, $T_{MIN}$ to $T_{MAX}$ | | –40 | | 85 | * | | * | °C |
| Operating | | –40 | | 125 | * | | * | °C |
| $\theta_{JA}$ | | | 80 | | | * | | °C/W |

* Specification same as XTR103BP.

NOTES: (1) Includes corrected Pt100 nonlinearity for process measurement spans greater than 100°C, and over-temperature zero and span effects. Does not include initial offset and gain errors which are normally trimmed to zero at 25°C. (2) Describes accuracy of the 4mA low-scale offset current. Does not include input amplifier effects. Can be trimmed to zero. (3) Voltage measured with respect to $I_O$ pin. (4) Does not include TCR of gain-setting resistor, $R_G$. (5) Measured with $R_{LIN}$ = ∞ to disable linearization feature.

## PIN CONFIGURATION

**TOP VIEW**




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply, V+ (referenced to $I_O$ pin) | 40V |
| Input Voltage, $V^+_{IN}$, $V^-_{IN}$ (referenced to $I_O$ pin) | 0V to V+ |
| Storage Temperature Range | –55°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Current Limit | Continuous |
| Junction Temperature | +165°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

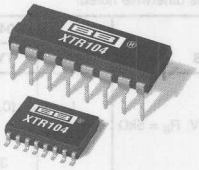
## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| XTR103AP | 16-pin Plastic DIP | 180 | –40°C to +85°C |
| XTR103BP | 16-pin Plastic DIP | 180 | –40°C to +85°C |
| XTR103AU | SOL-16 Surface Mount | 211 | –40°C to +85°C |
| XTR103BU | SOL-16 Surface Mount | 211 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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# XTR104

www.burr-brown.com/databook/XTR104.html

# 4-20mA Current Transmitter with BRIDGE EXCITATION AND LINEARIZATION



## FEATURES

- LESS THAN ±1% TOTAL ADJUSTED ERROR, –40°C TO +85°C
- BRIDGE EXCITATION AND LINEARIZATION
- WIDE SUPPLY RANGE: 9V to 40V
- LOW SPAN DRIFT: 50ppm/°C max
- HIGH PSR: 110dB min
- HIGH CMR: 80dB min

## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- FACTORY AUTOMATION
- SCADA
- WEIGHTING SYSTEMS
- ACCELEROMETERS

## DESCRIPTION

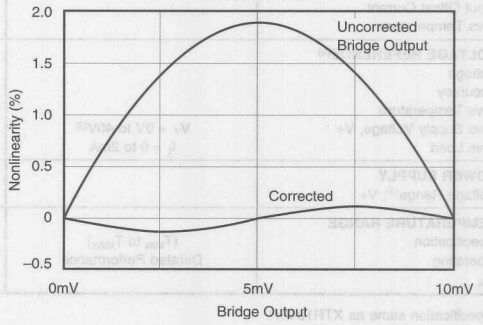
The XTR104 is a monolithic 4-20mA, two-wire current transmitter integrated circuit designed for bridge input signals. It provides complete bridge excitation, instrumentation amplifier, linearization, and current output circuitry necessary for high impedance strain gage sensors.

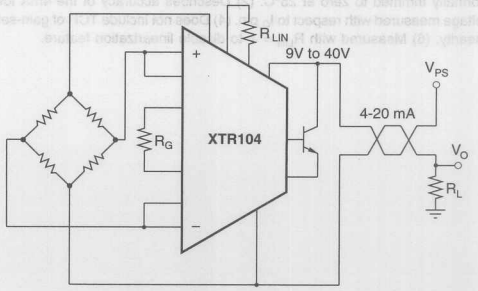
The instrumentation amplifier can be used over a wide range of gain, accommodating a variety of input signals and sensors. Total adjusted error of the complete current transmitter, including the linearized bridge is less than ±1% over the full –40°C to +85°C temperature range. This includes zero drift, span drift and non-linearity for bridge outputs as low as 10mV. The XTR104 operates on loop power supply voltages down to 9V.

Linearization circuitry consists of a second, fully independent instrumentation amplifier that controls the bridge excitation voltage. It provides second-order correction to the transfer function, typically achieving a 20:1 improvement in nonlinearity, even with low cost transducers.

The XTR104 is available in 16-pin plastic DIP and SOL-16 surface-mount packages specified for the –40°C to +85°C temperature range.

BRIDGE NONLINEARITY CORRECTION USING XTR104



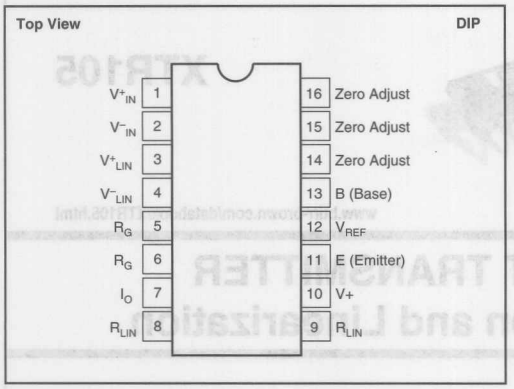

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| PARAMETER | CONDITIONS | XTR104BP, BU | | | XTR104AP, AU | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OUTPUT** | | | | | | | | |
| Output Current Equation | | | $I_O = V_{IN} \bullet (0.016 + 40/R_G) + 4mA$ | | | $V_{IN}$ in Volts, $R_G$ in Ω | | A |
| Total Adjusted Error(1) | $T_{MIN}$ to $T_{MAX}$, $V_{FS} \geq 10mV$, $R_B = 5k\Omega$ | | | ±1 | | | ±2 | % of FS |
| Current, Specified Range | | 4 | | 20 | * | | * | mA |
| Over-Scale Limit | | | 34 | 40 | | * | * | mA |
| Under Scale-Limit | | | 3.6 | 3.8 | | * | * | mA |
| Full Scale Output Error | $V_{IN} = 1V$, $R_G = \infty$ | | ±15 | ±50 | | * | ±100 | µA |
| Noise: 0.1Hz to 1kHz | $R_G = 40\Omega$ | | 8 | | | * | | µAp-p |
| **ZERO OUTPUT(2)** | $V_{IN} = 0V$, $R_G = \infty$ | | 4 | | | * | | mA |
| Initial Error | | | ±5 | ±50 | | * | ±100 | µA |
| vs Temperature | | | ±0.2 | ±0.5 | | * | ±1 | µA/°C |
| vs Supply Voltage, V+ | V+ = 9V to 40V(3) | | 0.5 | 2 | | * | * | µA/V |
| vs Common-Mode Voltage | $V_{CM}$ = 2V to 3V(3) | | 0.1 | 2 | | * | * | µA/V |
| **SPAN** | | | | | | | | |
| Span Equation (Transconductance) | | | $S = 0.016 + 40/R_G$ | | | * | | A/V |
| Untrimmed Error | $R_G \geq 75\Omega$ | | ±0.1 | ±1 | | * | * | % |
| vs Temperature(4) | | | ±20 | ±50 | | * | ±100 | ppm/°C |
| Nonlinearity: Ideal Input | | | | 0.01 | | | * | % |
| Bridge Input(5) | | | 0.1 | | | * | | % |
| **INPUT** | | | | | | | | |
| Differential Range | | | | 1 | | | * | V |
| Input Voltage Range(3) | | 2 | | 3 | * | | * | V |
| Common-Mode Rejection | $V_{IN}$ = 2V to 3V(3) | 80 | 100 | | * | * | | dB |
| Impedance: Differential | | | 3 | | | * | | GΩ |
| Common-Mode | | | 0.5 | | | * | | GΩ |
| Offset Voltage | | | ±0.5 | ±2.5 | | * | * | mV |
| vs Temperature | | | 1 | 2.5 | | 2 | 5 | µV/°C |
| vs Supply Voltage, V+ | V+ = 9V to 40V(3) | 110 | 130 | | * | * | | dB |
| Input Bias Current | | | 100 | 250 | | * | * | nA |
| vs Temperature | | | 0.1 | 2 | | * | * | nA/°C |
| Input Offset Current | | | 2 | 20 | | * | * | nA |
| vs Temperature | | | 0.01 | 0.25 | | * | * | nA/°C |
| **VOLTAGE REFERENCE(6)** | | | | | | | | |
| Voltage | | | 5 | | | * | | V |
| Accuracy | | | ±0.25 | ±0.5 | | * | ±1 | % |
| vs Temperature | | | ±10 | ±50 | | * | ±100 | ppm/°C |
| vs Supply Voltage, V+ | V+ = 9V to 40V(3) | | 5 | | | * | | ppm/V |
| vs Load | $I_L$ = 0 to 2mA | | 50 | | | * | | ppm/mA |
| **POWER SUPPLY** | | | | | | | | |
| Voltage Range(3), V+ | | 9 | | 40 | * | | * | V |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | ($T_{MIN}$ to $T_{MAX}$) | –40 | | 85 | * | | * | °C |
| Operating | Derated Performance | –40 | | 125 | * | | * | °C |
| $\theta_{JA}$ | | | 80 | | | * | | °C/W |

* Specification same as XTR104BP.

NOTES: (1) Includes corrected second-order nonlinearity of bridge, and over-temperature zero and span effects. Does not include initial offset and span errors which are normally trimmed to zero at 25°C. (2) Describes accuracy of the 4mA low-scale current. Does not include input amplifier effects. Can be trimmed to zero. (3) Voltage measured with respect to $I_O$ pin. (4) Does not include TCR of gain-setting resistor, $R_G$. (5) When configured to correct for ≤2% second-order bridge sensor nonlinearity. (6) Measured with $R_{LIN} = \infty$ to disable linearization feature.

## PIN CONFIGURATION




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply, V+ (referenced to $I_O$ pin) | 40V |
| Input Voltage, $V^+_{IN}$, $V^-_{IN}$, $V^+_{LIN}$, $V^-_{LIN}$ (referenced to $I_O$ pin) | 0V to V+ |
| Storage Temperature Range | –55°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Current Limit | Continuous |
| Junction Temperature | +165°C |

## PACKAGE/ORDERING INFORMATION

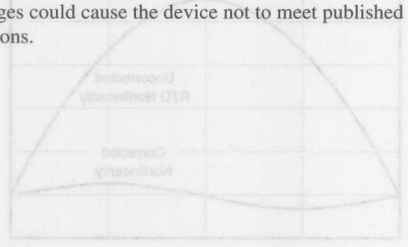
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| XTR104AP | 16-Pin Plastic DIP | 180 | –40°C to +85°C |
| XTR104BP | 16-Pin Plastic DIP | 180 | –40°C to +85°C |
| XTR104AU | SOL-16 Surface Mount | 211 | –40°C to +85°C |
| XTR104BU | SOL-16 Surface Mount | 211 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

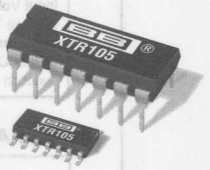
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.





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# XTR105

www.burr-brown.com/databook/XTR105.html

# 4-20mA CURRENT TRANSMITTER with Sensor Excitation and Linearization

## FEATURES

- LOW UNADJUSTED ERROR
- TWO PRECISION CURRENT SOURCES 800μA EACH
- RTD OR BRIDGE EXCITATION
- LINEARIZATION
- TWO OR THREE-WIRE RTD OPERATION
- LOW OFFSET DRIFT: 0.4μV/°C
- LOW OUTPUT CURRENT NOISE: 30nAp-p
- HIGH PSR: 110dB min
- HIGH CMR: 86dB min
- WIDE SUPPLY RANGE: 7.5V TO 36V
- 14-PIN DIP AND SO-14 SOIC PACKAGES

## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- FACTORY AUTOMATION
- SCADA REMOTE DATA ACQUISITION
- REMOTE TEMPERATURE AND PRESSURE TRANSDUCERS

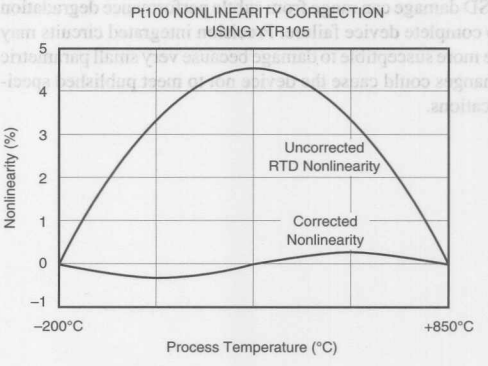
## DESCRIPTION

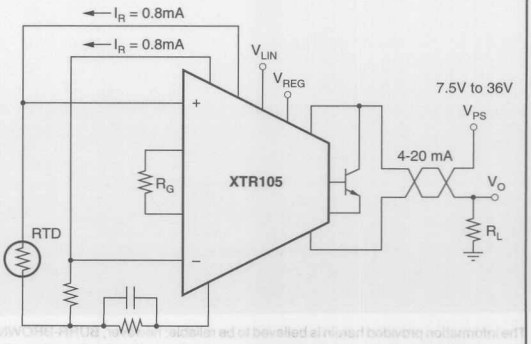
The XTR105 is a monolithic 4-20mA, two-wire current transmitter with two precision current sources. It provides complete current excitation for Platinum RTD temperature sensors and bridges, instrumentation amplifier, and current output circuitry on a single integrated circuit.

Versatile linearization circuitry provides a 2nd-order correction to the RTD, typically achieving a 40:1 improvement in linearity.

Instrumentation amplifier gain can be configured for a wide range of temperature or pressure measurements. Total unadjusted error of the complete current transmitter is low enough to permit use without adjustment in many applications. This includes zero output current drift, span drift and nonlinearity. The XTR105 operates on loop power supply voltages down to 7.5V.

The XTR105 is available in 14-pin plastic DIP and SO-14 surface-mount packages and is specified for the –40°C to +85°C industrial temperature range.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

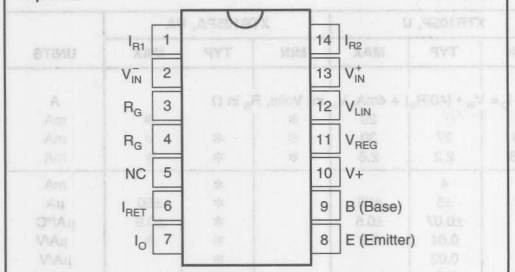
At $T_A$ = +25°C, V+ = 24V, and TIP29C external transistor, unless otherwise noted.

| PARAMETER | CONDITIONS | XTR105P, U MIN | XTR105P, U TYP | XTR105P, U MAX | XTR105PA, UA MIN | XTR105PA, UA TYP | XTR105PA, UA MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | | | |
| Output Current Equation | | | $I_O = V_{IN} \bullet (40/R_G) + 4mA$, $V_{IN}$ in Volts, $R_G$ in Ω | | | | | A |
| Output Current, Specified Range | | 4 | | 20 | * | | * | mA |
| Over-Scale Limit | | 24 | 27 | 30 | * | * | * | mA |
| Under-Scale Limit | $I_{REG}$ = 0V | 1.8 | 2.2 | 2.6 | * | * | * | mA |
| **ZERO OUTPUT**[1] | $V_{IN}$ = 0V, $R_G$ = ∞ | | 4 | | | * | | mA |
| Initial Error | | | ±5 | ±25 | | * | ±50 | µA |
| vs Temperature | | | ±0.07 | ±0.5 | | * | ±0.9 | µA/°C |
| vs Supply Voltage, V+ | V+ = 7.5V to 36V | | 0.04 | 0.2 | | * | * | µA/V |
| vs Common-Mode Voltage | $V_{CM}$ = 1.25V to 3.5V[2] | | 0.02 | | | * | | µA/V |
| vs $V_{REG}$ Output Current | | | 0.3 | | | * | | µA/mA |
| Noise: 0.1Hz to 10Hz | | | 0.03 | | | * | | µAp-p |
| **SPAN** | | | | | | | | |
| Span Equation (Transconductance) | | | S = 40/$R_G$ | | | * | | A/V |
| Initial Error[3] | Full Scale ($V_{IN}$) = 50mV | | ±0.05 | ±0.2 | | * | ±0.4 | % |
| vs Temperature[3] | | | ±3 | ±25 | | * | * | ppm/°C |
| Nonlinearity: Ideal Input[4] | Full Scale ($V_{IN}$) = 50mV | | 0.003 | 0.01 | | * | * | % |
| **INPUT**[5] | | | | | | | | |
| Offset Voltage | $V_{CM}$ = 2V | | ±50 | ±100 | | * | ±250 | µV |
| vs Temperature | | | ±0.4 | ±1.5 | | * | ±3 | µV/°C |
| vs Supply Voltage, V+ | V+ = 7.5V to 36V | | ±0.3 | ±3 | | * | * | µV/V |
| vs Common-Mode Voltage, RTI (CMRR) | $V_{CM}$ = 1.25V to 3.5V[2] | | ±10 | ±50 | | * | ±100 | µV/V |
| Common-Mode Input Range[2] | | 1.25 | | 3.5 | * | | * | V |
| Input Bias Current | | | 5 | 25 | | * | 50 | nA |
| vs Temperature | | | 20 | | | * | | pA/°C |
| Input Offset Current | | | ±0.2 | ±3 | | * | ±10 | nA |
| vs Temperature | | | 5 | | | * | | pA/°C |
| Impedance: Differential | | | 0.1 ‖ 1 | | | * | | GΩ ‖ pF |
| Common-Mode | | | 5 ‖ 10 | | | * | | GΩ ‖ pF |
| Noise: 0.1Hz to 10Hz | | | 0.6 | | | * | | µVp-p |
| **CURRENT SOURCES** | $V_O$ = 2V[6] | | | | | | | |
| Current | | | 800 | | | * | | µA |
| Accuracy | | | ±0.05 | ±0.2 | | * | ±0.4 | % |
| vs Temperature | | | ±15 | ±35 | | * | ±75 | ppm/°C |
| vs Power Supply, V+ | V+ = 7.5V to 36V | | ±10 | ±25 | | * | * | ppm/V |
| Matching | | | ±0.02 | ±0.1 | | * | ±0.2 | % |
| vs Temperature | | | ±3 | ±15 | | * | ±30 | ppm/°C |
| vs Power Supply, V+ | V+ = 7.5V to 36V | | 1 | 10 | | * | * | ppm/V |
| Compliance Voltage, Positive | | (V+) –3 | (V+) –2.5 | | * | * | | V |
| Negative[2] | | 0 | –0.2 | | * | * | | V |
| Output Impedance | | | 150 | | | * | | MΩ |
| Noise: 0.1Hz to 10Hz | | | 0.003 | | | * | | µAp-p |
| **$V_{REG}$**[2] | | | 5.1 | | | * | | V |
| Accuracy | | | ±0.02 | ±0.1 | | * | * | V |
| vs Temperature | | | ±0.2 | | | * | | mV/°C |
| vs Supply Voltage, V+ | | | 1 | | | * | | mV/V |
| Output Current | | | ±1 | | | * | | mA |
| Output Impedance | | | 75 | | | * | | Ω |
| **LINEARIZATION** | | | | | | | | |
| $R_{LIN}$ (internal) | | | 1 | | | * | | kΩ |
| Accuracy | | | ±0.2 | ±0.5 | | * | ±1 | % |
| vs Temperature | | | ±25 | ±100 | | * | * | ppm/°C |
| **POWER SUPPLY** | | | | | | | | |
| Specified | | | +24 | | | * | | V |
| Voltage Range | | +7.5 | | +36 | * | | * | V |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification, $T_{MIN}$ to $T_{MAX}$ | | –40 | | +85 | * | | * | °C |
| Operating | | –55 | | +125 | * | | * | °C |
| Storage | | –55 | | +125 | * | | * | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| 14-Pin DIP | | | 80 | | | * | | °C/W |
| *SO-14 Surface-Mount* | | | 100 | | | * | | °C/W |

* Specification same as XTR105P, XTR105U.

NOTES: (1) Describes accuracy of the 4mA low-scale offset current. Does not include input amplifier effects. Can be trimmed to zero. (2) Voltage measured with respect to $I_{RET}$ pin. (3) Does not include initial error or TCR of gain-setting resistor, $R_G$. (4) Increasing the full-scale input range improves nonlinearity. (5) Does not include Zero Output initial error. (6) Current source output voltage with respect to $I_{RET}$ pin.

Top View — DIP and SOIC




NC = No Internal Connection.

| | |
|---|---|
| Power Supply, V+ (referenced to $I_O$ pin) | 40V |
| Input Voltage, $V_{IN}^+$, $V_{IN}^-$ (referenced to $I_O$ pin) | 0V to V+ |
| Storage Temperature Range | –55°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Current Limit | Continuous |
| Junction Temperature | +165°C |

NOTE: (1) Stresses above these ratings may cause permanent damage.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

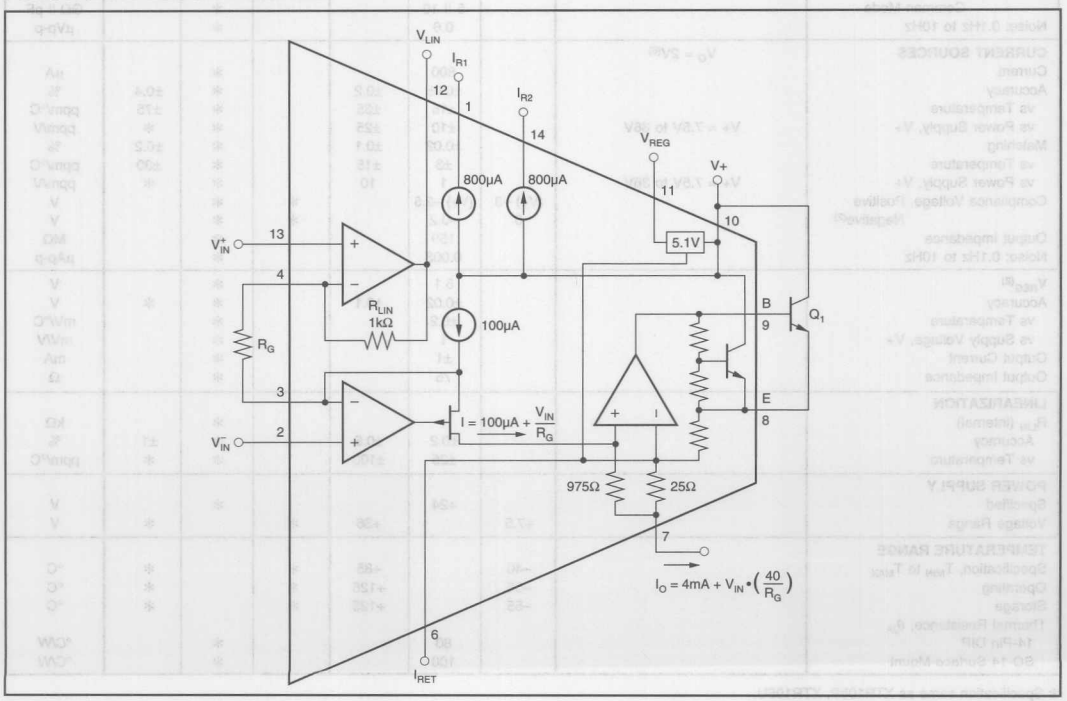
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| XTR105PA | 14-Pin Plastic DIP | 010 | –40°C to +85°C |
| XTR105P | 14-Pin Plastic DIP | 010 | –40°C to +85°C |
| XTR105UA | SO-14 Surface Mount | 235 | –40°C to +85°C |
| XTR105U | SO-14 Surface Mount | 235 | –40°C to +85°C |

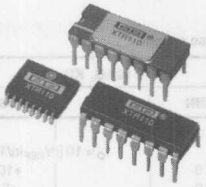
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## FUNCTIONAL BLOCK DIAGRAM




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# XTR110

www.burr-brown.com/databook/XTR110.html

# PRECISION VOLTAGE-TO-CURRENT CONVERTER/TRANSMITTER



## FEATURES

- 4mA TO 20mA TRANSMITTER
- SELECTABLE INPUT/OUTPUT RANGES:
  0V to +5V, 0V to +10V Inputs
  0mA to 20mA, 5mA to 25mA Outputs
  Other Ranges
- 0.005% MAX NONLINEARITY, 14 BIT
- PRECISION +10V REFERENCE OUTPUT
- SINGLE SUPPLY OPERATION
- WIDE SUPPLY RANGE: 13.5V to 40V

## APPLICATIONS

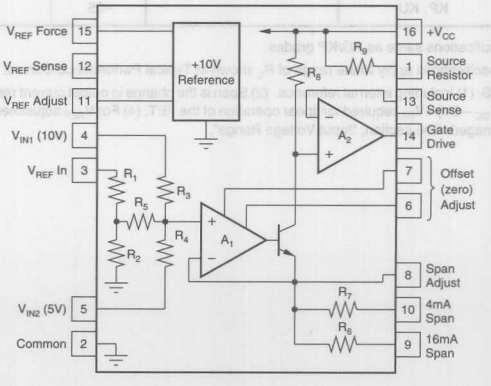
- INDUSTRIAL PROCESS CONTROL
- PRESSURE/TEMPERATURE TRANSMITTERS
- CURRENT-MODE BRIDGE EXCITATION
- GROUNDED TRANSDUCER CIRCUITS
- CURRENT SOURCE REFERENCE FOR DATA ACQUISITION
- PROGRAMMABLE CURRENT SOURCE FOR TEST EQUIPMENT
- POWER PLANT/ENERGY SYSTEM MONITORING

## DESCRIPTION

The XTR110 is a precision voltage-to-current converter designed for analog signal transmission. It accepts inputs of 0 to 5V or 0 to 10V and can be connected for outputs of 4 to 20mA, 0 to 20mA, 5 to 25mA and many other commonly used ranges.

A precision on-chip metal film resistor network provides input scaling and current offsetting. An internal 10V voltage reference can be used to drive external circuitry.

The XTR110 is available in 16-pin plastic DIP, ceramic DIP and SOL-16 surface-mount packages. Commercial and industrial temperature range models are available.




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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C and $V_{CC}$ = +24V and $R_L$ = 250Ω**, unless otherwise specified.

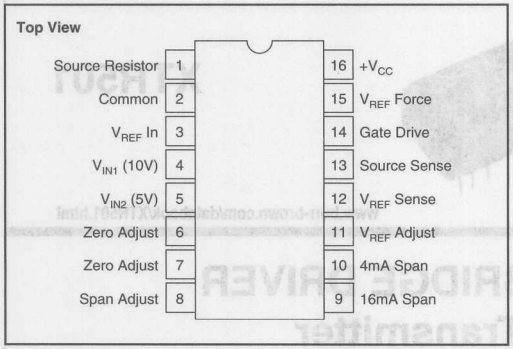
| PARAMETER | CONDITIONS | XTR110AG, KP, KU | | | XTR110BG | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **TRANSMITTER** | | | | | | | | |
| Transfer Function | | | $I_O = 10\,[(V_{REF}In/16) + (V_{IN1}/4) + (V_{IN2}/2)]\,/R_{SPAN}$ | | | | | |
| Input Range: $V_{IN1}$[5] | Specified Performance | 0 | | +10 | * | | * | V |
| $V_{IN2}$ | Specified Performance | 0 | | +5 | * | | * | V |
| Current, $I_O$ | Specified Performance[1] | 4 | | 20 | * | | * | mA |
| | Derated Performance[1] | 0 | | 40 | * | | * | mA |
| Nonlinearity | 16mA/20mA Span[2] | | 0.01 | 0.025 | | 0.002 | 0.005 | % of Span |
| Offset Current, $I_{OS}$ | $I_O$ = 4mA[1] | | | | | | | |
| Initial | [1] | | 0.2 | 0.4 | | 0.02 | 0.1 | % of Span |
| vs Temperature | [1] | | 0.0003 | 0.005 | | * | 0.003 | % of Span/°C |
| vs Supply, $V_{CC}$ | [1] | | 0.0005 | 0.005 | | * | * | % of Span/V |
| Span Error | $I_O$ = 20mA | | | | | | | |
| Initial | [1] | | 0.3 | 0.6 | | 0.05 | 0.2 | % of Span |
| vs Temperature | [1] | | 0.0025 | 0.005 | | 0.0009 | 0.003 | % of Span/°C |
| vs Supply, $V_{CC}$ | [1] | | 0.003 | 0.005 | | * | * | % of Span/V |
| Output Resistance | From Drain of FET ($Q_{EXT}$)[3] | | $10 \times 10^9$ | | | * | | Ω |
| Input Resistance | $V_{IN1}$ | | 27 | | | * | | kΩ |
| | $V_{IN2}$ | | 22 | | | * | | kΩ |
| | $V_{REF}$ In | | 19 | | | * | | kΩ |
| Dynamic Response | | | | | | | | |
| Settling Time | To 0.1% of Span | | 15 | | | * | | µs |
| | To 0.01% of Span | | 20 | | | * | | µs |
| Slew Rate | | | 1.3 | | | * | | mA/µs |
| **VOLTAGE REFERENCE** | | | | | | | | |
| Output Voltage | | +9.95 | +10 | +10.05 | +9.98 | * | +10.02 | V |
| vs Temperature | | | 35 | 50 | | 15 | 30 | ppm/°C |
| vs Supply, $V_{CC}$ | Line Regulation | | 0.0002 | 0.005 | | * | * | %/V |
| vs Output Current | Load Regulation | | 0.0005 | 0.01 | | * | * | %/mA |
| vs Time | | | 100 | | | * | | ppm/1k hrs |
| Trim Range | | –0.100 | | +0.25 | * | | * | V |
| Output Current | Specified Performance | 10 | | | * | | | mA |
| **POWER SUPPLY** | | | | | | | | |
| Input Voltage, $V_{CC}$ | | +13.5 | | +40 | * | | * | V |
| Quiescent Current | Excluding $I_O$ | | 3 | 4.5 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: AG, BG | | –40 | | +85 | * | | * | °C |
| KP, KU | | 0 | | +70 | | | | °C |
| Operating: AG, BG | | –55 | | +125 | * | | * | °C |
| KP, KU | | –25 | | +85 | | | | °C |

* Specifications same as AG/KP grades.

** Specifications apply to the range of $R_L$ shown in Typical Performance Curves.

NOTES: (1) Including internal reference. (2) Span is the change in output current resulting from a full-scale change in input voltage. (3) Within compliance range limited by $(+V_{CC} - 2V) + V_{DS}$ required for linear operation of the FET. (4) For $V_{REF}$ adjustment circuit see Figure 3. (5) For extended $I_{REF}$ drive circuit see Figure 4. (5) Unit may be damaged. See section, "Input Voltage Range".

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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply, $+V_{CC}$ | 40V |
| Input Voltage, $V_{IN1}$, $V_{IN2}$, $V_{REF\ IN}$ | $+V_{CC}$ |
| See text regarding safe negative input voltage range. | |
| Storage Temperature Range: A, B | –55°C to +125°C |
| K, U | –40°C to +85°C |
| Lead Temperature | |
| (soldering, 10s) G, P | 300°C |
| (wave soldering, 3s) U | 260°C |
| Output Short-Circuit Duration, Gate Drive and $V_{REF}$ Force | Continuous to common and $+V_{CC}$ |
| Output Current Using Internal 50Ω Resistor | 40mA |

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| XTR110AG | 16-Pin Ceramic DIP | 109 | –40°C to +85°C |
| XTR110BG | 16-Pin Ceramic DIP | 109 | –40°C to +85°C |
| XTR110KP | 16-Pin Plastic DIP | 180 | 0°C to +70°C |
| XTR110KU | SOL-16 Surface-Mount | 211 | 0°C to +70°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integral circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

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# XTR501

www.burr-brown.com/databook/XTR501.html

# HIGH CURRENT BRIDGE DRIVER and 4-20mA Transmitter

## FEATURES

- SENSOR EXCITATION OF 1W
- VARIABLE EXCITATION VOLTAGE: 1.5V to 5.0V
- SINGLE SUPPLY: 11.4V to 30VDC
- INRUSH CURRENT LIMITING
- 4-20mA TRANSMITTER

## APPLICATIONS

- GAS DETECTION SENSORS
- PELLISTOR CATALYTIC DETECTORS
- STRAIN GAGES
- HIGH CURRENT BRIDGES
- LOAD CELLS
- HOT-WIRE ANEMOMETERS

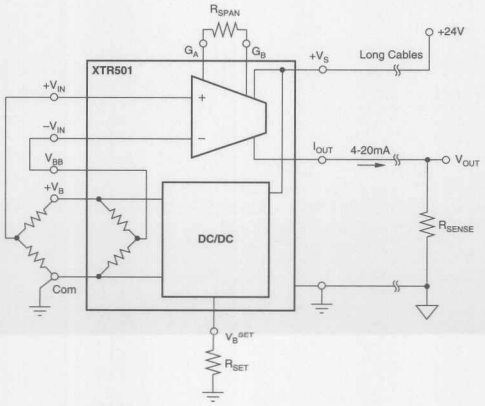
## DESCRIPTION

The XTR501 contains a high efficiency DC/DC converter and 4-20mA three wire current transmitter. It provides regulated bridge excitation, optional half bridge, differential inputs and current transmitter necessary for the excitation and signal conditioning of low impedance bridge sensors and high integrity signal transmission.

The DC/DC converter is capable of supplying 1W into a regulated bridge voltage of 1.5V to 5.0V from a supply of 11.4V to 30V. The combination of a low startup current and high efficiency current step-up allows for a combined supply line resistance of up to 100Ω when exciting low impedance sensors.

The instrumentation amplifier of the current transmitter can be used over a wide range of gains, accommodating a variety of input signals and sensors.

The XTR501 is particularly suited to excitation of high current/low impedance sensors used in bridge applications allowing the use of lighter cabling leading to considerable savings on cabling costs.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $V_S$ = 24V, $V_{BRIDGE}$ = 2V, $I_{LOAD}$ = 300mA, unless otherwise specified.

| PARAMETER | CONDITIONS | XTR501 MIN | XTR501 TYP | XTR501 MAX | UNITS |
|---|---|---|---|---|---|
| **INSTRUMENTATION AMPLIFIER/CURRENT TRANSMITTER** | | | | | |
| **SIGNAL OUTPUT** | | | | | |
| Output Current Equation | $R_G$ in Ω, $V_{IN}$ in V | | $I_O = 0.004 + 0.016\ [(1 + 50k\Omega/R_G)/4.94]\ V_{IN}$ | | A |
| Output Current | Linear Operating Range | 4 | | 20 | mA |
| Over-scale Limit | | 25 | 27 | | mA |
| Under-scale Limit | | | 0 | | mA |
| **ZERO** | | | | | |
| Output Current | | | 4 | | mA |
| Offset Error | | | ±50 | ±100 | µA |
| vs Temperature | | | 0.2 | | µA/°C |
| vs Supply Voltage | $V_S$ = 11.4V to 30V | | 0.5 | 2 | µA/V |
| **SPAN** | | | | | |
| Span Equation | $R_G$ in Ω, $V_{IN}$ in V | | Span = $0.016[(1 + 50k\Omega/R_G)/4.94]$ | | A/V |
| Untrimmed Error | G = 1 | | ±0.2 | ±2.5 | % |
| | G = 250 | | ±1.5 | ±10 | % |
| vs Temperature | | | 50 | | ppm/°C |
| Nonlinearity | G = 1; $I_O$ = 4mA to 20mA | | | ±0.025 | % |
| **INPUT** | | | | | |
| Common-Mode Range | | 0 | | 4.94(1) | V |
| Offset Voltage | | | 16 | | mV |
| vs Temperature | | | 50 | | µV/°C |
| vs Supply Voltage | | | 75 | | dB |
| Common-Mode Rejection | | | 85 | | dB |
| Impedance; Differential, Common-Mode | | | $10^{10}$ II 6 | | Ω II pF |
| **DC/DC CONVERTER** | | | | | |
| **BRIDGE EXCITATION VOLTAGE SOURCE** | | | | | |
| Output Voltage | | 1.5 | | 5 | V |
| vs Temperature | $V_{IN}$ = 0V, G= 1 | | 200 | | ppm/°C |
| vs Long Term Stability | | | 100 | | ppm/1000hrs |
| Output Power | | | | 1 | W |
| Line Voltage Regulation | $V_S$ = 11.4V to 30.0V | | 0.25 | | % |
| Load Voltage Regulation | Load Current 160mA to 340mA<br>Load Voltage 2V | | 0.25 | | % |
| Output Voltage Ripple | Load Current 300mA<br>Load Voltage 2V | | 150 | | mV |
| Output Voltage Ripple Frequency | | | 100 | | kHz |
| Output Short-Circuit Current | Limited Duration | | 2.6 | | A |
| Input Current | Output Short-Circuit | | 150 | | mA |
| **POWER SUPPLY** | | | | | |
| Supply Voltage, $V_S$ | | 11.4 | 24 | 30 | V |
| Supply Current | | | See Typical Curve | | |
| **TEMPERATURE** | | | | | |
| Operating | | –40 | | +70 | °C |
| Storage | | –40 | | +85 | °C |

NOTE: (1) Common-Mode Range is based on a multiple of a bandgap reference of 1.235V.



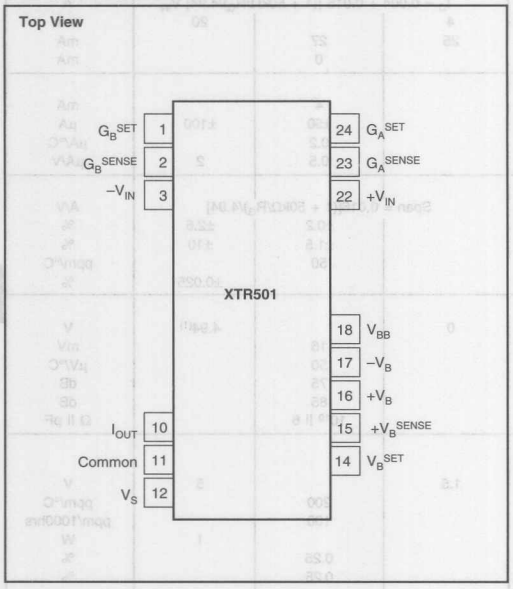
The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, $V_S$ | 30V |
| Input Voltage | 10V |
| Output Power | 1W |
| Operating Temperature Range | 0°C to +70°C |
| Storage Temperature Range | –40°C to +85°C |

## PIN CONFIGURATION

Top View




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

| PRODUCT | PACKAGE | TEMPERATURE RANGE |
|---|---|---|
| XTR501 | 24-Pin Plastic Module | –40°C to +70°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| XTR501 | 24-Pin Plastic Module | 269 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN DESCRIPTION

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | $G_B$SET | Connect to $R_{SPAN}$ to set transconductance. |
| 2 | $G_B$SENSE | Sense pin for $G_B$SET connect to $G_A$SET. |
| 3 | $-V_{IN}$ | Inverting input to transmitter. |
| 10 | $I_{OUT}$ | Output Current connect through $R_{SENSE}$ to common. |
| 11 | Common | Supply return for sense and $V_B$ connectors. |
| 12 | $V_S$ | Supply to XTR501 +11.4V to 30.0V. |
| 14 | $V_B$SET | Single resistor to common sets the bridge excitation voltage. |
| 15 | $+V_B$SENSE | Positive bridge sense input connect to positive excitation voltage at bridge. |
| 16 | $+V_B$ | Positive bridge excitation voltage. |
| 17 | $-V_B$ | Negative bridge excitation voltage. |
| 18 | $V_{BB}$ | Output from internal half bridge connect to $-V_{IN}$. |
| 22 | $+V_{IN}$ | Non-Inverting input to transmitter. |
| 23 | $G_A$SENSE | Sense pin for $G_A$SET connect to $G_A$SET. |
| 24 | $G_A$SET | Connect to $R_{SPAN}$ to set transconductance. |

# 5 Isolation Products

Isolation amplifiers can be used to amplify and measure low level signals in the presence of high common-mode voltages, break ground-loops and/or eliminate source ground connections, provide an interface between medical patient monitoring equipment, and provide isolation protection to electronic instruments/equipment.

Our isolation amplifiers feature three different technologies—transformer isolation, capacitor isolation, and opto-isolation. The following selection guides will help you determine the performance and functionality that best fit your requirements.

Choose from the industry's most complete line of isolation solutions including:

**ISO130**—Provides high isolation-mode rejection, wide bandwidth and low cost in 8-pin DIP and surface-mount packages.

**ISO124**—This new lowest-cost isolation amplifier is an excellent performer. It provides 1500V isolation and comes in standard DIP and SOIC packages.

**ISO120**—Industry's first hermetic isolation amplifier with 0.01% linearity. It is offered with specifications over the military temperature range.

**ISO103**—Unity-gain isolation amp combined with an internal isolated DC/DC converter in a space-saving, 24-pin ceramic DIP.

**ISO212**—Low cost, uncommitted input amplifier, differential output with an internal isolated DC/DC converter.

**ISO100**—Versatile, adjustable gain optically-coupled amplifier in a 18-pin DIP.

**3656**—Transformer-coupled amplifier with an internal isolated DC/DC converter that offers three port isolation.

**ISO150**—High speed, low cost dual digital transceiver that is TTL- and CMOS-compatible, available in a 24-pin plastic DIP and in a 28-lead SOIC.

**ISO174**—New, precision, input isolated programmable gain amplifiers. Capable of both fixed and variable gains, they allow flexibility of input stage for use in applications such as IPC and data acquisition systems.

**ISO175**—New, precision, input isolated instrumentation amplifiers that offer excellent accuracy. A single resistor sets any gain from 1 to 10,000. Available in a 24-pin plastic "skinny" DIP.

**ISO166 and ISO176**—New, precision, input isolated amplifiers incorporating and uncommitted input op-amp, available in both enhanced frequency response and enhanced linearity version.

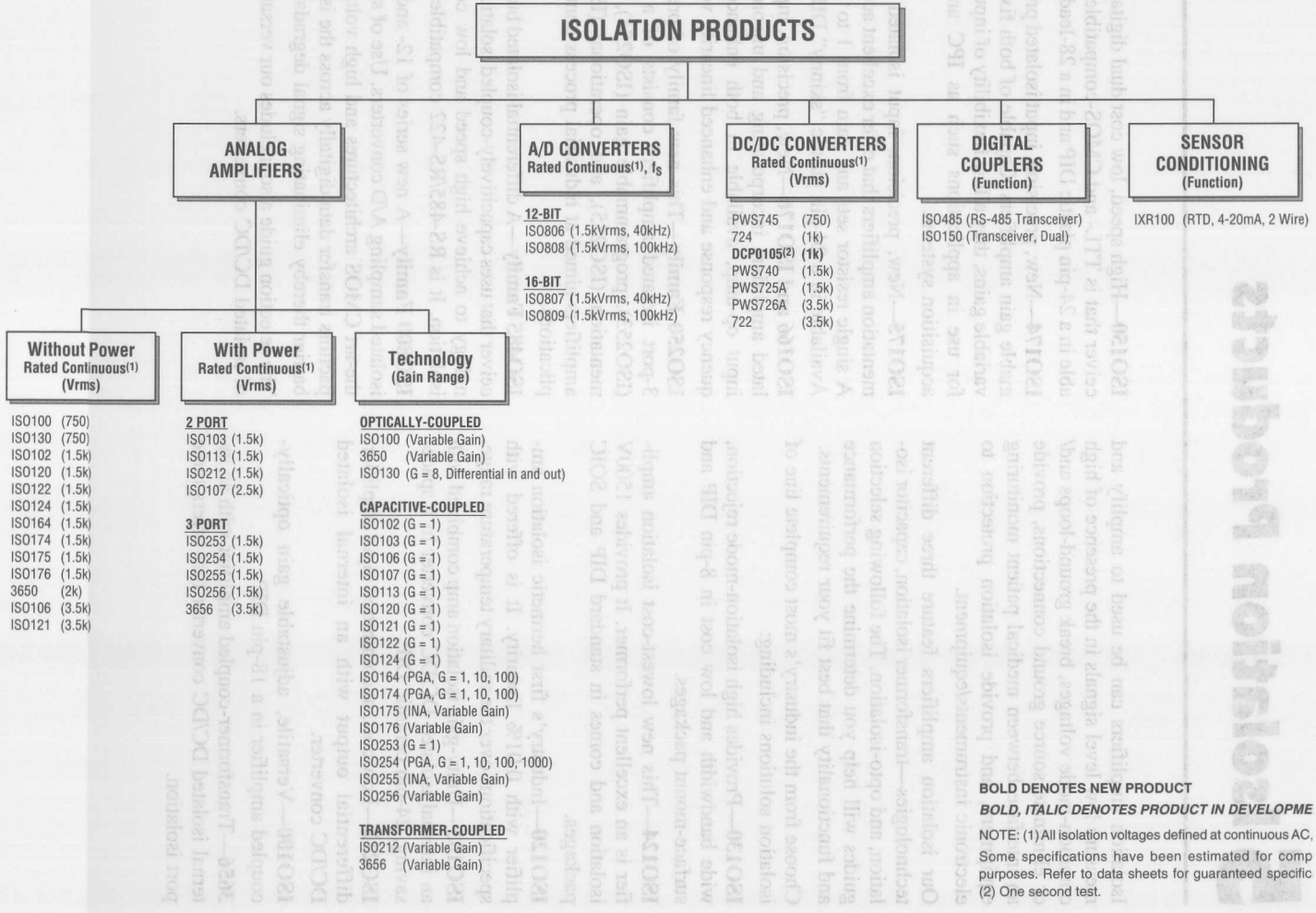
**ISO250 Family**—This new family of precision, 3-port isolated amplifiers consists of a buffer (ISO253), programmable gain (ISO254), instrumentation (ISO255), and operational (ISO256) amplifiers aimed at industrial process control applications.

**ISO485 Family**—A differential isolated bus transceiver that uses capacitively-coupled isolation technology to achieve high speed and low cost bus isolation. It is RS-485/RS-422 compatible.

**ISO800 Family**—A new series of 12- and 16-bit isolated sampling A/D converters. Use of state-of-the-art CMOS architectures and high voltage capacitors transfer data digitally across the isolation barrier thereby eliminating signal degradation.

The selection guide also includes our versatile line of isolated DC/DC converters.

# Isolation Products




**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPME***

NOTE: (1) All isolation voltages defined at continuous AC, Some specifications have been estimated for comp purposes. Refer to data sheets for guaranteed specific

(2) One second test.

## ANALOG WITHOUT POW

| Product | Isolation Voltage Cont Peak (DC) (V) | Isolation Voltage Pulse/Test Peak (V) | Isolation Mode Rejection DC typ (dB) | Isolation Mode Rejection 60Hz typ (dB) | Leakage Current at 240V/60Hz max (μArms) | Gain Non-linearity max (%) | Input Offset Voltage Drift max (±μV/°C) | Bias Current max (nA) | Small Signal Bandwidth typ (kHz) | Temp[1] Range | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO100 | 750 | 2500 | 146[4] | 108[4] | 0.3 | 0.07 | 2[4] | 10 | 60 | Ind | Low Drift Wide BW |
| ISO102 | 2121 | 4000 | 160 | 120 | 1.0 | ±0.003 | 250 | — | 70 | Ind[2] | 1500Vrms Isolation, Buffer |
| ISO106 | 4950 | 8000 | 160 | 130 | 1.0 | ±0.025 | 250 | — | 70 | Ind[2] | 3500Vrms Isolation, Buffer |
| ISO120 | 2121 | 2500[3] | 160 | 115 | 0.5 | ±0.01 | 150 | — | 60 | Mil[2] | 1500Vrms Isolation, Buffer |
| ISO121 | 4950 | 5600[3] | 160 | 115 | 0.5 | ±0.01 | 150 | — | 60 | Ind | 3500Vrms Isolation, Buffer |
| ISO122 | 2121 | 2400[3] | 160 | 140 | 0.5 | ±0.02 | 200* | — | 50 | Ind | 1500Vrms Isolation, Buffer |
| ISO124 | 2121 | 2400[3] | 160 | 140 | 0.5 | ±0.01 | 200* | — | 50 | Ind | Low Cost Isolation Buffer |
| ISO130 | 720 | 960[3] | 140 | 140 | — | ±0.25 | 2.1* | 670* | 85 | XInd | High IMR Wide BW, G = 8 |
| ISO164 | 2121 | 2500[3] | 115 | 115 (50Hz) | 0.8 (50Hz) | ±0.01 | 155 | 5 | 6 | XInd | 1500Vrms Isolation with PGA |
| ISO174 | 2121 | 2500[3] | 115 | 115 (50Hz) | 0.8 (50Hz) | ±0.04 | 505 | 5 | 60 | XInd | 1500Vrms Isolation with PGA |
| ISO175 | 2121 | 2500[3] | 160 | 115 | 1 | ±0.04 | 1.5 | ±10 | 50 | XInd | 1500Vrms, INA |
| ISO176 | 2121 | 2500[3] | 160 | 115 | 0.8 | ±0.04 | 500* | ±5 | 60* | XInd | 1500Vrms, Op Amp |
| 3650 | 2000 | 5000 | 140 | 120 | 0.35 | ±0.05 | 5 | 40 | 15 | Ind | Balanced Current Input, Buffer |

NOTES: All packages are DIPs except ISO130 and ISO122 which are also available in surface mount. (1) Ind = –25°C to +85°C, XInd = –40°C to 85°C, Mil = –55°C to +125°C. (2) Hermetic. (3) Partial discharge test voltage. (4) 10kΩ.

* DENOTES TYPICAL
**BOLD DENOTES NEW PRODUCT**
***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPME***

Some specifications have been estimated for comparisoi purposes. Refer to data sheets for guaranteed specificat

## ANALOG WITH POWER

| Product | Isolation Voltage Cont Peak (V) | Isolation Voltage Pulse/Test Peak (V) | Isolation Mode Rejection typ DC (dB) | Isolation Mode Rejection typ 60Hz (dB) | Leakage Current at 240V/60Hz max (µA) | Gain Non-linearity max (%) | Input Offset Voltage Drift max (±µV/°C) | Bias Current max (nA) | Small Signal Bandwidth typ (kHz) | Temp[1] Range | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO103 | 2121 | 5657 | 160 | 130 | 2.0 | ±0.025 | 250 | — | 20 | Ind | 1500Vrms Isolated Input Power, Buffer, 2 port |
| ISO107 | 3500 | 8000 | 160 | 100 | 2.0 | ±0.025 | 400 | — | 20 | Ind | 2500Vrms Isolated Input Power, Buffer, 2 port |
| ISO113 | 2121 | 5657 | 160 | 130 | 2.0 | ±0.02 | 250 | — | 20 | Ind | 1500Vrms Isolated Output Power, Buffer, 2 port |
| ISO212 | 2121 | 2400[3] | 160 | 115 | 2.0 | ±0.025 | (30 ±30/G) | 50 | 1 | Com | 1500Vrms Isolated Input Power, Low Cost, 2 port |
| ISO253 | 1500 | 2500[3] | 160 | 115 | 2.0 | ±0.1 | 150* | — | 50 | XInd | Buffer, 3 port |
| ISO254 | 1500 | 2500[3] | 160 | 150 | 2.0 | ±0.102 | ± (1 + 510/G) | 5 | 50 | XInd | Programmable Gain Amplifier, 3 port |
| ISO255 | 1500 | 2500[3] | 160 | 130 | 2.0 | ±0.102 | ± (1 + 520/G) | 10 | 50 | XInd | Instrumentation Amplifier, 3 port |
| ISO256 | 1500 | 2500[3] | 160 | 130 | 2.0 | ±0.1 | ±1.2 | ±5 | 50 | XInd | Operational Amplifier, Input, 3 port |
| 3656 | 3500 | 8000 | 160 | 125 | 0.5[2] | ±0.05 | (5+ 350/$G_1$) | 100 | 30 | Ind | High Isolation Voltage, 3 port |

NOTES: All packages are DIPs except the package for the ISO212 and ISO213 is a SIP. (1) Ind = –25°C to +85°C, Com = 0°C to +70°C, XInd = –40°C to 85°C. (2) At 120V/60Hz. (3) Partial discharge test voltage, ac Vrms.

## A/D CONVERTERS

| Product | Resolution (Bits) | Linearity Error max (%FSR) | Input Range (see table, pg 40) (V) | Sampling Rate (kHz) | NMC | THD (dB, max) | Temp Range | Pkg | Description |
|---|---|---|---|---|---|---|---|---|---|
| ISO806 | 12 | ±0.022 | C, D, S | 40 | 12 | –90* | XInd | XPDIP | Serial, Isolated, Rated 1500 Vrms |
| ISO807 | 16 | ±0.0046 | C, D, S | 40 | 15 | –100* | XInd | XPDIP | Serial, Isolated, Rated 1500 Vrms |
| ISO808 | 12 | ±0.022 | C, D, E, P, R, S | 100 | 12 | –90* | XInd | XPDIP | Serial, Isolated, Rated 1500 Vrms |
| ISO809 | 16 | ±0.006 | C, D, E, P, R, S | 100 | 15 | –100* | XInd | XPDIP | Serial, Isolated, Rated 1500 Vrms |

* DENOTES TYPICAL

**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

For Immediate Assistance, Contact Your Local Salesperson

## DC/DC CONVERTERS

| Product | Isolation Voltage Cont Peak (V) | Isolation Voltage Pulse Test Peak (V) | Input Voltage min (VDC) | Input Voltage max (VDC) | Leakage Current 240VAC 60Hz (μA) | Current, Balanced Loads On All Outputs Rated (mA) | Current, Balanced Loads On All Outputs Max[1] (mA) | Sensitivity To Input Change (V/V) | Temp[2] Range | Pkg | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **DCP0105** | **1400** | **1400** | **+4.75** | **+5.15** | **—** | **30** | **30** | **0.003** | **XInd** | **DIP** | **Single 5V Output, Standard JEDEC Package** |
| PWS725A | 2121 | 4000 | 7 | 18 | 2 | ±15 | ±40 | 1.15 | Ind | DIP | Single ±15V Output |
| PWS726A | 4950 | 8000 | 7 | 18 | 2 | ±15 | ±40 | 1.15 | Ind | DIP | Single ±15V Output |
| PWS740 | 2121 | 4000 | 7 | 20 | 1.5 | 30[3] | 60[3] | 1.20 | Ind | Sys[4] | Multiple Output (1-8) |
| PWS745[6] | 1060 | 1200[7] | 10[5] | 18[5] | 1.5 | ±15 | 30 | 1.20[5] | Ind | Comp | Multiple Output (1-8) |
| 722 | 3500 | 8000 | 5 | 16 | 1 | ±3-40 | ±50 | 1.13 | Ind | Mod | Dual ±15V Output |

NOTES: (1) See complete Product Data Sheet for full specifications, especially regarding output current capabilities. (2) Ind = –25°C to +85°C, XInd = –40°C to +100°C. (3) Per channel. (4) 1 TO-3 driver per 8 channels, plus 2 DIPs per channel. (5) 15V operation. (6) PWS745-1 driver may also be used with PWS740 components. (7) Partial discharge test voltage, ac Vrms.

## DIGITAL COUPLER

| Product | Isolation Voltage Cont Peak (Vrms) | Isolation Voltage Pulse Test Peak (V) | Leakage Current 240VAC 60Hz (μA) | Data Rate (MBd)* | Power Consumption Per Channel max (mW) | Ext Power Req | Temp[1] | Pkg | Description |
|---|---|---|---|---|---|---|---|---|---|
| ISO150 | 1500 | 2400[2] | 0.6 | 80 | 25 | Yes | XInd | DIP, SOIC | Dual Isolated Transceiver |
| ISO485 | 1500 | — | — | 20 | 180 at 5MBit/s | Yes | XInd | DIP | RS-485 Transceiver |

NOTES: (1) XInd = –40°C to +85°C. (2) Partial discharge test voltage, ac Vrms.

## SENSOR CONDITIONING

| Product | Isolation Voltage Cont Peak (V) | Span Untrimmed Error, max (%) | Span Non-linearity, typ (%) | Span Temp Drift (ppm/°C) | Input Offset Voltage typ | Input vs Temp max (μV/°C) | CMR vs Supply (dB) | Output Current Range (mA) | Output Current Limit (mA) | Temp[1] Range | Pkg | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IXR100 | 2121 | –2.5 | 0.01 (EMF)<br>0.1 (RTD) | 100 | 500μV | 5 | 100 | 4-20 | 32 | Special | Mod | Two-Wire Transmitter |

NOTE: (1) Special = –20°C to +70°C, Com = 0°C to 70°C.

* DENOTES TYPICAL
**BOLD DENOTES NEW PRODUCT**
***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

BURR-BROWN®




# DCP0105 Series

www.burr-brown.com/databook/DCP0105.html

# Miniature 5V Input, 1W Isolated UNREGULATED DC/DC CONVERTERS

## FEATURES

- STANDARD JEDEC PLASTIC PACKAGE
- MEETS EN55022 CLASS B
- LOW PROFILE: 0.15" (3.8mm)
- SYNCHRONIZABLE
- OUTPUT SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN
- STARTS INTO ANY CAPACITIVE LOAD
- FLOATING OUTPUTS
- EFFICIENCY: Up to 75% (at Full Load)
- 1000Vrms ISOLATION
- 400kHz SWITCHING
- 108 MILLION HOURS MTTF
- 5V, ±5V, 12V, ±12V, 15V, ±15V OUTPUTS

## APPLICATIONS

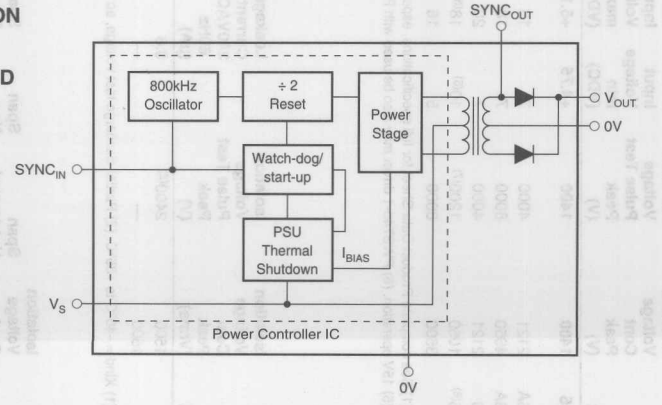
- POINT OF USE POWER CONVERSION
- DIGITAL INTERFACE POWER
- GROUND LOOP ELIMINATION
- DATA ACQUISITION
- INDUSTRIAL CONTROL AND INSTRUMENTATION
- TEST EQUIPMENT

## DESCRIPTION

The DCP0105 family is a series of high efficiency, 5V input isolated DC/DC converters. In addition to 1W nominal galvanically isolated output power capability, the range of DC/DCs are also fully synchronizable. The devices feature thermal shutdown, and overload protection is implemented via watchdog circuitry(1). Advanced power-on reset techniques give superior reset performance and the devices will start into any capacitive load up to full power output.

The DCP0105 family is implemented in standard-molded IC packaging, giving outlines suitable for high volume assembly.

NOTE: (1) Patents Pending.




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# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = +5V, unless otherwise specified.

| PARAMETER | CONDITIONS | DCP0105 SERIES MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **OUTPUT** | | | | | |
| Power | $V_S$ + 4% | | 1 | | W |
| | 100% Full Load | | 0.92 | | W |
| Voltage ($V_{NOM}$) | | | | | |
| DCP010505P | 75% Full Load[1] | 4.75 | 5 | 5.15 | V |
| DCP010505DP | 75% Full Load | ±4.75 | ±5 | ±5.25 | V |
| DCP010512P | 75% Full Load | 11.4 | 12 | 12.6 | V |
| DCP010512DP | 75% Full Load | ±11.4 | ±12 | ±12.6 | V |
| DCP010515P | 75% Full Load | 14.25 | 15 | 15.75 | V |
| DCP010515DP | 75% Full Load | ±14.25 | 15 | ±15.75 | V |
| Voltage vs Temperature | | | ±0.08 | | %/°C |
| Short-Circuit Duration | $V_S$ ± 10% | Indefinite | | | |
| Ripple | $C_L$ = O/P Capacitor = 10µF | | 20 | | mVp-p |
| **INPUT** | | | | | |
| Nominal Voltage ($V_S$) | | | 5 | | V |
| Voltage Range | | –10 | | 10 | % |
| Supply Current | 100% Full Load | | 250 | | mA |
| Reflected Ripple Current | $C_{IN}$ = I/P Capacitor = 1µF | | 20 | | mArms |
| | 50% Full Load | | | | |
| **ISOLATION** | | | | | |
| Voltage[2] | 1s Flash Test | 1 | | | kVrms |
| Continuous Voltage[3] | | | 1 | | kVrms |
| Insulation Resistance | | | >1 | | GΩ |
| Input/Output Capacitance | | | 2.5 | | pF |
| **REGULATION** | | | | | |
| Load Regulation | | | | | |
| DCP010505P | 100% to 75% Full Load | | 8 | 11 | % |
| | 75% to 10% Full Load | | 17 | 20 | % |
| DCP010505DP | 100% to 75% Full Load | | 8 | 10 | % |
| | 75% to 10% Full Load | | 19 | 22 | % |
| DCP010512P | 100% to 75% Full Load | | 7 | 9 | % |
| | 75% to 25% Full Load | | 12 | 17 | % |
| | 25% to 10% Full Load | | 7 | 12 | % |
| DCP010512DP | 100% to 75% Full Load | | 7 | 10 | % |
| | 75% to 25% Full Load | | 12 | 16 | % |
| | 25% to 10% Full Load | | 7 | 11 | % |
| DCP010515P | 100% to 75% Full Load | | 7 | 9 | % |
| | 75% to 25% Full Load | | 12 | 17 | % |
| | 25% to 10% Full Load | | 11 | 16 | % |
| DCP010515DP | 100% to 75% Full Load | | 7 | 10 | % |
| | 75% to 25% Full Load | | 12 | 16 | % |
| | 25% to 10% Full Load | | 11 | 15 | % |
| Line Regulation | 75% Full Load | | 1.003 | | %/1% of $V_S$ |
| **SWITCHING/SYNCHRONIZATION** | | | | | |
| Oscillator Frequency ($F_{OSC}$) | Switching Frequency = $F_{OSC}$/2 | | 800 | | kHz |
| Sync Input Low | | 0 | | 0.8 | V |
| Sync Input Current | $V_{SYNC}$ = +2V | | 48 | | µA |
| Reset Time | | | 3.8 | | µs |
| $SYNC_{OUT}$ Frequency | | | 400 | | kHz |
| **GENERAL** | | | | | |
| Quiescent Current | | | | | |
| DCP010505P | | | 38 | | mA |
| DCP010505DP | | | 40 | | mA |
| DCP010512P | | | 30 | | mA |
| DCP010512DP | | | 33 | | mA |
| DCP010515P | | | 34 | | mA |
| DCP010515DP | | | 34 | | mA |

## SPECIFICATIONS (CONT)

At $T_A$ = +25°C, $V_S$ = +5V, unless otherwise specified.

| PARAMETER | CONDITIONS | DCP0105 SERIES MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **GENERAL (Cont)** | | | | | |
| Efficiency | | | | | |
| DCP010505P | 100% Full Load | | 71 | | % |
| | 10% Full Load | | 40 | | % |
| DCP010505DP | 100% Full Load | | 66 | | % |
| | 10% Full Load | | 47 | | % |
| DCP010512P | 100% Full Load | | 72 | | % |
| | 10% Full Load | | 38 | | % |
| DCP010512DP | 100% Full Load | | 72 | | % |
| | 10% Full Load | | 36 | | % |
| DCP010515P | 100% Full Load | | 73 | | % |
| | 10% Full Load | | 40 | | % |
| DCP010515DP | 100% Full Load | | 75 | | % |
| | 10% Full Load | | 38 | | % |
| MTTF[3] | $T_A$ = +85°C | 158,000 | | | hrs |
| | $T_A$ = +55°C | 3,050,000 | | | hrs |
| | $T_A$ = +25°C | 108,000,000 | | | hrs |
| Weight | 14-Pin PDIP | | 1.08 | | g |
| **THERMAL SHUTDOWN** | | | | | |
| Internal Controller IC Temperature | | 115 | | 140 | °C |
| Shutdown Current | | | 3 | | mA |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –40 | | +100 | °C |

NOTES: (1) 100% load current = 1W/$V_{NOM}$ typical. (2) Rated working voltage = 130Vrms (IEC950 Convention). (3) Life test data.

### EMC SPECIFICATIONS

#### Specifications and Related Documents

The DCP010505P was tested to and complied with the limits of the following EMC specifications:

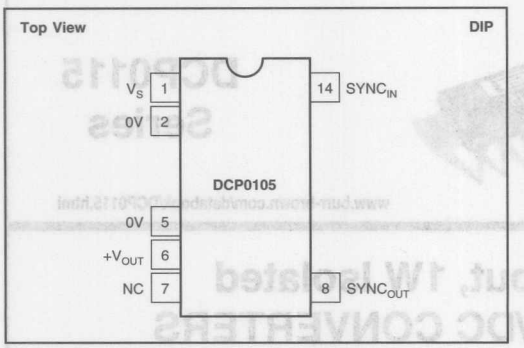
| | |
|---|---|
| prEN55022 (1992) | Conducted RF emission, telecomm lines. |
| EN55022 (1995) | Limits and methods of measurement of radio interference characteristics of information technology equipment. |
| ENV50140 (1993) | Electromagnetic compatibility. Basic immunity standard. Radiated RF immunity. |
| ENV50141 (1993) | Electromagnetic compatibility. Basic immunity standard. Conducted RF immunity. |
| EN61000-4-2 (1995) | Electromagnetic compatibility, Part 4. Testing and measurement techniques, Section 2. Electrostatic discharge. |
| EN61000-4-4 (1995) | Electromagnetic compatibility, Part 4. Testing and measurement techniques, Section 4. Electrical fast transient bursts. |
| EN61000-4-8 (1994) | Electromagnetic compatibility, Part 4. Testing and measurement techniques, Section 8. Power frequency magnetic field immunity. |

#### List of Tests

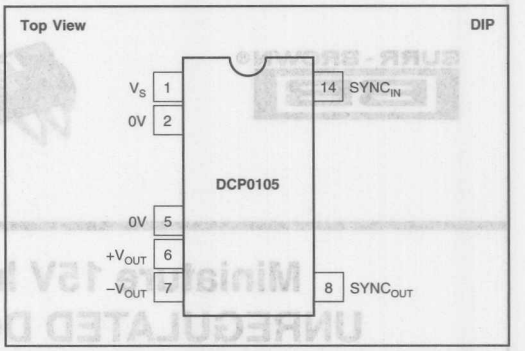
The following is a list of tests which were required for compliance with the above specifications:

| | |
|---|---|
| Conducted Emission Test | 150kHz to 30MHz, power and output lines, Class B limits applying. DC/DC loads of 0%, 8%, and 120% applying. |
| Radiated Emission Test | 30MHz to 1000MHz, Class B limits applying. DC/DC loads of 0%, 8%, and 120% applying. |
| Radiated Immunity Test, Electric Field | 80MHz to 1000MHz, 10V/m, 1kHz 80% AM. |
| Radiated Immunity Test, Electric Field | 900MHz, 10V/m, 200Hz 100% PM. |
| Electrostatic Discharge Test | 4kV, HCP/VCP indirect discharge only. |
| Electrical Fast Transient Tests | 2kV power lines, 2kV signal lines. |
| Conducted RF Immunity Tests | 150kHz to 80MHz, power and output lines, 10Vrms, 1kHz 80% AM. |
| Radiated Immunity Test, Magnetic Field | 50Hz, 30A/m |

## PIN CONFIGURATION (Single)




## PIN CONFIGURATION (Dual)




## PIN DEFINITIONS (Single)

| PIN # | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_S$ | Voltage Input. |
| 2 | 0V | Input Side Common. |
| 5 | 0V | Output Side Common. |
| 6 | $+V_{OUT}$ | +Voltage Out. |
| 7 | NC | Not Connected. |
| 8 | $SYNC_{OUT}$ | Unregulated 400kHz Output from Transformer. |
| 14 | $SYNC_{IN}$ | Synchronization Pin. |

## PIN DEFINITIONS (Dual)

| PIN # | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_S$ | Voltage Input. |
| 2 | 0V | Input Side Common. |
| 5 | 0V | Output Side Common. |
| 6 | $+V_{OUT}$ | +Voltage Out. |
| 7 | $-V_{OUT}$ | –Voltage Out. |
| 8 | $SYNC_{OUT}$ | Unregulated 400kHz Output from Transformer. |
| 14 | $SYNC_{IN}$ | Synchronization Pin. |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Input Voltage | 7V |
| Storage Temperature | –60°C to +150°C |
| Lead Temperature (soldering, 10s) | 300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

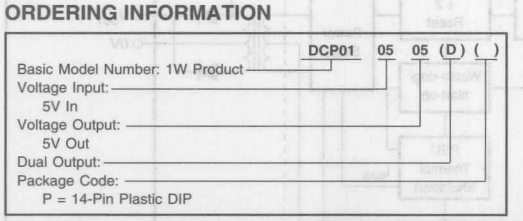
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| DCP010505P | 14-Pin Plastic DIP | 010-1 |
| DCP010505DP | 14-Pin Plastic DIP | 010-1 |
| DCP010512P | 14-Pin Plastic DIP | 010-1 |
| DCP010512DP | 14-Pin Plastic DIP | 010-1 |
| DCP010515P | 14-Pin Plastic DIP | 010-1 |
| DCP010515DP | 14-Pin Plastic DIP | 010-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

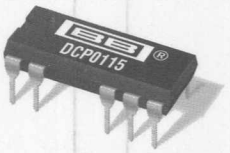
## ORDERING INFORMATION






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BURR - BROWN®




# DCP0115 Series

www.burr-brown.com/databook/DCP0115.html

# Miniature 15V Input, 1W Isolated UNREGULATED DC/DC CONVERTERS

## FEATURES

- STANDARD JEDEC PLASTIC PACKAGE
- LOW PROFILE: 0.15" (3.8mm)
- SYNCHRONIZABLE
- OUTPUT SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN
- STARTS INTO ANY CAPACITIVE LOAD
- EFFICIENCY: 76% (at Full Load)
- 1000Vrms ISOLATION
- 400kHz SWITCHING
- 93 MILLION HOURS MTTF

## APPLICATIONS

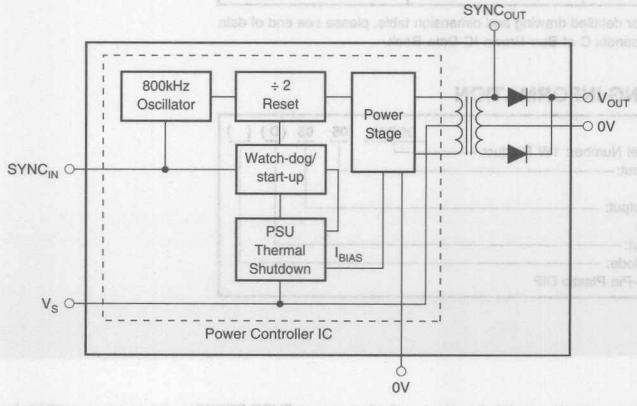
- POINT OF USE POWER CONVERSION
- GROUND LOOP ELIMINATION
- DATA ACQUISITION
- INDUSTRIAL CONTROL AND INSTRUMENTATION
- TEST EQUIPMENT

## DESCRIPTION

The DCP0115 family is a series of high efficiency, 15V input isolated DC/DC converters. In addition to 1W nominal galvanically isolated output power capability, the range of DC/DCs are also fully synchronizable. The devices feature thermal shutdown, and overload protection is implemented via watchdog circuitry(1). Advanced power-on reset techniques give superior reset performance and the devices will start into any capacitive load up to full power output.

The DCP01 family is implemented in standard-molded IC packaging, giving outlines suitable for high volume assembly.

NOTE: (1) Patents Pending.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = +15V, unless otherwise specified.

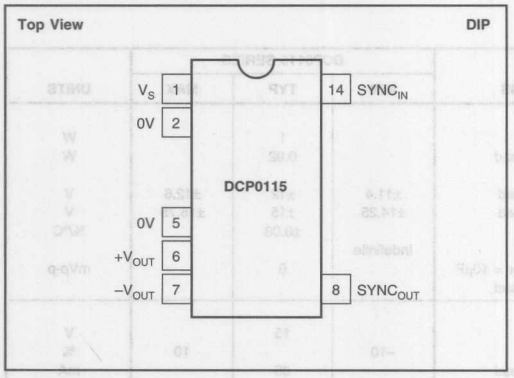
| PARAMETER | CONDITIONS | DCP0115 SERIES MIN | DCP0115 SERIES TYP | DCP0115 SERIES MAX | UNITS |
|---|---|---|---|---|---|
| **OUTPUT** | | | | | |
| Power | $V_S$ + 4% | | 1 | | W |
| | 100% Full Load | | 0.92 | | W |
| Voltage ($V_{NOM}$)[1] | | | | | |
| DCP011512D | 75% Full Load | ±11.4 | ±12 | ±12.6 | V |
| DCP011515D | 75% Full Load | ±14.25 | ±15 | ±15.75 | V |
| Voltage vs Temperature | | | ±0.08 | | %/°C |
| Short Circuit Duration | $V_S$ ± 10% | Indefinite | | | |
| Ripple | $C_L$ = O/P Capacitor = 10µF | | 6 | | mVp-p |
| | 100% Full Load | | | | |
| **INPUT** | | | | | |
| Nominal Voltage ($V_S$) | | | 15 | | V |
| Voltage Range | | –10 | | 10 | % |
| Supply Current | 100% Full Load | | 83 | | mA |
| Reflected Ripple Current | $C_{IN}$ = I/P Capacitor = 1µF | | 8 | | mArms |
| | 50% Full Load | | | | |
| **ISOLATION** | | | | | |
| Voltage[2] | 1s Flash Test | 1 | | | kVrms |
| Continuous Voltage[3] | | | 1 | | kVrms |
| Insulation Resistance | | | >1 | | GΩ |
| Input/Output Capacitance | | | 2.5 | | pF |
| **REGULATION** | | | | | |
| Load Regulation | | | | | |
| DCP011512D | 100% to 75% Full Load | | 7 | 14 | % |
| | 75% to 25% Full Load | | 5 | 10 | % |
| | 25% to 10% Full Load | | 10 | 15 | % |
| DCP011515D | 100% to 75% Full Load | | 4 | 8 | % |
| | 75% to 25% Full Load | | 9 | 16 | % |
| | 25% to 10% Full Load | | 10 | 15 | % |
| Line Regulation | 75% Full Load | | 1.003 | | %/1% of $V_S$ |
| **SWITCHING/SYNCHRONIZATION** | | | | | |
| Oscillator Frequency ($f_{OSC}$) | Switching Frequency = $f_{OSC}$/2 | | 800 | | kHz |
| Sync Input Low | | 0 | | 0.8 | V |
| Sync Input Current | $V_{SYNC}$ = +2V | | 48 | | µA |
| Reset Time | | | 3.8 | | µs |
| $SYNC_{OUT}$ Frequency | | | 400 | | kHz |
| **GENERAL** | | | | | |
| Quiescent Current | | | | | |
| DCP011512D | | | 14 | | mA |
| DCP011515D | | | 17 | | mA |
| Efficiency | | | | | |
| DCP011512D | 100% Full Load | | 76 | | % |
| | 10% Full Load | | 48 | | % |
| DCP011515D | 100% Full Load | | 76 | | % |
| | 10% Full Load | | 42 | | % |
| MTTF[3] | $T_A$ = +85°C | 136,000 | | | hrs |
| | $T_A$ = +55°C | 2,630,000 | | | hrs |
| | $T_A$ = +25°C | 92,600,000 | | | hrs |
| Weight | 14-Pin PDIP | | 1.08 | | g |
| **THERMAL SHUTDOWN** | | | | | |
| Die Temperature | | 115 | | 140 | °C |
| Shutdown Current | | | 3 | | mA |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –40 | | 100 | °C |

NOTES: (1) 100 % load current = 1W/$V_{NOM}$ typical. (2) Rated working voltage = 130Vrms (IEC950 convention). (3) Life test data.



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## PIN CONFIGURATION (Dual Out)




## PIN DEFINITION

| PIN # | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_S$ | Voltage Input. |
| 2 | 0V | Input Side Common. |
| 5 | 0V | Output Side Common. |
| 6 | $+V_{OUT}$ | +Voltage Out. |
| 7 | $-V_{OUT}$ | –Voltage Out. |
| 8 | $SYNC_{OUT}$ | Unregulated 400kHz Output from Transformer. |
| 14 | $SYNC_{IN}$ | Synchronization Pin. |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

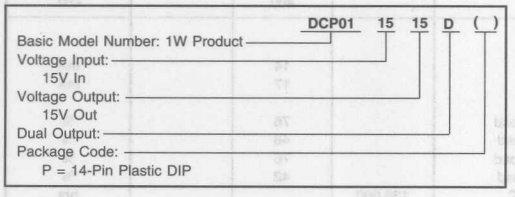
| | |
|---|---|
| Input Voltage | 18V |
| Storage Temperature | –60°C to +150°C |
| Lead Temperature (soldering, 10s) | 300°C |

## PACKAGE INFORMATION

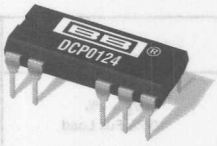
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| DCP011512DP | 14-Pin Plastic DIP | 010-1 |
| DCP011515DP | 14-Pin Plastic Dip | 010-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION



BURR-BROWN®




# DCP0124 Series

www.burr-brown.com/databook/DCP0124.html

# Miniature 24V Input, 1W Isolated UNREGULATED DC/DC CONVERTERS



## FEATURES

- STANDARD JEDEC PLASTIC PACKAGE
- LOW PROFILE: 0.15" (3.8mm)
- SYNCHRONIZABLE
- OUTPUT SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN
- STARTS INTO ANY CAPACITIVE LOAD
- EFFICIENCY: 76% (±15V Out)
- 1000Vrms ISOLATION
- 400kHz SWITCHING
- 93 MILLION HOURS MTTF

## APPLICATIONS

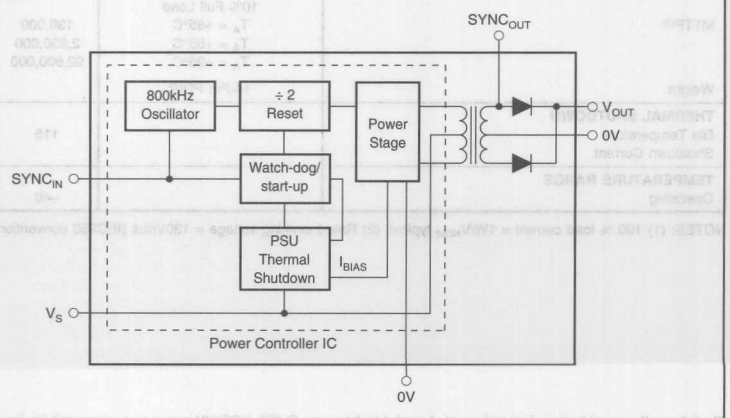
- POINT OF USE POWER CONVERSION
- GROUND LOOP ELIMINATION
- DATA ACQUISITION
- INDUSTRIAL CONTROL AND INSTRUMENTATION
- TEST EQUIPMENT

## DESCRIPTION

The DCP0124 family is a series of high efficiency, 24V input isolated DC/DC converters. In addition to 1W nominal galvanically isolated output power capability, the range of DC/DCs are also fully synchronizable. The devices feature thermal shutdown, and overload protection is implemented via watchdog circuitry(1). Advanced power-on reset techniques give superior reset performance and the devices will start into any capacitive load up to full power output.

The DCP01 family is implemented in standard-molded IC packaging, giving outlines suitable for high volume assembly.

NOTE: (1) Patents Pending.




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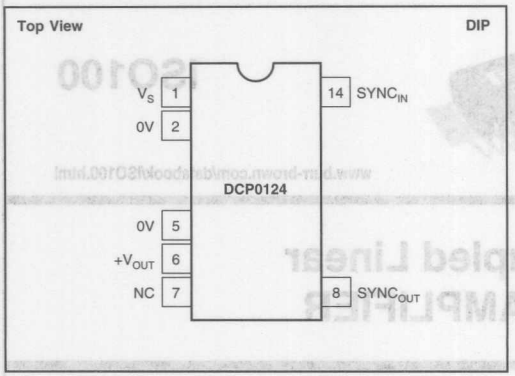
## SPECIFICATIONS

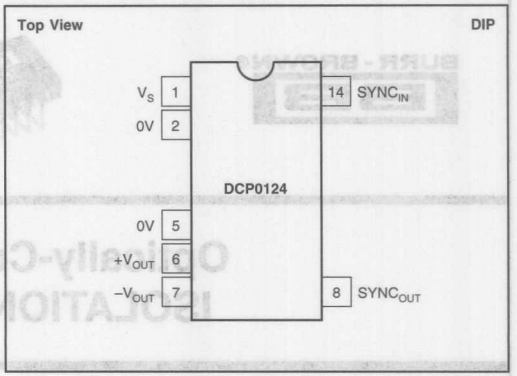
At $T_A$ = +25°C, $V_S$ = +24V, unless otherwise specified.

| PARAMETER | CONDITIONS | DCP0124 SERIES MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **OUTPUT** | | | | | |
| Power | $V_S$ + 4% | | 1 | | W |
| | 100% Full Load | | 0.92 | | W |
| Voltage ($V_{NOM}$)[1] | | | | | |
| DCP012405 | 75% Full Load | 4.75 | 5 | 5.25 | V |
| DCP012415D | 75% Full Load | ±14.25 | ±15 | ±15.75 | V |
| Voltage vs Temperature | | | ±0.08 | | %/°C |
| Short Circuit Duration | $V_S$ ± 10% | Indefinite | | | |
| Ripple | $C_L$ = O/P Capacitor = 11µF | | 25 | | mVp-p |
| | 100% Full Load | | | | |
| **INPUT** | | | | | |
| Nominal Voltage ($V_S$) | | | 24 | | V |
| Voltage Range | | –10 | | 10 | % |
| Supply Current | 100% Full Load | | 59 | | mA |
| Reflected Ripple Current | $C_{IN}$ = I/P Capacitor = 1µF | | 8 | | mArms |
| | 50% Full Load | | | | |
| **ISOLATION** | | | | | |
| Voltage[2] | 1s Flash Test | 1 | | | kVrms |
| Continuous Voltage[3] | | | 1 | | kVrms |
| Insulation Resistance | | | >1 | | GΩ |
| Input/Output Capacitance | | | 2.5 | | pF |
| **REGULATION** | | | | | |
| Load Regulation | | | | | |
| DCP012405 | 100% to 75% Full Load | | 4 | 8 | % |
| | 75% to 10% Full Load | | 9 | 15 | % |
| DCP012415D | 100% to 75% Full Load | | 4 | 7 | % |
| | 75% to 25% Full Load | | 8 | 12 | % |
| | 25% to 10% Full Load | | 11 | 16 | % |
| Line Regulation | 75% Full Load | | 1.003 | | %/1% of $V_S$ |
| **SWITCHING/SYNCHRONIZATION** | | | | | |
| Oscillator Frequency ($f_{OSC}$) | Switching Frequency = $f_{OSC}$/2 | | 800 | | kHz |
| Sync Input Low | | 0 | | 0.8 | V |
| Sync Input Current | $V_{SYNC}$ = +2V | | 48 | | µA |
| Reset Time | | | 3.8 | | µs |
| $SYNC_{OUT}$ Frequency | | | 400 | | kHz |
| **GENERAL** | | | | | |
| Quiescent Current | | | | | |
| DCP012405 | | | 14 | | mA |
| DCP012415D | | | 17 | | mA |
| Efficiency | | | | | |
| DCP012405 | 100% Full Load | | 65 | | % |
| | 10% Full Load | | 34 | | % |
| DCP012415D | 100% Full Load | | 76 | | % |
| | 10% Full Load | | 36 | | % |
| MTTF[3] | $T_A$ = +85°C | 136,000 | | | hrs |
| | $T_A$ = +55°C | 2,630,000 | | | hrs |
| | $T_A$ = +25°C | 92,600,000 | | | hrs |
| Weight | 14-Pin PDIP | | 1.08 | | g |
| **THERMAL SHUTDOWN** | | | | | |
| Die Temperature | | 115 | | 140 | °C |
| Shutdown Current | | | 3 | | mA |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –40 | | 100 | °C |

NOTES: (1) 100 % load current = 1W/$V_{NOM}$ typical. (2) Rated working voltage = 130Vrms (IEC950 convention). (3) Life test data.

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## PIN DEFINITION (Single)

| PIN # | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_S$ | Voltage Input. |
| 2 | 0V | Input Side Common. |
| 5 | 0V | Output Side Common. |
| 6 | $+V_{OUT}$ | +Voltage Out. |
| 7 | NC | No Connection. |
| 8 | $SYNC_{OUT}$ | Unregulated 400kHz Output from Transformer. |
| 14 | $SYNC_{IN}$ | Synchronization Pin. |

## PIN DEFINITION (Dual)

| PIN # | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_S$ | Voltage Input. |
| 2 | 0V | Input Side Common. |
| 5 | 0V | Output Side Common. |
| 6 | $+V_{OUT}$ | +Voltage Out. |
| 7 | $-V_{OUT}$ | –Voltage Out. |
| 8 | $SYNC_{OUT}$ | Unregulated 400kHz Output from Transformer. |
| 14 | $SYNC_{IN}$ | Synchronization Pin. |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Input Voltage | 29V |
| Storage Temperature | –60°C to +150°C |
| Lead Temperature (soldering, 10s) | 300°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| DCP012405P | 14-Pin Plastic DIP | 010-1 |
| DCP012415DP | 14-Pin Plastic Dip | 010-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

DCP01 24 05 (D) ( )

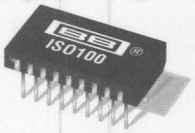
Basic Model Number: 1W Product
Voltage Input:
24V In
Voltage Output:
5V Out
Dual Output:
Package Code:
P = 14-Pin Plastic DIP

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR - BROWN®



# ISO100

www.burr-brown.com/databook/ISO100.html

# Optically-Coupled Linear ISOLATION AMPLIFIER

## FEATURES

- EASY TO USE, SIMILAR TO AN OP AMP
  $V_{OUT}/I_{IN} = R_F$, Current Input
  $V_{OUT}/V_{IN} = R_F/R_{IN}$, Voltage Input
- 100% TESTED FOR BREAKDOWN: 750V Continuous Isolation Voltage
- ULTRA-LOW LEAKAGE: 0.3μA, max, at 240V/60Hz
- WIDE BANDWIDTH: 60kHz
- 18-PIN DIP PACKAGE

## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer Sensing
  (Thermocouples, RTD, Pressure Bridges)
  4mA to 20mA Loops
  Motor and SCR Control
  Ground Loop Elimination
- BIOMEDICAL MEASUREMENTS
- TEST EQUIPMENT
- DATA ACQUISITION

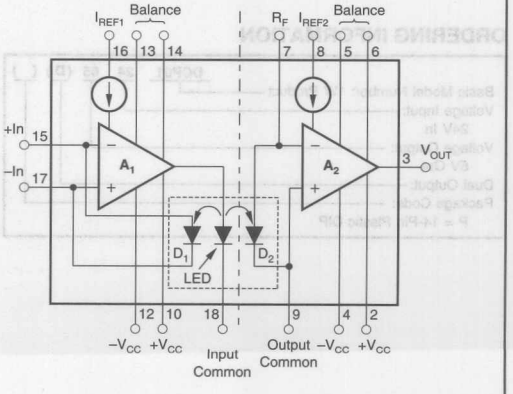
## DESCRIPTION

The ISO100 is an optically-coupled isolation amplifier. High accuracy, linearity, and time-temperature stability are achieved by coupling light from an LED back to the input (negative feedback) as well as forward to the output. Optical components are carefully matched and the amplifier is actively laser-trimmed to assure excellent tracking and low offset errors.

The circuit acts as a current-to-voltage converter with a minimum of 750V (2500V test) between input and output terminals. It also effectively breaks the galvanic connection between input and output commons as indicated by the ultra-low 60Hz leakage current of 0.3μA at 250V. Voltage input operation is easily achieved by using one external resistor.

Versatility along with outstanding DC and AC performance provide excellent solutions to a variety of challenging isolation problems. For example, the ISO100 is capable of operating in many modes, including: noninverting (unipolar and bipolar) and inverting (unipolar and bipolar) configurations. Two precision current sources are provided to accomplish bipolar operation. Since these are not required for unipolar operation, they are available for external use (see Applications section).

Designs using the ISO100 are easily accomplished with relatively few external components. Since $V_{OUT}$ of the ISO100 is simply $I_{IN}R_F$, gains can be changed by altering one resistor value. In addition, the ISO100 has sufficient bandwidth (DC to 60kHz) to amplify most industrial and test equipment signals.




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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C and $\pm V_{CC}$ = 15VDC, unless otherwise specified.

| PARAMETER | CONDITIONS | ISO100AP | | | ISO100BP | | | ISO100CP | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ISOLATION** | | | | | | | | | | | |
| Voltage | | | | | | | | | | | |
| Rated Continuous, AC peak or DC[1] | | 750 | | | * | | | * | | | V |
| Test Breakdown, DC | 10s | 2500 | | | * | | | * | | | V |
| Rejection[2] DC | | | 5 | | | * | | | * | | pA/V |
| | $R_{IN}$ = 10kΩ, Gain = 100 | | 146 | | | * | | | * | | dB |
| AC | 60Hz, 480V, $R_F$ = 1MΩ | | 400 | | | * | | | * | | pA/V |
| | $R_{IN}$ = 10kΩ, Gain = 100 | | 108 | | | * | | | * | | dB |
| Impedance | | | $10^{12}$\|\|2.5 | | | * | | | * | | Ω\|\|pF |
| Leakage Current | 240Vrms, 60Hz | | | 0.3 | | | * | | | * | µA, rms |
| **OFFSET VOLTAGE (RTI)** | | | | | | | | | | | |
| Input Stage ($V_{OSI}$) | | | | | | | | | | | |
| Initial Offset | | | | 500 | | | 300 | | | 200 | µV |
| vs Temperature | | | | 5 | | | 2 | | | 2 | µV/°C |
| vs Input Power Supplies | | | | 105 | | | * | | | * | dB |
| vs Time | | | 1 | | | * | | | * | | µV/kHr |
| Output Stage ($V_{OSO}$) | | | | | | | | | | | |
| Initial Offset | | | | 500 | | | 300 | | | 200 | µV |
| vs Temperature | | | | 5 | | | 2 | | | 2 | µV/°C |
| vs Output Power Supplies | | | | 105 | | | * | | | * | dB |
| vs Time | | | 1 | | | * | | | * | | µV/kHr |
| Common-Mode Rejection Ratio[2] | 60Hz, $R_F$ = 1MΩ | | 3 | | | * | | | * | | nA/V |
| | $R_{IN}$ = 10kΩ, Gain = 100 | | 90 | | | * | | | * | | dB |
| Common-Mode Range | | ±10 | | | * | | | * | | | V |
| **REFERENCE CURRENT SOURCES** | | | | | | | | | | | |
| Magnitude | | | | | | | | | | | |
| Nominal | | 10.5 | 12 | 12.5 | * | * | * | * | * | * | µA |
| vs Temperature | | | | 300 | | | * | | | 150 | ppm/°C |
| vs Power Supplies | | | 0.3 | 3 | | * | * | | * | * | nA/V |
| Matching | | | | | | | | | | | |
| Nominal | | | 50 | | | * | | | * | | nA |
| vs Temperature | | | 150 | | | * | | | * | | ppm/°C |
| vs Power Supplies | | | 0.3 | | | * | | | * | | nA/V |
| Compliance Voltage | | –10 | | +15 | * | | * | * | | * | V |
| Output Resistance | | | $2 \times 10^9$ | | | * | | | * | | Ω |
| **FREQUENCY RESPONSE** | | | | | | | | | | | |
| Small Signal Bandwidth | Gain = 1V/µA | | 60 | | | * | | | * | | kHz |
| Full Power Bandwidth | Gain = 1V/µA, $V_O$ = ±10V | | 5 | | | * | | | * | | kHz |
| Slew Rate | | 0.22 | 0.31 | | * | * | | * | * | | V/µs |
| Settling Time | 0.1% | | 100 | | | * | | | * | | µs |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification | | –25 | | +85 | * | | * | * | | * | °C |
| Operating | | –40 | | +100 | * | | * | * | | * | °C |
| Storage | | –40 | | +100 | * | | * | * | | * | °C |
| **UNIPOLAR OPERATION** | | | | | | | | | | | |
| **GENERAL PARAMETERS** | | | | | | | | | | | |
| Input Current Range | | | | | | | | | | | |
| Linear Operation | | –20 | | –0.02 | * | | * | * | | * | µA |
| Without Damage | | –1 | | +1 | * | | * | * | | * | mA |
| Input Impedance | | | 0.1 | | | * | | | * | | Ω |
| Output Voltage Swing | $R_L$ = 2kΩ, $R_F$ = 1MΩ | –10 | | 0 | * | | * | * | | * | V |
| Output Impedance | DC, Open-Loop | | 1200 | | | * | | | * | | Ω |
| **GAIN** | $V_O = R_F (I_{IN})$ | | | | | | | | | | |
| Initial Error (adjustable to zero) | | | 2 | 5 | | 1 | 2 | | 1 | 2 | % of FS |
| vs Temperature | | | 0.03 | 0.07 | | 0.01 | 0.05 | | 0.005 | 0.03 | %/°C |
| vs Time | | | 0.05 | | | * | | | * | | %/kHr |
| Nonlinearity[3] | | | 0.1 | 0.4 | | 0.03 | 0.1 | | 0.02 | 0.07 | % |
| **CURRENT NOISE** | $I_{IN}$ = 0.2µA | | | | | | | | | | |
| 0.01Hz to 10Hz | | | 20 | | | * | | | * | | pAp-p |
| 10Hz | | | 1 | | | * | | | * | | pA/√Hz |
| 100Hz | | | 0.7 | | | * | | | * | | pA/√Hz |
| 1kHz | | | 0.65 | | | * | | | * | | pA/√Hz |

# SPECIFICATIONS (CONT)

## ELECTRICAL

At $T_A$ = +25°C and $\pm V_{CC}$ = 15VDC, unless otherwise specified.

| PARAMETER | CONDITIONS | ISO100AP | | | ISO100BP | | | ISO100CP | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT OFFSET CURRENT ($I_{OS}$)** | | | | | | | | | | | |
| Initial Offset | | | 1 | 10 | | * | * | | * | * | nA |
| vs Temperature | | | 0.05 | | | * | | | * | | nA/°C |
| vs Power Supplies | | | 0.1 | | | * | | | * | | nA/V |
| vs Time | | | 100 | | | * | | | * | | pA/kHr |
| **POWER SUPPLIES** | | | | | | | | | | | |
| Input Stage | | | | | | | | | | | |
| Voltage (rated performance) | | | ±15 | | | * | | | * | | V |
| Voltage (derated performance) | | ±7 | | ±18 | * | | * | * | | * | V |
| Supply Current | $I_{IN}$ = –0.02µA | | ±1.1 | ±2 | | * | * | | * | * | mA |
| | $I_{IN}$ = –20µA | | +8, –1.1 | +13, –2 | | * | * | | * | * | mA |
| Output Stage | | | | | | | | | | | |
| Voltage (rated performance) | | | ±15 | | | * | | | * | | V |
| Voltage (derated performance) | | ±7 | | ±18 | * | | * | * | | * | V |
| Supply Current | $V_O$ = 0 | | ±1.1 | ±2 | | * | * | | * | * | mA |
| Short Circuit Current Limit | | | | ±40 | | | * | | | * | mA |
| **BIPOLAR OPERATION** | | | | | | | | | | | |
| **GENERAL PARAMETERS** | | | | | | | | | | | |
| Input Current Range | | | | | | | | | | | |
| Linear Operation | | –10 | | +10 | * | | * | * | | * | µA |
| Without Damage | | –1 | | +1 | * | | * | * | | * | mA |
| Input Impedance | | | 0.1 | | | * | | | * | | Ω |
| Output Voltage Swing | $R_L$ = 2kΩ, $R_F$ = 1MΩ | –10 | | +10 | * | | * | * | | * | V |
| Output Impedance | | | 1200 | | | * | | | * | | Ω |
| **GAIN** | $V_O = R_F (I_{IN})$ | | | | | | | | | | |
| Initial Error (Adjustable To Zero) | | | 2 | 5 | | 1 | 2 | | 1 | 2 | % of FS |
| vs Temperature | | | 0.03 | 0.07 | | 0.01 | 0.05 | | 0.005 | 0.03 | %/°C |
| vs Time | | | 0.05 | | | * | | | * | | %/kHr |
| Nonlinearity[3] | | | 0.1 | 0.4 | | 0.03 | 0.1 | | 0.02 | 0.07 | % |
| **CURRENT NOISE** | $I_{IN}$ = 0.2µA | | | | | | | | | | |
| 0.01Hz to 10Hz | | | 1.5 | | | * | | | * | | nA, p-p |
| 10Hz | | | 17 | | | * | | | * | | pA/√Hz |
| 100Hz | | | 7 | | | * | | | * | | pA/√Hz |
| 1kHz | | | 6 | | | * | | | * | | pA/√Hz |
| **INPUT OFFSET CURRENT** ($I_{OS}$, bipolar[4]) | | | | | | | | | | | |
| Initial Offset | | | 40 | 200 | | 20 | 70 | | 10 | 35 | nA |
| vs Temperature | | | | 3 | | | 2 | | | 1 | nA/°C |
| vs Power Supplies | | | | 0.7 | | | * | | | * | nA/V |
| vs Time | | | 250 | | | * | | | * | | pA/kHr |
| **POWER SUPPLIES** | | | | | | | | | | | |
| Input Stage | | | | | | | | | | | |
| Voltage (rated performance) | | | ±15 | | | * | | | * | | V |
| Voltage (derated performance) | | ±7 | | ±18 | * | | * | * | | * | V |
| Supply Current | $I_{IN}$ = +10µA | | +2, –1.1 | +3, –2 | | * | * | | * | * | mA |
| | $I_{IN}$ = –10µA | | +8, –1.1 | +13, –2 | | * | * | | * | * | mA |
| Output Stage | | | | | | | | | | | |
| Voltage (rated performance) | | | ±15 | | | * | | | * | | V |
| Voltage (derated performance) | | ±7 | | ±18 | * | | * | * | | * | V |
| Supply Current | $V_O$ = 0 | | ±1.1 | ±2 | | * | * | | * | * | mA |
| Short Circuit Current Limit | | | | ±40 | | | * | | | * | mA |

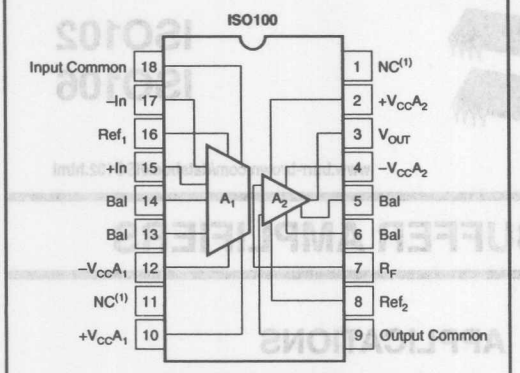
* Specification same as ISO100AP.

NOTES: (1) See Typical Performance Curves for temperature effects. (2) See Theory of Operation section for definitions. For dB see Ex. 2, CM and HV errors. (3) Nonlinearity is the peak deviation from a "best fit" straight line expressed as a percent of full scale output. (4) Bipolar offset current includes effects of reference current mismatch and unipolar offset current.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN CONFIGURATION

Bottom View




NOTE: (1) No internal connection.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ISO100AP | 18-Pin Bottom-Braze DIP | 220 | –25°C to +85°C |
| ISO100BP | 18-Pin Bottom-Braze DIP | 220 | –25°C to +85°C |
| ISO100CP | 18-Pin Bottom-Braze DIP | 220 | –25°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

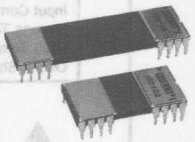
| | |
|---|---|
| Supply Voltages | ±18V |
| Isolation Voltage, AC pk or DC | 750V |
| Input Current | ±1mA |
| Storage Temperature Range | –40°C to +100°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short-Circuit Duration | Continuous to Ground |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR - BROWN®



# ISO102
# ISO106

www.burr-brown.com/databook/ISO102.html

# SIGNAL ISOLATION BUFFER AMPLIFIERS

## FEATURES

- 14-BIT LINEARITY
- INDUSTRY'S FIRST HERMETIC ISOLATION AMPLIFIERS AT LOW COST
- EASY-TO-USE COMPLETE CIRCUIT
- RUGGED BARRIER, HV CERAMIC CAPACITORS
- 100% TESTED FOR HIGH VOLTAGE BREAKDOWN
  ISO102: 4000Vrms/10s, 1500Vrms/1min
  ISO106: 8000Vpk/10s, 3500Vrms/1min
- ULTRA HIGH IMR: 125dB min at 60Hz, ISO106
- WIDE INPUT RANGE: –10V to +10V
- WIDE BANDWIDTH: 70kHz
- VOLTAGE REFERENCE OUTPUT: 5VDC

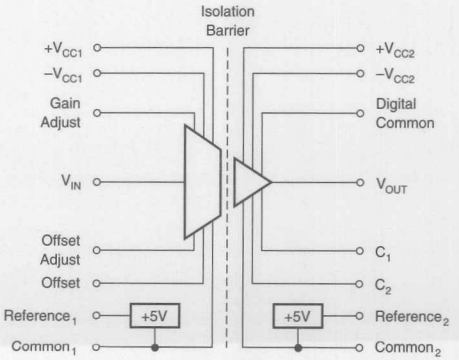
## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer channel isolator for thermocouples, RTDs, pressure bridges, flow meters
- 4mA TO 20mA LOOP ISOLATION
- MOTOR AND SCR CONTROL
- GROUND LOOP ELIMINATION
- BIOMEDICAL/ANALYTICAL MEASUREMENTS
- POWER PLANT MONITORING
- DATA ACQUISITION/TEST EQUIPMENT ISOLATION
- MILITARY EQUIPMENT

## DESCRIPTION

The ISO102 and ISO106 isolation buffer amplifiers are two members of our series of capacitive coupled isolation products from Burr-Brown. They have the same electrical performance and they differ in accuracy. The ISO102 is rated for 1500Vrms in a 24-pin DIP. The ISO106 is rated for 3500Vrms in a 40-pin DIP. Both side-brazed DIPs are 600mil wide and have industry standard package dimensions with the exception of missing pins between input and output stages. This permits utilization of automatic insertion techniques in production. The three-chip hybrid with its generous high voltage spacing is easy to use (no external components are required).

Each buffer accurately isolates ±10V analog signals by digitally encoding the input voltage and uniquely coupling across a differential ceramic capacitive barrier. All elements necessary for operation are contained within the DIP. This provides compact signal isolation in a hermetic package.




Covered by patent number 4,748,419 and others pending.

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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C and $V_{CC1}$ = $V_{CC2}$ = ±15V, unless otherwise noted.

| PARAMETER | CONDITIONS | ISO102, ISO106, ISO102B, ISO106B MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **ISOLATION** | | | | | |
| Voltage | | | | | |
| Rated Continuous[1] | | | | | |
| ISO102: AC, 60Hz | $T_{MIN}$ to $T_{MAX}$ | 1500 | | | Vrms |
| DC | $T_{MIN}$ to $T_{MAX}$ | 2121 | | | VDC |
| ISO106: AC, 60Hz | $T_{MIN}$ to $T_{MAX}$ | 3500 | | | Vrms |
| DC | $T_{MIN}$ to $T_{MAX}$ | 4950 | | | VDC |
| Test Breakdown, AC, 60Hz | | | | | |
| ISO102 | 10s | 4000 | | | Vrms |
| ISO106 | 10s | 8000 | | | Vpk |
| Isolation-Mode Rejection[2] | $V_{ISO}$ = Rated Continuous, 60Hz | | | | |
| AC: ISO102 | | 115 | 120 | | dB |
| | | | 1 | 2 | µVrms/V |
| ISO106 | | 125 | 130 | | dB |
| | | | 0.3 | 0.6 | µVrms/V |
| DC | | 140 | 160 | | dB |
| | | | 0.01 | 0.10 | µVDC/V |
| Barrier Resistance | | | $10^{14}$ | | Ω |
| Barrier Capacitance | | | 6 | | pF |
| Leakage Current | $V_{ISO}$ = 240Vrms, 60Hz | | 0.5 | 1 | µArms |
| **INPUT** | | | | | |
| Voltage Range | Rated Operation | –10 | | +10 | V |
| Resistance | | 75 | 100 | | kΩ |
| Capacitance | | | 5 | | pF |
| **OUTPUT** | | | | | |
| Voltage Range | Rated Operation | –10 | | +10 | V |
| | Derated Operation | –12 | | +12 | V |
| Current Drive | | ±5 | | | mA |
| Short Circuit Current | | 9 | 20 | 50 | mA |
| Ripple Voltage[6] | f = 0.5MHz to 1.5MHz | | 3 | | mVp-p |
| Resistance | | | 0.3 | 1 | Ω |
| Capacitive Load Drive Capability | | 10,000 | | | pF |
| Overload Recovery Time, 0.1% | $\|V_O\|$ > 12V | | 30 | | µs |
| **OUTPUT VOLTAGE NOISE** | | | | | |
| Voltage: f = 0.1Hz to 10Hz | | | 300 | | µVp-p |
| f = 0.1Hz to 70kHz | | | 16 | | µV/√Hz |
| Dynamic Range[7]: f = 0.1Hz to 70kHz | 12-Bit Resolution, 1LSB, 20V FS | | 74 | | dB |
| f = 0.1Hz to 280Hz | 16-Bit Resolution, 1LSB, 20V FS | | 96 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Small Signal Bandwidth | | | 70 | | kHz |
| Full Power Bandwidth, 0.1% THD | $V_O$ = ±10V | | 5 | | kHz |
| Slew Rate | $V_O$ = ±10V | | 0.5 | | V/µs |
| Settling Time, 0.1% | $V_O$ = –10V to +10V | | 100 | | µs |
| Overshoot, Small Signal[8] | $C_1$ = $C_2$ = 0 | | 40 | | % |
| **VOLTAGE REFERENCES** | | | | | |
| Voltage Output, $Ref_1$, $Ref_2$ | No Load | +4.975 | +5 | +5.025 | VDC |
| B Grade | No Load | +4.995 | +5 | +5.005 | VDC |
| vs Temperature | | | ±5 | 20 | ppm/°C |
| vs Supplies | | | 10 | | µV/V |
| vs Load | | | 400 | 1000 | µV/mA |
| Current Output | | –0.1 | +5 | | mA |
| Short Circuit Current | | 6 | 14 | 30 | mA |
| **POWER SUPPLIES** | | | | | |
| Rated Voltage, $\pm V_{CC1}$, $\pm V_{CC2}$ | Rated Performance | | ±15 | | V |
| Voltage Range | | ±10 | | ±20 | V |
| Quiescent Current: $+V_{CC1}$ | No Load | | +11 | +15 | mA |
| $-V_{CC1}$ | | | –9 | –12 | mA |
| $+V_{CC2}$ | | | +25 | +33 | mA |
| $-V_{CC2}$ | | | –15 | –20 | mA |
| Dissipation: $\pm V_{CC1}$ | | | 300 | 400 | mW |
| $\pm V_{CC2}$ | | | 600 | 800 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –25 | | +85 | °C |
| Operating[9] | | –25 | | +85 | °C |
| Storage | | –65 | | +150 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | 40 | | °C/W |
| $\theta_{JC}$ | | | 12 | | °C/W |

## ELECTRICAL (CONT)

| PARAMETER | CONDITIONS | ISO102 MIN | ISO102 TYP | ISO102 MAX | ISO102B MIN | ISO102B TYP | ISO102B MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **GAIN** | | | | | | | | |
| Nominal Gain | | | 1 | | | * | | V/V |
| Initial Error[3] | | | ±0.1 | ±0.25 | | 0.07 | 0.13 | % FSR |
| Gain vs Temperature | | | ±20 | ±50 | | ±12 | ±25 | ppm FSR/°C |
| Nonlinearity[4] | $V_O$ = –10V to +10V | | ±0.007 | ±0.012 | | ±0.002 | ±0.003 | % FSR |
| **INPUT OFFSET VOLTAGE** | | | | | | | | |
| Initial Offset | $V_{IN}$ = 0V | | ±25 | ±70 | | ±15 | ±25 | mV |
| vs Temperature | | | ±250 | ±500 | | ±150 | ±250 | µV/°C |
| vs Power Supplies[5] | Input Stage, $V_{CC1}$ = ±10V to ±20V | 0 | 1.4 | 4.0 | * | * | * | mV/V |
| | Output Stage, $V_{CC2}$ = ±10V to ±20V | –4 | –1.4 | 0 | * | * | * | mV/V |

* Specification same as ISO102.

| PARAMETER | CONDITIONS | ISO106 MIN | ISO106 TYP | ISO106 MAX | ISO106B MIN | ISO106B TYP | ISO106B MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **GAIN** | | | | | | | | |
| Nominal Gain | | | 1 | | | * | | V/V |
| Initial Error[3] | | | ±0.1 | ±0.25 | | 0.07 | * | % FSR |
| Gain vs Temperature | | | ±20 | ±50 | | ±12 | ±25 | ppm FSR/°C |
| Nonlinearity[4] | $V_O$ = –10V to +10V | | ±0.04 | ±0.075 | | ±0.007 | ±0.025 | % FSR |
| **INPUT OFFSET VOLTAGE** | | | | | | | | |
| Initial Offset | $V_{IN}$ = 0V | | ±25 | ±70 | | * | * | mV |
| vs Temperature | | | ±250 | ±500 | | ±150 | ±250 | µV/°C |
| vs Power Supplies[5] | Input Stage, $V_{CC1}$ = ±10V to ±20V | | 3.7 | | | * | | mV/V |
| | Output Stage, $V_{CC2}$ = ±10V to ±20V | | –3.7 | | | * | | mV/V |

* Specification same as ISO106.

NOTES: (1) 100% tested at rated continuous for one minute. (2) Isolation-mode rejection is the ratio of the change in output voltage to a change in isolation barrier voltage. It is a function of frequency as shown in the Typical Performance Curves. This is specified for barrier voltage slew rates not exceeding 100V/µs. (3) Adjustable to zero. FSR = Full Scale Range = 20V. (4) Nonlinearity is the peak deviation of the output voltage from the best fit straight line. It is expressed as the ratio of deviation to FSR. (5) Power supply rejection = change in $V_{OS}$/20V supply change. (6) Ripple is the residual component of the barrier carrier frequency generated internally. (7) Dynamic range = FSR/(voltage spectral noise density x square root of user bandwidth). (8) Overshoot can be eliminated by band-limiting. (9) See "Power Dissipation vs Temperature" performance curve for limitations. (10) Band limited to 10Hz, bypass capacitors located less than 0.25" from supply pins.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Without Damage | ±20V |
| Input Voltage Range | ±50V |
| Transient Immunity, dV/dt | 100kV/µs |
| Continuous Isolation Voltage Across Barrier | |
| ISO102 | 1500Vrms |
| ISO106 | 3500Vrms |
| Junction Temperature | +160°C |
| Storage Temperature Range | –65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Amplifier and Reference Output | |
| Short Circuit Duration | Continuous to Common |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| ISO102 | 24-Pin Ceramic | 208 | –25°C to +85°C |
| ISO102B | 24-Pin Ceramic | 208 | –25°C to +85°C |
| ISO106 | 24-Pin Ceramic | 206 | –25°C to +85°C |
| ISO106B | 24-Pin Ceramic | 206 | –25°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

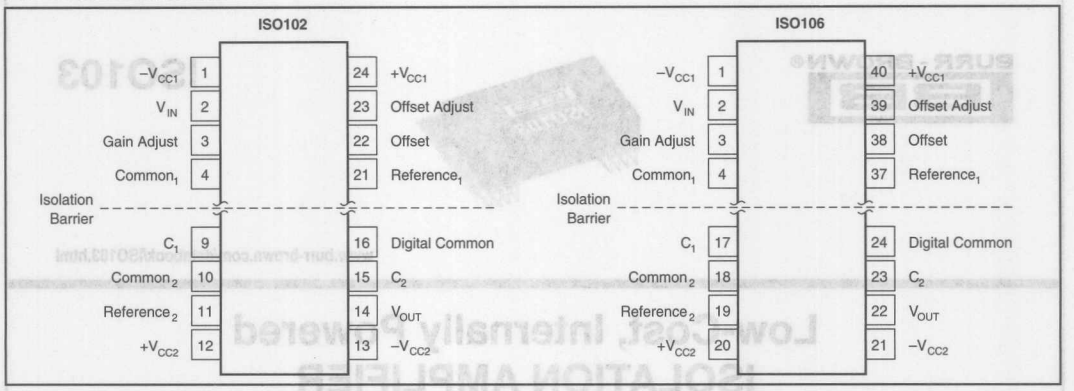
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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## PIN CONFIGURATION




## PIN DESCRIPTIONS

| | |
|---|---|
| $\pm V_{CC1}$, $Common_1$ | Positive and negative power supply voltages and common (or ground) for the input stage. $Common_1$ is the analog reference voltage for input signals. The voltage between $Common_1$ and $Common_2$ is the isolation voltage and appears across the internal high voltage barrier. |
| $\pm V_{CC2}$, $Common_2$ | Positive and negative power supply voltages and common (or ground) for the output stage. $Common_2$ is the analog reference voltage for output signals. The voltage between $Common_1$ and $Common_2$ is the isolation voltage and appears across the internal high voltage barrier. |
| $V_{IN}$ | Signal input pin. Input impedance is typically 100kΩ. The input range is rated for ±10V. The input level can actually exceed the input stage supplies. Output signal swing is limited only by the output supply voltages. |
| Gain Adjust | This pin is an optional signal input. A series 5kΩ potentiometer between this pin and the input signal allows a guaranteed ±1.5% gain adjustment range. When gain adjustment is not required, the Gain Adjust should be left open. Figure 4 illustrates the gain adjustment connection. |
| $Reference_1$ | +5V reference output. This low-drift zener voltage reference is necessary for setting the bipolar offset point of the input stage. **This pin must be strapped to either Offset or Offset Adjust to allow the isolation amplifier to function.** The reference is often useful for input signal conditioning circuits. See "Effect of Reference Loading on Offset" performance curve for the effect of offset voltage change with reference loading. $Reference_1$ is identical to, but independent of, $Reference_2$. This output is short circuit protected. |
| $Reference_2$ | +5V reference output. This reference circuit is identical to, but independent of, $Reference_1$. It controls the bipolar offset of the output stage through an internal connection. This output is short-circuit protected. |
| Offset | Offset input. **This input must be strapped to $Reference_1$** unless user adjustment of bipolar offset is required. |
| Offset Adjust | This pin is for optional offset control. When connected to the $Reference_1$ pin through a 1kΩ potentiometer, ±150mV of adjustment range is guaranteed. Under this condition, the Offset pin should be connected to the Offset Adjust pin. When offset adjustment is not required, the Offset Adjust pin is left open. See Figure 4. |
| Digital Common | Digital common or ground. This separate ground carries currents from the digital portions of the output stage circuit. The best grounding practices require that digital common current does not flow in analog common connections. Both pins can be tied directly to a ground plane if available. Difference in potentials between the $Common_2$ and Digital Common pins can be ±1V. See Figure 2. |
| $V_{OUT}$ | Signal output. Because the isolation amplifier has unity gain, the output signal is ideally identical to the input signal. The output is low impedance and is short-circuit protected. This signal is referenced to $Common_2$; subsequent circuitry should have a separate "sense" connection to $Common_1$ as well as $V_{OUT}$. |
| $C_1$, $C_2$ | Capacitors for small signal bandwidth control. These pins connect to the internal rolloff frequency controlling nodes of the output low-pass filter. Additional capacitance added to these pins will modify the bandwidth of the buffer. $C_2$ is always twice the value of $C_1$. See "Bandwidth Control" performance curve for the relationship between bandwidth and $C_1$ and $C_2$. When no connections are made to these pins, the full small-signal bandwidth is maintained. Be sure to shield $C_1$ and $C_2$ pins from high electric fields on the PC board. This preserves AC isolation-mode rejection by reducing capacitive coupling effects. |

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# ISO103

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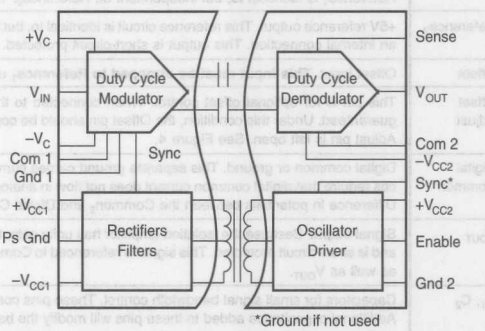
# Low-Cost, Internally Powered ISOLATION AMPLIFIER

## FEATURES

- SIGNAL AND POWER IN ONE DOUBLE-WIDE (0.6") SIDE-BRAZED PACKAGE
- 5600Vpk TEST VOLTAGE
- 1500Vrms CONTINUOUS AC BARRIER RATING
- WIDE INPUT SIGNAL RANGE: –10V to +10V
- WIDE BANDWIDTH: 20kHz Small Signal, 20kHz Full Power
- BUILT-IN ISOLATED POWER: ±10V to ±18V Input, ±50mA Output
- MULTICHANNEL SYNCHRONIZATION CAPABILITY (TTL)
- BOARD AREA ONLY 0.72in.$^2$ (4.6cm$^2$)

## APPLICATIONS

- MULTICHANNEL ISOLATED DATA ACQUISITION
- ISOLATED 4-20mA LOOP RECEIVER AND POWER
- POWER SUPPLY AND MOTOR CONTROL
- GROUND LOOP ELIMINATION




## DESCRIPTION

The ISO103 isolation amplifier provides both signal and power across an isolation barrier. The ceramic non-hermetic hybrid package with side-brazed pins contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel.

Extra power is available on the isolated input side for external input conditioning circuitry. The converter is protected from shorts to ground with an internal current limit, and the soft-start feature limits the initial currents from the power source. Multiple-channel synchronization can be accomplished by applying a TTL clock signal to paralleled Sync pins. The Enable control is used to turn off transformer drive while keeping the signal channel demodulator active. This feature provides a convenient way to reduce quiescent current for low power applications.

The wide barrier pin spacing and internal insulation allow for the generous 1500Vrms continuous rating. Reliability is assured by 100% barrier breakdown testing that conforms to UL1244 test methods. Low barrier capacitance minimizes AC leakage currents.

These specifications and built-in features make the ISO103 easy to use, as well as providing for compact PC board layouts.

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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C and $V_{CC2}$ = ±15V, ±15mA output current unless otherwise noted.

| PARAMETER | CONDITIONS | ISO103 MIN | ISO103 TYP | ISO103 MAX | ISO103B MIN | ISO103B TYP | ISO103B MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **ISOLATION** | | | | | | | | |
| Rated Continuous Voltage[1] | | | | | | | | |
| AC, 60Hz | $T_{MIN}$ to $T_{MAX}$ | 1500 | | | * | | | Vrms |
| DC | $T_{MIN}$ to $T_{MAX}$ | 2121 | | | * | | | VDC |
| Test Breakdown, 100% AC, 60Hz | 10s | 5657 | | | * | | | Vpk |
| Isolation-Mode Rejection | 1500Vrms, 60Hz | | 130 | | | * | | dB |
| | 2121VDC | | 160 | | | * | | dB |
| Barrier Impedance | | | $10^{12}$ \|\| 9 | | | * | | Ω \|\| pF |
| Leakage Current | 240Vrms, 60Hz | | 1 | 2 | | * | * | µA |
| **GAIN** | | | | | | | | |
| Nominal | | | 1 | | | * | | V/V |
| Initial Error | | | ±0.12 | ±0.3 | | ±0.08 | ±0.15 | % FSR |
| Gain vs Temperature | | | ±60 | ±100 | | ±20 | ±50 | ppm/°C |
| Nonlinearity | $V_O$ = –10V to 10V | | ±0.026 | ±0.075 | | ±0.018 | ±0.050 | % FSR |
| | $V_O$ = –5V to 5V | | ±0.009 | | | * | ±0.025 | %FSR |
| **INPUT OFFSET VOLTAGE** | | | | | | | | |
| Initial Offset | | | ±20 | ±60 | | * | * | mV |
| vs Temperature | | | ±300 | ±500 | | ±100 | ±250 | µV/°C |
| vs Power Supplies | $V_{CC2}$ = ±10V to ±18V | | 0.9 | | | * | | mV/V |
| vs Output Supply Load | $I_O$ = 0 to ±50mA | | ±0.3 | | | * | | mV/mA |
| **SIGNAL INPUT** | | | | | | | | |
| Voltage Range | Output Voltage in Range | ±10 | ±15 | | * | * | | V |
| Resistance | | | 200 | | | * | | kΩ |
| **SIGNAL OUTPUT** | | | | | | | | |
| Voltage Range | | ±10 | ±12.5 | | * | * | | V |
| Current Drive | | ±5 | ±15 | | * | * | | mA |
| Ripple Voltage, 800kHz Carrier | | | 25 | | | * | | mVp-p |
| | 400Ω/4.7nF (See Figure 4) | | 5 | | | * | | mVp-p |
| Capacitive Load Drive | | | 1000 | | | * | | pF |
| Voltage Noise | | | 4 | | | * | | µV/√Hz |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Small Signal Bandwidth | | | 20 | | | * | | kHz |
| Slew Rate | | | 1.5 | | | * | | V/µs |
| Settling Time | 0.1%, –10/10V | | 75 | | | * | | µs |
| **POWER SUPPLIES** | | | | | | | | |
| Rated Voltage, $V_{CC2}$ | | | ±15 | | | * | | V |
| Voltage Range | | ±10 | | ±18 | * | | * | V |
| Input Current | $I_O$ = ±15mA | | +90/–4.5 | | | * | | mA |
| | $I_O$ = 0mA | | +60/–4.5 | | | * | | mA |
| Ripple Current | No Filter | | 60 | | | * | | mAp-p |
| | $C_{IN}$ = 1µF | | 3 | | | * | | mAp-p |
| Rated Output Voltage | Load = 15mA | ±14.25 | ±15 | ±15.75 | * | * | * | V |
| Output | 50mA Balanced Load | 10 | | | | * | * | V |
| | 100mA Single-Ended Loads | 10 | | | | * | * | V |
| Load Regulation | Balanced Load | | 0.3 | | | * | | %/mA |
| Line Regulation | | | 1.12 | | | * | | V/V |
| Output Voltage vs Temperature | | | 2.5 | | | * | | mV/°C |
| Voltage Balance Error, $\pm V_{CC1}$ | | | 0.05 | | | * | | % |
| Voltage Ripple (800kHz) | No External Capacitors | | 50 | | | * | | mVp-p |
| | $C_{EXT}$ = 1µF | | 5 | | | * | | mVp-p |
| Output Capacitive Load | | | | 1 | | | * | µF |
| Sync Frequency | Sync-Pin Grounded [2] | | 1.6 | | | * | | MHz |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –25 | | +85 | * | | * | °C |
| Operating | | –25 | | +85 | * | | * | °C |
| Storage | | –25 | | +125 | * | | * | °C |

* Specification same as ISO103.

NOTE: (1) Conforms to UL1244 test methods. 100% tested at 1500Vrms for 1 minute. (2) If using external synchronization with a TTL-level clock, frequency should be between 1.2MHz and 2MHz with a duty-cycle greater than 25%.

## ABSOLUTE MAXIMUM RATINGS

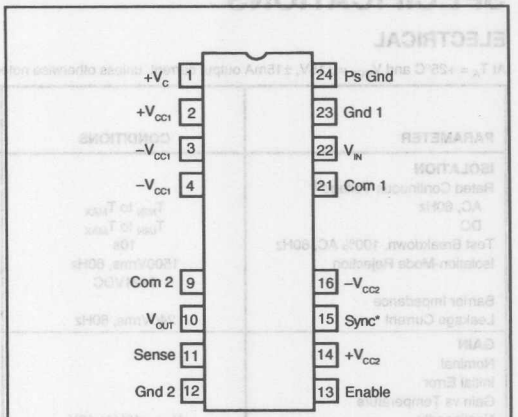
| | |
|---|---|
| Supply Without Damage | ±18V |
| $V_{IN}$, Sense Voltage | ±50V |
| Com 1 to Gnd 1 or Com 2 to Gnd 2 | ±200mV |
| Enable, Sync | 0V to $+V_{CC2}$ |
| Continuous Isolation Voltage | 1500Vrms |
| $V_{ISO}$, dv/dt | 20kV/µs |
| Junction Temperature | 150°C |
| Storage Temperature | –25°C to +125°C |
| Lead Temperature,10s | 300°C |
| Output Short to Gnd 2 Duration | Continuous |
| $\pm V_{CC1}$ to Gnd 1 Duration | Continuous |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION




*Operation requires this pin be grounded or driven with TTL levels.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ISO103 | 24-Pin DIP | 231 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# ISO107

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# High-Voltage, Internally Powered ISOLATION AMPLIFIER



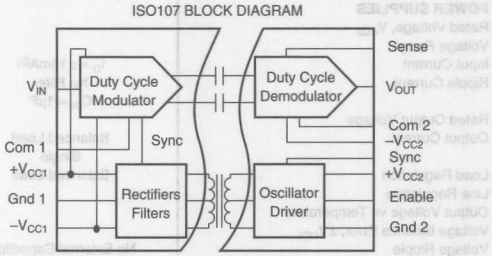
## FEATURES

- SIGNAL AND POWER IN ONE TRIPLE-WIDE PACKAGE
- 8000Vpk TEST VOLTAGE
- 2500Vrms CONTINUOUS AC BARRIER RATING
- WIDE INPUT SIGNAL RANGE: –10V to +10V
- WIDE BANDWIDTH: 20kHz Small Signal, 20kHz Full Power
- BUILT-IN ISOLATED POWER: ±10V to ±18V Input, ±50mA Output
- MULTICHANNEL SYNCHRONIZATION CAPABILITY (TTL)

## APPLICATIONS

- MULTICHANNEL ISOLATED DATA ACQUISITION
- BIOMEDICAL INSTRUMENTATION
- POWER SUPPLY AND MOTOR CONTROL
- GROUND LOOP ELIMINATION

ISO107 BLOCK DIAGRAM




## DESCRIPTION

The ISO107 isolation amplifier provides both signal and power across an isolation barrier. The ceramic side-brazed hybrid package contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel.

Extra power is available on the isolated input side for external input conditioning circuitry. The converter is protected from shorts to ground with an internal current limit, and the soft-start feature limits the initial currents from the power source. Multiple-channel synchronization can be accomplished by applying a TTL clock signal to paralleled Sync pins. The Enable control is used to turn off transformer drive while keeping the signal channel demodulator active. This feature provides a convenient way to reduce quiescent current for low power applications.

The wide barrier pin spacing and internal insulation allow for the generous 2500Vrms continuous rating. Reliability is assured by 100% barrier breakdown testing that conforms to UL544 test methods. Low barrier capacitance minimizes AC leakage currents.

These specifications and built-in features make the ISO107 easy to use, as well as providing for compact PC board layouts.

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At $T_A$ = +25°C and $V_{CC2}$ = ±15V, ±15mA output current, unless otherwise noted.

| PARAMETERS | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **ISOLATION** | | | | | |
| Rated Continuous Voltage (1) | | | | | |
| AC, 60Hz | $T_{MIN}$ to $T_{MAX}$ | 2500 | | | Vrms |
| DC | $T_{MIN}$ to $T_{MAX}$ | 3500 | | | VDC |
| Test Breakdown, AC, 60Hz | 10s | 8000 | | | Vpk |
| Isolation-Mode Rejection | 2500Vrms, 60Hz | | 100 | | dB |
| | 2121VDC | | 160 | | dB |
| Barrier Impedance | | | $10^{12}$ \|\| 13 | | Ω \|\| pF |
| Leakage Current | 240Vrms, 60Hz | | 1.2 | 2 | µA |
| **GAIN** | | | | | |
| Nominal | | | 1 | | V/V |
| Initial Error | | | ±0.1 | ±0.25 | % FSR |
| Gain vs Temperature | | | ±50 | ±120 | ppm/°C |
| Nonlinearity | | | ±0.01 | ±0.025 | % FSR |
| **INPUT OFFSET VOLTAGE** | | | | | |
| Initial Offset | | | ±20 | ±50 | mV |
| vs Temperature | | | ±150 | ±400 | µV/°C |
| vs Power Supplies | $V_{CC2}$ = ±10V to ±18V | | ±2 | | mV/V |
| **INPUT** | | | | | |
| Voltage Range | Output Voltage in Range | ±10 | ±15 | | V |
| Resistance | | | 200 | | kΩ |
| **SIGNAL OUTPUT** | | | | | |
| Voltage Range | | ±10 | ±12.5 | | V |
| Current Drive | | ±5 | ±15 | | mA |
| Ripple Voltage, 800kHz Carrier (See Figure 4) | | | 20 | | mVp-p |
| Capacitive Load Drive | | | 1000 | | pF |
| Voltage Noise | | | 4 | | µV/√Hz |
| **FREQUENCY RESPONSE** | | | | | |
| Small Signal Bandwidth | | | 20 | | kHz |
| Slew Rate | | | 1.5 | | V/µs |
| Settling Time | 0.1%, –10/10V | | 75 | | µs |
| **POWER SUPPLIES** | | | | | |
| Rated Voltage, $V_{CC2}$ | | | ±15 | | V |
| Voltage Range | | ±10 | | ±18 | V |
| Input Current | $I_O$ = ±15mA(2) | | +75/–4.5 | | mA |
| Ripple Current | No Filter | | 10 | | mAp-p |
| | $C_{IN}$ = 1µF | | 3 | | mAp-p |
| Rated Output Voltage | | ±14.25 | ±15 | ±15.75 | V |
| Output Current | Balanced Load | | ±15 | ±50 | mA |
| | Single | | 30 | 100 | mA |
| Load Regulation | Balanced Load | | 0.5 | | %/mA |
| Line Regulation | | | 1.18 | | V/V |
| Output Voltage vs Temperature | | | 10 | | mV/°C |
| Voltage Balance Error, ±$V_{CC1}$ | | | 0.05 | | % |
| Voltage Ripple | No External Capacitors | | 10 | | mVp-p |
| Output Capacitive Load (See Figure 1) | | | | 1 | µF |
| Sync Frequency | Sync-Pin Grounded(3) | | 1.6 | | MHz |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –25 | | +85 | °C |
| Operating | | –25 | | +85 | °C |
| Storage | | –25 | | +125 | °C |

NOTES: (1) Conforms to UL544 test methods. 100% tested at 2500Vrms for 1 minute. (2) For other conditions, see Performance Curve, Input Current (+$V_{CC2}$) vs Output Current. Input Current (–$V_{CC2}$) is constant at –4.5mA (typ) for all output currents. (3) If using external synchronization with a TTL-level clock, frequency should be between 1.2MHz and 2MHz with a duty-cycle greater than 25%.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Without Damage | ±18V |
| $V_{IN}$, Sense Voltage | ±50V |
| Com 1 to Gnd 1 or Com 2 to Gnd 2 | ±200mV |
| Enable, Sync | 0V to $+V_{CC2}$ |
| Continuous Isolation Voltage | 2500Vrms |
| $V_{ISO}$, dv/dt | 20kV/µs |
| Junction Temperature | 150°C |
| Storage Temperature | –25°C to +125°C |
| Lead Temperature, (soldering, 10s) | 300°C |
| Output Short to Gnd 2 Duration | Continuous |
| $\pm V_{CC1}$ to Gnd 1 Duration | Continuous |

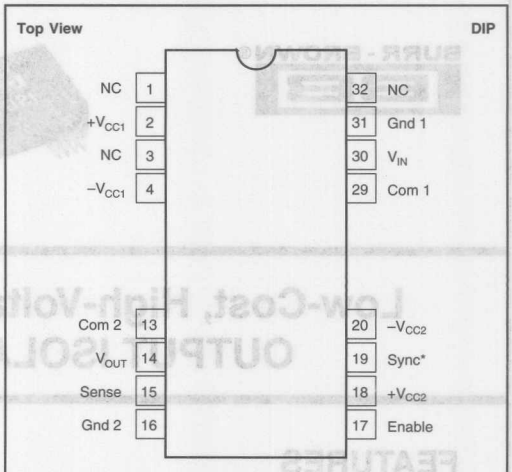
## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ISO107 | 32-Pin Side-Braze Ceramic | 210 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN CONFIGURATION

Top View DIP




*Operation requires that this pin be grounded or driven with TTL levels.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®




ISO113

www.burr-brown.com/databook/ISO113.html

# Low-Cost, High-Voltage, Internally Powered OUTPUT ISOLATION AMPLIFIER

## FEATURES

- SELF-CONTAINED ISOLATED SIGNAL AND OUTPUT POWER
- SMALL PACKAGE SIZE: Double-Wide (0.6") Sidebraze DIP
- CONTINUOUS AC BARRIER RATING: 1500Vrms
- WIDE BANDWIDTH: 20kHz Small Signal, 20kHz Full Power
- BUILT-IN ISOLATED OUTPUT POWER: ±10V to ±18V Input, ±50mA Output
- MULTICHANNEL SYNCHRONIZATION CAPABILITY
- BOARD AREA ONLY 0.72in.$^2$ (4.6cm$^2$)

## APPLICATIONS

- 4mA TO 20mA V/I CONVERTERS
- MOTOR AND VALVE CONTROLLERS
- ISOLATED RECORDER OUTPUTS
- MEDICAL INSTRUMENTATION OUTPUTS
- GAS ANALYZERS

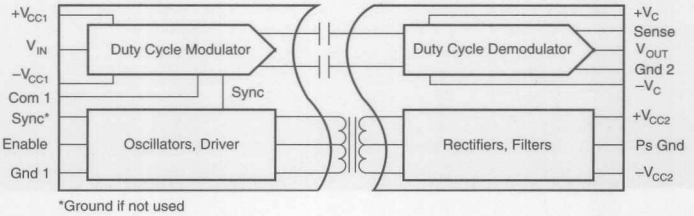
## DESCRIPTION

The ISO113 output isolation amplifier provides both signal and output power across an isolation barrier in a small double-wide DIP package. The ceramic non-hermetic hybrid package with side-brazed pins contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel.

Extra power is available on the isolated output side for driving external loads. The converter is protected from shorts to ground with an internal current limit, and the soft-start feature limits the initial currents from the power source. Multiple-channel synchronization can be accomplished by applying a TTL clock signal to paralleled Sync pins. The Enable control is used to turn off transformer drive while keeping the signal channel modulator active. This feature provides a convenient way to reduce quiescent current for low power applications.

The wide barrier pin spacing and internal insulation allow for the generous 1500Vrms continuous rating. Reliability is assured by 100% barrier breakdown testing that conforms to UL1244 test methods. Low barrier capacitance minimizes AC leakage currents.

These specifications and built-in features make the ISO113 easy to use, and provides for compact PC board layout.




*Ground if not used

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# SPECIFICATIONS

## ELECTRICAL

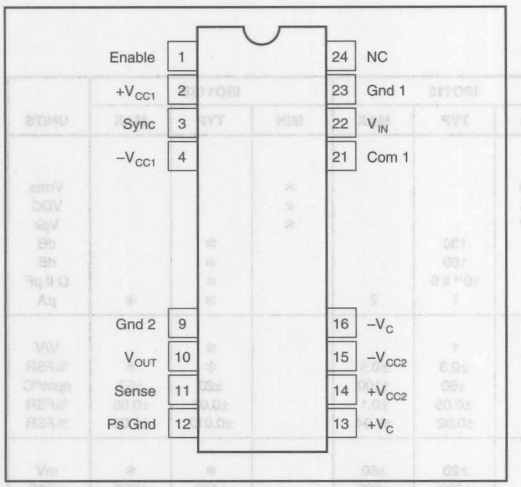
At $T_A$ = +25°C and $V_{CC1}$ = ±15V, ±15mA output, current unless otherwise noted.

| PARAMETER | CONDITIONS | ISO113 MIN | ISO113 TYP | ISO113 MAX | ISO113B MIN | ISO113B TYP | ISO113B MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **ISOLATION** | | | | | | | | |
| Rated Continuous Voltage | | | | | | | | |
| AC, 60Hz | $T_{MIN}$ to $T_{MAX}$ | 1500 | | | * | | | Vrms |
| DC | $T_{MIN}$ to $T_{MAX}$ | 2121 | | | * | | | VDC |
| Test Breakdown, 100% AC, 60Hz | 10s | 5657 | | | * | | | Vpk |
| Isolation-Mode Rejection | 1500Vrms, 60Hz | | 130 | | | * | | dB |
| | 2121VDC | | 160 | | | * | | dB |
| Barrier Impedance | | | $10^{12}$ \|\| 9 | | | * | | Ω \|\| pF |
| Leakage Current | 240Vrms, 60Hz | | 1 | 2 | | * | * | µA |
| **GAIN** | | | | | | | | |
| Nominal | | | 1 | | | * | | V/V |
| Initial Error | | | ±0.3 | ±0.5 | | * | * | %FSR |
| Gain vs Temperature | | | ±60 | ±100 | | ±20 | ±50 | ppm/°C |
| Nonlinearity | $V_O$ = –10V to 10V | | ±0.05 | ±0.1 | | ±0.03 | ±0.05 | %FSR |
| | $V_O$ = –5V to 5V | | ±0.02 | ±0.04 | | ±0.012 | ±0.02 | %FSR |
| **INPUT OFFSET VOLTAGE** | | | | | | | | |
| Initial Offset | | | ±20 | ±60 | | * | * | mV |
| vs Temperature | | | ±300 | ±500 | | ±100 | ±250 | µV/°C |
| vs Power Supplies | $V_{CC2}$ = ±10 to ±18V | | 0.9 | | | * | | mV/V |
| vs Output Supply Load | $I_O$ = 0 to ±50mA | | ±0.3 | | | * | | mV/mA |
| **SIGNAL INPUT** | | | | | | | | |
| Voltage Range | Output Voltage in Range | ±10 | ±15 | | * | * | | V |
| Resistance | | | 200 | | | * | | kΩ |
| **SIGNAL OUTPUT** | | | | | | | | |
| Voltage Range | | ±10 | ±12.5 | | * | * | | V |
| Current Drive | | ±5 | ±15 | | * | * | | mA |
| Ripple Voltage, 800kHz Carrier | | | 25 | | | * | | mVp-p |
| | 400Ω/4.7nF (See Figure 4) | | 5 | | | * | | mVp-p |
| Capacitive Load Drive | | | 1000 | | | * | | pF |
| Voltage Noise | | | 4 | | | * | | µV/√Hz |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Small Signal Bandwidth | | | 20 | | | * | | kHz |
| Slew Rate | | | 1.5 | | | * | | V/µs |
| Settling Time | 0.1%, –10/10V | | 75 | | | * | | µs |
| **POWER SUPPLIES** | | | | | | | | |
| Rated Voltage, $V_{CC1}$ | | | ±15 | | | * | | V |
| Voltage Range | | ±10 | | ±18 | * | | * | V |
| Input Current | $I_O$ = ±15mA | | +90/–4.5 | | | * | | mA |
| | $I_O$ = 0mA | | +60/–4.5 | | | * | | mA |
| Ripple Current | No Filter | | 60 | | | * | | mAp-p |
| | $C_{IN}$ = 1µF | | 3 | | | * | | mAp-p |
| Rated Output Voltage | Load = 15mA | ±14.25 | ±15 | ±15.75 | * | * | * | V |
| Output | 50mA Balanced Load | 10 | | | | * | | V |
| | 100mA Single-Ended Load | 10 | | | | * | | V |
| Load Regulation | Balanced Load | | 0.3 | | | * | | %/mA |
| Line Regulation | | | 1.12 | | | * | | V/V |
| Output Voltage vs Temperature | | | 2.5 | | | * | | mV/°C |
| Voltage Balance, ±$V_{CC2}$ | | | 0.05 | | | * | | % |
| Voltage Ripple (800kHz) | No External Capacitors | | 50 | | | * | | mVp-p |
| | $C_{EXT}$ = 1µF | | 5 | | | * | | mVp-p |
| Output Capacitive Load | | | | 1 | | | * | µF |
| Sync Frequency | Sync-Pin Grounded[2] | | 1.6 | | | * | | MHz |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –25 | | +85 | * | | * | °C |
| Operating | | –25 | | +85 | * | | * | °C |
| Storage | | –25 | | +125 | * | | * | °C |

* Specifications same as ISO113.

NOTE: (1) Conforms to UL1244 test methods. 100% tested at 1500Vrms for 1 minute. (2) If using external synchronization with a TTL-level clock, frequency should be between 1.2MHz and 2MHz with a duty-cycle greater than 25%.

## PIN CONFIGURATION




## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| ISO113 | 24-Pin DIP | 231 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Without Damage | ±18V |
| $V_{IN}$, Sense Voltage | ±50V |
| $Com_1$ to $Gnd_1$ | ±200mV |
| Enable, Sync | Gnd to +$V_{CC1}$ |
| Continuous Isolation Voltage | 1500Vrms |
| $V_{ISO}$, dv/dt | 20kV/µs |
| Junction Temperature | +150°C |
| Storage Temperature | −25°C to +125°C |
| Lead Temperature,10s | +300°C |
| Output Short to Gnd Duration | Continuous |
| ±$V_{CC2}$ to Gnd 2 Duration | Continuous |

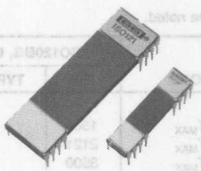
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# ISO120
# ISO121

www.burr-brown.com/databook/ISO120.html

# Precision Low Cost ISOLATION AMPLIFIER



## FEATURES

- 100% TESTED FOR PARTIAL DISCHARGE
- ISO120: Rated 1500Vrms
- ISO121: Rated 3500Vrms
- HIGH IMR: 115dB at 60Hz
- USER CONTROL OF CARRIER FREQUENCY
- LOW NONLINEARITY: ±0.01% max
- BIPOLAR OPERATION: $V_O$ = ±10V
- 0.3"-WIDE 24-PIN HERMETIC DIP, ISO120
- SYNCHRONIZATION CAPABILITY
- WIDE TEMP RANGE: –55°C to +125°C (ISO120)

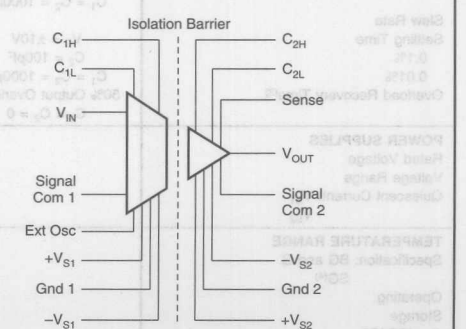
## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL: Transducer Isolator for Thermocouples, RTDs, Pressure Bridges, and Flow Meters, 4mA to 20mA Loop Isolation
- GROUND LOOP ELIMINATION
- MOTOR AND SCR CONTROL
- POWER MONITORING
- ANALYTICAL MEASUREMENTS
- BIOMEDICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT

## DESCRIPTION

The ISO120 and ISO121 are precision isolation amplifiers incorporating a novel duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2pF differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity, which results in excellent reliability and good high frequency transient immunity across the barrier. Both the amplifier and barrier capacitors are housed in a hermetic DIP. The ISO120 and ISO121 differ only in package size and isolation voltage rating.

These amplifiers are easy to use. No external components are required for 60kHz bandwidth. With the addition of two external capacitors, precision specifications of 0.01% max nonlinearity and 150µV/°C max $V_{OS}$ drift are guaranteed with 6kHz bandwidth. A power supply range of ±4.5V to ±18V and low quiescent current make these amplifiers ideal for a wide range of applications.




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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C: $V_{S1}$ = $V_{S2}$ = ±15V: and $R_L$ = 2kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | ISO120BG, ISO121BG | | | ISO120G, ISO120SG[4], ISO121G | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ISOLATION** | | | | | | | | |
| Voltage Rated Continuous ISO120: AC 60Hz | $T_{MIN}$ to $T_{MAX}$ | 1500 | | | * | | | Vrms |
| DC | $T_{MIN}$ to $T_{MAX}$ | 2121 | | | * | | | VDC |
| ISO121: AC 60Hz | $T_{MIN}$ to $T_{MAX}$ | 3500 | | | * | | | Vrms |
| DC | $T_{MIN}$ to $T_{MAX}$ | 4950 | | | * | | | VDC |
| 100% Test (AC 60Hz): ISO120 | 1s; Partial Discharge ≤ 5pC | 2500 | | | * | | | Vrms |
| ISO121 | 1s; Partial Discharge ≤ 5pC | 5600 | | | * | | | Vrms |
| Isolation Mode Rejection ISO 120: AC 60Hz | 1500Vrms | | 115 | | | * | | dB |
| DC | | | 160 | | | * | | dB |
| ISO121: AC60Hz | 3500Vrms | | 115 | | | * | | dB |
| DC | | | 160 | | | * | | dB |
| Barrier Impedance | | | $10^{14}$ ‖ 2 | | | * | | Ω ‖ pF |
| Leakage Current | $V_{ISO}$ = 240Vrms, 60Hz | | 0.18 | 0.5 | | * | * | μArms |
| **GAIN[4]** | $V_O$ = ±10V | | | | | | | |
| Nominal Gain | $C_1$ = $C_2$ = 1000pF | | 1 | | | 1 | | V/V |
| Gain Error | | | ±0.04 | ±0.1 | | ±0.05 | ±0.25 | %FSR |
| Gain vs Temperature | | | ±5 | ±20 | | ±10 | ±40 | ppm/°C |
| Nonlinearity | | | ±0.005 | ±0.01 | | ±0.01 | ±0.05 | %FSR |
| Nominal Gain | $C_1$ = $C_2$ = 0 | | 1 | | | 1 | | V/V |
| Gain Error | | | ±0.04 | ±0.25 | | ±0.05 | ±0.25 | %FSR |
| Gain vs Temperature | | | ±40 | | | ±40 | | ppm/°C |
| Nonlinearity | | | ±0.02 | ±0.1 | | ±0.04 | ±0.1 | %FSR |
| **INPUT OFFSET VOLTAGE[4]** | | | | | | | | |
| Initial Offset | $C_1$ = $C_2$ = 1000pF | | ±5 | ±25 | | ±10 | ±50 | mV |
| vs Temperature | | | ±100 | ±150 | | ±150 | ±400 | μV/°C |
| Initial Offset | $C_1$ = $C_2$ = 0 | | ±25 | ±100 | | ±40 | ±100 | mV |
| vs Temperature | | | ±250 | | | ±500 | | μV/°C |
| Initial Offset | | | | | | | | |
| vs Supply | $\pm V_{S1}$ or $\pm V_{S2}$ = ±4.5V to ±18V | | ±2 | | | ±2 | | mV/V |
| Noise | | | 4 | | | 4 | | $\mu V/\sqrt{Hz}$ |
| **INPUT** | | | | | | | | |
| Voltage Range[1] | | ±10 | ±15 | | * | * | | V |
| Resistance | | | 200 | | | * | | kΩ |
| **OUTPUT** | | | | | | | | |
| Voltage Range | | ±10 | ±12.5 | | * | * | | V |
| Current Drive | | ±5 | ±15 | | * | * | | mA |
| Capacitive Load Drive | | | 0.1 | | | * | | μF |
| Ripple Voltage[2] | | | 10 | | | * | | mVp-p |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Small Signal Bandwith | $C_1$ = $C_2$ = 0 | | 60 | | | * | | kHz |
| | $C_1$ = $C_2$ = 1000pF | | 6 | | | * | | kHz |
| Slew Rate | | | 2 | | | * | | V/μs |
| Settling Time | $V_O$ = ±10V | | | | | | | |
| 0.1% | $C_2$ = 100pF | | 50 | | | * | | μs |
| 0.01% | $C_1$ = $C_2$ = 1000pF | | 350 | | | * | | μs |
| Overload Recovery Time[3] | 50% Output Overload, $C_1$ = $C_2$ = 0 | | 150 | | | * | | μs |
| **POWER SUPPLIES** | | | | | | | | |
| Rated Voltage | | | 15 | | | * | | V |
| Voltage Range | | ±4.5 | ±18 | | * | * | | V |
| Quiescent Current: $V_{S1}$ | | | ±4.0 | ±5.5 | | * | * | mA |
| $V_{S2}$ | | | ±5.0 | ±6.5 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: BG and G | | –25 | | 85 | –25 | | 85 | °C |
| SG[4] | | –25 | | 85 | –55 | | 125 | °C |
| Operating | | –55 | | 125 | –55 | | 125 | °C |
| Storage | | –65 | | 150 | –55 | | 150 | °C |
| $\theta_{JA}$: ISO120 | | | 40 | | | 40 | | °C/W |
| ISO121 | | | 25 | | | 25 | | °C/W |

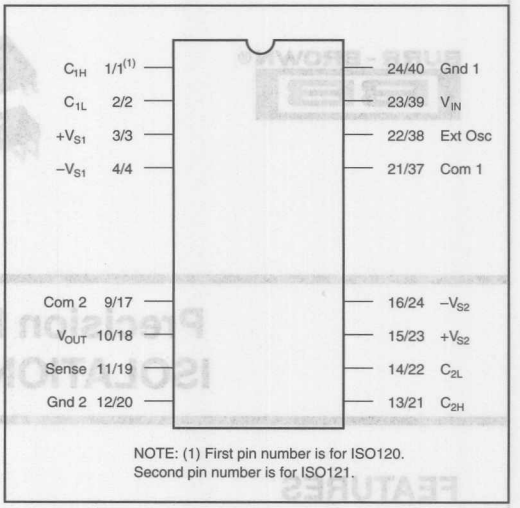
* Specification same as ISO120BG, ISO121BG.

NOTE: (1) Input voltage range = ±10V for $V_{S1}$, $V_{S2}$ = ±4.5VDC to ±18VDC. (2) Ripple frequency is at carrier frequency. (3) Overload recovery is approximately three times the settling time for other values of $C_2$. (4) The SG-grade is specified –55°C to +125°C; performance of the SG in the –25°C to +85°C temperature range is the same as the BG-grade.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage (any supply) | 18V |
| $V_{IN}$, Sense Voltage | ±100V |
| External Oscillator Input | ±25V |
| Signal Common 1 to Ground 1 | ±1V |
| Signal Common 2 to Ground 2 | ±1V |
| Continuous Isolation Voltage: ISO120 | 1500Vrms |
| ISO121 | 3500Vrms |
| $V_{ISO}$, dv/dt | 20kV/µs |
| Junction Temperature | 150°C |
| Storage Temperature | –65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short Duration | Continuous to Common |

## CONNECTION DIAGRAM




NOTE: (1) First pin number is for ISO120. Second pin number is for ISO121.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ISO120G | 24-Pin DIP | 225 | –25°C to 85°C |
| ISO120BG | 24-Pin DIP | 225 | –25°C to 85°C |
| ISO120SG | 24-Pin DIP | 225 | –55C to 125°C |
| ISO121G | 40-Pin DIP | 206 | –25°C to 85°C |
| ISO121BG | 40-Pin DIP | 206 | –25°C to 85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



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# ISO122

www.burr-brown.com/databook/ISO122.html

# Precision Lowest Cost ISOLATION AMPLIFIER

## FEATURES

- 100% TESTED FOR HIGH-VOLTAGE BREAKDOWN
- RATED 1500Vrms
- HIGH IMR: 140dB at 60Hz
- BIPOLAR OPERATION: $V_O = \pm 10V$
- 16-PIN PLASTIC DIP AND 28-LEAD SOIC
- EASE OF USE: Fixed Unity Gain Configuration
- 0.020% max NONLINEARITY
- ±4.5V to ±18V SUPPLY RANGE

## APPLICATIONS

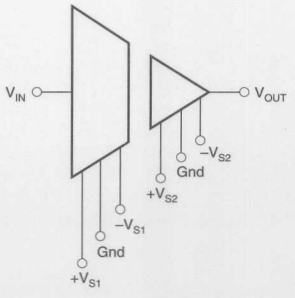
- INDUSTRIAL PROCESS CONTROL: Transducer Isolator, Isolator for Thermocouples, RTDs, Pressure Bridges, and Flow Meters, 4mA to 20mA Loop Isolation
- GROUND LOOP ELIMINATION
- MOTOR AND SCR CONTROL
- POWER MONITORING
- PC-BASED DATA ACQUISITION
- TEST EQUIPMENT

## DESCRIPTION

The ISO122 is a precision isolation amplifier incorporating a novel duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2pF differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity, resulting in excellent reliability and good high frequency transient immunity across the barrier. Both barrier capacitors are imbedded in the plastic body of the package.

The ISO122 is easy to use. No external components are required for operation. The key specifications are 0.020% max nonlinearity, 50kHz signal bandwidth, and 200µV/°C $V_{OS}$ drift. A power supply range of ±4.5V to ±18V and quiescent currents of ±5.0mA on $V_{S1}$ and ±5.5mA on $V_{S2}$ make these amplifiers ideal for a wide range of applications.

The ISO122 is available in 16-pin plastic DIP and 28-lead plastic surface mount packages.




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# SPECIFICATIONS

At $T_A$ = +25°C , $V_{S1}$ = $V_{S2}$ = ±15V, and $R_L$ = 2kΩ, unless otherwise noted.

| | | ISO122P, U | | | ISO122JP, JU | | | |
|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **CONDITIONS** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **ISOLATION** | | | | | | | | |
| Voltage Rated Continuous AC 60Hz | | 1500 | | | * | | | VAC |
| 100% Test (1) | 1s, 5pc PD | 2400 | | | * | | | VAC |
| Isolation Mode Rejection | 60Hz | | 140 | | | * | | dB |
| Barrier Impedance | | | $10^{14}$ \|\| 2 | | | * | | Ω \|\| pF |
| Leakage Current at 60Hz | $V_{ISO}$ = 240Vrms | | 0.18 | 0.5 | | * | * | µArms |
| **GAIN** | $V_O$ = ±10V | | | | | | | |
| Nominal Gain | | | 1 | | | * | | V/V |
| Gain Error | | | ±0.05 | ±0.50 | | * | * | %FSR |
| Gain vs Temperature | | | ±10 | | | * | | ppm/°C |
| Nonlinearity(2) | | | ±0.016 | ±0.020 | | ±0.025 | ±0.050 | %FSR |
| **INPUT OFFSET VOLTAGE** | | | | | | | | |
| Initial Offset | | | ±20 | ±50 | | * | * | mV |
| vs Temperature | | | ±200 | | | * | | µV/°C |
| vs Supply | | | ±2 | | | * | | mV/V |
| Noise | | | 4 | | | * | | µV/√Hz |
| **INPUT** | | | | | | | | |
| Voltage Range | | ±10 | ±12.5 | | * | * | | V |
| Resistance | | | 200 | | | * | | kΩ |
| **OUTPUT** | | | | | | | | |
| Voltage Range | | ±10 | ±12.5 | | * | * | | V |
| Current Drive | | ±5 | ±15 | | * | * | | mA |
| Capacitive Load Drive | | | 0.1 | | | * | | µF |
| Ripple Voltage(3) | | | 20 | | | * | | mVp-p |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Small Signal Bandwidth | | | 50 | | | * | | kHz |
| Slew Rate | | | 2 | | | * | | V/µs |
| Settling Time | $V_O$ = ±10V | | | | | | | |
| 0.1% | | | 50 | | | * | | µs |
| 0.01% | | | 350 | | | * | | µs |
| Overload Recover Time | | | 150 | | | * | | µs |
| **POWER SUPPLIES** | | | | | | | | |
| Rated Voltage | | | ±15 | | | * | | V |
| Voltage Range | | ±4.5 | | ±18 | * | | * | V |
| Quiescent Current: $V_{S1}$ | | | ±5.0 | ±7.0 | | * | * | mA |
| $V_{S2}$ | | | ±5.5 | ±7.0 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –25 | | +85 | * | | * | °C |
| Operating | | –25 | | +85 | * | | * | °C |
| Storage | | –40 | | +85 | * | | * | °C |
| $\theta_{JA}$ | | | 100 | | | * | | °C/W |
| $\theta_{JC}$ | | | 65 | | | * | | °C/W |

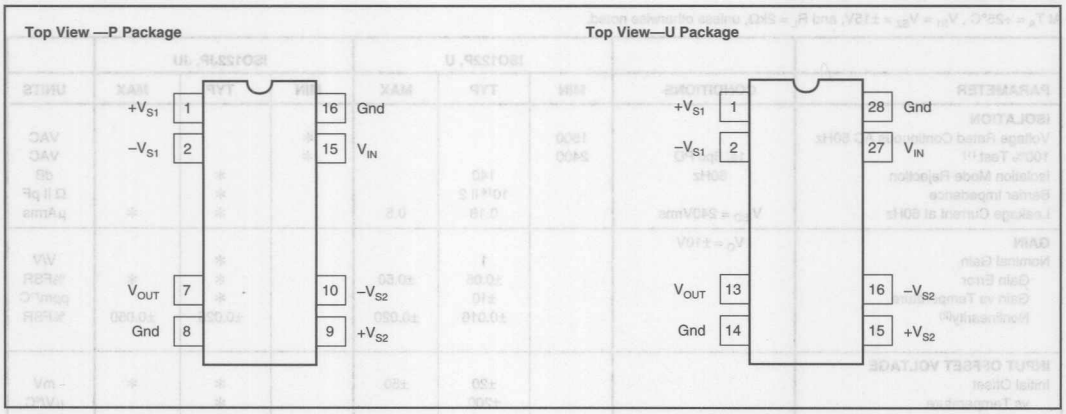
* Specification same as ISO122P, U.

NOTES: (1) Tested at 1.6 X rated, fail on 5pC partial discharge. (2) Nonlinearity is the peak deviation of the output voltage from the best-fit straight line. It is expressed as the ratio of deviation to FSR. (3) Ripple frequency is at carrier frequency (500kHz).



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## CONNECTION DIAGRAM




## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ISO122P | 16-Pin Plastic DIP | 238 |
| ISO122JP | 16-Pin Plastic DIP | 238 |
| ISO122U | 28-Pin Plastic SOIC | 217-1 |
| ISO122JU | 28-Pin Plastic SOIC | 217-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| $V_{IN}$ | ±100V |
| Continuous Isolation Voltage | 1500Vrms |
| Junction Temperature | +150°C |
| Storage Temperature | +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short to Common | Continuous |

## ORDERING INFORMATION

| PRODUCT | PACKAGE | NONLINEARITY MAX %FSR |
|---|---|---|
| ISO122P | Plastic DIP | ±0.020 |
| ISO122JP | Plastic DIP | ±0.050 |
| ISO122U | Plastic SOIC | ±0.020 |
| ISO122JU | Plastic SOIC | ±0.050 |

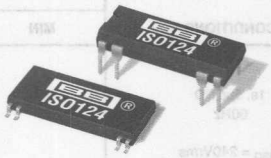
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# ISO124




www.burr-brown.com/databook/ISO124.html

# Precision Lowest Cost ISOLATION AMPLIFIER



## FEATURES

- 100% TESTED FOR HIGH-VOLTAGE BREAKDOWN
- RATED 1500Vrms
- HIGH IMR: 140dB at 60Hz
- 0.010% max NONLINEARITY
- BIPOLAR OPERATION: $V_O = \pm 10V$
- 16-PIN PLASTIC DIP AND 28-LEAD SOIC
- EASE OF USE: Fixed Unity Gain Configuration
- ±4.5V to ±18V SUPPLY RANGE

## APPLICATIONS

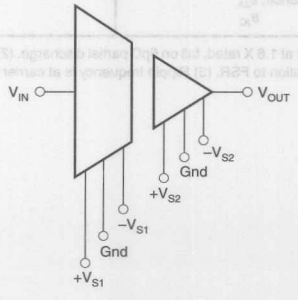
- INDUSTRIAL PROCESS CONTROL: Transducer Isolator, Isolator for Thermocouples, RTDs, Pressure Bridges, and Flow Meters, 4mA to 20mA Loop Isolation
- GROUND LOOP ELIMINATION
- MOTOR AND SCR CONTROL
- POWER MONITORING
- PC-BASED DATA ACQUISITION
- TEST EQUIPMENT

## DESCRIPTION

The ISO124 is a precision isolation amplifier incorporating a novel duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2pF differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity, resulting in excellent reliability and good high frequency transient immunity across the barrier. Both barrier capacitors are imbedded in the plastic body of the package.

The ISO124 is easy to use. No external components are required for operation. The key specifications are 0.010% max nonlinearity, 50kHz signal bandwidth, and 200µV/°C $V_{OS}$ drift. A power supply range of ±4.5V to ±18V and quiescent currents of ±5.0mA on $V_{S1}$ and ±5.5mA on $V_{S2}$ make these amplifiers ideal for a wide range of applications.

The ISO124 is available in 16-pin plastic DIP and 28-lead plastic surface mount packages.




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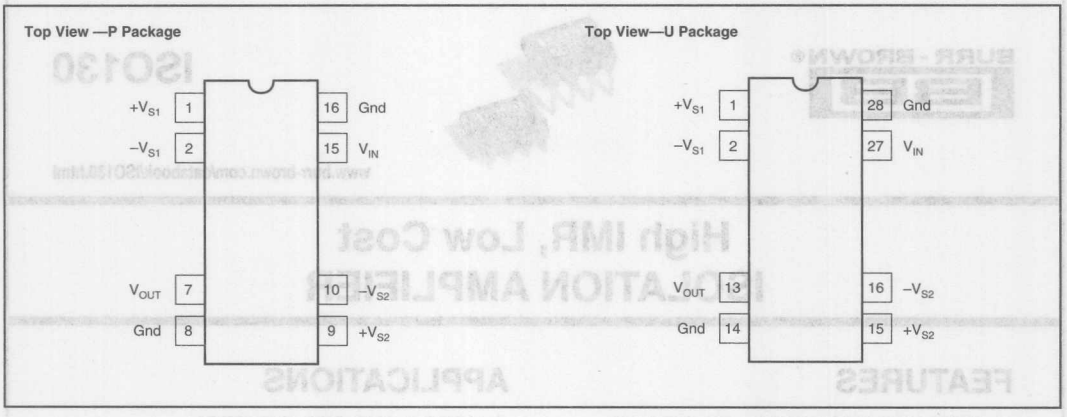
At $T_A$ = +25°C, $V_{S1} = V_{S2} = \pm 15V$, and $R_L = 2k\Omega$, unless otherwise noted.

| PARAMETER | CONDITIONS | ISO124P, U MIN | ISO124P, U TYP | ISO124P, U MAX | UNITS |
|---|---|---|---|---|---|
| **ISOLATION** | | | | | |
| Rated Voltage, continuous ac 60Hz | | 1500 | | | Vac |
| 100% Test (1) | 1s, 5pc PD | 2400 | | | Vac |
| Isolation Mode Rejection | 60Hz | | 140 | | dB |
| Barrier Impedance | | | $10^{14} \| 2$ | | Ω \| pF |
| Leakage Current at 60Hz | $V_{ISO}$ = 240Vrms | | 0.18 | 0.5 | µArms |
| **GAIN** | $V_O = \pm 10V$ | | | | |
| Nominal Gain | | | 1 | | V/V |
| Gain Error | | | ±0.05 | ±0.50 | %FSR |
| Gain vs Temperature | | | ±10 | | ppm/°C |
| Nonlinearity(2) | | | ±0.005 | ±0.010 | %FSR |
| **INPUT OFFSET VOLTAGE** | | | | | |
| Initial Offset | | | ±20 | ±50 | mV |
| vs Temperature | | | ±200 | | µV/°C |
| vs Supply | | | ±2 | | mV/V |
| Noise | | | 4 | | µV/√Hz |
| **INPUT** | | | | | |
| Voltage Range | | ±10 | ±12.5 | | V |
| Resistance | | | 200 | | kΩ |
| **OUTPUT** | | | | | |
| Voltage Range | | ±10 | ±12.5 | | V |
| Current Drive | | ±5 | ±15 | | mA |
| Capacitive Load Drive | | | 0.1 | | µF |
| Ripple Voltage(3) | | | 20 | | mVp-p |
| **FREQUENCY RESPONSE** | | | | | |
| Small Signal Bandwidth | | | 50 | | kHz |
| Slew Rate | | | 2 | | V/µs |
| Settling Time | $V_O = \pm 10V$ | | | | |
| 0.1% | | | 50 | | µs |
| 0.01% | | | 350 | | µs |
| Overload Recovery Time | | | 150 | | µs |
| **POWER SUPPLIES** | | | | | |
| Rated Voltage | | | ±15 | | V |
| Voltage Range | | ±4.5 | | ±18 | V |
| Quiescent Current: $V_{S1}$ | | | ±5.0 | ±7.0 | mA |
| $V_{S2}$ | | | ±5.5 | ±7.0 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –25 | | +85 | °C |
| Operating | | –25 | | +85 | °C |
| Storage | | –40 | | +85 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | 100 | | °C/W |
| $\theta_{JC}$ | | | 65 | | °C/W |

NOTES: (1) Tested at 1.6 X rated, fail on 5pC partial discharge. (2) Nonlinearity is the peak deviation of the output voltage from the best-fit straight line. It is expressed as the ratio of deviation to FSR. (3) Ripple frequency is at carrier frequency (500kHz).

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## CONNECTION DIAGRAM




## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| ISO124P | 16-Pin Plastic DIP | 238 |
| ISO124U | 28-Lead Plastic SOIC | 217-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

| PRODUCT | PACKAGE | NONLINEARITY MAX %FSR |
|---|---|---|
| ISO124P | 16-Pin Plastic DIP | ±0.010 |
| ISO124U | 28-Lead Plastic SOIC | ±0.010 |

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Supply Voltage | ±18V |
| $V_{IN}$ | ±100V |
| Continuous Isolation Voltage | 1500Vrms |
| Junction Temperature | +150°C |
| Storage Temperature | +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short to Common | Continuous |

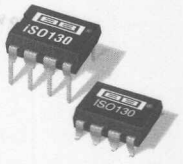
NOTE: (1) Stresses above these ratings may cause permanent damage.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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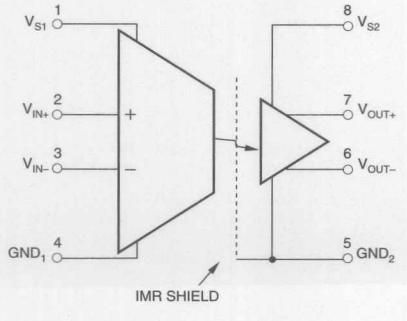
# ISO130

www.burr-brown.com/databook/ISO130.html

# High IMR, Low Cost ISOLATION AMPLIFIER

## FEATURES

- HIGH ISOLATION-MODE REJECTION: 10kV/μs (min)
- LARGE SIGNAL BANDWIDTH: 85kHz (typ)
- DIFFERENTIAL INPUT/DIFFERENTIAL OUTPUT
- VOLTAGE OFFSET DRIFT vs TEMPERATURE: 4.6μV/°C (typ)
- OFFSET VOLTAGE 1.8mV (max)
- INPUT REFERRED NOISE: 300μVrms (typ)
- NONLINEARITY: 0.25% (max)
- SINGLE SUPPLY OPERATION
- SIGMA-DELTA A/D CONVERTER TECHNOLOGY
- WORLDWIDE SAFETY APPROVAL: UL1577 (File No. E162573), VDE0884 (File No. 85511), CSA22.2 (File No. 88324)
- AVAILABLE IN 8-PIN PLASTIC DIP and 8-PIN GULL-WING PLASTIC SURFACE MOUNT




## APPLICATIONS

- MOTOR AND SCR CONTROL
- MOTOR PHASE CURRENT SENSING
- INDUSTRIAL PROCESS CONTROL: Transducer Isolator, Isolator for Thermocouples, RTDs
- GENERAL PURPOSE ANALOG SIGNAL ISOLATION
- POWER MONITORING
- GROUND LOOP ELIMINATION

## DESCRIPTION

The ISO130 is a high isolation-mode rejection, isolation amplifier suited for motor control applications. Its versatile design provides the precision and stability needed to accurately monitor motor currents in high-noise motor control environments. The ISO130 can also be used for general analog signal isolation applications requiring stability and linearity under severe noise conditions.

The signal is transmitted digitally across the isolation barrier optically, using a high-speed AlGaAs LED. The remainder of the ISO130 is fabricated on 1μm CMOS IC process. A sigma-delta analog-to-digital converter, chopper stabilized amplifiers and differential input and output topologies make the isolation amplifier suitable for a variety of applications.

The ISO130 is easy to use. No external components are required for operation. The key specifications are 10kV/μs isolation-mode rejection, 85kHz large signal bandwidth, and 4.6μV/°C $V_{OS}$ drift. A single power supply ranging from +4.5V to +5.5V makes this amplifier ideal for low power isolation applications.

The ISO130 is available in 8-pin plastic DIP and 8-pin plastic gull-wing surface mount packages.

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# SPECIFICATIONS

## ISOLATION SPECIFICATIONS – VDE0884 INSULATION CHARACTERISTICS

At $V_{IN}-$, $V_{IN}-$ = 0V, $T_A$ = 25°C, $V_{S1}$, $V_{S2}$ = 5.0V, unless otherwise noted.

| PARAMETER | CONDITIONS | ISO130P, ISO130PB ISO130U, ISO130UB CHARACTERISTIC | UNITS |
|---|---|---|---|
| **ISOLATION CHARACTERISTICS** | | | |
| Installation Classification | As Per VDE0109/12.83 | | |
| Table I | | | |
| Rated Mains Voltage ≤ 300Vrms | | I-IV | |
| Rated Mains Voltage ≤ 600Vrms | | I-III | |
| Climatic Classification | | 40/85/21 | |
| Pollution Degree(1) | As Per VDE0109/12.83 | 2 | |
| Maximum Working Insulation Voltage ($V_{IORM}$) | | 600 | Vrms |
| Side A to Side B Test Voltage, Method b ($V_{PR}$)(9) | | | |
| Partial Discharge < 5pC | $V_{PR}$ = 1.6 x $V_{IORM}$, $t_P$ = 1s | 960 | Vrms |
| Side A to Side B Test Voltage, Method a ($V_{PR}$)(9) | Type and Sample Test | | |
| Partial Discharge < 5pC | $V_{PR}$ = 1.2 x $V_{IORM}$, $t_P$ = 60s | 720 | Vrms |
| Highest Allowable Overvoltage ($V_{TR}$)(9) | Transient Overvoltage, $t_{TR}$ = 10s | 6000 | $V_{PEAK}$ |
| Safety-Limiting Values | | | |
| Case Temperature ($T_{SI}$) | | 175 | °C |
| Input Power ($P_{SI\ (INPUT)}$) | | 80 | mW |
| Output Power ($P_{SI\ (OUTPUT)}$) | | 250 | mW |
| **INSULATION RELATED SPECIFICATIONS** | | | |
| Min. External Air Gap (clearance) | | > 7 | mm |
| Min. External Tracking Path (creepage) | | 8 | mm |
| Internal Isolation Gap (clearance) | | 0.5 | mm |
| Tracking Resistance (CTI) | | 175 | V |
| Isolation Group | per VDE0109 | III a | |
| Insulation Resistance | 25°C, $V_{ISO}$ = 500V | ≥ $10^{11}$ | Ω |

# SPECIFICATIONS

## ISOLATION SPECIFICATIONS

At $V_{IN}+$, $V_{IN}-$ = 0V, $T_A$ = 25°C, $V_{S1}$, $V_{S2}$ = 5.0V, unless otherwise noted.

| PARAMETER | CONDITIONS | ISO130P, ISO130PB ISO130U, ISO130UP MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **ISOLATION** | | | | | |
| Input-Output Surge Withstand Voltage(8, 9), (In accordance with UL1577) | t = $1_{MIN}$, RH ≤ 50% | 3750 | | | Vrms |
| Barrier Impedance(9) | | | | | |
| Resistance | $V_{ISO}$ = 500VDC | | $10^{13}$ | | Ω |
| Capacitance | f = 1MHz | | 0.7 | | pF |
| Isolation Mode Voltage Errors | | | | | |
| Rising Edge Transient Immunity | $V_{IM}$ = 1kV, ∂ $V_{OUT}$ < 50mV | 10 | 25 | | kV/µs |
| Falling Edge Transient Immunity | $V_{IM}$ = 1kV, ∂ $V_{OUT}$ < 50mV | 10 | 15 | | kV/µs |
| Isolation Mode Rejection Ratio(2) | | | > 140 | | dB |

# SPECIFICATIONS

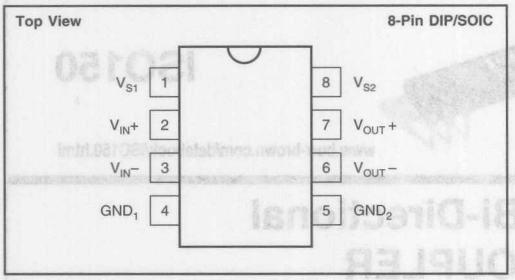
At $V_{IN}+$, $V_{IN}-$ = 0V, $T_A$ = 25°C, $V_{S1}$, $V_{S2}$ = 5.0V, unless otherwise noted.

| PARAMETER | CONDITIONS | ISO130P, ISO130PB ISO130U, ISO130UB MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT** | | | | | |
| Initial Offset Voltage | | –1.8 | –0.9 | 0.0 | mV |
| vs Temperature | | | 4.6 | | µV/°C |
| vs $V_{S1}$ | | | 30 | | µV/V |
| vs $V_{S2}$ | | | –40 | | µV/V |
| Power Supply Rejection; $V_{S1}$ and $V_{S2}$ Together | 1MHz Square Wave, 5ns Rise/Fall Time | | 5 | | mV/V |
| Noise | 0.1Hz to 100kHz | | 300 | | µVrms |
| Input Voltage Range | | –200 | | 200 | mV |
| Maximum Input Voltage Range before Output Clipping | | | ±300 | | mV |
| Initial Input Bias Current[3] | | | –670 | | nA |
| vs Temperature | | | 3 | | nA/°C |
| Input Resistance[3] | | | 530 | | kΩ |
| vs Temperature | | | 0.38 | | %/°C |
| Common-Mode Rejection Ratio[4] | | | 72 | | dB |
| **GAIN[5]** | | | | | |
| Initial Gain | | | | | |
| ISO130P/ISO130U | –200mV < $V_{IN}+$ < 200mV | 7.61 | 8.00 | 8.40 | V/V |
| ISO130PB/ISO130UB | –200mV < $V_{IN}+$ < 200mV | 7.85 | 7.93 | 8.01 | V/V |
| Gain vs Temperature | | | 10 | | ppm/°C |
| Gain vs $V_{S1}$ | | | 2.1 | | ppm/mV |
| Gain vs $V_{S2}$ | | | –0.6 | | ppm/mV |
| Gain Nonlinearity | | | | | |
| for –200mV < $V_{IN}+$ < 200mV | | | 0.2 | 0.35 | % |
| for –100mV < $V_{IN}+$ < 100mV | | | 0.1 | 0.25 | % |
| vs Temperature[6] | –200mV < $V_{IN}+$ < 200mV | | –0.001 | | % pts/°C |
| vs $V_{S1}$[6] | –200mV < $V_{IN}+$ < 200mV | | –0.005 | | % pts/V |
| vs $V_{S2}$[6] | –200mV < $V_{IN}+$ < 200mV | | –0.007 | | % pts/V |
| **OUTPUT** | | | | | |
| Voltage Range | | | | | |
| High | $V_{IN}+$ = +500mV | | 3.61 | | V |
| Low | $V_{IN}+$ = –500mV | | 1.18 | | V |
| Common-Mode Voltage | –40°C < $T_A$ < 85°C, 4.5V < $V_{S1}$ < 5.5V | 2.2 | 2.39 | 2.6 | V |
| Current Drive[7] | | | 1 | | mA |
| Short-Circuit Current | $V_{OUT}$ = 0V or $V_{OUT}$ = $V_{S2}$ | | 9.3 | | mA |
| Output Resistance | | | 11 | | Ω |
| vs Temperature | | | 0.6 | | %/°C |
| **FREQUENCY RESPONSE** | | | | | |
| Bandwidth | | | | | |
| –3dB | –40°C to 85°C | 50 | 85 | | kHz |
| –45° | | | 35 | | kHz |
| Rise/Fall Time (10% - 90%) | –40°C to 85°C | | 4.3 | 6.6 | µs |
| Propagation Delay | | | | | |
| to 10% | –40°C to 85°C | | 2.0 | 3.3 | µs |
| to 50% | –40°C to 85°C | | 3.4 | 5.6 | µs |
| to 90% | –40°C to 85°C | | 6.3 | 9.9 | µs |
| **POWER SUPPLIES** | | | | | |
| Rated Voltage | | | 5.0 | | V |
| Voltage Range | | 4.5 | | 5.5 | V |
| Quiescent Current | | | | | |
| $V_{S1}$ | $V_{IN}+$ = 200mV, –40°C < $T_A$ < 85°C, 4.5V < $V_{S1}$ < 5.5V | | 10.7 | 15.5 | mA |
| $V_{S2}$ | –40°C < $T_A$ < 85°C, 4.5V < $V_{S1}$ < 5.5V | | 11.6 | 15.5 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –40 | | 85 | °C |
| Operating | | –40 | | 100 | °C |
| Storage | | –55 | | 125 | °C |
| $\theta_{C-A}$ | | | 86 | | °C/W |

NOTES: (1) This part may also be used in Pollution Degree 3 environments where the rated mains voltage is 300Vrms (per DIN VDE0109/12.83). (2) IMRR = 20 log ($\partial V_{IN}/\partial V_{ISO}$). (3) Time averaged value. (4) $V_{IN}+$ = $V_{IN}-$ = $V_{CM}$. CMRR = 20 log ($\partial V_{CM}/\partial V_{OS}$). (5) The slope of the best-fit line of ($V_{OUT+}$ – $V_{OUT-}$) vs ($V_{IN+}$ – $V_{IN-}$). (6) Change in nonlinearity vs temperature or supply voltage expressed in number of percentage points per °C or volt. (7) For best offset voltage performance. (8) For devices with minimum $V_{ISO}$ specified at 3750Vrms, each isolation amplifier is proof-tested by applying an insulation test voltage ≥ *4500Vrms for 1 second* (leakage current < 5µA). This specification does not guarantee continuous operation. (9) Pins 1-4 are shorted together and pins 5-8 are shorted together for this test.

## PIN CONFIGURATION

Top View — 8-Pin DIP/SOIC




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltages: $V_{S1}$, $V_{S2}$ | 0V to 5.5V |
| Steady-State Input Voltage | –2V to $V_{S1}$ + 0.5V |
| 2 Second Transient Input Voltage | –6.0V |
| Output Voltages: $V_{OUT}+$, $V_{OUT}-$ | –0.5V to $V_{S2}$ + 0.5V |
| Lead Temperature Solder (1.6mm below seating plane, 10s) | 260°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| ISO130P | 8-Pin Plastic DIP | 006-3 |
| ISO130PB | 8-Pin Plastic DIP | 006-3 |
| ISO130U | 8-Pin Gull-Wing Plastic Surface Mount | 006-2 |
| ISO130UB | 8-Pin Gull-Wing Plastic Surface Mount | 006-2 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

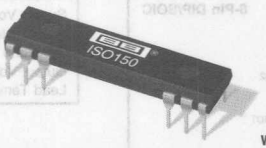
## ORDERING INFORMATION

| PRODUCT | PACKAGE | GAIN ERROR (MAX) |
|---|---|---|
| ISO130P | 8-Pin Plastic DIP | ±5% (mean value = 8.00) |
| ISO130PB | 8-Pin Plastic DIP | ±1% (mean value = 7.93) |
| ISO130U | 8-Pin Gull-Wing Plastic Surface Mount | ±5% (mean value = 8.00) |
| ISO130UB | 8-Pin Gull-Wing Plastic Surface Mount | ±1% (mean value = 7.93) |



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**ISO150**

www.burr-brown.com/databook/ISO150.html

# Dual, Isolated, Bi-Directional DIGITAL COUPLER

## FEATURES

- REPLACES HIGH-PERFORMANCE OPTOCOUPLERS
- DATA RATE: 80M Baud, typ
- LOW POWER CONSUMPTION: 25mW Per Channel, max
- TWO CHANNELS, EACH BI-DIRECTIONAL, PROGRAMMABLE BY USER
- PARTIAL DISCHARGE TESTED: 2400Vrms
- CREEPAGE DISTANCE OF 16.5mm (DIP)
- LOW COST PER CHANNEL
- PLASTIC DIP AND SOIC PACKAGES

## APPLICATIONS

- DIGITAL ISOLATION FOR A/D, D/A CONVERSION
- ISOLATED UART INTERFACE
- MULTIPLEXED DATA TRANSMISSION
- ISOLATED PARALLEL TO SERIAL INTERFACE
- TEST EQUIPMENT
- MICROPROCESSOR SYSTEM INTERFACE
- ISOLATED LINE RECEIVER
- GROUND LOOP ELIMINATION

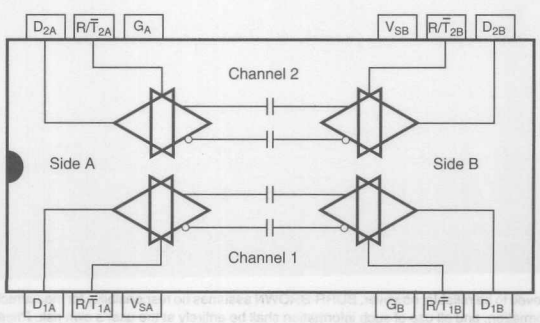
## DESCRIPTION

The ISO150 is a two-channel, galvanically isolated data coupler capable of data rates of 80MBaud, typical. Each channel can be individually programmed to transmit data in either direction.

Data is transmitted across the isolation barrier by coupling complementary pulses through high voltage 0.4pF capacitors. Receiver circuitry restores the pulses to standard logic levels. Differential signal transmission rejects isolation-mode voltage transients up to 1.6kV/µs.

ISO150 avoids the problems commonly associated with optocouplers. Optically isolated couplers require high current pulses and allowance must be made for LED aging. The ISO150's Bi-CMOS circuitry operates at 25mW per channel.

ISO150 is available in a 24-pin DIP package and in a 28-lead SOIC. Both are specified for operation from –40°C to 85°C.




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# SPECIFICATIONS

At $T_A$ = +25°C and $V_S$ = +5V, unless otherwise noted.

| PARAMETER | CONDITION | ISO150AP, AU MIN | ISO150AP, AU TYP | ISO150AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **ISOLATION PARAMETERS** | | | | | |
| Rated Voltage, Continuous | 60Hz | 1500 | | | Vrms |
| Partial Discharge, 100% Test[1] | 1s, 5pC | 2400 | | | Vrms |
| Creepage Distance (External) | | | | | |
| DIP—"P" Package | | | 16 | | mm |
| SOIC—"U" Package | | | 7.2 | | mm |
| Internal Isolation Distance | | | 0.10 | | mm |
| Isolation Voltage Transient Immunity[2] | | | 1.6 | | kV/µs |
| Barrier Impedance | | | $>10^{14}$ \|\| 7 | | Ω \|\| pF |
| Leakage Current | 240Vrms, 60Hz | | 0.6 | | µArms |
| **DC PARAMETERS** | | | | | |
| Logic Output Voltage, High, $V_{OH}$ | $I_{OH}$ = 6mA | $V_S$–1 | | $V_S$ | V |
| Low, $V_{OL}$ | $I_{OL}$ = 6mA | 0 | | 0.4 | V |
| Logic Output Short-Circuit Current | Source or Sink | | 30 | | mA |
| Logic Input Voltage, High[3] | | 2 | | $V_S$ | V |
| Low[3] | | 0 | | 0.8 | V |
| Logic Input Capacitance | | | 5 | | pF |
| Logic Input Current | | | <1 | | nA |
| Power Supply Voltage Range[3] | | 3 | 5 | 5.5 | V |
| Power Supply Current[4] | | | | | |
| Transmit Mode | DC | | 0.001 | 100 | µA |
| | 50MBaud | | 14 | | mA |
| Receive Mode | DC | | 7.2 | 10 | mA |
| | 50MBaud | | 16 | | mA |
| **AC PARAMETERS** | | | | | |
| Data Rate, Maximum[5] | $C_L$ = 50pF | 50 | 80 | | MBaud |
| Data Rate, Minimum | | DC | | | |
| Propagation Time[6] | $C_L$ = 50pF | | 27 | 40 | ns |
| Propagation Delay Skew[7] | $C_L$ = 50pF | | 0.5 | 2 | ns |
| Pulse Width Distortion[8] | $C_L$ = 50pF | | 1.5 | 6 | ns |
| Output Rise/Fall Time, 10% to 90% | $C_L$ = 50pF | | 9 | 14 | ns |
| Mode Switching Time | | | | | |
| Receive-to-Transmit | | | 13 | | ns |
| Transmit-to-Receive | | | 75 | | ns |
| **TEMPERATURE RANGE** | | | | | |
| Operating Range | | –40 | | 85 | °C |
| Storage | | –40 | | 125 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | 75 | | °C/W |

NOTES: (1) All devices receive a 1s test. Failure criterion is ≥5 pulses of ≥5pC. (2) The voltage rate-of-change across the isolation barrier that can be sustained without data errors. (3) Logic inputs are HCT-type and thresholds are a function of power supply voltage with approximately 0.4V hystersis—see text. (4) Supply current measured with both transceivers set for the indicated mode. Supply current varies with data rate—see typical curves. (5) Calculated from the maximum Pulse Width Distortion (PWD), where Data Rate = 0.3/PWD. (6) Propagation time measured from $V_{IN}$ = 1.5V to $V_O$ = 2.5V. (7) The difference in propagation time of channel A and channel B in any combination of transmission directions. (8) The difference between propagation time of a rising edge and a falling edge.



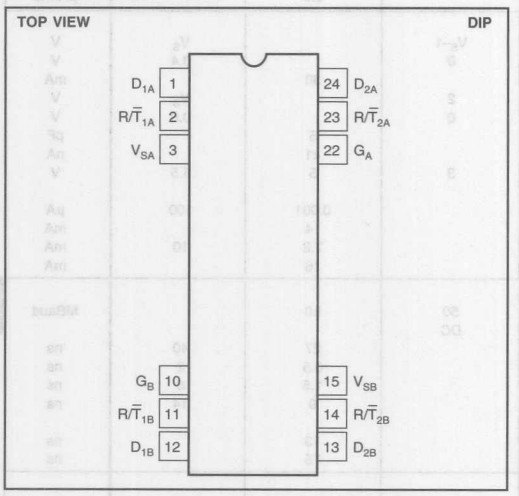
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## ABSOLUTE MAXIMUM RATINGS

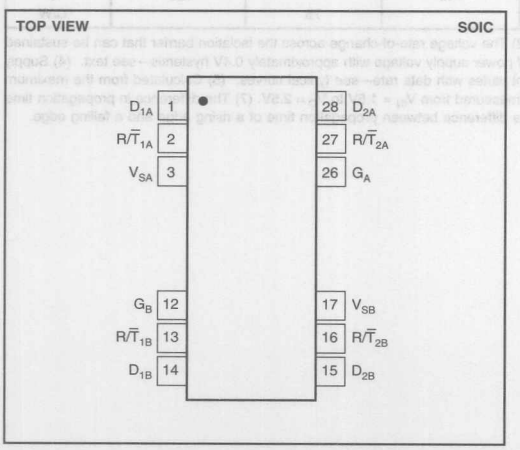
| | |
|---|---|
| Storage Temperature | –40°C to +125°C |
| Supply Voltages, $V_S$ | –0.5 to 6V |
| Transmitter Input Voltage, $V_I$ | –0.5 to $V_S$ + 0.5V |
| Receiver Output Voltage, $V_O$ | –0.5 to $V_S$ + 0.5V |
| $R/\overline{T}_X$ Inputs | –0.5 to $V_S$ + 0.5V |
| Isolation Voltage dV/dt, $V_{ISO}$ | 500kV/µs |
| $D_X$ Short to Ground | Continuous |
| Junction Temperature, $T_J$ | 175°C |
| Lead Temperature (soldering, 10s) | 260°C |
| 1.6mm below seating plane (DIP package) | 300°C |

## PIN CONFIGURATION

TOP VIEW DIP




TOP VIEW SOIC




## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ISO150AP | 24-Pin Single-Wide DIP | 243-1 |
| ISO150AU | 28-Lead SOIC | 217-2 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN DESCRIPTIONS

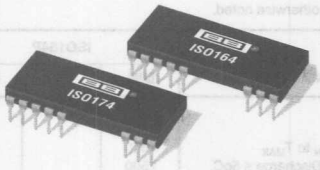
| NAME | FUNCTION |
|---|---|
| $D_{1A}$ | Data in or data out for transceiver 1A. $R/\overline{T}_{1A}$ held low makes $D_{1A}$ an input pin. |
| $R/\overline{T}_{1A}$ | Receive/Transmit switch controlling transceiver 1A. |
| $V_{SA}$ | +5V supply pin for side A which powers transceivers 1A and 2A. |
| $G_B$ | Ground pin for transceivers 1B and 2B. |
| $R/\overline{T}_{1B}$ | Receive/Transmit switch controlling transceiver 1B. |
| $D_{1B}$ | Data in or data out for transceiver 1B. $R/\overline{T}_{1B}$ held low makes $D_{1B}$ an input pin. |
| $D_{2B}$ | Data in or data out for transceiver 2B. $R/\overline{T}_{2B}$ held low makes $D_{2B}$ an input pin. |
| $R/\overline{T}_{2B}$ | Receive/Transmit switch controlling $D_{2B}$. |
| $V_{SB}$ | +5V supply pin for side B which powers transceivers 1B and 2B. |
| $G_A$ | Ground pin for transceivers 1A and 2A. |
| $R/\overline{T}_{2A}$ | Receive/Transmit switch controlling transceiver 2A. |
| $D_{2A}$ | Data in or data out for transceiver 2A. $R/\overline{T}_{2A}$ held low makes $D_{2A}$ in input pin. |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®




# ISO164
# ISO174

www.burr-brown.com/databook/ISO164.html

# Precision, Isolated PROGRAMMABLE GAIN AMPLIFIER



## FEATURES

- RATED
  1500Vrms Continuous
  2500Vrms for One Minute
  100% TESTED FOR PARTIAL DISCHARGE
- PROGRAMMABLE GAINS OF
  1, 10, 100
- HIGH IMR: 115dB at 50Hz
- LOW NONLINEARITY: ±0.01%
- LOW INPUT BIAS CURRENT: ±5nA max
- INPUTS PROTECTED TO ±40V
- BIPOLAR OPERATION: $V_O$ = ±10V
- SYNCHRONIZATION CAPABILITY
- 24-PIN PLASTIC DIP: 0.6" Wide

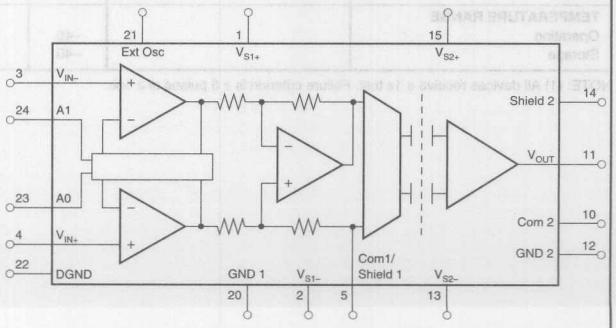
## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer Isolator, Thermocouple Isolator, RTD Isolator, Pressure Bridge Isolator, Flow Meter Isolator
- POWER MONITORING
- MEDICAL INSTRUMENTATION
- ANALYTICAL MEASUREMENTS
- BIOMEDICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT
- POWER MONITORING
- GROUND LOOP ELIMINATION

## DESCRIPTION

ISO164 and ISO174 are PGA input isolation amplifiers incorporating a novel duty cycle modulation-demodulation technique which provides excellent accuracy. Internal input protection can withstand up to ±40V differential inputs without damage. The signal is transmitted digitally across a differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity. This results in excellent reliability and good high frequency transient immunity across the barrier. Both the amplifier and barrier capacitors are housed in a plastic DIP. ISO164 and ISO174 differ in frequency response and linearity.

These amplifiers are easy to use. No external components are required. A power supply range of ±4.5V to ±18V makes these amplifiers ideal for a wide range of applications.




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# SPECIFICATIONS

At $T_A$ = +25°C, $V_{S1} = V_{S2}$ = ±15V, and $R_L$ = 2kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | ISO164P | | | ISO174P | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ISOLATION**(1) | | | | | | | | |
| Voltage Rated Continuous: | | | | | | | | |
| AC | $T_{MIN}$ to $T_{MAX}$ | 1500 | | | 1500 | | | Vrms |
| 100% Test (AC 50Hz) | 1s; Partial Discharge ≤ 5pC | 2500 | | | 2500 | | | Vrms |
| Isolation-Mode Rejection | | | | | | | | |
| AC 50Hz | 1500Vrms | | 115 | | | 115 | | dB |
| Barrier Impedance | | | $10^{14}$ ‖ 10 | | | $10^{14}$ ‖ 10 | | Ω ‖ pF |
| Leakage Current | VISO = 240Vrms, 50Hz | | 0.8 | 1 | | 0.8 | 1 | μArms |
| **GAIN** | | | | | | | | |
| Gain Error | G = 1 | | | ±0.3 | | | ±0.3 | % |
| | G = 10 | | ±0.06 | | | ±0.06 | | |
| | G = 100 | | | ±0.3 | | | ±0.3 | % |
| Gain vs Temperature | G = 1 | | ±12.5 | | | ±42.5 | | ppm/°C |
| | G = 10 | | ±12.5 | | | ±42.5 | | ppm/°C |
| | G = 100 | | ±12.5 | | | ±42.5 | | ppm/°C |
| Nonlinearity | G = 1 | | ±0.01 | ±0.052 | | ±0.04 | ±0.102 | % |
| | G = 10 | | ±0.01 | | | ±0.04 | | % |
| | G = 100 | | ±0.01 | ±0.054 | | ±0.04 | ±0.104 | % |
| **INPUT OFFSET VOLTAGE** | | | | | | | | |
| Initial Offset | | | $\pm\left(0.125+\frac{51}{G}\right)$ | | | $\pm\left(0.125+\frac{101}{G}\right)$ | | mV |
| vs Temperature | G = 1 | | ±155 | | | ±505 | | μV/°C |
| vs Supply | DC, G = 1 | | 2 | | | 2 | | mV/V |
| CMRR | DC, G = 1 | | 90 | | | 90 | | dB |
| **INPUT** | | | | | | | | |
| Voltage Range | | ±10.0 | | | ±10.0 | | | V |
| Bias Current | | | | ±5 | | | ±5 | nA |
| vs Temperature | | | ±8 | | | ±8 | | pA/°C |
| Offset Current | | | | ±5 | | | ±5 | nA |
| vs Temperature | | | ±8 | | | ±8 | | pA/°C |
| **OUTPUT** | | | | | | | | |
| Voltage Range | | ±10 | | | ±10 | | | V |
| Current Drive | | ±5 | | | ±5 | | | mA |
| Capacitive Load Drive | | | 0.1 | | | 0.1 | | μF |
| Ripple Voltage | | | 10 | | | 10 | | mVp-p |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Small Signal Bandwidth | 100mVrms, G = 1 | | 6 | | | 60 | | kHz |
| | 100mVrms, G = 10 | | 6 | | | 60 | | kHz |
| | 100mVrms, G = 100 | | 6 | | | 10 | | kHz |
| Slew Rate | $V_O$ = ±10V, G = 10 | | 0.7 | | | 0.7 | | V/μs |
| **POWER SUPPLIES** | | | | | | | | |
| Rated Voltage | | | 15 | | | 15 | | V |
| Voltage Range | | ±4.5 | | ±18 | ±4.5 | | ±18 | V |
| Quiescent Current | | | | | | | | |
| $V_{S1}$ | | | | ±15 | | | ±15 | mA |
| $V_{S2}$ | | | | ±7.5 | | | ±7.5 | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Operating | | –40 | | 85 | –40 | | 85 | °C |
| Storage | | –40 | | 125 | –40 | | 125 | °C |

NOTE: (1) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pc.

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## ABSOLUTE MAXIMUM RATINGS

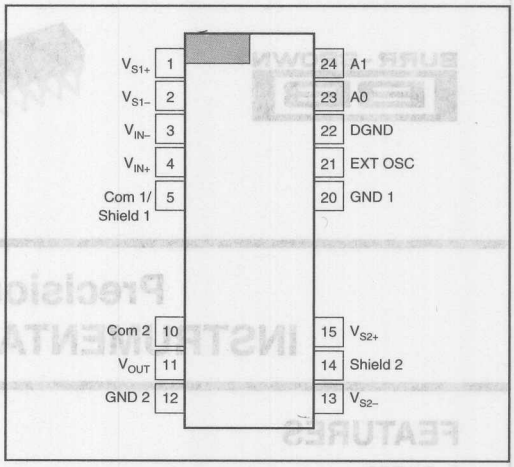
| | |
|---|---|
| Supply Voltage | ±18V |
| $V_{IN}$, Analog Input Voltage Range | ±40V |
| External Oscillator Input | ±25V |
| Signal Common 1 to Ground 1 | ±1V |
| Signal Common 2 to Ground 2 | ±1V |
| Continuous Isolation Voltage | 1500Vrms |
| IMV, dv/dt | 20kV/µs |
| Junction Temperature | 150°C |
| Storage Temperature | –40°C to 125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short Duration | Continuous to Common |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION




## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | BANDWIDTH |
|---|---|---|---|
| ISO164P | 24-Pin Plastic DIP | 167-1 | 6kHz |
| ISO174P | 24-Pin Plastic DIP | 167-1 | 60kHz |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR - BROWN®




# ISO175

www.burr-brown.com/databook/ISO175.html

# Precision, Isolated INSTRUMENTATION AMPLIFIER

## FEATURES

- RATED
  1500Vrms Continuous
  2500Vrms for One Minute
  100% TESTED FOR PARTIAL DISCHARGE
- HIGH IMR: 115dB at 50Hz
- LOW NONLINEARITY: ±0.01%
- LOW INPUT BIAS CURRENT: 10nA max
- LOW INPUT OFFSET VOLTAGE: 101mV max
- INPUTS PROTECTED TO ±40V
- BIPOLAR OPERATION: $V_O$ = ±10V
- SYNCHRONIZATION CAPABILITY
- 24-PIN PLASTIC DIP: 0.3" Wide

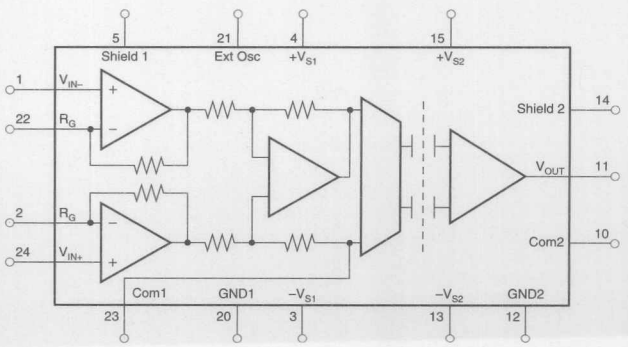
## DESCRIPTION

ISO175 is a precision isolated instrumentation amplifier incorporating a novel duty cycle modulation-demodulation technique and excellent accuracy. A single external resistor sets the gain. Internal input protection can withstand up to ±40V without damage. The signal is transmitted digitally across a differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity. This results in excellent reliability and good high frequency transient immunity across the barrier. Both the amplifier and barrier capacitors are housed in a plastic DIP.

ISO175 is easy to use. A power supply range of ±4.5V to ±18V makes this amplifier ideal for a wide range of applications.

## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer Isolator, Thermocouple Isolator, RTD Isolator, Pressure Bridge Isolator, Flow Meter Isolator
- POWER MONITORING
- MEDICAL INSTRUMENTATION
- ANALYTICAL MEASUREMENTS
- BIOMEDICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT
- POWER MONITORING
- GROUND LOOP ELIMINATION




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At $T_A$ = +25°C, $V_{S1}$ = $V_{S2}$ = ±15V, and $R_L$ = 2kΩ unless otherwise noted.

| PARAMETER | CONDITIONS | ISO175P MIN | ISO175P TYP | ISO175P MAX | UNITS |
|---|---|---|---|---|---|
| **ISOLATION**[1] | | | | | |
| Voltage Rated Continuous: | | | | | |
| AC | $T_{MIN}$ to $T_{MAX}$ | 1500 | | | Vrms |
| DC | $T_{MIN}$ to $T_{MAX}$ | 2121 | | | VDC |
| 100% Test (AC, 50Hz) | 1s; Partial Discharge ≤ 5pC | 2500 | | | Vrms |
| Isolation-Mode Rejection | | | | | |
| AC 50Hz | 1500Vrms | | 115 | | dB |
| DC | | | 160 | | dB |
| Barrier Impedance | | | $10^{14}$ \|\| 6 | | Ω \|\| pF |
| Leakage Current | VISO = 240Vrms, 50Hz | | 0.8 | 1 | µArms |
| **GAIN** | | | $1+\left(\frac{50k}{R_G}\right)$ | | V/V |
| Gain Error | G = 1 | | | ±0.35 | % |
| | G = 10 | | ±0.07 | | % |
| | G = 100 | | | ±0.95 | % |
| Gain vs Temperature | G = 1 | | ±11 | | ppm/°C |
| Nonlinearity | G = 1 | | | ±0.102 | % |
| | G = 10 | | ±0.04 | | % |
| | G = 100 | | | ±0.104 | % |
| **INPUT OFFSET VOLTAGE** | | | | | |
| Initial Offset | G = 1, 100 | | | $\pm\left(0.125+\frac{101}{G}\right)$ | mV |
| vs Temperature | | | $\pm\left(1+\frac{520}{G}\right)$ | | µV/°C |
| vs Supply | G = 1 | | ±2 | | mV/V |
| **INPUT** | | | | | |
| Voltage Range | | ±10 | | | V |
| Bias Current | | | | ±10 | nA |
| vs Temperature | | | ±40 | | pA/°C |
| Offset Current | | | | ±10 | nA |
| vs Temperature | | | ±40 | | pA/°C |
| **OUTPUT** | | | | | |
| Voltage Range | | ±10 | | | V |
| Current Drive | | ±5 | | | mA |
| Capacitive Load Drive | | | 0.1 | | µF |
| Ripple Voltage | | | 10 | | mVp-p |
| **FREQUENCY RESPONSE** | | | | | |
| Small Signal Bandwidth | G = 1 | | 60 | | kHz |
| | G = 10 | | 60 | | kHz |
| | G = 100 | | 50 | | kHz |
| Slew Rate | $V_O$ = ±10V, G = 10 | | 0.9 | | V/µs |
| **POWER SUPPLIES** | | | | | |
| Rated Voltage | | | 15 | | V |
| Voltage Range | | ±4.5 | | ±18 | V |
| Quiescent Current | | | | | |
| $V_{S1}$ | | | | ±7.4 | mA |
| $V_{S2}$ | | | | ±7.5 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –40 | | 85 | °C |
| Storage | | –40 | | 125 | °C |

NOTE: (1) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pc.

## ABSOLUTE MAXIMUM RATINGS

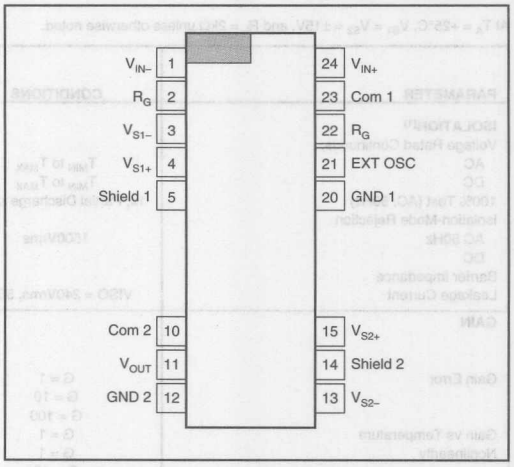
| | |
|---|---|
| Supply Voltage | ±18V |
| Analog Input Voltage Range | ±40V |
| External Oscillator Input | ±25V |
| Com 1 to GND1 | ±1V |
| Com 2 to GND2 | ±1V |
| Continuous Isolation Voltage: | 1500Vrms |
| IMV, dv/dt | 20kV/µs |
| Junction Temperature | 150°C |
| Storage Temperature | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short Duration | Continuous to Common |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION




## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | BANDWIDTH |
|---|---|---|---|
| ISO175P | 24-Pin Plastic DIP | 243-2 | 60kHz |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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# ISO176

www.burr-brown.com/databook/ISO176.html

# Precision, Isolated OPERATIONAL AMPLIFIER



## FEATURES

- RATED
  1500Vrms Continuous
  2500Vrms for One Minute
  100% TESTED FOR PARTIAL DISCHARGE
- HIGH IMR: 115dB at 50Hz
- LOW NONLINEARITY: ±0.05%
- LOW INPUT BIAS CURRENT: ±5nA max
- LOW INPUT OFFSET VOLTAGE: ±20µV
- OP AMP INPUTS PROTECTED TO ±30V
- MOD INPUT PROTECTED TO ±100V
- BIPOLAR OPERATION: $V_O$ = ±10V
- SYNCHRONIZATION CAPABILITY
- 24-PIN PLASTIC DIP: 0.3" Wide

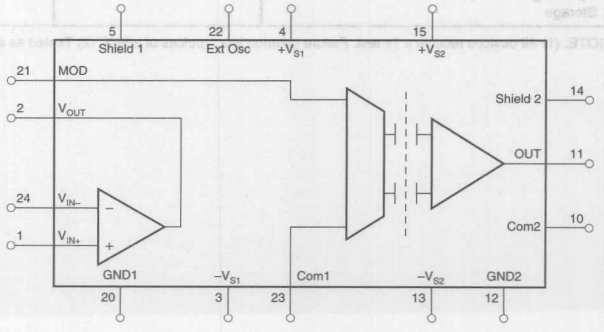
## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer Isolator, Thermocouple Isolator, RTD Isolator, Pressure Bridge Isolator, Flow Meter Isolator
- POWER MONITORING
- MEDICAL INSTRUMENTATION
- ANALYTICAL MEASUREMENTS
- BIOMEDICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT
- POWER MONITORING
- GROUND LOOP ELIMINATION

## DESCRIPTION

ISO176 is a precision isolation amplifier incorporating an uncommitted operational amplifier for input conditioning, a novel duty cycle modulation-demodulation technique and excellent accuracy. Internal input protection can withstand up to ±30V differential without damage. The signal is transmitted digitally across a differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity. This results in excellent reliability and good high frequency transient immunity across the barrier. Both the amplifier and barrier capacitors are housed in a plastic DIP.

ISO176 is easy to use. No external components are required. A power supply range of ±4.5V to ±18V makes this amplifier ideal for a wide range of applications.



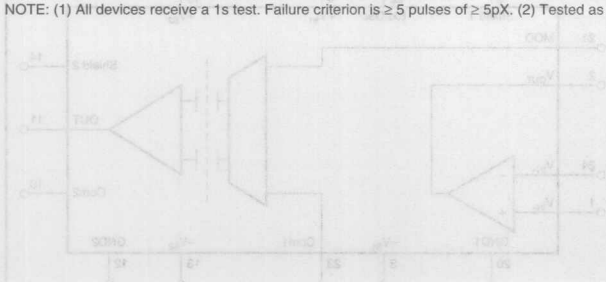

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## SPECIFICATIONS

At $T_A$ = +25°C, $V_{S1}$ = $V_{S2}$ = ±15V, and $R_L$ = 2kΩ unless otherwise noted.

| PARAMETER | CONDITIONS | ISO176P MIN | ISO176P TYP | ISO176P MAX | UNITS |
|---|---|---|---|---|---|
| **ISOLATION**[1] | | | | | |
| Voltage Rated Continuous: | | | | | |
| AC | $T_{MIN}$ to $T_{MAX}$ | 1500 | | | Vrms |
| DC | $T_{MIN}$ to $T_{MAX}$ | 2121 | | | VDC |
| 100% Test (AC, 50Hz) | 1s; Partial Discharge ≤ 5pC | 2500 | | | Vrms |
| Isolation-Mode Rejection | | | | | |
| AC 50Hz | 1500Vrms | | 115 | | dB |
| DC | | | 160 | | dB |
| Barrier Impedance | | | $10^{14}$ ‖ 6 | | Ω ‖ pF |
| Leakage Current | $V_{ISO}$ = 240Vrms, 50Hz | | 0.8 | 1 | μArms |
| **ISO AMP - GAIN** | | | | | |
| Gain Error[2] | G = 1 | | ±0.05 | | %FSR |
| Gain vs Temperature | G = 1 | | ±10 | | ppm/°C |
| Nonlinearity | G = 1 | | | ±0.102 | % |
| **ISO AMP - OFFSET VOLTAGE** | | | | | |
| Offset | | | | 100 | mV |
| vs Temperature | | | ±500 | | μV/°C |
| vs Supply | | | ±2 | | μV/V |
| **ISO AMP - INPUT** | | | | | |
| Input Resistance | | | 200 | | kΩ |
| **ISO AMP - OUTPUT** | | | | | |
| Voltage Range | | ±10 | | | V |
| Current Drive | | ±5 | | | mA |
| Capacitive Load Drive | | | 0.1 | | μF |
| Ripple Voltage | | | 10 | | mVp-p |
| **OP AMP - INPUT** | | | | | |
| Voltage Range | | | ±13 | | V |
| Bias Current | | | | ±5 | nA |
| vs Temperature | | | ±15 | | pA/°C |
| Offset Voltage | | | ±20 | | μV |
| Offset Current | | | | ±5 | nA |
| vs Temperature | | | ±1.5 | | pA/°C |
| **FREQUENCY RESPONSE** | | | | | |
| Small Signal Bandwidth | 100mV, G = 1 | | 60 | | kHz |
| | 100mV, G = 10 | | 60 | | kHz |
| | 100mV, G = 100 | | 60 | | kHz |
| Slew Rate | $V_O$ = ±10V, G = 10 | | 0.3 | | V/μs |
| **POWER SUPPLIES** | | | | | |
| Rated Voltage | | | 15 | | V |
| Voltage Range | | ±4.5 | | ±18 | V |
| Quiescent Current | | | | | |
| $V_{CC1}$ | | | 9 | | mA |
| $V_{CC2}$ | | | 7.5 | | mA |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –40 | | 85 | °C |
| Storage | | –40 | | 125 | °C |

NOTE: (1) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pX. (2) Tested as a OPA and ISO, max ±0.35% FSR.



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## ABSOLUTE MAXIMUM RATINGS

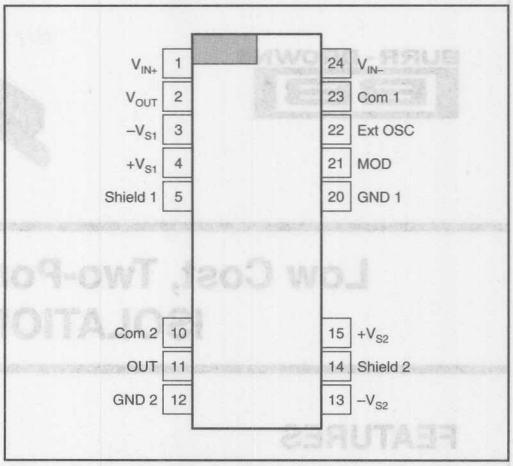
| | |
|---|---|
| Supply Voltage | ±18V |
| Op Amp Analog Input Voltage Range | $\pm V_{S1}$ |
| External Oscillator Input | ±25V |
| Signal Common 1 to Ground 1 | ±1V |
| Signal Common 2 to Ground 2 | ±1V |
| Continuous Isolation Voltage: | 1500Vrms |
| IMV, dv/dt | 20kV/µs |
| Junction Temperature | 150°C |
| Storage Temperature | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short Duration | Continuous to Common |
| MOD Input Voltage Range | ±100V |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION

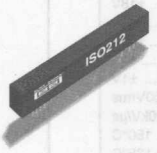



## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | BANDWIDTH |
|---|---|---|---|
| ISO176P | 24-Pin Plastic DIP | 243-2 | 60kHz |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# ISO212P

www.burr-brown.com/databook/ISO212.html

# Low Cost, Two-Port Isolated, 1500Vrms ISOLATION AMPLIFIER

## FEATURES

- 12-BIT ACCURACY
- 2.5mA (typ) QUIESCENT CURRENT
- LOW PROFILE (LESS THAN 0.5" HIGH)
- SMALL FOOTPRINT
- EXTERNAL POWER CAPABILITY (±8V at 5mA)
- "MASTER/SLAVES" SYNCHRONIZATION CAPABILITY
- INPUT OFFSET ADJUSTMENT
- LOW POWER (53mW)
- SINGLE 10V TO 15V SUPPLY OPERATION

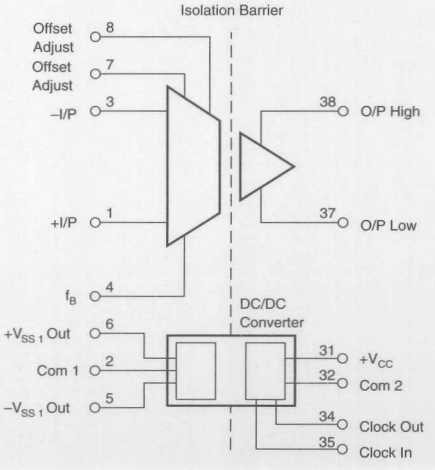
## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL: Transducer Channel Isolator for Thermocouples, RTDs, Pressure Bridges, Flow Meters
- 4mA TO 20mA LOOP ISOLATION
- MOTOR AND SCR CONTROL
- GROUND LOOP ELIMINATION
- ANALYTICAL MEASUREMENTS
- POWER PLANT MONITORING
- DATA ACQUISITION/TEST EQUIPMENT ISOLATION
- MULTIPLEXED SYSTEMS WITH CHANNEL TO CHANNEL ISOLATION

## DESCRIPTION

The ISO212P signal isolation amplifier is a member of a series of low-cost isolation products from Burr-Brown. The low-profile SIL plastic package allows PCB spacings of 0.5" to be achieved, and the small footprint results in efficient use of board space.

To provide isolation, the design uses high-efficiency, miniature toroidal transformers in both the signal and power paths. An uncommitted input amplifier and an isolated external bipolar supply ensure the majority of input interfacing or conditioning needs can be met. The ISO212P accepts an input voltage range of ±5V for single 15V supply operation or ±3.0V for single 10V supply operation.




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# SPECIFICATIONS

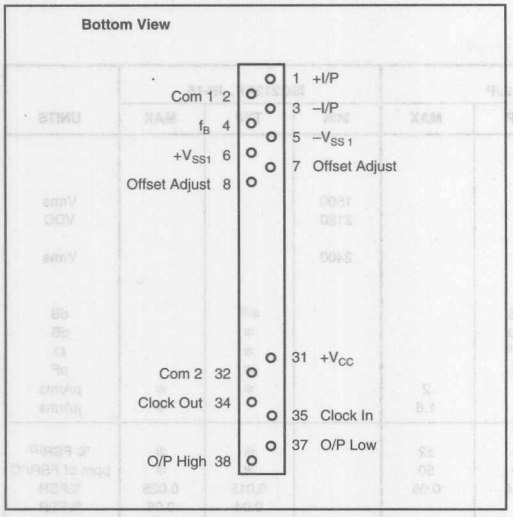
## ELECTRICAL

At $T_A$ = +25°C and $V_{CC}$ = +15V, unless otherwise noted.

| PARAMETER | CONDITIONS | ISO212JP MIN | ISO212JP TYP | ISO212JP MAX | ISO212KP, JP-15 MIN | ISO212KP, JP-15 TYP | ISO212KP, JP-15 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **ISOLATION** | | | | | | | | |
| Voltage | | | | | | | | |
| Rated Continuous | | | | | | | | |
| AC, 50Hz | | 750 | | | 1500 | | | Vrms |
| DC | | 1060 | | | 2120 | | | VDC |
| 100% Test (AC, 50Hz) | Partial Discharge 1s : <5pC | 1200 | | | 2400 | | | Vrms |
| Isolation-Mode Rejection[1] | $V_{ISO}$ = Rated Continuous 60Hz | | | | | | | |
| AC | | | 115 | | | *[9] | | dB |
| DC | | | 160 | | | * | | dB |
| Barrier Resistance | | | $10^{10}$ | | | * | | Ω |
| Barrier Capacitance | | | 12 | | | * | | pF |
| Leakage Current[8] | $V_{ISO}$ = 240Vrms, 60Hz | | 1 | 2 | | * | * | µArms |
| | $V_{ISO}$ = 240Vrms, 50Hz | | | 1.6 | | | * | µArms |
| **GAIN** | | | | | | | | |
| Initial Error | | | ±1 | ±2 | | * | * | % FSR[2] |
| Gain vs Temperature | | | 20 | 50 | | * | * | ppm of FSR/°C |
| Nonlinearity[3]: KP | $V_O$ = –5V to +5V | | 0.04 | 0.05 | | 0.015 | 0.025 | %FSR |
| JP-15 | | | | | | 0.04 | 0.05 | %FSR |
| **INPUT OFFSET VOLTAGE** | | | | | | | | |
| Offset Voltage RTI: KP | | | | ±10 ±10/G | | | ±7.5 ±7.5/G | mV |
| JP-15 | | | | | | | ±10 ±10/G | mV |
| vs Temperature | | | 30 ±30/G | | | * | | µV/°C |
| vs Power Supply[4] | $V_{CC}$ = 14V to 16V | | ±1.5 | | | * | | mV/V |
| Adjustment Range | | ±20 | | | * | | | mV |
| **INPUT CURRENT** | | | | | | | | |
| Bias | | | | 50 | | | * | nA |
| Offset | | | | 4 | | | * | nA |
| **INPUT** | | | | | | | | |
| Voltage Range[5] | G = 1 | ±5 | | | * | | | V |
| Resistance | | | $10^{12}$ | | | * | | Ω |
| **OUTPUT** | | | | | | | | |
| Output Impedance | | | 3 | | | * | | kΩ |
| Voltage Range | Out Hi to Out Lo Min Load = 1MΩ | ±5 | | | * | | | V |
| Ripple Voltage[6] | f = 0 to 100kHz | | 8 | | | * | | mVp-p |
| | f = 0 to 5kHz | | 0.4 | | | * | | mVrms |
| Ouput Compliance | Out Hi or Out Lo | | 7.5 | | | | | V |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Small Signal Bandwidth | I/P = 1Vp-p, –3dB G = 1 | | 1 | | | * | | kHz |
| Full Signal Bandwidth | I/P = 10Vp-p, G = 1 | | 200 | | | * | | Hz |
| | G = 10 (–3dB) | | 1.8 | | | | | kHz |
| **ISOLATED POWER OUTPUTS** | | | | | | | | |
| Voltage Outputs ($\pm V_{SS\ 1}$)[7] | No Load | ±7.5 | ±8 | | * | * | | VDC |
| vs Temperature | | | –8 | | | * | | mV/°C |
| vs Load | | | 90 | | | * | | mV/mA |
| Current Output [7] | | | | | | | | |
| (Both Loaded) | | | | 5 | | | * | mA |
| (One Loaded) | | | | 8 | | | * | mA |
| **POWER SUPPLIES** | | | | | | | | |
| Rated Voltage | Rated Performance | | 15 | | | * | | V |
| Voltage Range[5] | | | 11.4 to 16 | | * | | * | V |
| Quiescent Current | No Load | | 2.5 | 3.5 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | 0 | | +70 | * | | * | °C |
| Operating | | –25 | | +85 | * | | * | °C |

NOTES: (1) Isolation-mode rejection is the ratio of the change in output voltage to a change in isolation barrier voltage. It is a function of frequency. (2) FSR = Full Scale Range = 10V. (3) Nonlinearity is the peak deviation of the output voltage from the best-fit straight line. It is expressed as the ratio of deviation to FSR. (4) Power Supply Rejection is the change in $V_{OS}$/Supply Change. (5) At $V_{CC}$ = +10.0V, input voltage range = ±3.0V min. (6) Ripple is the residual component of the barrier carrier frequency generated internally. (7) Derated at $V_{CC}$ < +15V. (8) Tested at 2400Vrms, 50Hz limit 16µA. (9) Asterisk (*) same as ISO212JP.

## PIN CONFIGURATION




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage Without Damage | 18V |
| Continuous Isolation Voltage Across Barrier: JP | 750Vrms |
| KP, JP-15 | 1500Vrms |
| Storage Temperature Range | –25°C to 100°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Amplifier Output Short-Circuit Duration | Continuous to Common |
| Output Voltage Hi or Lo to Com 2 | $\pm V_{CC}/2$ |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ISO212JP | 38-Pin Plastic SIP | 326 | –25°C to +85°C |
| ISO212JP-15 | 38-Pin Plastic SIP | 326 | –25°C to +85°C |
| ISO212KP | 38-Pin Plastic SIP | 326 | –25°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# ISO253




www.burr-brown.com/databook/ISO253.html

# Precision, Powered, Three-Port Isolated BUFFER AMPLIFIER



## FEATURES

- RATED
  1500Vrms Continuous
  2500Vrms for One Minute
- 100% TESTED FOR PARTIAL DISCHARGE
- LOW NONLINEARITY: ±0.01% typ
- INPUT PROTECTED TO ±100V
- BIPOLAR OPERATION: $V_O$ = ±10V
- SYNCHRONIZATION CAPABILITY
- 28-PIN PLASTIC DIP: 0.6" Wide

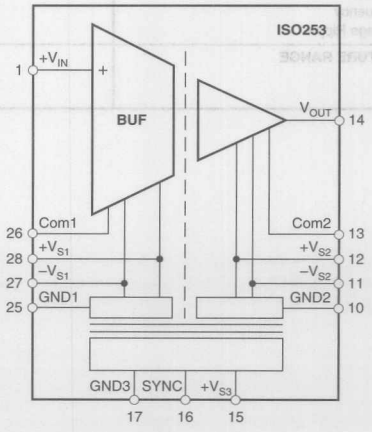
## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer Isolator, Thermocouple Isolator, RTD Isolator, Pressure Bridge Isolator, Flow Meter Isolator
- POWER MONITORING
- MEDICAL INSTRUMENTATION
- ANALYTICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT
- GROUND LOOP ELIMINATION

## DESCRIPTION

ISO253 is a precision three-port isolated buffer amplifier incorporating a novel duty cycle modulation-demodulation technique and has excellent accuracy. The input is protected to withstand ±100V without damage. The signal is transmitted digitally across a differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity. This results in excellent reliability and good high frequency transient immunity across the barrier. The DC/DC converter, amplifier and barrier capacitors are housed in a plastic DIP.

This amplifier is easy to use as no external components are required. A power supply range of 11V to 18V makes this amplifier ideal for a wide range of applications.




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# SPECIFICATIONS

At $T_A$ = +25°C, $V_{S3}$ = 15V, $R_L$ = 2kΩ, and 220nF capacitors on all generated supplies, unless otherwise noted.

| PARAMETER | CONDITIONS | ISO253P | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **ISOLATION** | | | | | |
| Voltage Rated Continuous: | | | | | |
| AC | $T_{MIN}$ to $T_{MAX}$ | 1500 | | | Vrms |
| 100% Test (AC 50Hz) | 1s; Partial Discharge ≤ 5pC | 2500 | | | Vrms |
| Rated One Min | | 2500 | | | Vrms |
| Isolation-Mode Rejection | | | | | |
| DC | | | 120 | | dB |
| AC 50Hz | 1500Vrms | | 95 | | dB |
| Barrier Impedance | | | $10^{14}$ \|\| 2 | | Ω \|\| pF |
| Leakage Current | VISO = 240Vrms, 50Hz | | 1.4 | 2 | μArms |
| **GAIN** | | | | | |
| Nominal Gain | | | 1 | | V/V |
| Gain Error | | | 0.15 | ±0.3 | % |
| Gain vs Temperature | | | 15 | | ppm/°C |
| Nonlinearity | | | 0.01 | ±0.1 | % |
| **INPUT OFFSET VOLTAGE** | | | | | |
| Initial Offset | | | | ±100 | mV |
| vs Temperature | | | 150 | | μV/°C |
| vs Supply | | | 1 | | mV/V |
| **INPUT** | | | | | |
| Voltage Range | | ±10 | ±15 | | V |
| Resistance | | | 200 | | kΩ |
| **OUTPUT** | | | | | |
| Voltage Range | | ±10 | | | V |
| Current Drive | | ±5 | | | mA |
| Capacitive Load Drive | | | 0.1 | | μF |
| Ripple Voltage | | | 25 | | mVp-p |
| **FREQUENCY RESPONSE** | | | | | |
| Small Signal Bandwidth | | | 50 | | kHz |
| Slew Rate | | | 0.25 | | V/μs |
| Settling Time, 0.1% | | | 50 | | μs |
| **POWER SUPPLIES** | | | | | |
| Rated Voltage | | | 15 | | V |
| Voltage Range | | 11 | | 18 | V |
| Quiescent Current | | 25 | 40 | 55 | mA |
| Rated Output Voltage | No Load | 13 | 14.5 | | V |
| | 50mA Load On Two Supplies | 12 | 13.2 | 16 | V |
| Load Regulation | | | 28 | | mV/mA |
| Line Regulation | | | 1 | | V/V |
| SYNC Frequency | | 1 | | 1.4 | MHz |
| Output Voltage Ripple | | | 50 | | mV |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –40 | | 85 | °C |
| Storage | | –40 | | 85 | °C |

## ABSOLUTE MAXIMUM RATINGS

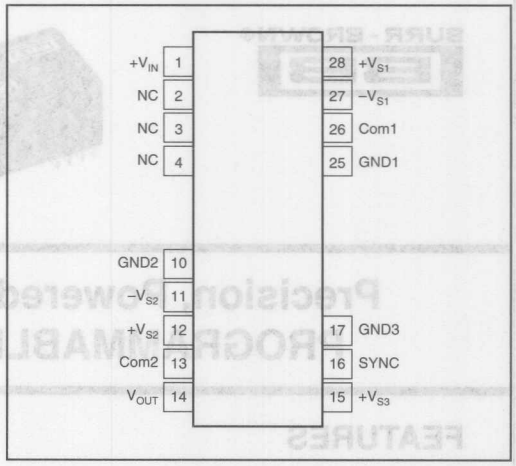
| | |
|---|---|
| Supply Voltage | +18V |
| $V_{IN}$, Analog Input Voltage Range | ±100V |
| Com1 to GND1 | ±1V |
| Com2 to GND2 | ±1V |
| Continuous Isolation Voltage: | 1500Vrms |
| | 2500Vrms one min |
| IMV, dv/dt | 20kV/µs |
| Junction Temperature | 150°C |
| Storage Temperature | –40°C to +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short Duration | Continuous to Common |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION




## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| ISO253P | 28-Pin Plastic DIP | 335 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



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# ISO254

www.burr-brown.com/databook/ISO254.html

# Precision, Powered, Three-Port Isolated PROGRAMMABLE GAIN AMPLIFIER

## FEATURES

- RATED
  1500Vrms Continuous
  2500Vrms for One Minute
  100% TESTED FOR PARTIAL DISCHARGE
- PROGRAMMABLE GAINS OF
  1, 10, 100, 1000
- LOW NONLINEARITY: ±0.01% typ
- LOW INPUT BIAS CURRENT: ±5nA max
- LOW INPUT OFFSET VOLTAGE:
  625µV max
- INPUTS PROTECTED TO ±40V
- BIPOLAR OPERATION: $V_O$ = ±10V
- SYNCHRONIZATION CAPABILITY
- 28-PIN PLASTIC DIP: 0.6" Wide

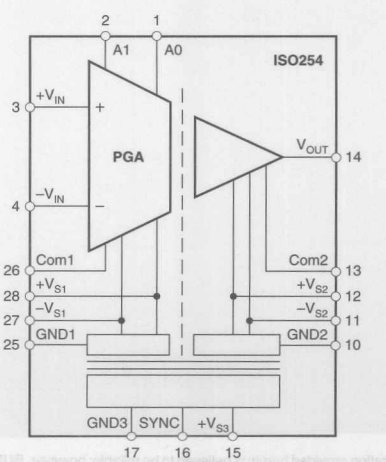
## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer Isolator, Thermocouple Isolator, RTD Isolator, Pressure Bridge Isolator, Flow Meter Isolator
- POWER MONITORING
- MEDICAL INSTRUMENTATION
- ANALYTICAL MEASUREMENTS
- BIOMEDICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT
- GROUND LOOP ELIMINATION

## DESCRIPTION

ISO254 is a precision three-port isolated programmable gain instrumentation amplifier incorporating a novel duty cycle modulation-demodulation technique and has excellent accuracy. Internal input protection can withstand up to ±40V input differential without damage. The signal is transmitted digitally across a differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity. This results in excellent reliability and good high frequency transient immunity across the barrier. The DC/DC converter, amplifier and barrier capacitors are housed in a plastic DIP.

This amplifier is easy to use as no external components are required. A power supply range of 11V to 18V makes this amplifier ideal for a wide range of applications.




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# SPECIFICATIONS

At $T_A$ = +25°C, $+V_{S3}$ = 15V, $R_L$ = 2kΩ, and 220nF capacitors on all generated supplies, unless otherwise noted.

| PARAMETER | CONDITIONS | ISO254P MIN | ISO254P TYP | ISO254P MAX | UNITS |
|---|---|---|---|---|---|
| **ISOLATION** | | | | | |
| Voltage Rated Continuous: | | | | | |
| AC | $T_{MIN}$ to $T_{MAX}$ | 1500 | | | Vrms |
| 100% Test (AC 50Hz) | 1s; Partial Discharge ≤ 5pC | 2500 | | | Vrms |
| Rated One Min | | 2500 | | | Vrms |
| Isolation-Mode Rejection | | | | | |
| DC | | | 120 | | dB |
| AC 50Hz | 1500Vrms | | 95 | | dB |
| Barrier Impedance | | | $10^{14}$ ‖ 2 | | Ω ‖ pF |
| Leakage Current | VISO = 240Vrms, 50Hz | | 1.4 | 2 | μArms |
| **GAIN** | | | | | |
| Gain Error | G = 1 | | 0.15 | ±0.3 | % |
| | G = 10 | | 0.15 | | |
| | G = 100 | | 0.15 | ±0.3 | % |
| | G = 1000 | | 0.2 | | |
| Gain vs Temperature | G = 1 | | ±15 | | ppm/°C |
| | G = 10 | | ±15 | | ppm/°C |
| | G = 100 | | ±15 | | ppm/°C |
| | G = 1000 | | ±15 | | ppm/°C |
| Nonlinearity | G = 1 | | ±0.01 | ±0.102 | % |
| | G = 10 | | ±0.01 | | |
| | G = 100 | | 0.01 | ±0.104 | % |
| | G = 1000 | | ±0.01 | | |
| **INPUT OFFSET VOLTAGE** | | | | | |
| Initial Offset | | | | ±(0.125 +101/G) | mV |
| vs Temperature | | | ±(1 + 510/G) | | μV/°C |
| CMRR | | | 90 | | dB |
| vs Supply | | | 1 | | mV/V |
| **INPUT** | | | | | |
| Voltage Range | | ±10 | | | V |
| Bias Current | | | | ±5 | nA |
| vs Temperature | | | ±8 | | pA/°C |
| Offset Current | | | | ±5 | nA |
| vs Temperature | | | ±8 | | pA/°C |
| **OUTPUT** | | | | | |
| Voltage Range | | ±10 | | | V |
| Current Drive | | ±5 | | | mA |
| Capacitive Load Drive | | | 0.1 | | μF |
| Ripple Voltage | | | 25 | | mVp-p |
| **FREQUENCY RESPONSE** | | | | | |
| Small Signal Bandwidth | G = 1 | | 50 | | kHz |
| | G = 10 | | 30 | | kHz |
| | G = 100 | | 10 | | kHz |
| | G = 1000 | | 1 | | kHz |
| Slew Rate | | | 0.5 | | V/μs |
| Settling Time, 0.1% | G = 1 | | 80 | | μs |
| | G = 10 | | 380 | | μs |
| | G = 100 | | 490 | | μs |
| | G = 1000 | | 1650 | | μs |
| **POWER SUPPLIES** | | | | | |
| Rated Voltage | | | 15 | | V |
| Voltage Range | | 11 | | 18 | V |
| Quiescent Current | | 25 | 40 | 55 | mA |
| Rated Output Voltage | No Load | 13 | 14.5 | | V |
| | 50mA Load On Two Supplies | 12 | 13.2 | 16 | V |
| Load Regulation | | | 35 | | mV/mA |
| Line Regulation | | | 1 | | V/V |
| SYNC Frequency | | 1 | | 1.4 | MHz |
| Output Voltage Ripple | | | 50 | | mV |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –40 | | 85 | °C |
| Storage | | –40 | | 85 | °C |

## ABSOLUTE MAXIMUM RATINGS

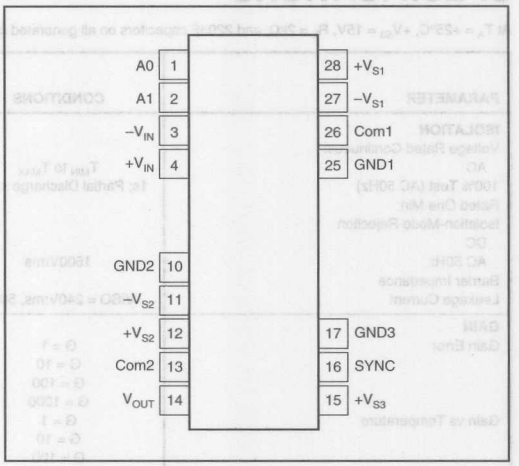
| | |
|---|---|
| Supply Voltage | +18V |
| $V_{IN}$, Analog Input Voltage Range | ±40V |
| Com1 to GND1 | ±1V |
| Com2 to GND2 | ±1V |
| Continuous Isolation Voltage | 1500Vrms |
| | 2500Vrms one min |
| IMV, dv/dt | 20kV/µs |
| Junction Temperature | 150°C |
| Storage Temperature | –40°C to +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short Duration | Continuous to Common |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION




## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| ISO254P | 28-Pin Plastic DIP | 335 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# ISO255

www.burr-brown.com/databook/ISO255.html

# Precision, Powered, Three-Port Isolated INSTRUMENTATION AMPLIFIER

## FEATURES

- RATED
  1500Vrms Continuous
  2500Vrms for One Minute
  100% Tested for Partial Discharge
- GAINS OF 1 TO 10,000
- LOW NONLINEARITY: ±0.05% typ
- LOW INPUT BIAS CURRENT: ±10nA max
- LOW INPUT OFFSET VOLTAGE
- INPUTS PROTECTED TO ±40V
- BIPOLAR OPERATION $V_O$ = ±10V
- SYNCHRONIZATION CAPABILITY
- 28-PIN PLASTIC DIP: 0.6" Wide

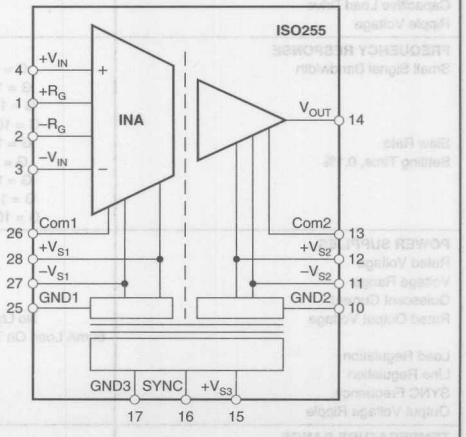
## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer Isolator, Thermocouple Isolator, RTD Isolator, Pressure Bridge Isolator, Flow Meter Isolator
- POWER MONITORING
- MEDICAL INSTRUMENTATION
- ANALYTICAL MEASUREMENTS
- BIOMEDICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT
- GROUND LOOP ELIMINATION

## DESCRIPTION

ISO255 is a precision three-port isolated instrumentation amplifier incorporating a novel duty cycle modulation-demodulation technique and has excellent accuracy. Internal input protection can withstand up to ±40V input differential without damage. The signal is transmitted digitally across a differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity. This results in excellent reliability and good high frequency transient immunity across the barrier. The DC/DC converter, amplifier and barrier capacitors are housed in a plastic DIP.

A power supply range of 11V to 18V makes this amplifier ideal for a wide range of applications.





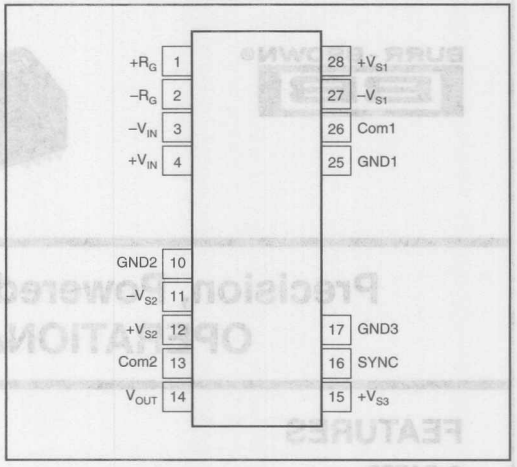

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# SPECIFICATIONS

At $T_A$ = +25°C, $V_{S3}$ = 15V, $R_L$ = 2kΩ, and 220nF capacitors on all generated supplies, unless otherwise noted.

| PARAMETER | CONDITIONS | ISO255P MIN | ISO255P TYP | ISO255P MAX | UNITS |
|---|---|---|---|---|---|
| **ISOLATION** | | | | | |
| Voltage Rated Continuous: | | | | | |
| AC | $T_{MIN}$ to $T_{MAX}$ | 1500 | | | Vrms |
| 100% Test (AC 50Hz) | 1s; Partial Discharge ≤ 5pC | 2500 | | | Vrms |
| Rated One Min | | 2500 | | | Vrms |
| Isolation-Mode Rejection | | | | | |
| DC | | | 120 | | dB |
| AC 50Hz | 1500Vrms | | 95 | | dB |
| Barrier Impedance | | | $10^{14}$ \|\| 2 | | Ω \|\| pF |
| Leakage Current | VISO = 240Vrms, 50Hz | | 1.4 | 2 | μArms |
| **GAIN** | | | | | |
| Gain Equation | | | 1 + 50kΩ/$R_G$ | | V/V |
| Gain Error | G = 1 | | 0.15 | ±0.35 | % |
| | G = 10 | | 0.15 | | |
| | G = 100 | | 0.15 | ±0.95 | % |
| | G = 1000 | | 0.2 | | |
| Gain vs Temperature | G = 1 | | ±50 | | ppm/°C |
| | G = 10 | | ±50 | | ppm/°C |
| | G = 100 | | ±50 | | ppm/°C |
| | G = 1000 | | ±50 | | ppm/°C |
| Nonlinearity | G = 1 | | ±0.05 | ±0.102 | % |
| | G = 10 | | ±0.05 | | |
| | G = 100 | | ±0.05 | ±0.104 | % |
| | G = 1000 | | ±0.05 | | |
| **INPUT OFFSET VOLTAGE** | | | | | |
| Initial Offset | | | | ± (0.125 + 101/G) | mV |
| vs Temperature | | | ± (1 + 520/G) | | μV/°C |
| CMRR | | | 90 | | dB |
| vs Supply | | | 1 | | mV/V |
| **INPUT** | | | | | |
| Voltage Range | | ±10 | | | V |
| Bias Current | | | | ±10 | nA |
| vs Temperature | | | ±40 | | pA/°C |
| Offset Current | | | | ±10 | nA |
| vs Temperature | | | ±40 | | pA/°C |
| **OUTPUT** | | | | | |
| Voltage Range | | ±10 | | | V |
| Current Drive | | ±5 | | | mA |
| Capacitive Load Drive | | | 0.1 | | μF |
| Ripple Voltage | | | 25 | | mVp-p |
| **FREQUENCY RESPONSE** | | | | | |
| Small Signal Bandwidth | G = 1 | | 50 | | kHz |
| | G = 10 | | 50 | | kHz |
| | G = 100 | | 30 | | kHz |
| | G = 1000 | | 4 | | kHz |
| Slew Rate | G = 10 | | 0.2 | | V/μs |
| Settling Time, 0.1% | G = 1 | | 20 | | μs |
| | G = 10 | | 20 | | μs |
| | G = 100 | | 30 | | μs |
| | G = 1000 | | 240 | | μs |
| **POWER SUPPLIES** | | | | | |
| Rated Voltage | | | 15 | | V |
| Voltage Range | | 11 | | 18 | V |
| Quiescent Current | | 25 | 40 | 55 | mA |
| Rated Output Voltage | No Load | 13 | 14.5 | | V |
| | 50mA Load On Two Supplies | 12 | 13.2 | 16 | V |
| Load Regulation | | | 28 | | mV/mA |
| Line Regulation | | | 1 | | V/V |
| SYNC Frequency | | 1 | | 1.4 | MHz |
| Output Voltage Ripple | | | 50 | | mV |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –40 | | 85 | °C |
| Storage | | –40 | | 85 | °C |

| | |
|---|---|
| Supply Voltage | +18V |
| $V_{IN}$, Analog Input Voltage Range | ±40V |
| Com1 to GND1 | ±1V |
| Com2 to GND2 | ±1V |
| Continuous Isolation Voltage: | 1500Vrms |
| | 2500Vrms one min |
| IMV, dv/dt | 20kV/µs |
| Junction Temperature | 150°C |
| Storage Temperature | –40°C to +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short Duration | Continuous to Common |




## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| ISO255P | 28-Pin Plastic DIP | 335 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



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# ISO256

www.burr-brown.com/databook/ISO256.html

# Precision, Powered, Three-Port Isolated OPERATIONAL AMPLIFIER

## FEATURES

- RATED
  1500Vrms Continuous
  2500Vrms for One Minute
- 100% TESTED FOR PARTIAL DISCHARGE
- LOW NONLINEARITY: ±0.05% typ
- LOW INPUT BIAS CURRENT: ±5nA max
- INPUTS PROTECTED TO ±30V
- BIPOLAR OPERATION $V_O$ = ±10V
- SYNCHRONIZATION CAPABILITY
- 28-PIN PLASTIC DIP: 0.6" Wide

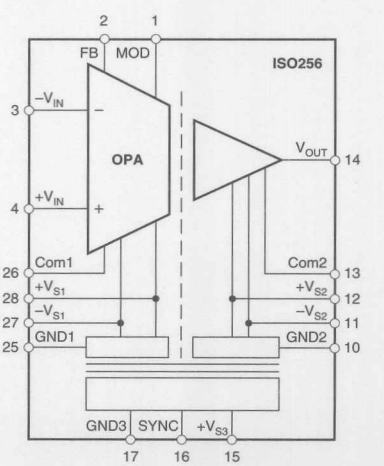
## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer Isolator, Thermocouple Isolator, RTD Isolator, Pressure Bridge Isolator, Flow Meter Isolator
- POWER MONITORING
- MEDICAL INSTRUMENTATION
- ANALYTICAL MEASUREMENTS
- BIOMEDICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT
- GROUND LOOP ELIMINATION

## DESCRIPTION

ISO256 is a precision three-port isolation operational amplifier incorporating an uncommitted operational amplifier for input conditioning and a novel duty cycle modulation-demodulation technique which has excellent accuracy. Internal input protection can withstand up to ±30V input differential without damage. The signal is transmitted digitally across a differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity. This results in excellent reliability and good high frequency transient immunity across the barrier. The DC/DC converter, amplifier and barrier capacitors are housed in a plastic DIP.

A power supply range of 11V to 18V makes this amplifier ideal for a wide range of applications.




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# SPECIFICATIONS

At $T_A$ = +25°C, $V_{S3}$ = 15V, $R_L$ = 2kΩ, and 220nF capacitors on all generated supplies, unless otherwise noted.

| PARAMETER | CONDITIONS | ISO256P MIN | ISO256P TYP | ISO256P MAX | UNITS |
|---|---|---|---|---|---|
| **ISOLATION** | | | | | |
| Voltage Rated Continuous: | | | | | |
| AC | $T_{MIN}$ to $T_{MAX}$ | 1500 | | | Vrms |
| 100% Test (AC 50Hz) | 1s; Partial Discharge ≤ 5pC | 2500 | | | Vrms |
| Rated One Minute | | 2500 | | | Vrms |
| Isolation-Mode Rejection | | | | | |
| DC | | | 120 | | dB |
| AC 50Hz | 1500Vrms | | 95 | | dB |
| Barrier Impedance | | | $10^{14}$ ‖ 2 | | Ω ‖ pF |
| Leakage Current | VISO = 240Vrms, 50Hz | | 1.4 | 2 | μArms |
| **GAIN ISO AMP** | | | | | |
| Gain Error | G = 1 | | 0.15 | ±0.3 | % |
| Gain vs Temperature | G = 1 | | ±50 | | ppm/°C |
| Nonlinearity | G = 1 | | 0.046 | ±0.1 | % |
| **INPUT OFFSET VOLTAGE OP AMP** | | | | | |
| Initial Offset | | | 60 | | μV |
| vs Temperature | | | ± 1.2 | | μV/°C |
| vs Supply | | | 3 | | μV/V |
| CMRR | | | 115 | | dB |
| **INPUT OP AMP** | | | | | |
| Voltage Range | | ±10 | | | V |
| Bias Current | | | ±5 | | nA |
| vs Temperature | | | ±60 | | pA/°C |
| Offset Current | | | | ±5 | nA |
| vs Temperature | | | ±85 | | pA/°C |
| **INPUT ISO AMP** | | | | | |
| Initial Offset | | | ±50 | ±100 | mV |
| vs Supply | | | 1 | | mV/V |
| Input Resistance | | | 200 | | kΩ |
| **OUTPUT ISO AMP** | | | | | |
| Voltage Range | | ±10 | | | V |
| Current Drive | | ±5 | | | mA |
| Capacitive Load Drive | | | 0.1 | | μF |
| Ripple Voltage | | | 10 | | mVp-p |
| **FREQUENCY RESPONSE** | | | | | |
| Small Signal Bandwidth | G = 1 | | 20 | | kHz |
| | G = 10 | | 20 | | kHz |
| | G = 100 | | 4 | | kHz |
| | G = 1000 | | 7 | | kHz |
| Slew Rate | | | 0.2 | | V/μs |
| Settling Time, 0.1% | G = 1 | | 100 | | μs |
| | G = 10 | | 400 | | μs |
| | G = 100 | | 600 | | μs |
| | G = 1000 | | 950 | | μs |
| **POWER SUPPLIES** | | | | | |
| Rated Voltage | | | 15 | | V |
| Voltage Range | | 11 | | 18 | V |
| Quiescent Current | | 25 | 40 | 55 | mA |
| Rated Output Voltage | No Load | 13 | 14.5 | | V |
| | 50mA Load On Two Supplies | 12 | 13.2 | 16 | V |
| Load Regulation | | | 28 | | mV/mA |
| Line Regulation | | | 1 | | V/V |
| SYNC Frequency | | | 1 to 1.4 | | MHz |
| Output Voltage Ripple | | | 50 | | mV |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –40 | | 85 | °C |
| Storage | | –40 | | 85 | °C |

## ABSOLUTE MAXIMUM RATINGS

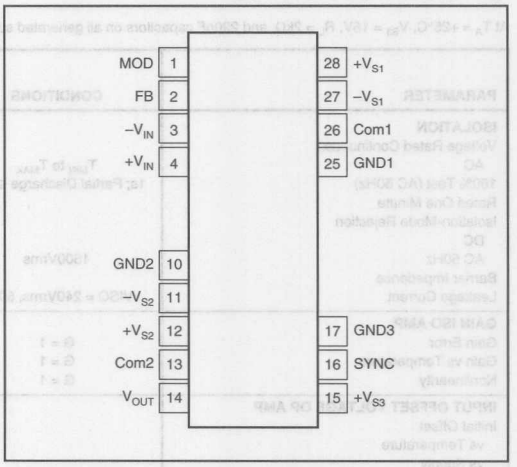
| | |
|---|---|
| Supply Voltage | +18V |
| $V_{IN}$, Analog Input Voltage Range | ±40V |
| Com1 to GND1 | ±1V |
| Com2 to GND2 | ±1V |
| Continuous Isolation Voltage: | 1500Vrms |
| | 2500Vrms one min |
| IMV, dv/dt | 20kV/µs |
| Junction Temperature | 150°C |
| Storage Temperature | –40°C to +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short Duration | Continuous to Common |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION



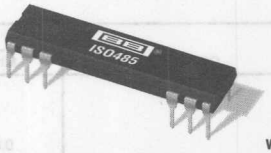

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ISO256P | 28-Pin Plastic DIP | 335 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# ISO485

www.burr-brown.com/databook/ISO485.html

# Isolated RS-485 DIFFERENTIAL BUS TRANSCEIVER

## FEATURES

- RS-485 AND RS-422 COMPATIBLE
- 100% TESTED FOR HIGH-VOLTAGE BREAKDOWN
- RATED 1500Vrms
- SINGLE-WIDE 24-PIN PLASTIC DIP
- EASY TO USE
- LOW POWER: 180mW typ at 5Mbit/s

## APPLICATIONS

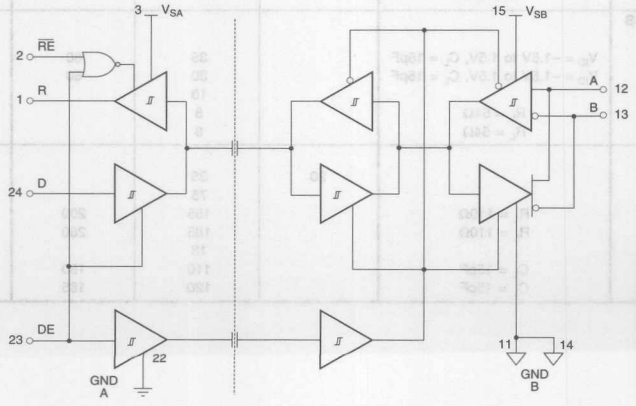
- MULTIPOINT DATA TRANSMISSION ON LONG BUS LINES IN NOISY ENVIRONMENTS

## DESCRIPTION

The ISO485 differential, isolated bus transceiver uses Burr-Brown's capacitively coupled isolation technology to provide high-speed, low cost bus isolation. The ISO485 is designed for bi-directional data communication on multipoint bus transmission lines and meets EIA Standard RS-485 as well as EIA Standard RS-422A requirements.

The ISO485 uses high voltage 0.4pF capacitors instead of the LED and photodetector which are used in equivalent optocoupler solutions. As a consequence the part count of the isolated RS-485 channel is reduced from multiple optocoupler channels, an RS-485 transceiver chip and supporting circuitry to one ISO485. The capacitors in the ISO485 provide a high voltage barrier, 1500Vrms and greatly reduce current spikes on the power line.

The ISO485 combines a 3-state differential line driver and a differential-input line receiver both of which operate from a single 5V power supply. The driver differential outputs and the receiver differential input/output bus ports are designed to offer minimum loading to the bus whenever the driver is disabled or $V_S$ = 0V.




**TRUTH TABLE**

| DE | $\overline{RE}$ | RS-485 BUS |
|---|---|---|
| 0 | 0 | $R_X$ |
| 0 | 1 | HIGH Z |
| 1 | 0 | HIGH Z |
| 1 | 1 | $T_X$ |

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

## SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = 5V, unless otherwise specified.

| PARAMETER | CONDITION | ISO485P MIN | ISO485P TYP | ISO485P MAX | UNITS |
|---|---|---|---|---|---|
| **DRIVER DC CHARACTERISTICS** | | | | | |
| Input Voltage | | | | | |
| High MIN | | | | 2 | V |
| Low MAX | | 0.8 | | | V |
| Input Current | | | | | |
| High-Level | $V_{IN}$ = 2.4V | | | ±1 | µA |
| Low-Level | $V_{IN}$ = 0.4V | | | ±1 | µA |
| Output Voltage | $I_{OUT}$ = 0 | 0 | | 5 | V |
| Differential Output Voltage | $I_{OA} - I_{OB} = 0$ | 1.5 | | 5 | V |
| | $R_{LOAD}$ = 100Ω | 2 | 2.5 | 5 | V |
| | $R_{LOAD}$ = 54Ω | 1.5 | 2.5 | 5 | V |
| Change In Magnitude of Differential Output Voltage | $R_{LOAD}$ = 54Ω or 100Ω | | | ±0.5 | V |
| Common-Mode Output Voltage | $R_{LOAD}$ = 54Ω or 100Ω | | | 3 | V |
| Change in Magnitude of Common-Mode Output Voltage | $R_{LOAD}$ = 54Ω or 100Ω | | | ±0.2 | V |
| Output Current | $V_{OUT}$ = 7V, output disabled | | | 1 | mA |
| | $V_{OUT}$ = –7V, output disabled | | | –0.8 | mA |
| Short-Circuit Output Current (1 sec max) | $V_{OUT}$ = –7V | | –250 | | mA |
| | $V_{OUT}$ = 0V | | –150 | | mA |
| | $V_{OUT} = V_S$ | | 250 | | mA |
| | $V_{OUT}$ = 12V | | 250 | | mA |
| **DRIVER SWITCHING CHARACTERISTICS** | | | | | |
| Propagation Delay Time, Low-to-High Level Output | $R_{LOAD}$ = 54Ω | | | 60 | ns |
| Propagation Delay Time, High-to-Low Level Output | $R_{LOAD}$ = 54Ω | | | 60 | ns |
| Input to Output Propagation Delay Skew | $R_{LOAD}$ = 54Ω | | 10 | | ns |
| Output Rise Time | $R_{LOAD}$ = 54Ω | | 10 | | ns |
| Output Fall Time | $R_{LOAD}$ = 54Ω | | 10 | | ns |
| **RECEIVER DC CHARACTERISTICS** | | | | | |
| Differential-Input-Threshold Voltage | | | | | |
| High | $V_{OUT}$ = 2.7V, $I_{OUT}$ = –0.4mA | | | 0.2 | V |
| Low | $V_{OUT}$ = 0.5V, $I_{OUT}$ = 8mA | –0.2 | | | V |
| Hysteresis | | | 70 | | mV |
| High-Level Output Voltage | $V_{ID}$ = 200mV, $I_{OH}$ = 400µA | 2.4 | | | V |
| Low-Level Output Voltage | $V_{ID}$ = 200mV, $I_{OL}$ = 8mA | | | 0.4 | V |
| High-Impedance-State Output Current | $V_{OUT}$ = 1.4V | | | ±1 | µA |
| Line Input Current | $V_{IN}$ = 12V, other output = 0V | | 0.7 | | mA |
| | $V_{IN}$ = –7V, other output = 0V | | –0.6 | | mA |
| Enable-Input Current | | | | | |
| High | $V_{IH}$ = 2.7V | | | 1 | µA |
| Low | $V_{IL}$ = 0.4V | | | 1 | µA |
| Input Resistance | | 12 | | | kΩ |
| Short-Circuit Output Current | 1 sec max | | 40 | | mA |
| **RECEIVER SWITCHING CHARACTERISTICS** | | | | | |
| Propagation Delay Time, Low-to-High Level Output | $V_{ID}$ = –1.5V to 1.5V, $C_L$ = 15pF | | 35 | 60 | ns |
| High-to-Low Level Output | $V_{ID}$ = –1.5V to 1.5V, $C_L$ = 15pF | | 30 | 60 | ns |
| Input to Output Propagation Delay Skew | | | 10 | | ns |
| Output Rise Time | $R_L$ = 54Ω | | 8 | | ns |
| Output Fall Time | $R_L$ = 54Ω | | 8 | | ns |
| **TRANSCEIVER SPECIFICATIONS** | | | | | |
| Maximum Data Rate | | 20 | 35 | | Mbits/s |
| Propagation Delay Driver to Receiver | | | 75 | | ns |
| Driver Output Enable Time | $R_L$ = 110Ω | | 155 | 200 | ns |
| Driver Output Disable Time | $R_L$ = 110Ω | | 185 | 280 | ns |
| Propagation Delay Receiver to Driver | | | 13 | | ns |
| Receiver Output Enable Time | $C_L$ = 15pF | | 110 | 180 | ns |
| Receiver Output Disable Time | $C_L$ = 15pF | | 120 | 185 | ns |

## SPECIFICATIONS (CONT)

At $T_A$ = +25°C, $V_S$ = 5V, unless otherwise specified.

| PARAMETER | CONDITION | ISO485P MIN | ISO485P TYP | ISO485P MAX | UNITS |
|---|---|---|---|---|---|
| **TRANSCEIVER SPECIFICATIONS (CONT)** | | | | | |
| Supply Voltage | | | | | |
| $V_S$A | | 3 | 5 | 5.5 | V |
| $V_S$B | | 4.75 | 5 | 5.25 | V |
| Supply Current | DE RE RS-485 BUS | | | | |
| $V_S$A | 0 0 Rx | | | 5 | mA |
| $V_S$A | 0 1 HIGH Z | | | 0.4 | mA |
| $V_S$A | 1 0 HIGH Z | | | 0.4 | mA |
| $V_S$A | 1 1 Tx | | | 0.4 | mA |
| $V_S$B | 0 0 Rx | | | 55 | mA |
| $V_S$B | 0 1 HIGH Z | | | 55 | mA |
| $V_S$B | 1 0 HIGH Z | | | 51 | mA |
| $V_S$B | 1 1 Tx | | | 51 | mA |
| **RECOMMENDED OPERATING CONDITIONS** | | | | | |
| Voltage at Any Bus Terminal | (separately or common-mode) | –7 | | 12 | V |
| High-Level Driver Input Voltage | | 2 | | | V |
| Low-Level Driver Input Voltage | | | | 0.8 | V |
| Differential Receiver Input Voltage | | | | ±12 | V |
| Output Current High-Level | | | | | |
| | Driver | | | –60 | mA |
| | Receiver | | | –400 | µA |
| Output Current Low-Level | | | | | |
| | Driver | | | 60 | mA |
| | Receiver | | | 8 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –40 | | 85 | °C |
| Storage | | –40 | | 125 | °C |
| **ISOLATION PARAMETERS** | | | | | |
| Rated Voltage, Continuous | 50Hz | 1500 | | | Vrms |
| Partial Discharge, 100% Test(1) | 1s, 5pC | 2400 | | | Vrms |
| Creepage Distance (External) DIP = "P" Package | | | 16 | | mm |
| Internal Isolation Distance | | | 0.10 | | mm |
| Isolation Voltage Transient Immunity(2) | | | 1.6 | | kV/µs |
| Barrier Impedance | | | $> 10^{14}$ ‖ 7 | | Ω ‖ pF |
| Leakage Current | 240Vrms, 60Hz | | 0.6 | | µArms |

NOTES: (1) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pC. (2) The voltage rate-of-change across the isolation barrier that can be sustained without data errors.

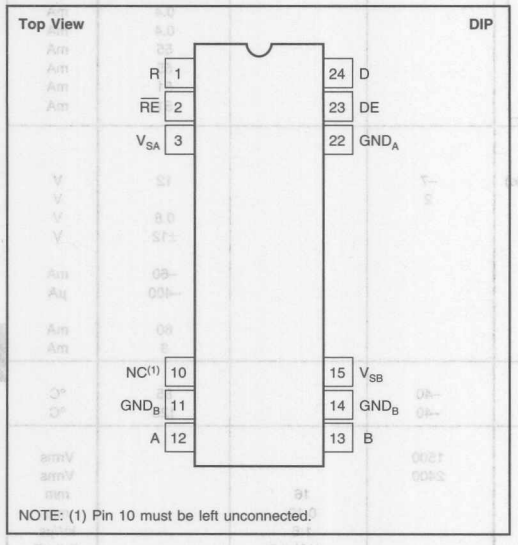


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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltages, $V_S$ | 5.5V |
| Voltage at any bus terminal | –10 to 15V |
| Enable Input Voltage | 0 to $V_{CC}$ + 0.5V |
| Continuous total dissipation at 25°C free-air temp. | 750mW |
| Lead solder temperature, 260°C for 10s, 1.6mm below seating plane | 300°C |
| Junction Temperature | 150°C |
| Package thermal transfer, $\theta_{JA}$ | 75°C/W |

## PIN CONFIGURATION




NOTE: (1) Pin 10 must be left unconnected.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ISO485P | 24-Pin Single-Wide DIP | 243-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN ASSIGNMENTS

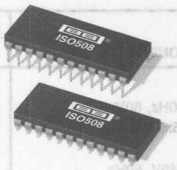
| PIN # | NAME | DESCRIPTION |
|---|---|---|
| 1 | R | Data Received From Transmission Line |
| 2 | $\overline{RE}$ | Receive Switch Controlling Receiving Of Data |
| 3 | $V_{SA}$ | +5V Supply Pin For Side A |
| 10 | NC | This Pin MUST Be Left Unconnected |
| 11 | $GND_B$ | Ground Pin For Side B. Also Connected To Pin 14 |
| 12 | A | Data, Driver Out/Receiver In |
| 13 | B | Data, Driver Out/Receiver In |
| 14 | $GND_B$ | Ground Pin For Side B. Also Connected To Pin 11 |
| 15 | $V_{SB}$ | +5V Supply Pin For Side B |
| 22 | $GND_A$ | Ground Pin For Side A |
| 23 | DE | Driver Switch Controlling Output Of Data |
| 24 | D | Data To Be Transmitted |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# ISO508

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www.burr-brown.com/databook/ISO508.html

# Bi-Directional ISOLATED DIGITAL COUPLERS

## FEATURES

- LOW POWER CONSUMPTION: 3mW per Channel
- 1500Vrms ISOLATION

## APPLICATIONS

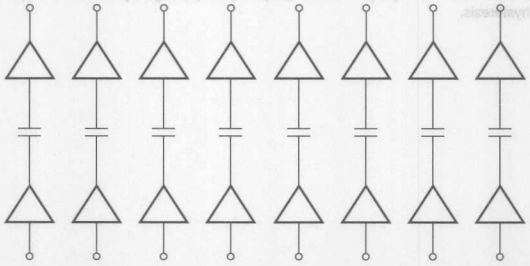
- PARALLEL ADCs/DACs
- DIGITAL INTERFACES
- DIGITAL TRANSMISSION
- GROUND-LOOP ISOLATION

## DESCRIPTION

ISO508 is an 8-channel, isolated, digital coupler based on the Burr-Brown capacitive barrier technology. The ISO508 has additional circuitry to ensure DC accuracy and overcome the edge-sensitive nature of normal capacitive devices even on power-up conditions. The novel circuitry involved will detect a transient interruption and restore the correct output condition, should that be necessary.

ISO508 will transfer an 8-bit word at rates up to 2Mwords/s without the skew problems associated in implementing this function with optocouplers. The ISO508 is available in 24-pin PDIP or 24-pin Gullwing packages. Both are specified for operation from –40°C to +85°C.

ISO508



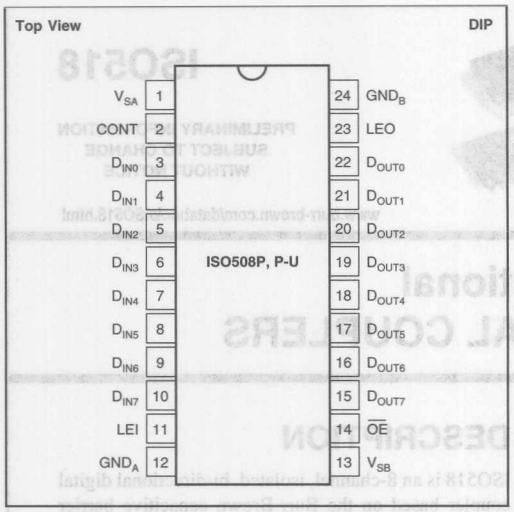


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| PARAMETER | | CONDITIONS | ISO508P, P-U MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **ISOLATION** | | | | | | |
| Rated Voltage, Continuous | $V_{ISO}$ | 50Hz, 60Hz | 1500 | | | Vrms |
| Partial Discharge Voltage | | 1s, 5x5pC/cycle[1] | 2500 | | | Vrms |
| Barrier Impedance | | | | $>10^{14}$, 10 | | |
| Leakage Current | | 240V, 60Hz | | 1 | | |
| | | 2500V, 50Hz | | | 8 | |
| Creepage Distance | | PDIP = "P" Package | | 11 | | mm |
| | | PDIP = "P" Package | | 0.1 | | mm |
| Transient Recovery Time | | 5kV/µs Edge | | | 1 | |
| **DC CHARACTERISTICS** | | | | | | |
| High Level Input Voltage | $V_{IH}$ | See Note 2 | 2 | | | V |
| Low Level Input Voltage | $V_{IL}$ | See Note 2 | | | 0.8 | V |
| Input Leakage Current | $I_L$ | | | 5 | | nA |
| Input Capacitance | $C_{IN}$ | | | 5 | | pF |
| High Level Output Voltage | $V_{OH}$ | $I_{OH}$ = 6mA | $V_S - 1$ | | | V |
| Low Level Output Voltage | $V_{OL}$ | $I_{OL}$ = 6mA | | | 0.4 | V |
| Output Short-Circuit Current | $I_{OS}$ | 1 second, max | | 30 | | mA |
| **TIMING** | | | | | | |
| LE Width (LOW) | $t_{WL}$ | | 100 | | | ns |
| LE Width (HIGH) | $t_{WH}$ | | 15 | | | ns |
| Data Set-Up to LEI | $t_{SU}$ | LEI HI to LO | 10 | | | ns |
| Data Hold from LEI | $t_H$ | LEI HI to LO | 20 | | | ns |
| Propagation Delay | $t_{PD}$ | Data In to Data Out | | | 1000 | ns |
| | | LEI LOW to Data Out (Sync) | | | 500 | ns |
| Data Output Delay | $t_{OD}$ | LEO HI to Data Out Change | | | 25 | ns |
| Output Rise and Fall Time | $t_{RF}$ | 10% to 90%, $C_L$ = 50pF | | 9 | 14 | ns |
| Output Enable | $t_{OE}$ | OE to Data Valid HI or LO | | | 25 | ns |
| Output Disable | $t_{DIS}$ | OE to Data Hi-Z | | | 10 | ns |
| Max Data Transfer Rate | | | 2 | | | Mw/s |
| **POWER** | | | | | | |
| Supply Voltage | $V_{SA}$, $V_{SB}$ | Either Side | 4.5 | | 5.5 | V |
| Supply Current | $I_{SA}$ | Transmit Side DC | | 0.1 | 1 | mA |
| | | Transmit Side DC Max Rate | | 16 | | mA |
| Supply Current | $I_{SB}$ | Receive Side DC | | 8 | 12 | mA |
| | | Receive Side Max Rate | | 18 | | mA |
| **TEMPERATURE RANGE** | | | | | | |
| Operating | | | –40 | | +85 | °C |
| Storage | | | –40 | | +125 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | 75 | | °C/W |

NOTES: (1) All devices receive a 1s test. Failure criterion is > 5pC pulses of ≥ 5pC per cycle. (2) Logic inputs are HCT-type and thresholds are a function of power supply voltage with approximately 400mV hysteresis.

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| NAME | FUNCTION |
|---|---|
| $D_{IN}$ (0 - 7) | Input Data Bus. Inputs are TTL compatible. |
| $D_{OUT}$ (0 - 7) | Output Data Bus. Outputs are TTL compatible. |
| LEI | Input Latch Enable. Latch enable signal for the input data buffer. A logic LOW will latch the input data preventing further changes being made before data transmission across the barrier. |
| LEO | Output Latch Enable. Latch enable signal for the output data buffer. A logic LOW will latch the internal data to the output pins and prevent further changes to the output data. |
| CONT | Synchronous/Asynchronous Mode Select. |
| $\overline{OE}$ | Output Tri-State Enable. Makes the output data pins high impedance to allow multiple parallel access to the data bus. A logic HIGH will make $D_{OUT}$ (0 - 7) high impedance. A logic LOW will allow $D_{OUT}$ (0 - 7) to be driven to the correct logic level. |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage: $V_{SA}$ | –0.5V to +6V |
| $V_{SB}$ | –0.5V to +6V |
| Continuous Isolation Voltage | 1500Vrms |
| Storage Temperature | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +260°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| ISO508P | 24-Pin Plastic DIP | 167 |
| ISO508P-U | 24-Pin Gullwing Surface Mount | 167-4 |

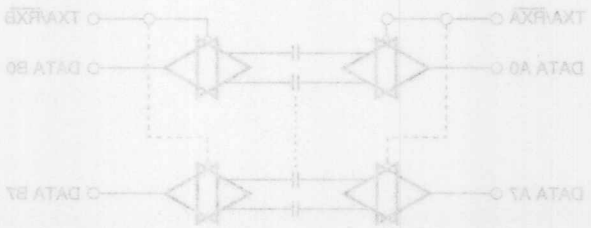
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

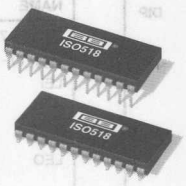
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.





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# ISO518

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# Bi-Directional ISOLATED DIGITAL COUPLERS

## FEATURES

- LOW POWER CONSUMPTION: 3mW per Channel
- 1500Vrms ISOLATION

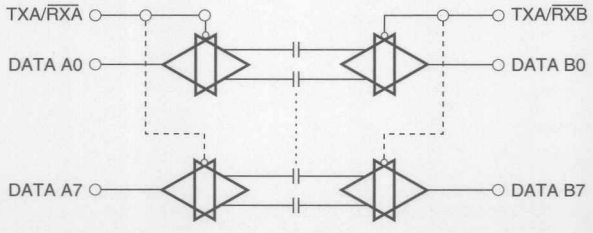
## APPLICATIONS

- PARALLEL ADCs/DACs
- DIGITAL INTERFACES
- DIGITAL TRANSMISSION
- GROUND-LOOP ISOLATION

## DESCRIPTION

ISO518 is an 8-channel, isolated, bi-directional digital coupler based on the Burr-Brown capacitive barrier technology. The ISO518 has additional circuitry to ensure DC accuracy and overcome the edge-sensitive nature of normal capacitive devices even on power-up conditions. The novel circuitry involved will detect a transient interruption and restore the correct output condition, should that be necessary.

ISO518 will transfer an 8-bit word at rates up to 2Mwords/s without the skew problems associated in implementing this function with optocouplers. The ISO518 is available in 24-pin PDIP or 24-pin Gullwing packages. Both are specified for operation from –40°C to +85°C.




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## SPECIFICATIONS—PRELIMINARY

At $T_A$ = +25°C, and $V_S$ = +5V, unless otherwise noted.

| PARAMETER | | CONDITIONS | ISO518P, P-U MIN | ISO518P, P-U TYP | ISO518P, P-U MAX | UNITS |
|---|---|---|---|---|---|---|
| **ISOLATION** | | | | | | |
| Rated Voltage, Continuous | $V_{ISO}$ | 50Hz, 60Hz | 1500 | | | Vrms |
| Partial Discharge Voltage | | 1s, 5x5pC/cycle(1) | 2500 | | | Vrms |
| Barrier Impedance | | | | $>10^{14}$ \|\| 10 | | Ω/pF |
| Leakage Current | | 240V, 60Hz | | 1 | | µA |
| | | 2500V, 50Hz | | | 8 | |
| Creepage Distance | | PDIP = "P" Package | | 11 | | mm |
| Internal Isolation Distance | | PDIP = "P" Package | | 0.1 | | mm |
| Transient Recovery Time | | 5kV/µs Edge | | | 1 | µs |
| **DC CHARACTERISTICS** | | | | | | |
| High Level Input Voltage | $V_{IH}$ | See Note 2 | 2 | | | V |
| Low Level Input Voltage | $V_{IL}$ | See Note 2 | | | 0.8 | V |
| Input Leakage Current | $I_L$ | | | 5 | | nA |
| Input Capacitance | $C_{IN}$ | | | 5 | | pF |
| High Level Output Voltage | $V_{OH}$ | $I_{OH}$ = 6mA | $V_S$ –1 | | | V |
| Low Level Output Voltage | $V_{OL}$ | $I_{OL}$ = 6mA | | | 0.4 | V |
| Output Short-Circuit Current | $I_{OS}$ | 1 second, max | | 30 | | mA |
| **TIMING** | | | | | | |
| LE Width (LOW) | $t_{WL}$ | | 100 | | | ns |
| LE Width (HIGH) | $t_{WH}$ | | 15 | | | ns |
| Data Set-Up to LEI | $t_{SU}$ | LEI HI to LO | 10 | | | ns |
| Data Hold from LEI | $t_H$ | LEI HI to LO | 20 | | | ns |
| Propagation Delay | $t_{PD}$ | LEI LOW to Data Out (Sync) | | | 1000 | ns |
| | | LEO HI to Data Out Change | | | 500 | ns |
| Data Output Delay | $t_{OD}$ | | | | 25 | ns |
| Output Rise and Fall Time | $t_{RF}$ | 10% to 90%, $C_L$ = 50pF | | 9 | 14 | ns |
| Output Enable | $t_{EN}$ | OE to Data Valid HI or LO | | | 25 | ns |
| Output Disable | $t_{DIS}$ | OD to Data Hi-Z | | | 10 | ns |
| Max Data Transfer Rate | | | 2 | | | Mw/s |
| Mode Switch | $t_{RT}$ | Receive to Transmit | | 15 | | ns |
| Mode Switch | $t_{TR}$ | Transmit to Receive | | 80 | | ns |
| **POWER** | | | | | | |
| Supply Voltage | $V_{SA}$, $V_{SB}$ | Either Side | 4.5 | | 5.5 | V |
| Supply Current | $I_{SA}$ | Transmit Side DC | | 0.1 | 1 | mA |
| | | Transmit Side DC Max Rate | | 16 | | mA |
| Supply Current | $I_{SB}$ | Receive Side DC | | 8 | 12 | mA |
| | | Receive Side Max Rate | | 18 | | mA |
| **TEMPERATURE RANGE** | | | | | | |
| Operating | | | –40 | | +85 | °C |
| Storage | | | –40 | | +125 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | +75 | | °C/W |

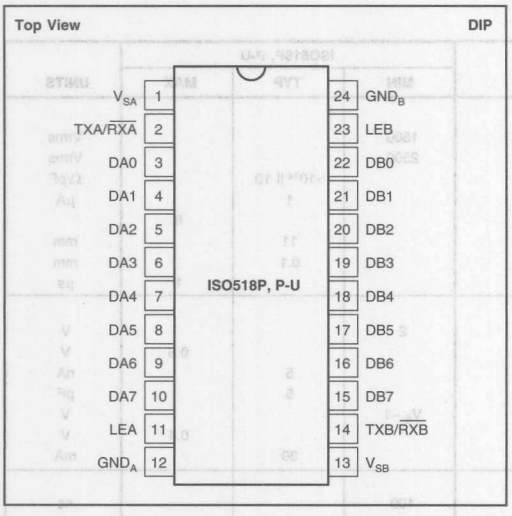
NOTES: (1) All devices receive a 1s test. Failure criterion is > 5pC pulses of ≥ 5pC per cycle. (2) Logic inputs are HCT-type and thresholds are a function of power supply voltage with approximately 400mV hysteresis.



The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN CONFIGURATION

Top View DIP




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage: $V_{SA}$ | –0.5V to +6V |
| $V_{SB}$ | –0.5V to +6V |
| Continuous Isolation Voltage | 1500Vrms |
| Storage Temperature | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +260°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ISO518P | 24-Pin Plastic DIP | 167 |
| ISO518P-U | 24-Pin Gullwing Surface Mount | 167-4 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## FUNCTIONAL DESCRIPTION

| NAME | FUNCTION |
|---|---|
| DA (0 - 7) | Data Bus A. The logic levels on thes pins are transmitted to, or received from the corresponding pins on data bus B. |
| DB (0 -7) | Data Bus B. The logic levels on these pins are transmitted to, or received from the corresponding pins on data bus A. |
| LEA(1) | Latch Enable A. Latch enable signal for the A data buffer. |
| LEB(1) | Latch Enable B. Latch enable signal for the B data buffer. |
| TX/$\overline{RXA}$(2) | Transmit/Receive Control for Side A. |
| TX/$\overline{RXB}$(2) | Transmit/Receive Control for Side B. |

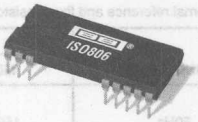
NOTES: (1) In transmit mode (TX/$\overline{RX}$ = 1), a logic 0 (LOW) will latch the input buffer data into the input register and initialize the transmission. A logic 0 (LOW) will latch the internal buffer data into the output register and prevent any further changes in the output data. A logic 1 (HIGH) will pass the internal buffer data to the output register and permit each new set of data to appear as soon as available after transmission. (2) A logic 1 (HIGH) will set that side to transmit mode and the same side's data bus to input mode. A logic 0 (LOW) will set that side to receive mode and the same side's data bus to output mode.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

BURR - BROWN®




# ISO806

www.burr-brown.com/databook/ISO806.html

# Isolated 12-Bit Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- 1500Vrms ISOLATION CONTINUOUS
- 25µS CONVERSION TIME
- 12-BIT SERIAL OUTPUT
- SINGLE +5V SUPPLY
- 28-PIN 0.6" PLASTIC DIP

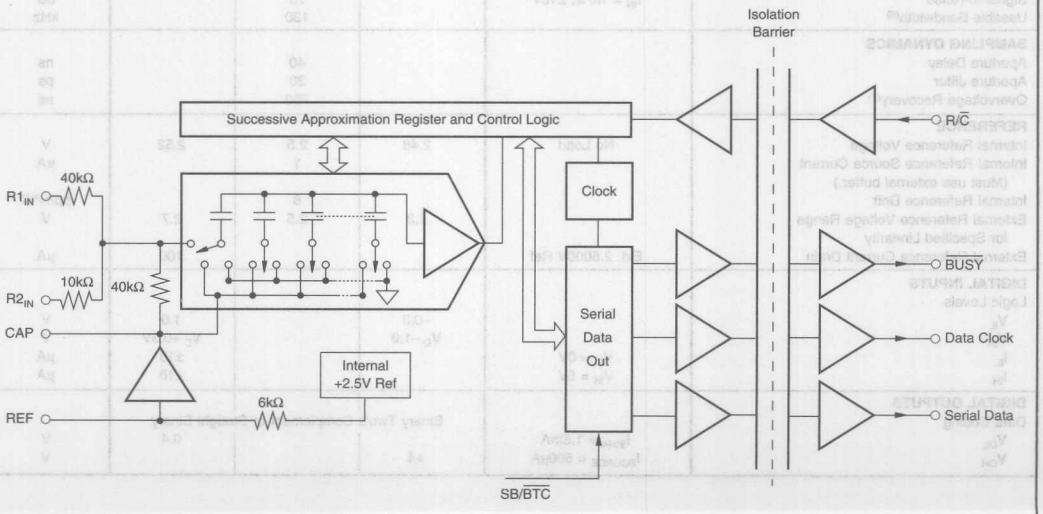
## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- PC-BASED DATA ACQUISITION TEST EQUIPMENT

## DESCRIPTION

The ISO806 is a low-power isolated sampling ADC using state-of-the-art CMOS structures and high voltage capacitors. The ISO806 contains a complete 12-bit capacitor based SAR, ADC with S/H, clock, reference, µP interface, serial out and galvanic isolation.

Laser-trimmed scaling resistors provide standard industrial input ranges including ±10V, ±5V, 0-5V, 0-4V. They are available in 28-pin 0.6" wide plastic DIP and are specified over the industrial temperature range of –40°C to +85°C.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 40kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference and fixed resistors shown in Figure 3b, unless otherwise specified.

| PARAMETER | CONDITIONS | ISO806P MIN | ISO806P TYP | ISO806P MAX | UNITS |
|---|---|---|---|---|---|
| **ISOLATION PARAMETERS** | | | | | |
| Rated Voltage, Continuous | 50Hz | 1500 | | | Vrms |
| Partial Discharge, 100% Test[8] | 1s, 5pC | 2500 | | | Vrms |
| Creepage Distance (External) DIP = "P" Package | | | 16 | | mm |
| Internal Isolation Distance | | | 0.10 | | mm |
| Barrier Impedance | | | $>10^{13}$ II 15 | | Ω II pF |
| Leakage Current[9] | 240Vrms, 60Hz | | | 1.7 | μArms |
| | 240Vrms, 50Hz | | | 1.4 | μArms |
| **RESOLUTION** | | | | 12 | Bit |
| **ANALOG INPUT** | | | | | |
| Voltage Ranges | | | ±10, 0 to +5, 0 to +4 | | V |
| Impedance | | | (See Table II) | | |
| Capacitance | | | 35 | | pF |
| **THROUGHPUT SPEED** | | | | | |
| Conversion Time | | | | 20 | μs |
| Complete Cycle | Acquire and Convert | | | 25 | μs |
| Throughput Rate | | 40 | | | kHz |
| **DC ACCURACY** | | | | | |
| Integral Linearity Error | | | ±0.15 | ±0.9 | LSB[1] |
| Differential Linearity Error | | | ±0.15 | ±0.9 | LSB |
| No Missing Codes | | | Guaranteed | | Bits |
| Transition Noise[2] | | | 0.1 | | LSB |
| Full Scale Error[3,4] | | | | ±0.5 | % |
| Full Scale Error Drift | | | ±7 | | ppm/°C |
| Full Scale Error Drift | Ext. 2.5000V Ref | | ±0.5 | | ppm/°C |
| Bipolar Zero Error[3] | ±10V Range | | | ±10 | mV |
| Bipolar Zero Error Drift | ±10V Range | | ±0.5 | | ppm/°C |
| Unipolar Zero Error[3] | 0V to 5V, 0V to 4V Ranges | | | ±3 | mV |
| Unipolar Zero Error Drift | 0V to 5V, 0V to 4V Ranges | | ±0.5 | | ppm/°C |
| Power Supply Sensitivity ($V_{DIG}$ = $V_{ANA}$ = $V_S$) | +4.75V < $V_S$ < +5.25V | | | ±0.5 | LSB |
| **AC ACCURACY** | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 1kHz, ±10V | | 90 | | dB[5] |
| Total Harmonic Distortion | $f_{IN}$ = 1kHz, ±10V | | –90 | | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 1kHz, ±10V | | 73 | | dB |
| Signal-to-Noise | $f_{IN}$ = 1kHz, ±10V | | 73 | | dB |
| Useable Bandwidth[6] | | | 130 | | kHz |
| **SAMPLING DYNAMICS** | | | | | |
| Aperture Delay | | | 40 | | ns |
| Aperture Jitter | | | 20 | | ps |
| Overvoltage Recovery[7] | | | 750 | | ns |
| **REFERENCE** | | | | | |
| Internal Reference Voltage | No Load | 2.48 | 2.5 | 2.52 | V |
| Internal Reference Source Current (Must use external buffer.) | | | 1 | | μA |
| Internal Reference Drift | | | 8 | | ppm/°C |
| External Reference Voltage Range for Specified Linearity | | 2.3 | 2.5 | 2.7 | V |
| External Reference Current Drain | Ext. 2.5000V Ref | | | 100 | μA |
| **DIGITAL INPUTS** | | | | | |
| Logic Levels | | | | | |
| $V_{IL}$ | | –0.3 | | 1.0 | V |
| $V_{IH}$ | | $V_D$ –1.0 | | $V_D$ +0.3V | V |
| $I_{IL}$ | $V_{IL}$ = 0V | | | ±10 | μA |
| $I_{IH}$ | $V_{IH}$ = 5V | | | ±10 | μA |
| **DIGITAL OUTPUTS** | | | | | |
| Data Coding | | Binary Two's Complement or Straight Binary | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | 0.4 | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500μA | +4 | | | V |

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# SPECIFICATIONS (CONT)

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 40kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference and fixed resistors shown in Figure 3b, unless otherwise specified.

| PARAMETER | CONDITIONS | ISO806P MIN | ISO806P TYP | ISO806P MAX | UNITS |
|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | |
| Specified Performance | | | | | |
| $V_{DIG1}$ | Must be ≤ $V_{ANA}$ | +4.75 | +5 | +5.25 | V |
| $V_{ANA}$ | | +4.75 | +5 | +5.25 | V |
| $V_{DIG2}$ | | +4.75 | | +5.25 | V |
| $I_{DIG1}$ | | | 4.2 | | mA |
| $I_{ANA}$ | | | 5.0 | | mA |
| $I_{DIG2}$ | | | 10.8 | | mA |
| Power Dissipation | $V_{ANA}$ = $V_{DIG}$ = 5V, $F_S$ = 40kHz | | 125 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified Performance | | –40 | | +85 | °C |
| Storage | | –65 | | +150 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| Plastic DIP | | | 75 | | °C/W |

NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 4.88mV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale input. (6) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage. (8) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pC. (9) Tested at 2500Vrms, 50Hz limit 10µA.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $R1_{IN}$ | ±25V |
| $R2_{IN}$ | ±25V |
| CAP | $V_{ANA}$ +0.3V to AGND2 –0.3V |
| REF | Indefinite Short to AGND2, Momentary Short to $V_{ANA}$ |
| Ground Voltage Differences: DGND and AGND1 | ±0.3V |
| DGND, AGND, and $GND_{ISO}$ | 1563Vrms |
| $V_{ANA}$ | 7V |
| $V_{DIG}$ to $V_{ANA}$ | +0.3V |
| $V_{DIG}$ | 7V |
| Digital Inputs | –0.3V to $V_{DIG}$ +0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ISO806P | Plastic DIP | 215-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

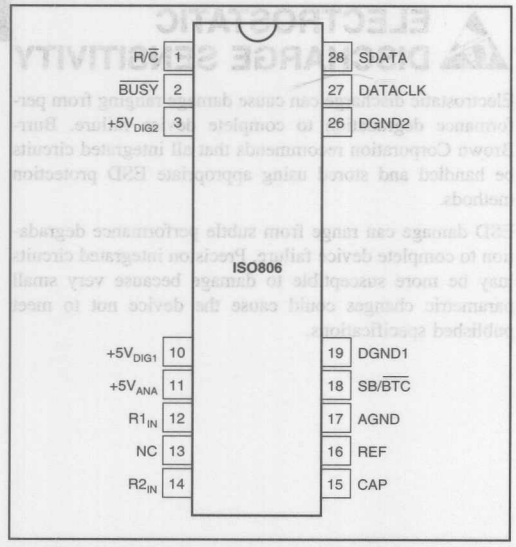
## ORDERING INFORMATION

| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | TYPICAL SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE |
|---|---|---|---|---|
| ISO806P | ±0.9 | 70 | –40°C to +85°C | Plastic DIP |

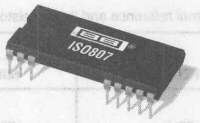
| PIN # | NAME | DIGITAL I/O | DESCRIPTION |
|---|---|---|---|
| 1 | R/$\overline{C}$ | I | Read/$\overline{Convert}$. With $\overline{BUSY}$ high, a falling edge on R/$\overline{C}$ initiates a new conversion. |
| 2 | $\overline{BUSY}$ | O | At the start of conversion $\overline{BUSY}$ goes LOW and stays LOW until conversion is complete. |
| 3 | $+5V_{DIG2}$ | | Isolated Digital Supply Volts. |
| 10 | $+5V_{DIG1}$ | | Digital Supply Volts. |
| 11 | $+5V_{ANA}$ | | Analog Supply Volts. |
| 12 | $R1_{IN}$ | | Analog Input. |
| 13 | NC | | No Connection. Leave unconnected. |
| 14 | $R2_{IN}$ | | Analog Input. |
| 15 | CAP | | Reference Buffer Output. 2.2µF tantalum capacitor to ground. |
| 16 | REF | | Reference Input/Output. 2.2µF tantalum capacitor to ground. |
| 17 | AGND | | Analog Ground. |
| 18 | SB/$\overline{BTC}$ | I | Selects Straight Binary or Binary Two's Complement for Output Data Format. |
| 19 | DGND1 | | Digital Ground. |
| 26 | DGND2 | | Isolated Ground. |
| 27 | DATACLK | O | Data Clock Output. |
| 28 | SDATA | O | Serial Output Synchronized to DATACLK. |

TABLE I. Pin Assignments.

## PIN CONFIGURATION



BURR - BROWN®




# ISO807

www.burr-brown.com/databook/ISO807.html

# Isolated 16-Bit Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- 1500Vrms ISOLATION CONTINUOUS
- 25µS CONVERSION TIME
- 16-BIT SERIAL OUTPUT
- SINGLE +5V SUPPLY
- 28-PIN 0.6" PLASTIC DIP

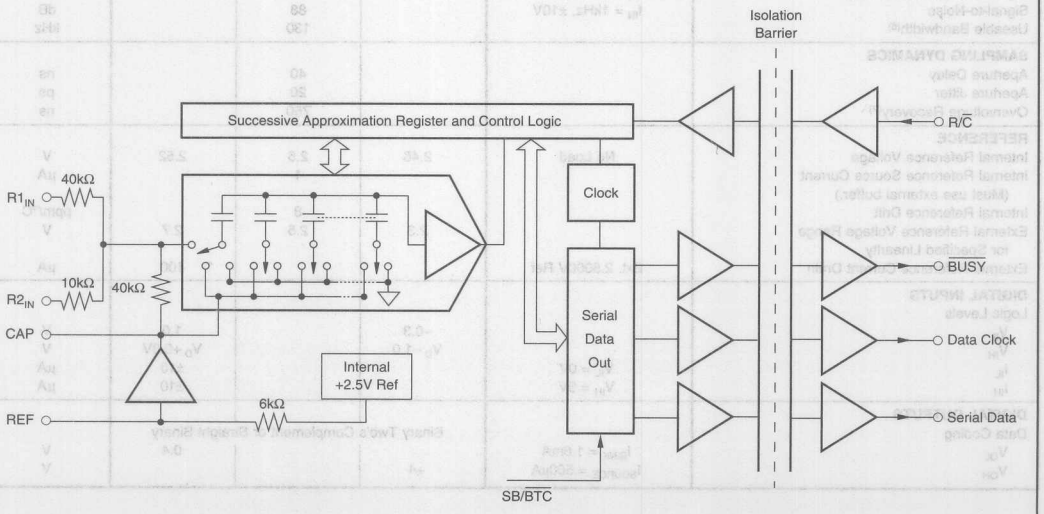
## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- PC-BASED DATA ACQUISITION TEST EQUIPMENT

## DESCRIPTION

The ISO807 is a low-power isolated sampling ADC using state-of-the-art CMOS structures and high voltage capacitors. The ISO807 contains a complete 16-bit capacitor based SAR, ADC with S/H, clock, reference, µP interface, serial out and galvanic isolation.

Laser-trimmed scaling resistors provide standard industrial input ranges including ±10V, ±5V, 0-5V, 0-4V. They are available in 28-pin 0.6" wide plastic DIP and are specified over the industrial temperature range of –40°C to +85°C.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 40kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference and fixed resistors shown in Figure 3b, unless otherwise specified.

| PARAMETER | CONDITIONS | ISO807P MIN | ISO807P TYP | ISO807P MAX | UNITS |
|---|---|---|---|---|---|
| **ISOLATION PARAMETERS** | | | | | |
| Rated Voltage, Continuous | 50Hz | 1500 | | | Vrms |
| Partial Discharge, 100% Test[8] | 1s, 5pC | 2500 | | | Vrms |
| Creepage Distance (External) DIP = "P" Package | | | 16 | | mm |
| Internal Isolation Distance | | | 0.10 | | mm |
| Barrier Impedance | | | $>10^{13}$ II 15 | | Ω II pF |
| Leakage Current[9] | 240Vrms, 60Hz | | | 1.7 | μArms |
| | 240Vrms, 50Hz | | | 1.4 | μArms |
| **RESOLUTION** | | | | 16 | Bit |
| **ANALOG INPUT** | | | | | |
| Voltage Ranges | | | ±10, 0 to +5, 0 to +4 | | V |
| Impedance | | | (See Table II) | | |
| Capacitance | | | 35 | | pF |
| **THROUGHPUT SPEED** | | | | | |
| Conversion Time | | | | 20 | μs |
| Complete Cycle | Acquire and Convert | | | 25 | μs |
| Throughput Rate | | 40 | | | kHz |
| **DC ACCURACY** | | | | | |
| Integral Linearity Error | | | | ±3 | LSB[1] |
| Differential Linearity Error | | | | +3, –2 | LSB |
| No Missing Codes | | 15 | | | Bits |
| Transition Noise[2] | | | 0.8 | | LSB |
| Full Scale Error[3,4] | | | | ±0.5 | % |
| Full Scale Error Drift | | | ±7 | | ppm/°C |
| Full Scale Error Drift | Ext. 2.5000V Ref | | ±0.5 | | ppm/°C |
| Bipolar Zero Error[3] | ±10V Range | | | ±10 | mV |
| Bipolar Zero Error Drift | ±10V Range | | ±0.5 | | ppm/°C |
| Unipolar Zero Error[3] | 0V to 5V, 0V to 4V Ranges | | | ±3 | mV |
| Unipolar Zero Error Drift | 0V to 5V, 0V to 4V Ranges | | ±0.5 | | ppm/°C |
| Power Supply Sensitivity ($V_{DIG}$ = $V_{ANA}$ = $V_S$) | +4.75V < $V_S$ < +5.25V | | | ±8 | LSB |
| **AC ACCURACY** | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 1kHz, ±10V | | 100 | | dB[5] |
| Total Harmonic Distortion | $f_{IN}$ = 1kHz, ±10V | | –100 | | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 1kHz, ±10V | | 88 | | dB |
| Signal-to-Noise | $f_{IN}$ = 1kHz, ±10V | | 88 | | dB |
| Useable Bandwidth[6] | | | 130 | | kHz |
| **SAMPLING DYNAMICS** | | | | | |
| Aperture Delay | | | 40 | | ns |
| Aperture Jitter | | | 20 | | ps |
| Overvoltage Recovery[7] | | | 750 | | ns |
| **REFERENCE** | | | | | |
| Internal Reference Voltage | No Load | 2.48 | 2.5 | 2.52 | V |
| Internal Reference Source Current (Must use external buffer.) | | | 1 | | μA |
| Internal Reference Drift | | | 8 | | ppm/°C |
| External Reference Voltage Range for Specified Linearity | | 2.3 | 2.5 | 2.7 | V |
| External Reference Current Drain | Ext. 2.5000V Ref | | | 100 | μA |
| **DIGITAL INPUTS** | | | | | |
| Logic Levels | | | | | |
| $V_{IL}$ | | –0.3 | | 1.0 | V |
| $V_{IH}$ | | $V_D$ –1.0 | | $V_D$ +0.3V | V |
| $I_{IL}$ | $V_{IL}$ = 0V | | | ±10 | μA |
| $I_{IH}$ | $V_{IH}$ = 5V | | | ±10 | μA |
| **DIGITAL OUTPUTS** | | | | | |
| Data Coding | | Binary Two's Complement or Straight Binary | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | 0.4 | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500μA | +4 | | | V |

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# SPECIFICATIONS (CONT)

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 40kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference and fixed resistors shown in Figure 3b, unless otherwise specified.

| PARAMETER | CONDITIONS | ISO807P MIN | ISO807P TYP | ISO807P MAX | UNITS |
|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | |
| Specified Performance | | | | | |
| $V_{DIG1}$ | Must be ≤ $V_{ANA}$ | +4.75 | +5 | +5.25 | V |
| $V_{ANA}$ | | +4.75 | +5 | +5.25 | V |
| $V_{DIG2}$ | | +4.75 | | +5.25 | V |
| $I_{DIG1}$ | | | 4.2 | | mA |
| $I_{ANA}$ | | | 5.0 | | mA |
| $I_{DIG2}$ | | | 10.8 | | mA |
| Power Dissipation | $V_{ANA}$ = $V_{DIG}$ = 5V, $F_S$ = 40kHz | | 125 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified Performance | | –40 | | +85 | °C |
| Storage | | –65 | | +150 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| Plastic DIP | | | 75 | | °C/W |

NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 3.05µV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale input. (6) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage. (8) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pC. (9) Tested at 2500Vrms, 50Hz limit 10µA.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $R1_{IN}$ | ±25V |
| $R2_{IN}$ | ±25V |
| CAP | $V_{ANA}$ +0.3V to AGND2 –0.3V |
| REF | Indefinite Short to AGND2, Momentary Short to $V_{ANA}$ |
| Ground Voltage Differences: DGND and AGND1 | ±0.3V |
| DGND, AGND, and $GND_{ISO}$ | 1563Vrms |
| $V_{ANA}$ | 7V |
| $V_{DIG}$ to $V_{ANA}$ | +0.3V |
| $V_{DIG}$ | 7V |
| Digital Inputs | –0.3V to $V_{DIG}$ +0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ISO807P | Plastic DIP | 215-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

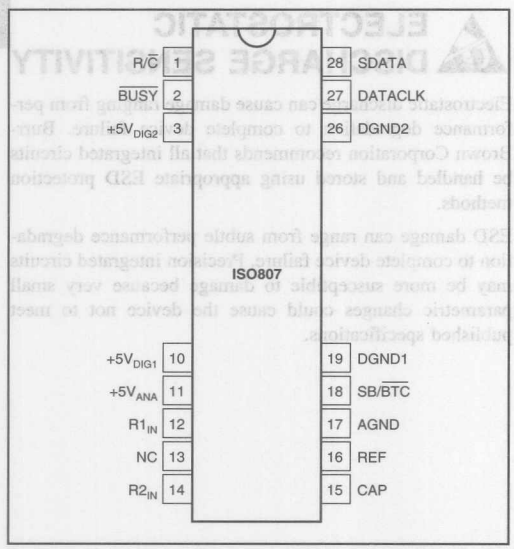
## ORDERING INFORMATION

| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | TYPICAL SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE |
|---|---|---|---|---|
| ISO807P | ±3 | 83 | –40°C to +85°C | Plastic DIP |

| | | | |
|---|---|---|---|
| 1 | R/$\overline{C}$ | I | Read/$\overline{Convert}$. With $\overline{BUSY}$ high, a falling edge on R/$\overline{C}$ initiates a new conversion. |
| 2 | $\overline{BUSY}$ | O | At the start of conversion $\overline{BUSY}$ goes LOW and stays LOW until conversion is complete. |
| 3 | $+5V_{DIG2}$ | | Isolated Digital Supply Volts. |
| 10 | $+5V_{DIG1}$ | | Digital Supply Volts. |
| 11 | $+5V_{ANA}$ | | Analog Supply Volts. |
| 12 | $R1_{IN}$ | | Analog Input. |
| 13 | NC | | No Connection. Leave unconnected. |
| 14 | $R2_{IN}$ | | Analog Input. |
| 15 | CAP | | Reference Buffer Output. 2.2µF tantalum capacitor to ground. |
| 16 | REF | | Reference Input/Output. 2.2µF tantalum capacitor to ground. |
| 17 | AGND | | Analog Ground. |
| 18 | SB/$\overline{BTC}$ | I | Selects Straight Binary or Binary Two's Complement for Output Data Format. |
| 19 | DGND1 | | Digital Ground. |
| 26 | DGND2 | | Isolated Ground. |
| 27 | DATACLK | O | Data Clock Output. |
| 28 | SDATA | O | Serial Output Synchronized to DATACLK. |

TABLE I. Pin Assignments.

## PIN CONFIGURATION



BURR-BROWN®



# ISO808

www.burr-brown.com/databook/ISO808.html

# Isolated 12-Bit Sampling ANALOG-TO-DIGITAL CONVERTER



## FEATURES

- 100kHz SAMPLING RATE
- 1500Vrms ISOLATION CONTINUOUS
- 10μS CONVERSION TIME
- 12-BIT SERIAL OUTPUT
- SINGLE +5V SUPPLY
- 28-PIN 0.6" PLASTIC DIP

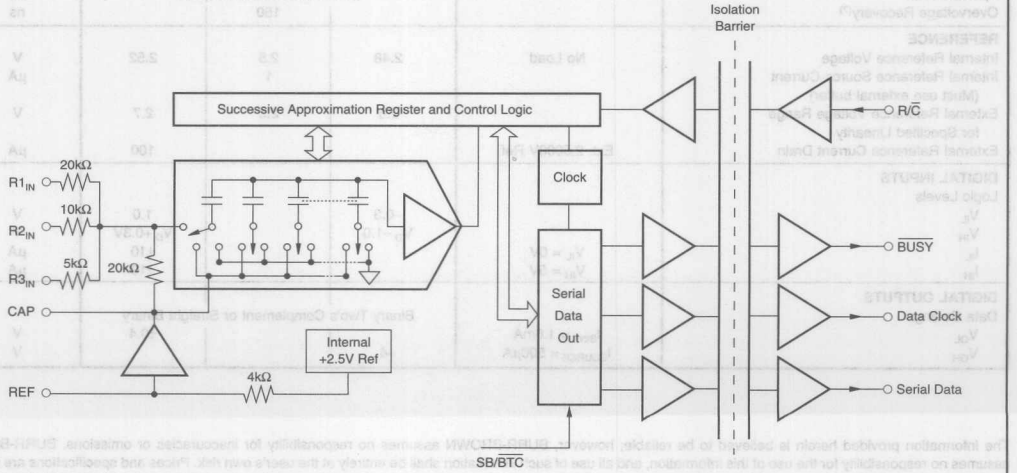
## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- PC-BASED DATA ACQUISITION TEST EQUIPMENT

## DESCRIPTION

The ISO808 is a low-power isolated sampling ADC using state-of-the-art CMOS structures and high voltage capacitors. The ISO808 contains a complete 12-bit capacitor based SAR, ADC with S/H, clock, reference, μP interface, serial out and galvanic isolation.

Laser-trimmed scaling resistors provide standard industrial input ranges including ±10V, ±5V, 0-5V, 0-4V. They are available in 28-pin 0.6" wide plastic DIP and are specified over the industrial temperature range of –40°C to +85°C.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 100kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference and fixed resistors shown in Figure 3, unless otherwise specified.

| PARAMETER | CONDITIONS | ISO808P MIN | ISO808P TYP | ISO808P MAX | UNITS |
|---|---|---|---|---|---|
| **ISOLATION PARAMETERS** | | | | | |
| Rated Voltage, Continuous | 50Hz | 1500 | | | Vrms |
| Partial Discharge, 100% Test[8] | 1s, 5pC | 2500 | | | Vrms |
| Creepage Distance (External) DIP = "P" Package | | | 16 | | mm |
| Internal Isolation Distance | | | 0.10 | | mm |
| Barrier Impedance | | | $>10^{13}$ II 15 | | Ω II pF |
| Leakage Current[9] | 240Vrms, 60Hz | | | 1.7 | µArms |
| | 240Vrms, 50Hz | | | 1.4 | µArms |
| **RESOLUTION** | | | | 12 | Bits |
| **ANALOG INPUT** | | | | | |
| Voltage Ranges | | | ±10V, 0V to 5V, etc. (See Table I) | | |
| Impedance | | | See Table I | | |
| Capacitance | | | 35 | | pF |
| **THROUGHPUT SPEED** | | | | | |
| Conversion Time | | | 5.7 | 8 | µs |
| Complete Cycle | Acquire and Convert | | | 10 | µs |
| Throughput Rate | | 100 | | | kHz |
| **DC ACCURACY** | | | | | |
| Integral Linearity Error | | | | ±0.9 | LSB[1] |
| Differential Linearity Error | | | | ±0.9 | LSB |
| No Missing Codes | | | Guaranteed | | |
| Transition Noise[2] | | | 0.1 | | LSB |
| Full Scale Error[3,4] | | | | ±0.5 | % |
| Full Scale Error Drift | | | ±7 | | ppm/°C |
| Full Scale Error Drift | Ext. 2.5000V Ref | | ±2 | | ppm/°C |
| Bipolar Zero Error[3] | Bipolar Ranges | | | ±10 | mV |
| Bipolar Zero Error Drift | Bipolar Ranges | | ±2 | | ppm/°C |
| Unipolar Zero Error[3] | Unipolar Ranges | | | ±5 | mV |
| Unipolar Zero Error Drift | Unipolar Ranges | | ±2 | | ppm/°C |
| Power Supply Sensitivity ($V_{DIG}$ = $V_{ANA}$ = $V_D$) | +4.75V < $V_D$ < +5.25V | | | ±0.5 | LSB |
| **AC ACCURACY** | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 45kHz ±10V | | 90 | | dB[5] |
| Total Harmonic Distortion | $f_{IN}$ = 45kHz ±10V | | –90 | | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 45kHz ±10V | | 73 | | dB |
| Signal-to-Noise | $f_{IN}$ = 45kHz ±10V | | 73 | | dB |
| Full-Power Bandwidth[6] | | | 250 | | kHz |
| **SAMPLING DYNAMICS** | | | | | |
| Aperture Delay | | | 40 | | ns |
| Aperture Jitter | | | Sufficient to meet AC specs | | ns |
| Overvoltage Recovery[7] | | | 150 | | ns |
| **REFERENCE** | | | | | |
| Internal Reference Voltage | No Load | 2.48 | 2.5 | 2.52 | V |
| Internal Reference Source Current (Must use external buffer) | | | 1 | | µA |
| External Reference Voltage Range for Specified Linearity | | 2.3 | 2.5 | 2.7 | V |
| External Reference Current Drain | Ext. 2.5000V Ref | | | 100 | µA |
| **DIGITAL INPUTS** | | | | | |
| Logic Levels | | | | | |
| $V_{IL}$ | | –0.3 | | 1.0 | V |
| $V_{IH}$ | | $V_D$ –1.0 | | $V_D$ +0.3V | V |
| $I_{IL}$ | $V_{IL}$ = 0V | | | ±10 | µA |
| $I_{IH}$ | $V_{IH}$ = 5V | | | ±10 | µA |
| **DIGITAL OUTPUTS** | | | | | |
| Data Coding | | | Binary Two's Complement or Straight Binary | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | ±0.4 | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +4 | | | V |

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# SPECIFICATIONS (CONT)

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 100kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference and fixed resistors shown in Figure 3, unless otherwise specified.

| PARAMETER | CONDITIONS | ISO808P MIN | ISO808P TYP | ISO808P MAX | UNITS |
|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | |
| Specified Performance | | | | | |
| $V_{DIG1}$ | Must be ≤ $V_{ANA}$ | +4.75 | +5 | +5.25 | V |
| $V_{ANA}$ | | +4.75 | +5 | +5.25 | V |
| $V_{DIG2}$ | | +4.75 | | +5.25 | V |
| $I_{DIG1}$ | | | 4.2 | | mA |
| $I_{ANA}$ | | | 16 | | mA |
| $I_{DIG2}$ | | | 10.8 | | mA |
| Power Dissipation | $V_{ANA}$ = $V_{DIG}$ = 5V, $f_S$ = 100kHz | | 175 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified Performance | | –40 | | +85 | °C |
| Storage | | –65 | | +150 | °C |
| Thermal Resistance, $\phi_{JA}$ | | | | | |
| Plastic DIP | | | 75 | | °C/W |

NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 4.88mV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale input. (6) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage. (8) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pC. (9) Tested at 2500Vrms, 50Hz limit 10µA.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $R1_{IN}$ | ±25V |
| $R2_{IN}$ | ±25V |
| $R3_{IN}$ | ±25V |
| CAP | $V_{ANA}$ +0.3V to AGND2 –0.3V |
| REF | Indefinite Short to AGND, Momentary Short to $V_{ANA}$ |
| Ground Voltage Differences: DGND and AGND | ±0.3V |
| DGND, AGND, and $GND_{ISO}$ | 1563Vrms |
| $V_{ANA}$ | 7V |
| $V_{DIG}$ to $V_{ANA}$ | +0.3V |
| $V_{DIG}$ | 7V |
| Digital Inputs | –0.3V to $V_{DIG}$ +0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 700mW |
| Lead Temperature (soldering, 10s) | +300°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ISO808P | 28-Pin Plastic DIP | 215-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

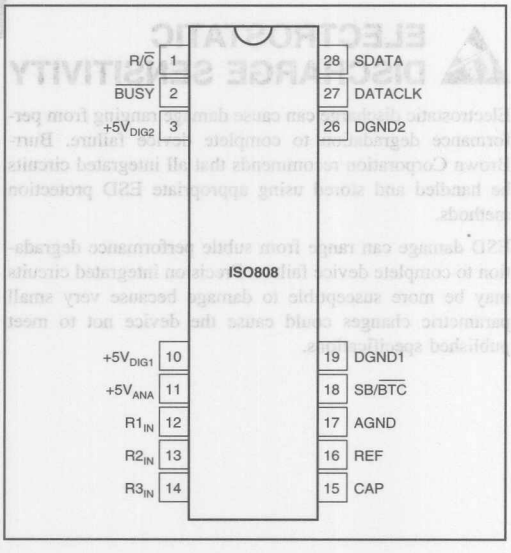
## ORDERING INFORMATION

| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | TYPICAL SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB) | SPECIFICATION TEMPERATURE RANGE (°C) | PACKAGE |
|---|---|---|---|---|
| ISO808P | ±0.9 | 70 | –40°C to +85°C | 28-Pin Plastic DIP |

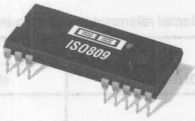
| PIN # | NAME | DIGITAL I/O | DESCRIPTION |
|---|---|---|---|
| 1 | R/$\overline{C}$ | I | Read/$\overline{\text{Convert}}$. With $\overline{\text{BUSY}}$ high, a falling edge on R/$\overline{C}$ initiates a new conversion. |
| 2 | $\overline{\text{BUSY}}$ | O | At the start of conversion $\overline{\text{BUSY}}$ goes LOW and stays LOW until conversion is complete. |
| 3 | $+5V_{DIG2}$ | | Isolated Digital Supply Volts. |
| 10 | $+5V_{DIG1}$ | | Digital Supply Volts. |
| 11 | $+5V_{ANA}$ | | Analog Supply Volts. |
| 12 | $R1_{IN}$ | | Analog Input. |
| 13 | $R2_{N}$ | | Analog Input. |
| 14 | $R3_{N}$ | | Analog Input. |
| 15 | CAP | | Reference Buffer Output. 2.2µF tantalum capacitor to ground. |
| 16 | REF | | Reference Input/Output. 2.2µF tantalum capacitor to ground. |
| 17 | AGND | | Analog Ground. |
| 18 | SB/$\overline{\text{BTC}}$ | I | Selects Straight Binary or Binary Two's Complement for output data format. |
| 19 | DGND1 | | Digital Ground. |
| 26 | DGND2 | | Isolated Ground. |
| 27 | DATACLK | O | Data Clock Output. |
| 28 | SDATA | O | Serial Output Synchronized to DATACLK. |

TABLE I. Pin Assignments.

## PIN CONFIGURATION



BURR-BROWN®



# ISO809

www.burr-brown.com/databook/ISO809.html

# Isolated 16-Bit Sampling ANALOG-TO-DIGITAL CONVERTER



## FEATURES

- 100kHz SAMPLING RATE
- 1500Vrms ISOLATION CONTINUOUS
- 10µS CONVERSION TIME
- 16-BIT SERIAL OUTPUT
- SINGLE +5V SUPPLY
- 28-PIN 0.6" PLASTIC DIP

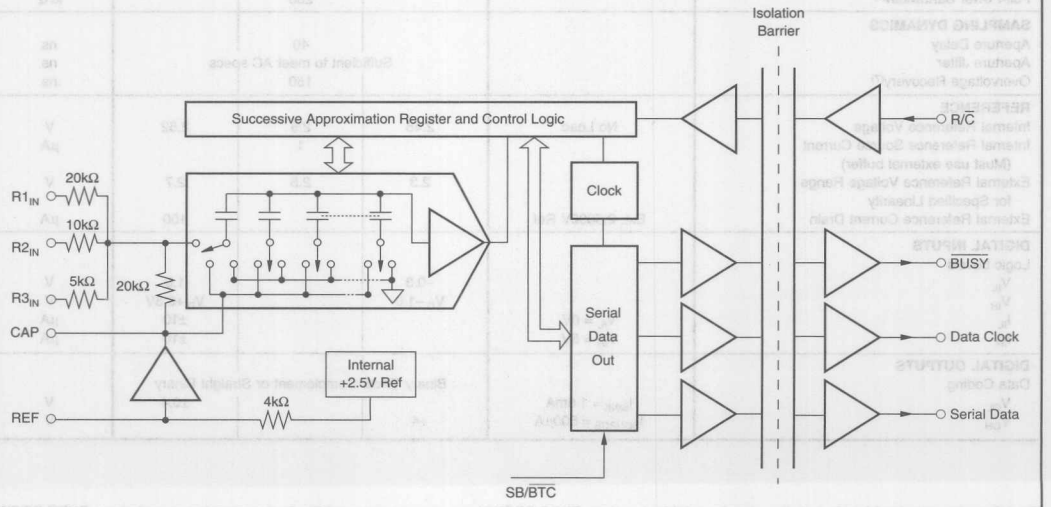
## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- PC-BASED DATA ACQUISITION TEST EQUIPMENT

## DESCRIPTION

The ISO809 is a low-power isolated sampling ADC using state-of-the-art CMOS structures and high voltage capacitors. The ISO809 contains a complete 16-bit capacitor based SAR, ADC with S/H, clock, reference, µP interface, serial out and galvanic isolation.

Laser-trimmed scaling resistors provide standard industrial input ranges including ±10V, ±5V, 0-5V, 0-4V. They are available in 28-pin 0.6" wide plastic DIP and are specified over the industrial temperature range of –40°C to +85°C.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 100kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference and fixed resistors shown in Figure 3, unless otherwise specified.

| PARAMETER | CONDITIONS | ISO809P MIN | ISO809P TYP | ISO809P MAX | UNITS |
|---|---|---|---|---|---|
| **ISOLATION PARAMETERS** | | | | | |
| Rated Voltage, Continuous | 50Hz | 1500 | | | Vrms |
| Partial Discharge, 100% Test[8] | 1s, 5pC | 2500 | | | Vrms |
| Creepage Distance (External) DIP = "P" Package | | | 16 | | mm |
| Internal Isolation Distance | | | 0.10 | | mm |
| Barrier Impedance | | | $>10^{13}$ II 15 | | Ω II pF |
| Leakage Current[9] | 240Vrms, 60Hz | | | 1.2 | μArms |
| | 240Vrms, 50Hz | | | 1.0 | μArms |
| **RESOLUTION** | | | | 16 | Bits |
| **ANALOG INPUT** | | | | | |
| Voltage Ranges | ±10V, 0V to 5V, etc. (See Table I) | | | | |
| Impedance | | | See Table I | | |
| Capacitance | | | 35 | | pF |
| **THROUGHPUT SPEED** | | | | | |
| Conversion Time | | | 7.6 | 8 | μs |
| Complete Cycle | Acquire and Convert | | | 10 | μs |
| Throughput Rate | | 100 | | | kHz |
| **DC ACCURACY** | | | | | |
| Integral Linearity Error | | | | ±4 | LSB[1] |
| Differential Linearity Error | | | | ±4 | LSB |
| No Missing Codes | | 15 | | | |
| Transition Noise[2] | | | 1.3 | | LSB |
| Full Scale Error[3,4] | | | | ±0.5 | % |
| Full Scale Error Drift | | | ±7 | | ppm/°C |
| Full Scale Error Drift | Ext. 2.5000V Ref | | ±2 | | ppm/°C |
| Bipolar Zero Error[3] | Bipolar Ranges | | | ±10 | mV |
| Bipolar Zero Error Drift | Bipolar Ranges | | ±2 | | ppm/°C |
| Unipolar Zero Error[3] | Unipolar Ranges | | | 3 | mV |
| Unipolar Zero Error Drift | Unipolar Ranges | | ±2 | | ppm/°C |
| Power Supply Sensitivity ($V_{DIG}$ = $V_{ANA}$ = $V_D$) | +4.75V < $V_D$ < +5.25V | | | 8 | LSB |
| **AC ACCURACY** | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 45kHz ±10V | | 100 | | dB[5] |
| Total Harmonic Distortion | $f_{IN}$ = 45kHz ±10V | | –100 | | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 45kHz ±10V | | 88 | | dB |
| Signal-to-Noise | $f_{IN}$ = 45kHz ±10V | | 88 | | dB |
| Full-Power Bandwidth[6] | | | 250 | | kHz |
| **SAMPLING DYNAMICS** | | | | | |
| Aperture Delay | | | 40 | | ns |
| Aperture Jitter | | | Sufficient to meet AC specs | | ns |
| Overvoltage Recovery[7] | | | 150 | | ns |
| **REFERENCE** | | | | | |
| Internal Reference Voltage | No Load | 2.48 | 2.5 | 2.52 | V |
| Internal Reference Source Current (Must use external buffer) | | | 1 | | μA |
| External Reference Voltage Range for Specified Linearity | | 2.3 | 2.5 | 2.7 | V |
| External Reference Current Drain | Ext. 2.5000V Ref | | | 100 | μA |
| **DIGITAL INPUTS** | | | | | |
| Logic Levels | | | | | |
| $V_{IL}$ | | –0.3 | | 1.0 | V |
| $V_{IH}$ | | $V_D$ –1.0 | | $V_D$ +0.3V | V |
| $I_{IL}$ | $V_{IL}$ = 0V | | | ±10 | μA |
| $I_{IH}$ | $V_{IH}$ = 5V | | | ±10 | μA |
| **DIGITAL OUTPUTS** | | | | | |
| Data Coding | | Binary Two's Complement or Straight Binary | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | ±0.4 | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500μA | +4 | | | V |

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# SPECIFICATIONS (CONT)

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 100kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference and fixed resistors shown in Figure 3, unless otherwise specified.

| PARAMETER | CONDITIONS | ISO809P MIN | ISO809P TYP | ISO809P MAX | UNITS |
|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | |
| Specified Performance | | | | | |
| $V_{DIG1}$ | Must be ≤ $V_{ANA}$ | +4.75 | +5 | +5.25 | V |
| $V_{ANA}$ | | +4.75 | +5 | +5.25 | V |
| $V_{DIG2}$ | | +4.75 | | +5.25 | V |
| $I_{DIG1}$ | | | 4.2 | | mA |
| $I_{ANA}$ | | | 21 | | mA |
| $I_{DIG2}$ | | | 10.8 | | mA |
| Power Dissipation | $V_{ANA}$ = $V_{DIG}$ = 5V, $f_S$ = 100kHz | | 175 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified Performance | | –40 | | +85 | °C |
| Storage | | –65 | | +150 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| Plastic DIP | | | 75 | | °C/W |

NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 3.05µV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale input. (6) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage. (8) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pC. (9) Tested at 2500Vrms, 50Hz limit 10µA.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $R1_{IN}$ | ±25V |
| $R2_{IN}$ | ±25V |
| $R3_{IN}$ | ±25V |
| CAP | $V_{ANA}$ +0.3V to AGND2 –0.3V |
| REF | Indefinite Short to AGND, Momentary Short to $V_{ANA}$ |
| Ground Voltage Differences: DGND and AGND | ±0.3V |
| DGND, AGND, and $GND_{ISO}$ | 1563Vrms |
| $V_{ANA}$ | 7V |
| $V_{DIG}$ to $V_{ANA}$ | +0.3V |
| $V_{DIG}$ | 7V |
| Digital Inputs | –0.3V to $V_{DIG}$ +0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 700mW |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ISO809P | 28-Pin Plastic DIP | 215-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

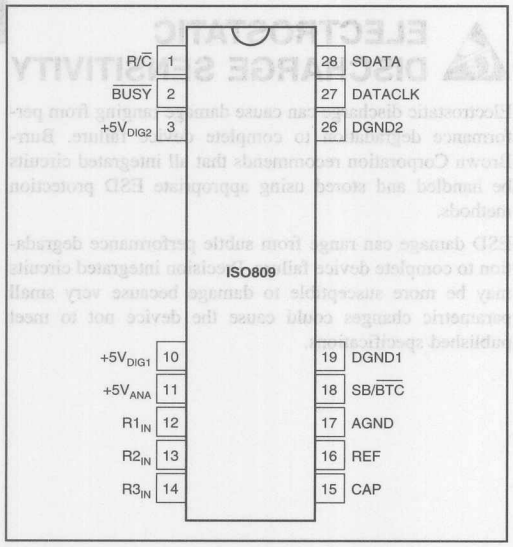
## ORDERING INFORMATION

| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | TYPICAL SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB) | SPECIFICATION TEMPERATURE RANGE (°C) | PACKAGE |
|---|---|---|---|---|
| ISO809P | ±4 | 83 | –40°C to +85°C | 28-Pin Plastic DIP |

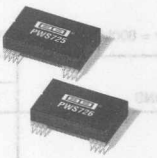
| PIN # | NAME | DIGITAL I/O | DESCRIPTION |
|---|---|---|---|
| 1 | R/$\overline{C}$ | I | Read/$\overline{Convert}$. With $\overline{BUSY}$ high, a falling edge on R/$\overline{C}$ initiates a new conversion. |
| 2 | $\overline{BUSY}$ | O | At the start of conversion $\overline{BUSY}$ goes LOW and stays LOW until conversion is complete. |
| 3 | $+5V_{DIG2}$ | | Isolated Digital Supply Volts. |
| 10 | $+5V_{DIG1}$ | | Digital Supply Volts. |
| 11 | $+5V_{ANA}$ | | Analog Supply Volts. |
| 12 | $R1_{IN}$ | | Analog Input. |
| 13 | $R2_{N}$ | | Analog Input. |
| 14 | $R3_{N}$ | | Analog Input. |
| 15 | CAP | | Reference Buffer Output. 2.2µF tantalum capacitor to ground. |
| 16 | REF | | Reference Input/Output. 2.2µF tantalum capacitor to ground. |
| 17 | AGND | | Analog Ground. |
| 18 | SB/$\overline{BTC}$ | I | Selects Straight Binary or Binary Two's Complement for output data format. |
| 19 | DGND1 | | Digital Ground. |
| 26 | DGND2 | | Isolated Ground. |
| 27 | DATACLK | O | Data Clock Output. |
| 28 | SDATA | O | Serial Output Synchronized to DATACLK. |

TABLE I. Pin Assignments.

## PIN CONFIGURATION



BURR-BROWN®



# PWS725A
# PWS726A

www.burr-brown.com/databook/PWS725.html

# Isolated, Unregulated DC/DC CONVERTERS



## FEATURES

- ISOLATED ±7 TO ±18VDC OUTPUT FROM SINGLE 7 TO 18VDC SUPPLY
- ±15mA OUTPUT AT RATED VOLTAGE ACCURACY
- HIGH ISOLATION VOLTAGE
  PWS725A, 1500Vrms
  PWS726A, 3500Vrms
- LOW LEAKAGE CAPACITANCE: 9pF
- LOW LEAKAGE CURRENT: 2μA max, at 240VAC 50/60Hz
- HIGH RELIABILITY DESIGN
- AVAILABLE WITH OUTPUT SYNCHRONIZATION SIGNAL FOR USE WITH ISO120 AND ISO121
- PROTECTED AGAINST OUTPUT FAULTS
- COMPACT
- LOW COST
- EASY TO APPLY—FEW EXTERNAL PARTS

## APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS EQUIPMENT
- TEST EQUIPMENT
- DATA ACQUISITION

## DESCRIPTION

The PWS725A and PWS726A convert a single 7 to 18VDC input to bipolar voltages of the same value as the input voltage. The converters are capable of providing ±15mA at rated voltage accuracy and up to ±40mA without damage. (See Output Current Rating.)

The PWS725A and PWS726A converters provide reliable, engineered solutions where isolated power is required in critical applications. The high isolation voltage rating is achieved through use of a specially-designed transformer and physical spacing. An additional high dielectric-strength, low leakage transformer coating increases the isolation rating of the PWS726A.

Reliability and performance are designed in. The bifilar wound, wirebonded transformer simultaneously provides lower output ripple than competing designs, and a higher performance/cost ratio. The soft-start oscillator/driver design assures full operation of the oscillator before either MOSFET driver turns on, protects the switches, and eliminates high inrush currents during turn-on. Input current sensing protects both the converter and the load from possible thermal damage during a fault condition.

Special design features make these converters especially easy to apply. The compact size allows dense circuit layout while maintaining critical isolation requirements. The Input Sync connection allows frequency synchronization of multiple converters. The Output Sync is available to synchronize ISO120 and ISO121 isolation amplifiers. The Enable input allows control over output power in instances where shutdown is desired to conserve power, such as in battery-powered equipment, or where sequencing of power turn-on/turn-off is desired.

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# SPECIFICATIONS

## ELECTRICAL

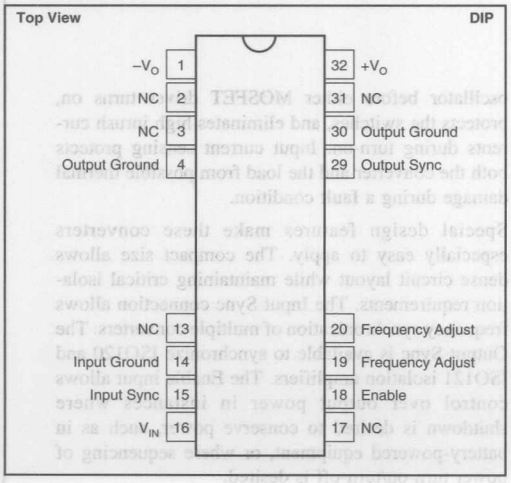
$T_A$ = +25°C, $C_L$ = 1µF ceramic, $V_{IN}$ = 15VDC, operating frequency = 800kHz, $V_{OUT}$ = ±15VDC, $C_{IN}$ = 1µF ceramic, $I_{OUT}$ = ±15mA, unless otherwise specified.

| PARAMETER | CONDITIONS | PWS725A | | | PSW726A | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT** | | | | | | | | |
| Rated Voltage | | | 15 | | | * | | VDC |
| Input Voltage Range | | 7 | | 18 | * | | * | VDC |
| Input Current | $I_O$ = ±15mA | | 77 | | | * | | mA |
| Input Current Ripple | No External Filtering | | 150 | | | * | | mAp-p |
| | L-C Input Filter, $L_{IN}$ = 100µH, $C_{IN}$ = 1µF[1] | | 5 | | | * | | mAp-p |
| | C Only, $C_{IN}$ = 1µF | | 60 | | | | | mAp-p |
| **ISOLATION** | | | | | | | | |
| Test Voltages | Input to Output, 10 seconds | 4000 | | | 8000 | | | VDC |
| | Input to Output, 60 seconds, min | 1500 | | | 3500 | | | Vrms |
| Rated Voltage | Input to Output, Continuous, AC 60Hz | | | 1500 | | | 3500 | Vrms |
| | Input to Output, Continuous DC | | | 2121 | | | 4950 | VDC |
| Isolation Impedance | Input to Output | | $10^{12}$ \|\| 9 | | | * | | Ω \|\| pF |
| Leakage Current | Input to Output, 240Vrms, 60Hz | | 1.2 | 2.0 | | * | * | µA |
| **OUTPUT** | | | | | | | | |
| Rated Output Voltage | | 14.25 | 15 | 15.75 | * | * | * | VDC |
| Output Current | Balanced Loads | | 15 | 40 | | * | * | mA |
| | Single-Ended | | | 80 | | | * | mA |
| Load Regulation | Balanced Loads, ±10mA < $I_{OUT}$ < ±40mA | | | 0.4 | | | * | %/mA |
| Ripple Voltage (400kHz) | No External Capacitor | | 60 | | | * | | mVp-p |
| | $L_O$ = 10µH, $C_O$ = 1µF (Figure 1) | | 10 | | | * | | mVp-p |
| | $L_O$ = 0µH, $C_O$ Filter Only | | | | See Performance Curves | | | |
| Output Switching Noise | $L_O$ = 10µH, $C_O$ = 1µF | | 1 | | | * | | mVp-p |
| Output Capacitive Load | $L_O$ = 100µH, C Filter | | | 10 | | | * | µF |
| | C Filter Only | | | 1 | | | * | µF |
| Voltage Balance, V+, V– | | | 0.04 | | | | | % |
| Sensitivity to $\Delta V_{IN}$ | | | 1.15 | | | | | V/V |
| Output Voltage Temp. Coefficient | | | 10 | | | | | mV/°C |
| Output Sync Signal | Square Wave, 50% Duty Cycle | | 30 | | | * | | Vp-p |
| **TEMPERATURE** | | | | | | | | |
| Specification | | –25 | | +85 | * | | * | °C |
| Operating | | –25 | | +85 | * | | * | °C |
| Storage | | –25 | | +125 | * | | * | °C |

* Specification same as PWS725A.

## PIN CONFIGURATION

Top View DIP




## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| PWS725A | 32-Pin Ceramic DIP | 210 |
| PWS726A | 32-Pin Ceramic DIP | 210 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

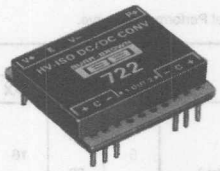
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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722

www.burr-brown.com/databook/722.html

# DUAL ISOLATED DC/DC CONVERTER



## FEATURES

- DUAL ISOLATED ±5V TO ±16V OUTPUTS
- HIGH BREAKDOWN VOLTAGE: 8000V Test
- LOW LEAKAGE CURRENT: <1μA at 240V/60Hz
- LOW COST PER ISOLATED CHANNEL
- SMALL SIZE: 27.9mm x 27.9mm x 7.6mm (1.1" x 1.1" x 0.3")

## APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS
- NUCLEAR INSTRUMENTATION

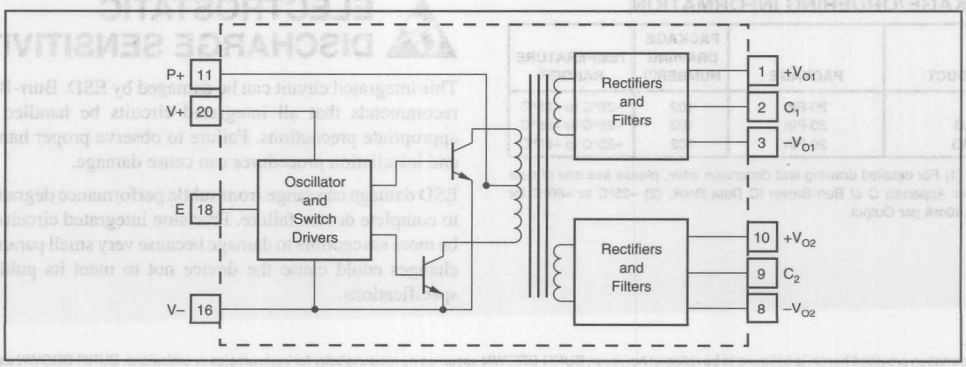
## DESCRIPTION

The 722 converts a single 5VDC to 16VDC input into a pair of bipolar output voltages of the same value as the input voltage. The converter is capable of providing a total output current of 64mA at rated voltage accuracy and up to 200mA without damage.

The two output channels are isolated from the input and from each other. They may be connected independently, in series for higher output voltage or in parallel for higher output current, as a single channel isolated DC/DC converter.

Integrated circuit construction of the 722 reduces size and cost. High isolation breakdown voltages and low leakage currents are assured by special design and construction which includes use of a high dielectric strength, low leakage coating used on the internal assembly.

A self-contained 900kHz oscillator drives switching circuitry, which is designed to eliminate the common problem of input current spiking due to transformer saturation or crossover switching.




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# SPECIFICATIONS

At $T_A$ = +25°C, $V_{IN}$ = 15VDC, C = 0.47µF, $R_1$ selected per Typical Performance Curve.

| PARAMETER | CONDITIONS | 722 | | | 722BG | | | 722MG | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT** | | | | | | | | | | | |
| Rated Input Voltage | | | 15 | | | * | | | * | | VDC |
| Input Voltage Range(1) | | 5 | | 16 | * | | * | * | | * | VDC |
| Input Current | Total Output Current = 12mA | | 50 | | | * | | | * | | mA |
| | Total Output Current = 64mA | | 105 | 120 | | * | * | | * | * | mA |
| | Total Output Current = 64mA at $T_A$ = +85°C | | 120 | | | * | | | * | | mA |
| | Total Output Current = 160mA | | — | — | | 225 | 275 | | — | — | mA |
| Input Ripple(2) | Total Output Current = 12mA | | 3 | | | * | | | * | | mA, pk |
| | Total Output Current = 64mA | | 6 | | | * | | | * | | mA, pk |
| | Total Output Current = 160mA | | — | | | 12 | | | — | | mA, pk |
| **ISOLATION** | | | | | | | | | | | |
| Test Voltages | Input-to-Output, 5 seconds, min | | | 8000 | | | * | | | * | Vpk |
| | Input-to-Output, 1 minute, min | | | — | | | — | | | 2500 | Vrms |
| | Channel-to-Channel, 5 seconds, min | | | 5000 | | | * | | | * | Vpk |
| Rated Voltages | Input-to-Output, continuous | | | 3500 | | | * | | | * | V |
| | Channel-to-Channel, continuous | | | 2000 | * | | * | | | * | V |
| Isolation Impedance | Input-to-Output | | 10 \|\| 6 | | | * | | | * | | GΩ \|\| pF |
| Leakage Current(3) | Input-to-Output, 240V, 60Hz | | | 1 | | | * | | | * | µA |
| **OUTPUT** | | | | | | | | | | | |
| Rated Output Voltages(4) | $I_{LOAD}$ = 3mA per Output | 15.4 | | 16.2 | * | | * | * | | * | VDC |
| | $I_{LOAD}$ = 16mA per Output | 14.3 | | 16.2 | * | | * | * | | * | VDC |
| | $I_{LOAD}$ = 40mA per Output | — | — | — | 13.7 | 14.2 | 16.2 | — | — | — | VDC |
| Output Current | Total of All Outputs | | | 200 | | | * | | | * | mA |
| | Any One Output(5) | 3 | | 100 | * | | * | * | | * | mA |
| Load Regulation | | | (5) | | | * | | | * | | |
| Ripple Voltage | $I_{LOAD}$ = 3mA per Output | | 15 | | | * | | | * | | mVpk |
| | $I_{LOAD}$ = 16mA per Output | | 35 | 100 | | * | * | | * | * | mVpk |
| | $I_{LOAD}$ = 40mA per Output | | — | | | 50 | | | * | | mVpk |
| Tracking Error between Dual Outputs | Balanced Loads | | ±100 | | | * | | | * | | mVDC |
| Sensitivity to Input Voltage Changes | | | 1.13 | | | * | | | * | | V/V |
| Output Voltage Temperature Coefficient | $T_A = T_{SPECIFICATION\ RANGE}$ | | ±0.02 | | | * | | | * | | %/°C |
| **TEMPERATURE** | | | | | | | | | | | |
| Specification | $I_{LOAD} \leq$ 16mA per Output | –25 | | +85 | * | | * | * | | * | °C |
| | $I_{LOAD} \leq$ 40mA per Output | –25 | | +60 | * | | * | * | | * | °C |
| Storage | | –55 | | +125 | * | | * | * | | * | °C |
| Junction Temperature | | | | +125 | | | * | | | * | °C |

*Specifications same as 722.

NOTES: (1) For ambient temperature above +70°C the input voltage is 12.5V (max). The input voltage remains 16V (max) if case temperature is kept below +85°C. (2) External capacitor across "P+" to "V–" pins and 12" of #24 wire to $V_{IN}$. (3) Reference UL544, paragraph 27.5, Leakage Current. (4) See "Typical Performance Curves." (5) A minimum output current of 3mA at each output is recommended to maintain output voltage accuracy.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE(2) |
|---|---|---|---|
| 722 | 20-Pin | 102 | –25°C to +85°C |
| 722BG | 20-Pin | 102 | –25°C to +85°C |
| 722MG | 20-Pin | 102 | –25°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) –25°C to +60°C for $I_{LOAD} \leq$ 40mA per Output.

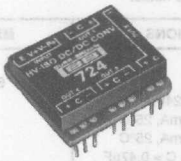
## ELECTROSTATIC DISCHARGE SENSITIVITY

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724

www.burr-brown.com/databook/724.html

# QUAD ISOLATED DC/DC CONVERTER

## FEATURES

- QUAD ISOLATED ±8V OUTPUTS
- HIGH BREAKDOWN VOLTAGE: 3000V Test
- LOW LEAKAGE CURRENT: <1μA at 240V/60Hz
- LOW COST PER ISOLATED CHANNEL
- SMALL SIZE: 27.9mm X 27.9mm X 6.6mm (1.1" X 1.1" X 0.26")

## APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS
- NUCLEAR INSTRUMENTATION

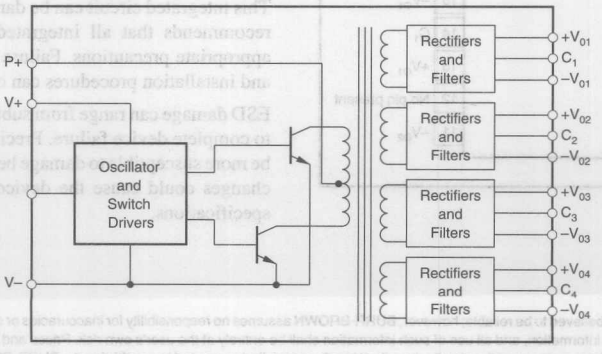
## DESCRIPTION

The 724 converts a single 5VDC to 16VDC input into four pairs of bipolar output voltages of approximately half the output voltage. The converter is capable of providing a total output current of 128mA at rated voltage accuracy and up to 500mA without damage.

The four output channels are isolated from the input and from each other. They may be connected independently, in series for higher output voltage, or in parallel for higher output current as a single channel isolated DC/DC converter.

Integrated circuit construction of the 724 reduces size and cost. High isolation breakdown voltages and low leakage currents are assured by special design and construction which includes use of a high dielectric strength, and low leakage coating used on the internal assembly.

A self-contained 800kHz oscillator drives switching circuitry, which is designed to eliminate the common problem of input current spiking due to transformer saturation or crossover switching.




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# SPECIFICATIONS

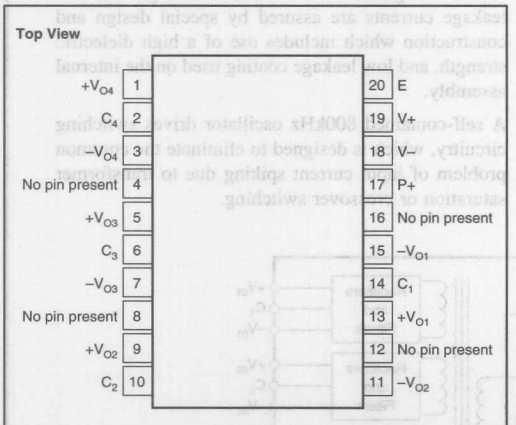
At 25°C with $V_{IN}$ = 15V, $R_1$ = 1.3kΩ, C = 0.47µF, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT** | | | | | |
| Input Voltage | | 5 | 15 | 16 | VDC |
| Input Current | Σ $I_{OUT}$ = 24mA | | 50 | | mA |
| | Σ $I_{OUT}$ = 128mA, 25°C | | 110 | 125 | mA |
| | Σ $I_{OUT}$ = 128mA, 25°C | | 120 | | mA |
| Input Ripple[1, 5] | Σ $I_{OUT}$ = 24mA, C = 0.47µF | | 10 | | mA, pk |
| | Σ $I_{OUT}$ = 128mA, C = 0.47µF | | | 25 | mA, pk |
| **ISOLATION** | | | | | |
| Test Voltage[2] | Input-to-Output, 5s min | | | 3000 | VDC |
| | Channel-to-Channel, 5s min | | | 3000 | VDC |
| Rated Voltage[2] | Input-to-Output, Continuous | | | 1000 | VDC |
| | Channel-to-Channel, Continuous | | | 1000 | VDC |
| Isolation Impedance | Input-to-Output | | 10 ll 6 | | GΩ ll pF |
| Leakage Current | Input-to-Output, 240V/60Hz | | | 1.0 | µA |
| **OUTPUT** | | | | | |
| Voltage[3] | At 15V Input $I_L$ = 3mA | 8.0 | 8.5 | 9.0 | V |
| | $I_L$ = 16mA | 7.5 | 7.9 | 8.3 | V |
| Current for Rated Voltage | Total of All Outputs | | | 128 | mA |
| | Any One Output[4] | 3 | | | |
| Total Safe Nondestructive Current | Total of All Outputs | | | 500 | mA |
| | Any One Output | | | 200 | mA |
| Load Regulation[3] | | | [4] | | |
| Ripple Voltage[5] | $I_L$ = 3mA | | 35 | | mV, pk |
| | $I_L$ = 16mA | | | 200 | mV, pk |
| Difference of $+V_O$ and $-V_O$ | $+I_L = -I_L$ | | ±30 | | mV |
| Sensitivity to Input Voltage Change | | | 0.63 | | V/V |
| Output Voltage Change Over Temperature | –25°C to +85°C | | 2 | | % |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –25 | | +85 | °C |
| Storage | | –55 | | +125 | °C |

NOTES: (1) 0.47µF external capacitor across "P+" to "V–" pins and 12" of #24 wire to $V_{IN}$. (2) See "Isolation Voltage Ratings" on page 5. The input to output and channel to channel continuous AC rating is 700Vrms. (3) See "Typical Performance Curves." (4) A minimum output current of 3mA at each output is recommended to maintain output voltage accuracy. (5) Test bandwidth 10MHz, max.

## CONNECTION DIAGRAMS

**Top View**




## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| 724 | 20-Pin | 102 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

# 6 Optical Sensors

Optical Electronic Integrated Sensors (OEICs) combine the building blocks traditionally used in a transimpedance amplifier on a single monolithic die. The photodiode; low noise, low bias current FET-input operational amplifier, and feedback network are matched to optimize performance.

Our monolithic sensor/amplifier combinations free designers from the tedious design rules necessary to optimize responsivity and speed while maintaining stability and minimal gain peaking in discrete solutions. Other errors that are reduced by a monolithic solution are leakage current errors and noise.

Light falling on the photodiode section of the die is converted to a current. The op amp is connected as a transimpedance amplifier, converting the photodiode current into an output voltage which is proportional to the intensity and wavelength of the light.

Several products and package options are available to allow flexibility in configuring light measurement systems. An external resistor can be placed in series with the internal 1MΩ to increase responsivity in all packages, or placed in parallel to reduce the overall responsivity (in all packages except the SIP).

**OPT101**—This device was designed to operate on a single power supply of +2.7V to +36V, with a quiescent current of only 120µA at dark. Response peaks at 850nm with a response of 0.6A/W.

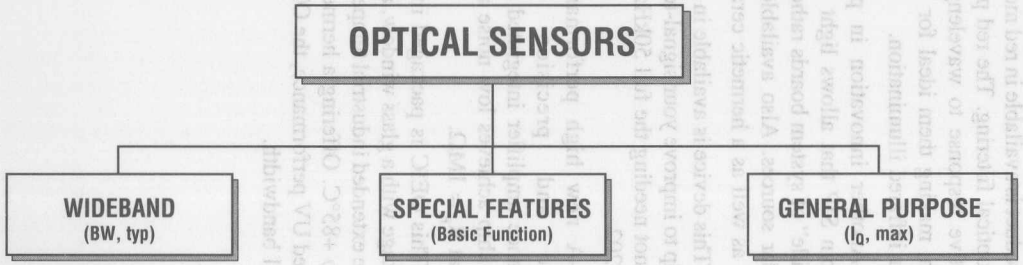
**OPT101-R**—A new innovation in package design, this product is available in red molded plastic to provide optical filtering. The red package provides selective response to wavelengths greater than 570nm, making them ideal for applications using red or infrared illumination.

**OPT202**—Another innovation in package design—a 5-pin SIP that allows light to originate from the "side" of system boards rather than from perpendicular sources. Also available in a clear plastic DIP as well as a hermetic ceramic DIP.

**OPT209**—This device is available in plastic DIP, and will help to improve your signal-to-noise ratio in systems not needing the full 50kHz bandwidth of the OPT202.

**OPT210**—A new high performance silicon photodiode and precision FET-input transimpedance amplifier integrated on a single monolithic chip achieves low noise and 300kHz bandwidth at $R_F$ = 1MΩ.

**OPT301**—This OEIC is packaged in a hermetic TO-99 package with a glass window, and is specified over the extended industrial temperature range of –40°C to +85°C. Offering a hermetic package and enhanced UV performance, the OPT301 has a 4kHz signal bandwidth.




**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMEN***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specificatic

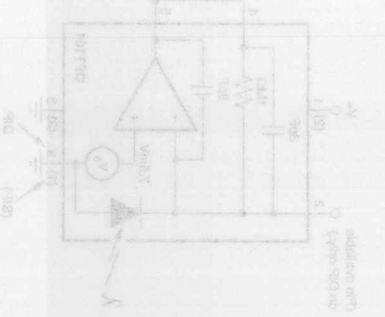


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## Optical Electric Integrated Circuits

| Product | Small Signal Bandwidth typ (kHz) | Photodiode Dimensions | Feedback Resistor typ | Dark Error max (mV) | Power Supply Range (mV) | Quiescent Current max (μA) | Description |
|---|---|---|---|---|---|---|---|
| OPT101 | 14 | 0.09" x 0.09" | 1MΩ or external | +5 to +10 (offset for single single supply) | +2.7V to +36V | 240 | Low cost, general purpose. Single supply operation with nominal 7.5mV output offset pedestal. |
| OPT210 | (900 with external bootstrap buffer) | 0.09" x 0.09" | 1MΩ internal or external | ±10 | ±2.25V to ±18V | 4000 | Wide bandwidth with infrared response and extended bandwidth using bootstrap buffer. |
| OPT301[1] | 4 | 0.09" x 0.09" | 1MΩ or external | ±2 | ±2.25V to ±18V | 500 | Hermetic, general purpose, extended ultraviolet response, wide temp |

NOTES: (1) Hermetic, TO-99 package with glass window operating over Mil temperature range (–55°C to 125°C).

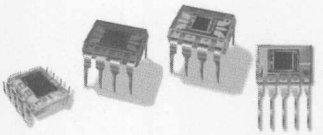


**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

BURR-BROWN®



# OPT101

www.burr-brown.com/databook/OPT101.html

# MONOLITHIC PHOTODIODE AND SINGLE-SUPPLY TRANSIMPEDANCE AMPLIFIER

## FEATURES

- SINGLE SUPPLY: +2.7 to +36V
- PHOTODIODE SIZE: 0.090 x 0.090 inch
- INTERNAL 1MΩ FEEDBACK RESISTOR
- HIGH RESPONSIVITY: 0.45A/W (650nm)
- BANDWIDTH: 14kHz at $R_F$ = 1MΩ
- LOW QUIESCENT CURRENT: 120μA
- AVAILABLE IN 8-PIN DIP, 5-PIN SIP, AND 8-LEAD SURFACE MOUNT PACKAGES

## APPLICATIONS

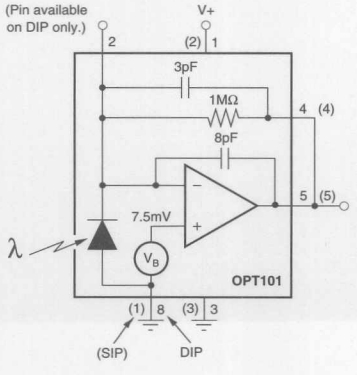
- MEDICAL INSTRUMENTATION
- LABORATORY INSTRUMENTATION
- POSITION AND PROXIMITY SENSORS
- PHOTOGRAPHIC ANALYZERS
- BARCODE SCANNERS
- SMOKE DETECTORS
- CURRENCY CHANGERS

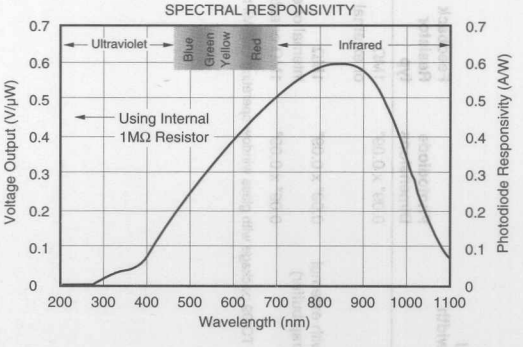
## DESCRIPTION

The OPT101 is a monolithic photodiode with on-chip transimpedance amplifier. Output voltage increases linearly with light intensity. The amplifier is designed for single or dual power supply operation, making it ideal for battery operated equipment.

The integrated combination of photodiode and transimpedance amplifier on a single chip eliminates the problems commonly encountered in discrete designs such as leakage current errors, noise pick-up and gain peaking due to stray capacitance. The 0.09 x 0.09 inch photodiode is operated in the photoconductive mode for excellent linearity and low dark current.

The OPT101 operates from +2.7V to +36V supplies and quiescent current is only 120μA. It is available in clear plastic 8-pin DIP, 5-pin SIP and J-formed DIP for surface mounting. Temperature range is 0°C to 70°C.




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# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = +2.7V to +36V, λ = 650nm, internal 1MΩ feedback resistor, and $R_L$ = 10kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | OPT101P, W MIN | OPT101P, W TYP | OPT101P, W MAX | UNITS |
|---|---|---|---|---|---|
| **RESPONSIVITY** | | | | | |
| Photodiode Current | 650nm | | 0.45 | | A/W |
| Voltage Output | 650nm | | 0.45 | | V/µW |
| vs Temperature | | | 100 | | ppm/°C |
| Unit to Unit Variation | 650nm | | ±5 | | % |
| Nonlinearity[1] | FS Output = 24V | | ±0.01 | | % of FS |
| Photodiode Area | (0.090 x 0.090in) | | 0.008 | | in² |
| | (2.29 x 2.29mm) | | 5.2 | | mm² |
| **DARK ERRORS, RTO[2]** | | | | | |
| Offset Voltage, Output | | +5 | +7.5 | +10 | mV |
| vs Temperature | | | ±2.5 | | µV/°C |
| vs Power Supply | $V_S$ = +2.7V to +36V | | 10 | 100 | µV/V |
| Voltage Noise, Dark, $f_B$ = 0.1Hz to 20kHz | $V_S$ = +15V, $V_{PIN3}$ = –15V | | 300 | | µVrms |
| **TRANSIMPEDANCE GAIN** | | | | | |
| Resistor | | | 1 | | MΩ |
| Tolerance, P | | | ±0.5 | ±2 | % |
| W | | | ±0.5 | | % |
| vs Temperature | | | ±50 | | ppm/°C |
| **FREQUENCY RESPONSE** | | | | | |
| Bandwidth | $V_{OUT}$ = 10Vp-p | | 14 | | kHz |
| Rise Fall Time, 10% to 90% | $V_{OUT}$ = 10V Step | | 28 | | µs |
| Settling Time, 0.05% | $V_{OUT}$ = 10V Step | | 160 | | µs |
| 0.1% | | | 80 | | µs |
| 1% | | | 70 | | µs |
| Overload Recovery | 100%, Return to Linear Operation | | 50 | | µs |
| **OUTPUT** | | | | | |
| Voltage Output, High | | ($V_S$) – 1.3 | ($V_S$) – 1.15 | | V |
| Capacitive Load, Stable Operation | | | 10 | | nF |
| Short-Circuit Current | $V_S$ = 36V | | 15 | | mA |
| **POWER SUPPLY** | | | | | |
| Operating Voltage Range | | +2.7 | | +36 | V |
| Quiescent Current | Dark, $V_{PIN3}$ = 0V | | 120 | 240 | µA |
| | $R_L$ = ∞, $V_{OUT}$ = 10V | | 220 | | µA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | 0 | | +70 | °C |
| Operating | | 0 | | +70 | °C |
| Storage | | –25 | | +85 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | 100 | | °C/W |

NOTES: (1) Deviation in percent of full scale from best-fit straight line. (2) Referred to Output. Includes all error sources.

# PHOTODIODE SPECIFICATIONS

$T_A$ = +25°C, $V_S$ = +2.7V to +36V unless otherwise noted.

| PARAMETER | CONDITIONS | Photodiode of OPT101P MIN | Photodiode of OPT101P TYP | Photodiode of OPT101P MAX | UNITS |
|---|---|---|---|---|---|
| Photodiode Area | (0.090 x 0.090in) | | 0.008 | | in² |
| | (2.29 x 2.29mm) | | 5.2 | | mm² |
| Current Responsivity | 650nm | | 0.45 | | A/W |
| | 650nm | | 865 | | µA/W/cm² |
| Dark Current | $V_{DIODE}$ = 7.5mV | | 2.5 | | pA |
| vs Temperature | | | doubles every 7°C | | |
| Capacitance | | | 1200 | | pF |



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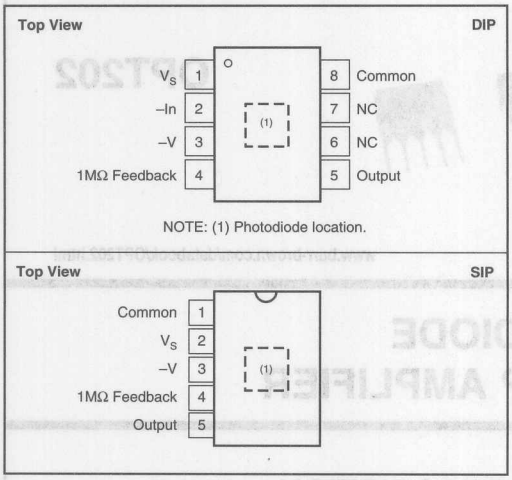
# OP AMP SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = +2.7V to +36V, λ = 650nm, internal 1MΩ feedback resistor, and $R_L$ = 10kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | OPT101 Op Amp[1] MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT** | | | | | |
| Offset Voltage | | | ±0.5 | | mV |
| vs Temperature | | | ±2.5 | | µV/°C |
| vs Power Supply | | | 10 | | µV/V |
| Input Bias Current | (–) Input | | 165 | | pA |
| vs Temperature | (–) Input | | 1 | | pA/°C |
| Input Impedance | | | | | |
| Differential | | | 400 ll 5 | | MΩ ll pF |
| Common-Mode | | | 250 ll 35 | | GΩ ll pF |
| Common-Mode Input Voltage Range | Linear Operation | | 0 to [($V_S$) – 1] | | V |
| Common-Mode Rejection | | | 90 | | dB |
| **OPEN-LOOP GAIN** | | | | | |
| Open-loop Voltage Gain | | | 90 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product[2] | | | 2 | | MHz |
| Slew Rate | | | 1 | | V/µs |
| Settling Time 1% | | | 5.8 | | µs |
| 0.1% | | | 7.7 | | µs |
| 0.05% | | | 8.0 | | µs |
| **OUTPUT** | | | | | |
| Voltage Output, High | | ($V_S$) – 1.3 | ($V_S$) – 1.15 | | V |
| Short-Circuit Current | $V_S$ = +36V | | 15 | | mA |
| **POWER SUPPLY** | | | | | |
| Operating Voltage Range | | +2.7 | | +36 | V |
| Quiescent Current | Dark, $V_{PIN3}$ = 0V | | 120 | 240 | µA |
| | $R_L$ ∞, $V_{OUT}$ = 10V | | 220 | | µA |

NOTES: (1) Op amp specifications provided for information and comparison only. (2) Stable gains ≥ 10V/V.

## PIN CONFIGURATIONS




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage ($V_S$ to *"Common"* or pin 3) | 0 to +36V |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | –25°C to +85°C |
| Storage Temperature | –25°C to +85°C |
| Junction Temperature | +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (Vapor-Phase Soldering Not Recommended) | |

## PACKAGE INFORMATION

| PRODUCT | COLOR | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|---|
| OPT101P | Clear | 8-Pin Plastic DIP | 006-1 |
| OPT101P-J | Clear | 8-Lead Surface Mount (2) | 006-4 |
| OPT101W | Clear | 5-Pin Plastic SIP | 321 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) 8-pin DIP with J-formed leads for surface mounting.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

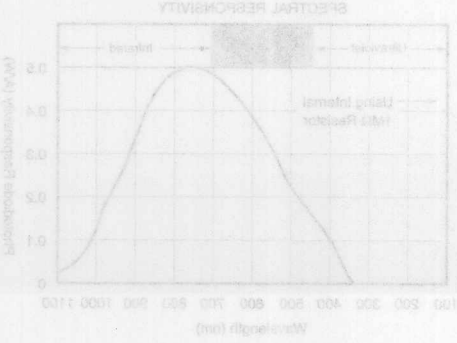
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

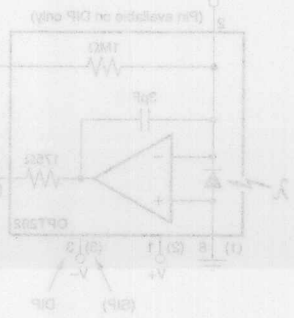
## MOISTURE SENSITIVITY AND SOLDERING

Clear plastic does not contain the structural-enhancing fillers used in black plastic molding compound. As a result, clear plastic is more sensitive to environmental stress than black plastic. This can cause difficulties if devices have been stored in high humidity prior to soldering. The rapid heating during soldering can stress wire bonds and cause failures. Prior to soldering, it is recommended that plastic devices be baked-out at +85°C for 24 hours.

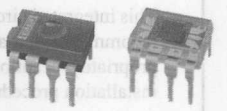
The fire-retardant fillers used in black plastic are not compatible with clear molding compound. The OPT101 plastic packages cannot meet flammability test, UL-94.







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# OPT202

www.burr-brown.com/databook/OPT202.html

# PHOTODIODE WITH ON-CHIP AMPLIFIER

## FEATURES

- BANDWIDTH: 50kHz
- PHOTODIODE SIZE: 0.090 x 0.090 inch (2.29 x 2.29mm)
- 1MΩ FEEDBACK RESISTOR
- HIGH RESPONSIVITY: 0.45A/W (650nm)
- LOW DARK ERRORS: 2mV
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 400µA
- TRANSPARENT 8-PIN DIP AND 5-PIN SIP
- HERMETIC 8-PIN CERAMIC DIP

## APPLICATIONS

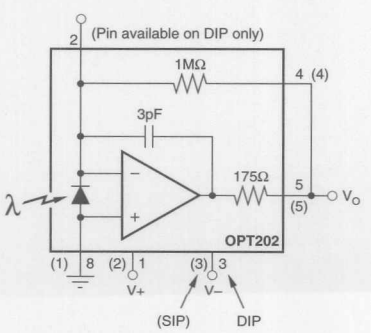
- MEDICAL INSTRUMENTATION
- LABORATORY INSTRUMENTATION
- POSITION AND PROXIMITY SENSORS
- PHOTOGRAPHIC ANALYZERS
- SMOKE DETECTORS

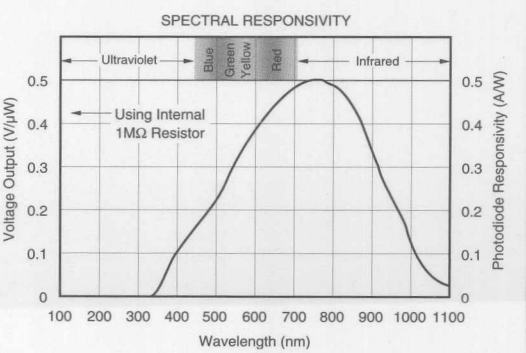
## DESCRIPTION

The OPT202 is an opto-electronic integrated circuit containing a photodiode and transimpedance amplifier on a single dielectrically isolated chip. The transimpedance amplifier consists of a precision FET-input op amp and an on-chip metal film resistor. The 0.09 x 0.09 inch photodiode is operated at zero bias for excellent linearity and low dark current.

The integrated combination of photodiode and transimpedance amplifier on a single chip eliminates the problems commonly encountered in discrete designs such as leakage current errors, noise pick-up and gain peaking due to stray capacitance.

The OPT202 operates over a wide supply range (±2.25 to ±18V) and supply current is only 400µA. It is packaged in a transparent plastic 8-pin DIP or 5-pin SIP, specified for the 0°C to +70°C temperature range as well as a hermetic ceramic 8-pin DIP with a glass window, specified for the –40°C to +85°C temperature range.




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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $V_S$ = ±15V, λ = 650nm, internal 1MΩ feedback resistor, unless otherwise noted.

| PARAMETER | CONDITIONS | OPT202P, W, G MIN | OPT202P, W, G TYP | OPT202P, W, G MAX | UNITS |
|---|---|---|---|---|---|
| **RESPONSIVITY** | | | | | |
| Photodiode Current | 650nm | | 0.45 | | A/W |
| Voltage Output | 650nm | | 0.45 | | V/µW |
| vs Temperature | | | 100 | | ppm/°C |
| Unit-to-Unit Variation | 650nm | | ±5 | | % |
| Nonlinearity(1) | FS Output = 10V | | 0.01 | | % of FS |
| Photodiode Area | (0.090 x 0.090in) | | 0.008 | | $in^2$ |
| | (2.29 x 2.29mm) | | 5.2 | | $mm^2$ |
| **DARK ERRORS, RTO(2)** | | | | | |
| Offset Voltage, Output: P, W Packages | | | ±0.5 | ±2 | mV |
| G Package | | | ±0.5 | ±3 | mV |
| vs Temperature | | | ±10 | | µV/°C |
| vs Power Supply | $V_S$ = ±2.25V to ±18V | | 10 | 100 | µV/V |
| Voltage Noise | Measured BW = 0.1Hz to 100kHz | | 1 | | mVrms |
| **RESISTOR—1MΩ Internal** | | | | | |
| Resistance | | | 1 | | MΩ |
| Tolerance: P, G Packages | | | ±0.5 | ±2 | % |
| W Package | | | ±0.5 | | % |
| vs Temperature | | | 50 | | ppm/°C |
| **FREQUENCY RESPONSE** | | | | | |
| Bandwidth, Large or Small-Signal, –3dB | | | 50 | | kHz |
| Rise Time, 10% to 90% | | | 10 | | µs |
| Settling Time, 1% | FS to Dark | | 10 | | µs |
| 0.1% | FS to Dark | | 20 | | µs |
| 0.01% | FS to Dark | | 40 | | µs |
| Overload Recovery Time (to 1%) | 100% Overdrive, $V_S$ = ±15V | | 44 | | µs |
| | 100% Overdrive, $V_S$ = ±5V | | 100 | | µs |
| | 100% Overdrive, $V_S$ = ±2.25V | | 240 | | µs |
| **OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 10kΩ | (V+) – 1.25 | (V+) – 1 | | V |
| | $R_L$ = 5kΩ | (V+) – 2 | (V+) – 1.5 | | V |
| Capacitive Load, Stable Operation | | | 10 | | nF |
| Short-Circuit Current | | | ±18 | | mA |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±15 | | V |
| Operating Voltage Range | | ±2.25 | | ±18 | V |
| Quiescent Current | $V_O$ = 0 | | ±400 | ±500 | µA |
| **TEMPERATURE RANGE** | | | | | |
| Specification; P, W Packages | | 0 | | +70 | °C |
| G Package | | –40 | | +85 | °C |
| Operating, P, W Packages | | 0 | | +70 | °C |
| G Package | | –55 | | +125 | °C |
| Storage P, W Packages | | –25 | | +85 | °C |
| G Package | | –55 | | +125 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | 100 | | °C/W |

NOTES: (1) Deviation in percent of full scale from best-fit straight line. (2) Referred to Output. Includes all error sources.

## ELECTRICAL

### Op Amp Section of OPT202[1]

At $T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

| PARAMETER | CONDITIONS | OPT202 Op Amp MIN | OPT202 Op Amp TYP | OPT202 Op Amp MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT** | | | | | |
| Offset Voltage | | | ±0.5 | | mV |
| vs Temperature | | | ±5 | | µV/°C |
| vs Power Supply | $V_S$ = ±2.25V to ±18V | | 10 | | µV/V |
| Input Bias Current | | | 1 | | pA |
| vs Temperature | | | doubles every 10°C | | |
| **NOISE** | | | | | |
| Input Voltage Noise | | | | | |
| Voltage Noise Density, f = 10Hz | | | 30 | | $nV/\sqrt{Hz}$ |
| f = 100Hz | | | 25 | | $nV/\sqrt{Hz}$ |
| f = 1kHz | | | 15 | | $nV/\sqrt{Hz}$ |
| Current Noise Density, f = 1kHz | | | 0.8 | | $fA/\sqrt{Hz}$ |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range | | | ±14.4 | | V |
| Common-Mode Rejection | | | 106 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $10^{12}$\|\|3 | | Ω \|\| pF |
| Common-Mode | | | $10^{12}$\|\|3 | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | | | 120 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product | | | 16 | | MHz |
| Slew Rate | | | 6 | | V/µs |
| Settling Time 0.1% | | | 4 | | µs |
| 0.01% | | | 5 | | µs |
| **OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 10kΩ | (V+) – 1.25 | (V+) – 1 | | V |
| | $R_L$ = 5kΩ | (V+) – 2 | (V+) – 1.5 | | V |
| Short-Circuit Current | | | ±18 | | mA |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±15 | | V |
| Operating Voltage Range | | ±2.25 | | ±18 | V |
| Quiescent Current | $I_O$ = 0 | | ±400 | ±500 | µA |

NOTE: (1) Op amp specifications provided for information and comparison only.

# PHOTODIODE SPECIFICATIONS

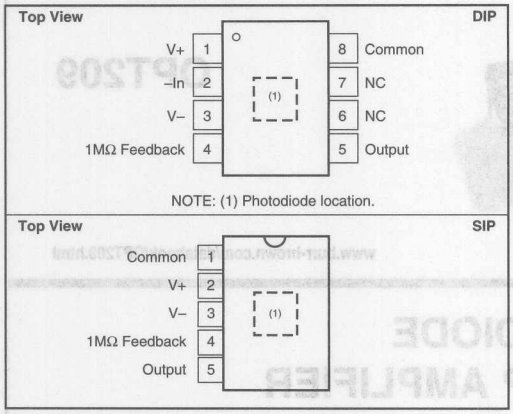
At $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | Photodiode of OPT202 MIN | Photodiode of OPT202 TYP | Photodiode of OPT202 MAX | UNITS |
|---|---|---|---|---|---|
| Photodiode Area | (0.090 x 0.090in) | | 0.008 | | $in^2$ |
| | (2.29 x 2.29mm) | | 5.2 | | $mm^2$ |
| Current Responsivity | 650nm | | 0.45 | | A/W |
| Dark Current | $V_D$ = 0V[1] | | 500 | | fA |
| vs Temperature | | | doubles every 10°C | | |
| Capacitance | $V_D$ = 0V[1] | | 600 | | pF |

NOTE: (1) Voltage Across Photodiode.

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## PIN CONFIGURATIONS




## ABSOLUTE MAXIMUM RATINGS

| | | |
|---|---|---|
| Supply Voltage | | ±18V |
| Input Voltage Range (Common Pin) | | $\pm V_S$ |
| Output Short-Circuit (to ground) | | Continuous |
| Operating Temperature: | P, W | –25°C to +85°C |
| | G | –55°C to +125°C |
| Storage Temperature: | P, W | –25°C to +85°C |
| | G | –55°C to +125°C |
| Junction Temperature: | P, W | +85°C |
| | G | +150°C |
| Lead Temperature (soldering, 10s) | | +300°C |
| (Vapor-Phase Soldering Not Recommended on Plastic Packages) | | |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| OPT202P | 8-Pin Plastic DIP | 006-1 |
| OPT202W | 5-Pin Plastic SIP | 321 |
| OPT202G | 8-Pin Ceramic DIP | 161-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

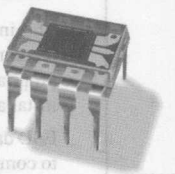
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## MOISTURE SENSITIVITY AND SOLDERING

Clear plastic does not contain the structural-enhancing fillers used in black plastic molding compound. As a result, clear plastic is more sensitive to environmental stress than black plastic. This can cause difficulties if devices have been stored in high humidity prior to soldering. The rapid heating during soldering can stress wire bonds and cause failures. Prior to soldering, it is recommended that plastic devices be baked-out at 85°C for 24 hours.

The fire-retardant fillers used in black plastic are not compatible with clear molding compound. The OPT202 plastic packages cannot meet flammability test, UL-94.

BURR-BROWN®



# OPT209

www.burr-brown.com/databook/OPT209.html

# PHOTODIODE WITH ON-CHIP AMPLIFIER

## FEATURES

- PHOTODIODE SIZE: 0.090 x 0.090 inch (2.29 x 2.29mm)
- 1MΩ FEEDBACK RESISTOR
- HIGH RESPONSIVITY: 0.45A/W (650nm)
- LOW DARK ERRORS: 2mV
- BANDWIDTH: 16kHz
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 400µA
- TRANSPARENT 8-PIN DIP

## APPLICATIONS

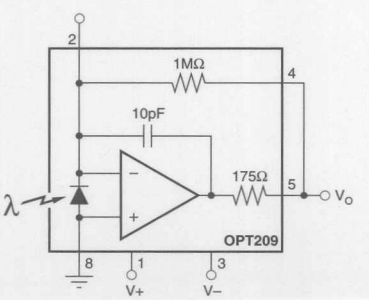
- MEDICAL INSTRUMENTATION
- LABORATORY INSTRUMENTATION
- POSITION AND PROXIMITY SENSORS
- PHOTOGRAPHIC ANALYZERS
- SMOKE DETECTORS

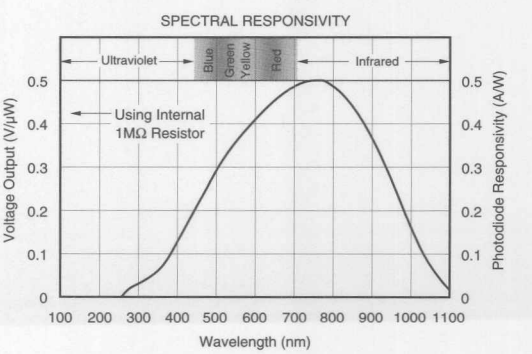
## DESCRIPTION

The OPT209 is an opto-electronic integrated circuit containing a photodiode and transimpedance amplifier on a single dielectrically isolated chip. The transimpedance amplifier consists of a precision FET-input op amp and an on-chip metal film resistor. The 0.09 x 0.09 inch photodiode is operated at zero bias for excellent linearity and low dark current.

The integrated combination of photodiode and transimpedance amplifier on a single chip eliminates the problems commonly encountered in discrete designs such as leakage current errors, noise pick-up and gain peaking due to stray capacitance.

The OPT209 operates over a wide supply range (±2.25 to ±18V) and supply current is only 400µA. It is packaged in a transparent plastic 8-pin DIP, specified for the 0°C to 70°C temperature range.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $V_S$ = ±15V, λ = 650nm, internal 1MΩ feedback resistor, unless otherwise noted.

| PARAMETER | CONDITIONS | OPT209P MIN | OPT209P TYP | OPT209P MAX | UNITS |
|---|---|---|---|---|---|
| **RESPONSIVITY** | | | | | |
| Photodiode Current | 650nm | | 0.45 | | A/W |
| Voltage Output | 650nm | | 0.45 | | V/µW |
| vs Temperature | | | 100 | | ppm/°C |
| Unit-to-Unit Variation | 650nm | | ±5 | | % |
| Nonlinearity(1) | FS Output = 10V | | 0.01 | | % of FS |
| Photodiode Area | (0.090 x 0.090in) | | 0.008 | | $in^2$ |
| | (2.29 x 2.29mm) | | 5.2 | | $mm^2$ |
| **DARK ERRORS, RTO(2)** | | | | | |
| Offset Voltage, Output | | | ±0.5 | ±2 | mV |
| vs Temperature | | | ±10 | | µV/°C |
| vs Power Supply | $V_S$ = ±2.25V to ±18V | | 10 | 100 | µV/V |
| Voltage Noise | Measured BW = 0.1 to 100kHz | | 350 | | µVrms |
| **RESISTOR—1MΩ Internal** | | | | | |
| Resistance | | | 1 | | MΩ |
| Tolerance | | | ±0.5 | ±2 | % |
| vs Temperature | | | 50 | | ppm/°C |
| **FREQUENCY RESPONSE** | | | | | |
| Bandwidth, Large or Small-Signal, –3dB | | | 16 | | kHz |
| Rise Time, 10% to 90% | | | 22 | | µs |
| Settling Time, 1% | FS to Dark | | 60 | | µs |
| 0.1% | FS to Dark | | 85 | | µs |
| 0.01% | FS to Dark | | 100 | | µs |
| Overload Recovery Time (to 1%) | 100% 0verdrive, $V_S$ = ±15V | | 44 | | µs |
| | 100% 0verdrive, $V_S$ = ±5V | | 100 | | µs |
| | 100% 0verdrive, $V_S$ = ±2.25V | | 240 | | µs |
| **OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 10kΩ | (V+) – 1.25 | (V+) – 1 | | V |
| | $R_L$ = 5kΩ | (V+) – 2 | (V+) – 1.5 | | V |
| Capacitive Load, Stable Operation | | | 1 | | nF |
| Short-Circuit Current | | | ±18 | | mA |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±15 | | V |
| Operating Voltage Range | | ±2.25 | | ±18 | V |
| Quiescent Current | $V_O$ = 0 | | ±400 | ±500 | µA |
| **TEMPERATURE RANGE** | | | | | |
| Specification, Operating | | 0 | | +70 | °C |
| Storage | | –25 | | +85 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | 100 | | °C/W |

NOTES: (1) Deviation in percent of full scale from best-fit straight line. (2) Referred to Output. Includes all error sources.

# PHOTODIODE SPECIFICATIONS

At $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | Photodiode of OPT209 MIN | Photodiode of OPT209 TYP | Photodiode of OPT209 MAX | UNITS |
|---|---|---|---|---|---|
| Photodiode Area | (0.090 x 0.090in) | | 0.008 | | $in^2$ |
| | (2.29 x 2.29mm) | | 5.1 | | $mm^2$ |
| Current Responsivity | 650nm | | 0.45 | | A/W |
| Dark Current | $V_D$ = 0V(1) | | 500 | | fA |
| vs Temperature | | | doubles every 10°C | | |
| Capacitance | $V_D$ = 0V(1) | | 600 | | pF |

NOTE: (1) Voltage Across Photodiode.

## ELECTRICAL

### Op Amp Section of OPT209[1]

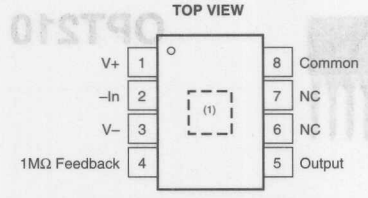
At $T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

| PARAMETER | CONDITIONS | OPT209 Op Amp MIN | OPT209 Op Amp TYP | OPT209 Op Amp MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT** | | | | | |
| Offset Voltage | | | ±0.5 | | mV |
| vs Temperature | | | ±5 | | µV/°C |
| vs Power Supply | $V_S$ = ±2.25V to ±18V | | 10 | | µV/V |
| Input Bias Current | | | 1 | | pA |
| vs Temperature | | | doubles every 10°C | | |
| **NOISE** | | | | | |
| Input Voltage Noise | | | | | |
| Voltage Noise Density, f=10Hz | | | 30 | | nV/√Hz |
| f=100Hz | | | 25 | | nV/√Hz |
| f=1kHz | | | 15 | | nV/√Hz |
| Current Noise Density, f=1kHz | | | 0.8 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range | | | ±14.4 | | V |
| Common-Mode Rejection | | | 106 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $10^{12}$\|\|3 | | Ω\|\|pF |
| Common-Mode | | | $10^{12}$\|\|3 | | Ω\|\|pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | | | 120 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product | | | 4 | | MHz |
| Slew Rate | | | 6 | | V/µs |
| Settling Time 0.1% | | | 4 | | µs |
| 0.01% | | | 5 | | µs |
| **OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 10kΩ | (V+) – 1.25 | (V+) – 1 | | V |
| | $R_L$ = 5kΩ | (V+) – 2 | (V+) – 1.5 | | V |
| Short-Circuit Current | | | ±18 | | mA |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±15 | | V |
| Operating Voltage Range | | ±2.25 | | ±18 | V |
| Quiescent Current | $I_O$ = 0 | | ±400 | ±500 | µA |

NOTE: (1) Op amp specifications provided for information and comparison only.

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## PIN CONFIGURATION




NOTE: (1) Photodiode location.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Input Voltage Range (Common Pin) | $\pm V_S$ |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | –25°C to +85°C |
| Storage Temperature | –25°C to +85°C |
| Junction Temperature | +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (Vapor-Phase Soldering Not Recommended) | |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| OPT209P | 8-Pin DIP | 006-1 |
| OPT209P-J | 8-Lead Surface Mount[2] | 006-4 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) 8-Pin DIP with leads formed for surface mounting.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

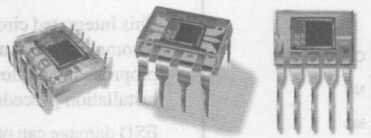
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## MOISTURE SENSITIVITY AND SOLDERING

Clear plastic does not contain the structural-enhancing fillers used in black plastic molding compound. As a result, clear plastic is more sensitive to environmental stress than black plastic. This can cause difficulties if devices have been stored in high humidity prior to soldering. The rapid heating during soldering can stress wire bonds and cause failures. Prior to soldering, it is recommended that devices be baked-out at 85°C for 24 hours.

The fire-retardant fillers used in black plastic are not compatible with clear molding compound. The OPT209 cannot meet flammability test, UL-94.

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# OPT210

www.burr-brown.com/databook/OPT210.html

# MONOLITHIC PHOTODIODE AND AMPLIFIER
# 300kHz Bandwidth at $R_F$ = 1MΩ

## FEATURES

- BOOTSTRAP ANODE DRIVE: Extends Bandwidth: 900kHz ($R_F$ = 100KΩ) Reduces Noise
- LARGE PHOTODIODE: 0.09" x 0.09"
- HIGH RESPONSIVITY: 0.45A/W (650nm)
- EXCELLENT SPECTRAL RESPONSE
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- TRANSPARENT DIP, SIP AND SURFACE-MOUNT PACKAGES

## APPLICATIONS

- BARCODE SCANNERS
- MEDICAL INSTRUMENTATION
- LABORATORY INSTRUMENTATION
- POSITION AND PROXIMITY DETECTORS
- PARTICLE DETECTORS

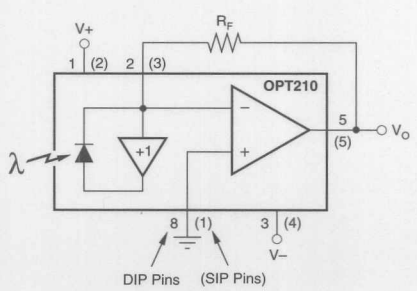
## DESCRIPTION

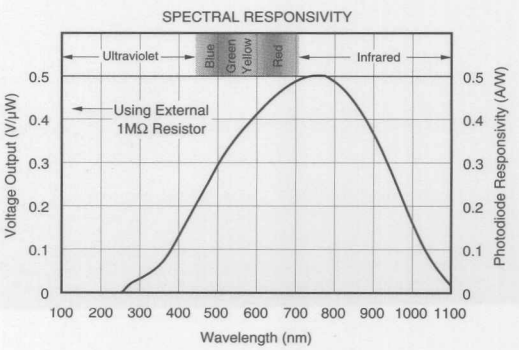
The OPT210 is a photodetector consisting of a high performance silicon photodiode and precision FET-input transimpedance amplifier integrated on a single monolithic chip. Output is an analog voltage proportional to light intensity.

The large 0.09" x 0.09" photodiode is operated at low bias voltage for low dark current and excellent linearity. A novel photodiode anode bootstrap circuit reduces the effects of photodiode capacitance to extend bandwidth and reduces noise.

The integrated combination of photodiode and transimpedance amplifier on a single chip eliminates the problems commonly encountered with discrete designs such as leakage current errors, noise pick-up and gain peaking due to stray capacitance.

The OPT210 operates from ±2.25 to ±18V supplies and quiescent current is only 2mA. Available in a transparent 8-pin DIP, 8-lead surface-mount and 5-pin SIP, it is specified for 0° to 70°C operation.




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# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = ±15V, λ = 650nm, External $R_F$ = 1MΩ, $R_L$ = 10kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | OPT210P OPT210W MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **RESPONSIVITY** | | | | | |
| Photodiode Current | λ = 650nm | | 0.45 | | A/W |
| Unit-to-Unit Variation | | | ±5 | | % |
| Voltage Output | λ = 650nm, External $R_F$ = 1MΩ | | 0.45 | | V/µW |
| Nonlinearity | | | 0.01 | | % of FS |
| Photodiode Area | (0.09 x 0.09in) | | 0.008 | | in² |
| | (2.29 x 2.29mm) | | 5.2 | | mm² |
| **DARK ERROR, RTO** | | | | | |
| Offset Voltage | | | ±2 | ±10 | mV |
| vs Temperature | | | ±35 | | µV/°C |
| vs Power Supply | $V_S$ = ±2.25V to ±18V | | 100 | 1000 | µV/V |
| Voltage Noise | BW = 0.01Hz to 100kHz | | 160 | | µVrms |
| **FREQUENCY RESPONSE** | | | | | |
| Bandwidth | External $R_F$ = 1MΩ | | 300 | | kHz |
| Rise Time | 10% to 90% | | 1.2 | | µs |
| Settling Time, 1% | FS to Dark step | | 3 | | µs |
| 0.1% | | | 8 | | µs |
| 0.01% | | | 20 | | µs |
| Overload Recovery | 100% Overdrive | | 7 | | µs |
| **OUTPUT** | | | | | |
| Voltage Output, Positive | $R_L$ = 10kΩ | (V+)–1.25 | (V+)–0.75 | | V |
| Positive | $R_L$ = 5kΩ | | (V+)–1 | | |
| Negative[1] | $R_L$ = 10kΩ | –0.4 | –0.5 | | V |
| Capacitive Load, Stable Operation | | | 500 | | pF |
| Short-Circuit Current[2] | | | +50 | | mA |
| **POWER SUPPLY** | | | | | |
| Operating Range | | ±2.25 | | ±18 | V |
| Quiescent Current | | | +2.0/–1.7 | ±4 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | 0 | | 70 | °C |
| Operating | | 0 | | 70 | °C |
| Storage | | –25 | | 85 | °C |
| $\theta_{JA}$ | | | 100 | | °C/W |

NOTES: (1) Output typically swings to 0.5V below the voltage applied to the non-inverting input terminal, which is normally connected to ground. (2) Positive current (sourcing) is limited. Negative current (sinking) is not limited.

# PHOTODIODE SPECIFICATIONS

| PARAMETER | CONDITIONS | PHOTODIODE MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Photodiode Area | (0.09 x 0.09in) | | 0.008 | | in² |
| | (2.29 x 2.29mm) | | 5.2 | | mm² |
| Current Responsivity | λ = 650nm | | 0.45 | | A/W |
| | | | 865 | | µA/W/cm² |
| Dark Current | $V_D$ = –1.2V | | 70 | | pA |
| vs Temperature | | | Doubles every 10°C | | |
| Capacitance | $V_D$ = –1.2V | | 550 | | pF |
| Effective Capacitance[1] | $V_D$ = –1.2V | | 10 | | pF |

NOTES: (1) Effect of photodiode capacitance is reduced by internal buffer bootstrap drive. See text

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Op amp specifications provided for comparative information only.

| PARAMETER | CONDITIONS | OP AMP MIN | OP AMP TYP | OP AMP MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT** | | | | | |
| Offset Voltage | | | ±2 | | mV |
| vs Temperature | | | ±35 | | µV/°C |
| vs Power Supply | | | 100 | | µV/V |
| Input Bias Current | | | | | |
| Inverting Input | | | 15 | | pA |
| vs Temperature | | | Doubles every 10°C | | |
| Non-inverting Input | | | 300 | | µA |
| **NOISE** | | | | | |
| Voltage Noise | | | | | |
| f = 10Hz | | | 20 | | nV/√Hz |
| f = 100Hz | | | 9 | | nV/√Hz |
| f = 1kHz | | | 6 | | nV/√Hz |
| Current Noise Density, Inverting Input | BW = 0.01Hz to 100kHz | | 0.8 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range[1] | | | $V_S$±2.25 | | V |
| Common-Mode Rejection | | | 65 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Inverting Input Impedance | | | $3x10^{10}$\|\|3 | | Ω \|\| pF |
| Non-Inverting Input Impedance | | | 250 | | kΩ |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | $V_O$ = 0V to +13.75V | | 70 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Bandwidth, Small Signal | | | 35 | | MHz |
| Rise Time, Large Signal | 10% to 90% | | 25 | | ns |
| Settling Time, 1% | 10V step | | 240 | | ns |
| 0.1% | | | 390 | | ns |
| 0.01% | | | 800 | | ns |
| Overload Recovery | 100% Overdrive | | 7 | | µs |
| **OUTPUT** | | | | | |
| Voltage Output, Positive | $R_L$ = 10kΩ | (V+)–1.25 | (V+)–0.75 | | V |
| Positive | $R_L$ = 5kΩ | | (V+)–1 | | |
| Negative[1] | $R_L$ = 10kΩ | –0.4 | –0.5 | | V |
| Capacitive Load, Stable Operation | | | 500 | | pF |
| Short-Circuit Current[2] | | | +50 | | mA |
| **POWER SUPPLY** | | | | | |
| Operating Voltage | | ±2.25 | | ±18 | V |
| Quiescent Current | | | +1.7/–1.4 | ±4 | mA |

NOTES: (1) Output typically swings to 0.5V below the voltage applied to the non-inverting input terminal, which is normally connected to ground. (2) Positive current (sourcing) is limited. Negative current (sinking) is not limited.

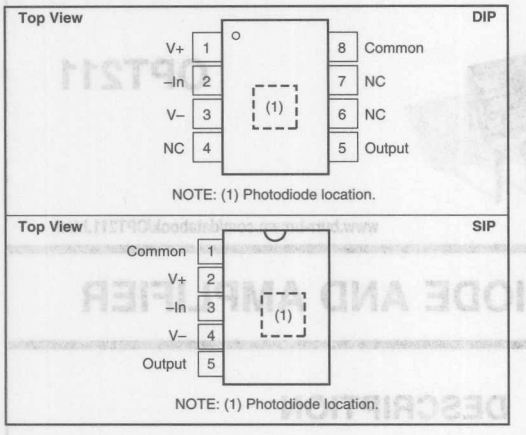
# BUFFER SPECIFICATIONS

Buffer specifications provided for comparative information only.

| PARAMETER | CONDITIONS | BUFFER MIN | BUFFER TYP | BUFFER MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT** | | | | | |
| Offset Voltage[1] | | | –1.2 | | V |
| Input Bias Current | | | 15 | | pA |
| vs Temperature | | | Doubles every 10°C | | |
| Input Impedance | | | $10^{11}$\|\|3 | | Ω \|\| pF |
| **FREQUENCY RESPONSE** | | | | | |
| Bandwidth, Small Signal | | | 500 | | MHz |
| **OUTPUT** | | | | | |
| Current | | | ±200 | | µA |
| Voltage Gain | | | 0.99 | | V/V |
| **POWER SUPPLY** | | | | | |
| Operating Range | | ±2.25 | | ±18 | V |
| Quiescent Current | | | ±0.3 | | mA |

NOTE: (1) Intentional voltage offset to reverse bias photodiode.

## PIN CONFIGURATIONS




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Input Voltage Range (Common Pin) | $\pm V_S$ |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature: P, W | –25°C to +85°C |
| Storage Temperature: P, W | –25°C to +85°C |
| Junction Temperature: P, W | +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (Vapor-Phase Soldering Not Recommended on Plastic Packages) | |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| OPT210P | 8-Pin Plastic DIP | 006-5 |
| OPT210P-J | 8-Lead Surface Mount[2] | 006-6 |
| OPT210W | 5-Pin Plastic SIP | 321-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) 8-pin DIP with leads formed for surface mounting.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

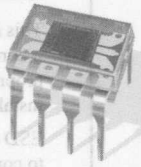
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## MOISTURE SENSITIVITY AND SOLDERING

Clear plastic does not contain the structural-enhancing fillers used in black plastic molding compound. As a result, clear plastic is more sensitive to environmental stress than black plastic. This can cause difficulties if devices have been stored in high humidity prior to soldering. The rapid heating during soldering can stress wire bonds and cause failures. Prior to soldering, it is recommended that plastic devices be baked-out at 85°C for 24 hours.

The fire-retardant fillers used in black plastic are not compatible with clear molding compound. The OPT210 plastic packages cannot meet flammability test, UL-94.

BURR-BROWN®



# OPT211

www.burr-brown.com/databook/OPT211.html

# MONOLITHIC PHOTODIODE AND AMPLIFIER

## FEATURES

- WIDE BANDWIDTH, HIGH RESPONSIVITY:

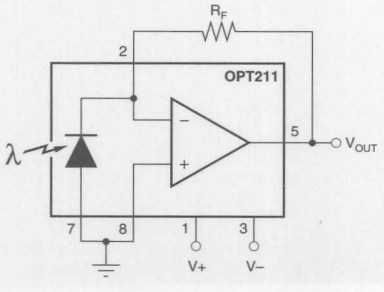
| $R_F$ | BANDWIDTH | |
|---|---|---|
| 1MΩ | 50kHz | *150kHz |
| 100MΩ | 5kHz | *13kHz |

*with bootstrap buffer

- PHOTODIODE SIZE: 0.090 x 0.090 inch (2.29 x 2.29mm)
- HIGH RESPONSIVITY: 0.45A/W (650nm)
- LOW DARK ERRORS: 2mV max
- EXCELLENT SPECTRAL RESPONSE
- LOW QUIESCENT CURRENT: 400μA
- TRANSPARENT 8-PIN DIP

## APPLICATIONS

- MEDICAL INSTRUMENTATION
- LABORATORY INSTRUMENTATION
- POSITION AND PROXIMITY SENSORS
- PHOTOGRAPHIC ANALYZERS
- BARCODE SCANNERS
- SMOKE DETECTORS

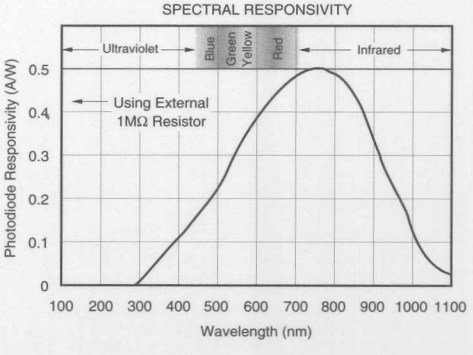



## DESCRIPTION

The OPT211 is a monolithic photodiode with on-chip FET-input transpedance amplifier, that provides wide bandwidth at very high gains. Uncommitted input and feedback nodes allow a variety of feedback options for maximum versatility. Trade-offs in responsivity (gain), bandwidth and SNR can easily be made.

The monolithic combination of photodiode and transimpedance amplifier on a single chip eliminates the problems commonly encountered in discrete designs such as leakage current errors, noise pickup and gain peaking due to stray capacitance. The 0.09 x 0.09 inch photodiode is operated at zero bias for excellent linearity and low dark current. Direct access to the detector's anode allows photodiode bootstrapping, which increases speed performance.

The OPT211 operates over a wide supply range (±2.25V to ±18V) and supply current is only 400μA. It is packaged in a transparent plastic 8-pin DIP specified for the 0°C to 70°C temperature range.




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# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = ±15V, λ = 650nm, external 1MΩ feedback resistor, circuit shown in Figure 1, unless otherwise noted.

| PARAMETER | CONDITIONS | OPT211P MIN | OPT211P TYP | OPT211P MAX | UNITS |
|---|---|---|---|---|---|
| **RESPONSIVITY** | | | | | |
| Photodiode Current | 650nm | | 0.45 | | A/W |
| Unit-to-Unit Variation | 650nm | | ±5 | | % |
| Voltage Output | λ = 650nm, $R_F$ = 1MΩ | | 0.45 | | V/µW |
| Nonlinearity | | | 0.01 | | % of FS |
| Photodiode Area | (0.090 x 0.090 inches) | | 0.008 | | $in^2$ |
| | (2.29 x 2.29mm) | | 5.2 | | $mm^2$ |
| **DARK ERRORS, RTO**[1] | | | | | |
| Offset Voltage, Output | | | ±0.5 | ±2 | mV |
| vs Temperature | | | ±10 | | µV/°C |
| vs Power Supply | $V_S$ = ±2.25V to ±18V | | 10 | 100 | µV/V |
| Voltage Noise, Dark | Dark, $f_B$ = 0.1Hz to 100kHz | | 1 | | mVrms |
| **FREQUENCY RESPONSE** | | | | | |
| Bandwidth | Anode Grounded[2] | | 50 | | kHz |
| | Anode Bootstrapped[3] | | 150 | | kHz |
| Rise Time, 10% to 90%, $R_F$ = 1MΩ | Anode Grounded[2] | | 5 | | µs |
| | Anode Bootstrapped[3] | | 2 | | µs |
| Settling Time, FS to Dark | Anode Grounded[2] | | | | |
| 1% | | | 10 | | µs |
| 0.1% | | | 25 | | µs |
| 0.01% | | | 30 | | µs |
| 100% Overload Recovery Time | FS to Dark (to 1%) | | 44 | | µs |
| | $V_S$ = ±5V | | 100 | | µs |
| | $V_S$ = ±2.25V | | 240 | | µs |
| **OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 10kΩ | (V+) – 1.25 | (V+) – 1 | | V |
| | $R_L$ = 5kΩ | (V+) – 2 | (V+) – 1.5 | | V |
| Capacitive Load, Stable Operation[4] | | | 250 | | pF |
| Short-Circuit Current | | | ±18 | | mA |
| **POWER SUPPLY** | | | | | |
| Operating Voltage Range | | ±2.25 | ±15 | ±18 | V |
| Quiescent Current | $V_{OUT}$ = 0V | | ±400 | ±500 | µA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | 0 | | +70 | °C |
| Operating | | 0 | | +70 | °C |
| Storage | | –25 | | +85 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | 100 | | °C/W |

NOTES: (1) Referred to Output. Includes all error sources. (2) See Figure 1. (3) See Figure 3. (4) See Figure 2.

# PHOTODIODE SPECIFICATIONS

At $T_A$ = +25°C, λ = 650nm, unless otherwise noted.

| PARAMETER | CONDITIONS | Photodiode of OPT211 MIN | Photodiode of OPT211 TYP | Photodiode of OPT211 MAX | UNITS |
|---|---|---|---|---|---|
| Photodiode Area | (0.090 x 0.090 inches) | | 0.008 | | $in^2$ |
| | (2.29 x 2.29mm) | | 5.2 | | $mm^2$ |
| Current Responsivity | λ = 650nm | | 0.45 | | A/W |
| | | | 865 | | µA/W/$cm^2$ |
| Dark Current | $V_D$ = 0V | | 500 | | fA |
| vs Temperature | | | doubles every 10°C | | |
| Capacitance | $V_D$ = 0V | | 600 | | pF |



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## OPTICAL SENSORS

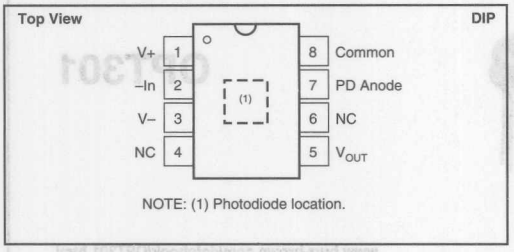
## OPT211 OP AMP SPECIFICATIONS

$T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 10kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | OPT211 Op Amp[1] MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT** | | | | | |
| Offset Voltage | | | ±0.5 | | mV |
| vs Temperature | | | ±5 | | µV/°C |
| vs Power Supply | $V_S$ = ±2.25V to ±18V | | 10 | | µV/V |
| Input Bias Current | | | ±1 | | pA |
| vs Temperature | | | doubles every 10°C | | |
| Input Impedance | | | | | |
| Differential | | | $10^{12}$ II 3 | | Ω II pF |
| Common-Mode | | | $10^{12}$ II 3 | | Ω II pF |
| Common-Mode Input Voltage Range | Linear Operation | | ±14.4 | | V |
| Common-Mode Rejection | | | 106 | | dB |
| **NOISE** | | | | | |
| Voltage Noise Density | f = 10Hz | | 30 | | nV/√Hz |
| | f = 100Hz | | 25 | | nV/√Hz |
| | f = 1kHz | | 15 | | nV/√Hz |
| Current Noise Density | f = 1kHz | | 0.8 | | fA/√Hz |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | | | 120 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product[2] | | | 16 | | MHz |
| Slew Rate | | | 6 | | V/µs |
| Settling Time 0.1% | | | 4 | | µs |
| 0.01% | | | 5 | | µs |
| **OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 10kΩ | (V+) – 1.25 | (V+) – 1 | | V |
| | $R_L$ = 5kΩ | (V+) – 2 | (V+) – 1.5 | | V |
| Short-Circuit Current | | | ±18 | | mA |
| **POWER SUPPLY** | | | | | |
| Operating Voltage Range | | ±2.25 | ±15 | ±18 | V |
| Quiescent Current | $I_O$ = 0mA | | ±400 | ±500 | µA |

NOTES: (1) Op amp specifications provided for information and comparison only. (2) Stable in gains ≥ 20V/V.

## PIN CONFIGURATIONS




NOTE: (1) Photodiode location.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Input Voltage Range | $\pm V_S$ |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | –25°C to +85°C |
| Storage Temperature | –25°C to +85°C |
| Junction Temperature | +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (Vapor-Phase Soldering Not Recommended) | |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| OPT211P | 8-Pin DIP | 006-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## MOISTURE SENSITIVITY AND SOLDERING

Clear plastic does not contain the structural-enhancing fillers used in black plastic molding compound. As a result, clear plastic is more sensitive to environmental stress than black plastic. This can cause difficulties if devices have been stored in high humidity prior to soldering. The rapid heating during soldering can stress wire bonds and cause failures. Prior to soldering, it is recommended that plastic devices be baked-out at +85°C for 24 hours.

The fire-retardant fillers used in black plastic are not compatible with clear molding compound. The OPT211 plastic packages cannot meet flammability test, UL-94.

BURR-BROWN®



# OPT301

www.burr-brown.com/databook/OPT301.html

# INTEGRATED PHOTODIODE AND AMPLIFIER

## FEATURES

- PHOTODIODE SIZE: 0.090 x 0.090 inch (2.29 x 2.29mm)
- 1MΩ FEEDBACK RESISTOR
- HIGH RESPONSIVITY: 0.47A/W (650nm)
- IMPROVED UV RESPONSE
- LOW DARK ERRORS: 2mV
- BANDWIDTH: 4kHz
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 400µA
- HERMETIC TO-99

## APPLICATIONS

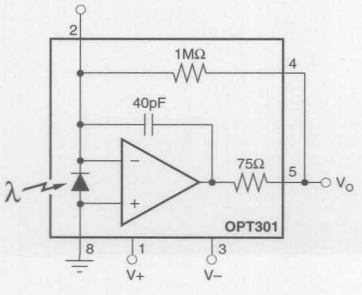
- MEDICAL INSTRUMENTATION
- LABORATORY INSTRUMENTATION
- POSITION AND PROXIMITY SENSORS
- PHOTOGRAPHIC ANALYZERS
- SMOKE DETECTORS

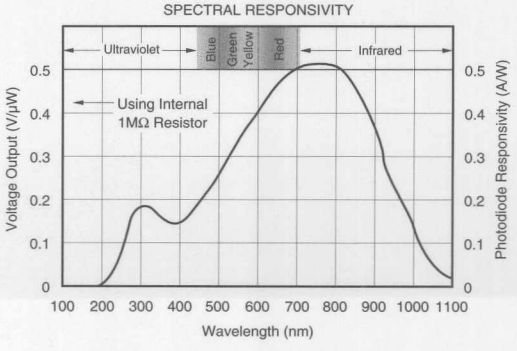
## DESCRIPTION

The OPT301 is an opto-electronic integrated circuit containing a photodiode and transimpedance amplifier on a single dielectrically isolated chip. The transimpedance amplifier consists of a precision FET-input op amp and an on-chip metal film resistor. The 0.09 x 0.09 inch photodiode is operated at zero bias for excellent linearity and low dark current.

The integrated combination of photodiode and transimpedance amplifier on a single chip eliminates the problems commonly encountered in discrete designs such as leakage current errors, noise pick-up and gain peaking due to stray capacitance.

The OPT301 operates over a wide supply range (±2.25 to ±18V) and supply current is only 400µA. It is packaged in a hermetic TO-99 metal package with a glass window, and is specified for the –40°C to 85°C temperature range.




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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $V_S$ = ±15V, λ = 650nm, internal 1MΩ feedback resistor, unless otherwise noted.

| PARAMETER | CONDITIONS | OPT301M MIN | OPT301M TYP | OPT301M MAX | UNITS |
|---|---|---|---|---|---|
| **RESPONSIVITY** | | | | | |
| Photodiode Current | 650nm | | 0.47 | | A/W |
| Voltage Output | 650nm | | 0.47 | | V/µW |
| vs Temperature | | | 200 | | ppm/°C |
| Unit-to-Unit Variation | 650nm | | ±5 | | % |
| Nonlinearity(1) | FS Output = 10V | | 0.01 | | % of FS |
| Photodiode Area | (0.090 x 0.090in) | | 0.008 | | $in^2$ |
| | (2.29 x 2.29mm) | | 5.2 | | $mm^2$ |
| **DARK ERRORS, RTO(2)** | | | | | |
| Offset Voltage, Output | | | ±0.5 | ±2 | mV |
| vs Temperature | | | ±10 | | µV/°C |
| vs Power Supply | $V_S$ = ±2.25V to ±18V | | 10 | 100 | µV/V |
| Voltage Noise | Measured BW = 0.1 to 100kHz | | 160 | | µVrms |
| **RESISTOR—1MΩ Internal** | | | | | |
| Resistance | | | 1 | | MΩ |
| Tolerance | | | ±0.5 | ±2 | % |
| vs Temperature | | | 50 | | ppm/°C |
| **FREQUENCY RESPONSE** | | | | | |
| Bandwidth, Large or Small-Signal, –3dB | | | 4 | | kHz |
| Rise Time, 10% to 90% | | | 90 | | µs |
| Settling Time, 1% | FS to Dark | | 240 | | µs |
| 0.1% | FS to Dark | | 350 | | µs |
| 0.01% | FS to Dark | | 900 | | µs |
| Overload Recovery Time | 100% overdrive, $V_S$ = ±15V | | 240 | | µs |
| | 100% overdrive, $V_S$ = ±5V | | 500 | | µs |
| | 100% overdrive, $V_S$ = ±2.25V | | 1000 | | µs |
| **OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 10kΩ | (V+) – 1.25 | (V+) – 0.65 | | V |
| | $R_L$ = 5kΩ | (V+) – 2 | (V+) – 1 | | V |
| Capacitive Load, Stable Operation | | | 10 | | nF |
| Short-Circuit Current | | | ±18 | | mA |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±15 | | V |
| Operating Voltage Range | | ±2.25 | | ±18 | V |
| Quiescent Current | $I_O$ = 0 | | ±0.4 | ±0.5 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –40 | | +85 | °C |
| Operating/Storage | | –55 | | +125 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | 200 | | °C/W |

NOTES: (1) Deviation in percent of full scale from best-fit straight line. (2) Referred to Output. Includes all error sources.

# PHOTODIODE SPECIFICATIONS

At $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | Photodiode of OPT301 MIN | Photodiode of OPT301 TYP | Photodiode of OPT301 MAX | UNITS |
|---|---|---|---|---|---|
| Photodiode Area | (0.090 x 0.090in) | | 0.008 | | $in^2$ |
| | (2.29 x 2.29mm) | | 5.1 | | $mm^2$ |
| Current Responsivity | 650nm | | 0.47 | | A/W |
| Dark Current | $V_D$ = 0V(1) | | 500 | | fA |
| vs Temperature | | | doubles every 10°C | | |
| Capacitance | $V_D$ = 0V(1) | | 4000 | | pF |

NOTE: (1) Voltage Across Photodiode.

# SPECIFICATIONS (CONT)

## ELECTRICAL

**Op Amp Section of OPT301[1]**

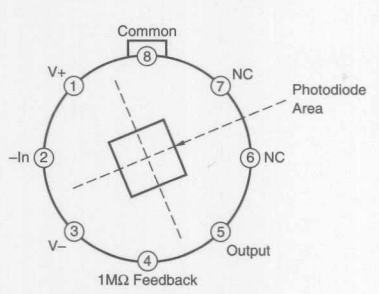
At $T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

| PARAMETER | CONDITIONS | OPT301 Op Amp MIN | OPT301 Op Amp TYP | OPT301 Op Amp MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT** | | | | | |
| Offset Voltage | | | ±0.5 | | mV |
| vs Temperature | | | ±5 | | µV/°C |
| vs Power Supply | $V_S$ = ±2.25V to ±18V | | 10 | | µV/V |
| Input Bias Current | | | 1 | | pA |
| vs Temperature | | | doubles every 10°C | | |
| **NOISE** | | | | | |
| Input Voltage Noise | | | | | |
| Voltage Noise Density, f=10Hz | | | 30 | | nV/√Hz |
| f=100Hz | | | 25 | | nV/√Hz |
| f=1kHz | | | 15 | | nV/√Hz |
| Current Noise Density, f=1kHz | | | 0.8 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range | | | ±14.4 | | V |
| Common-Mode Rejection | | | 106 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $10^{12}$\|\|3 | | Ω\|\|pF |
| Common-Mode | | | $10^{12}$\|\|3 | | Ω\|\|pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | | | 120 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product | | | 380 | | kHz |
| Slew Rate | | | 0.5 | | V/µs |
| Settling Time 0.1% | | | 4 | | µs |
| 0.01% | | | 5 | | µs |
| **OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 10kΩ | (V+) – 1.25 | (V+) – 0.65 | | V |
| | $R_L$ = 5kΩ | (V+) – 2 | (V+) – 1 | | V |
| Short-Circuit Current | | | ±18 | | mA |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±15 | | V |
| Operating Voltage Range | | ±2.25 | | ±18 | V |
| Quiescent Current | $I_O$ = 0 | | ±0.4 | ±0.5 | mA |

NOTE: (1) Op amp specifications provided for information and comparison only.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN CONFIGURATION




NOTE: Metal package is internally connected to common (Pin 8).

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Input Voltage Range (Common Pin) | $\pm V_S$ |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | –55°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | +125°C |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

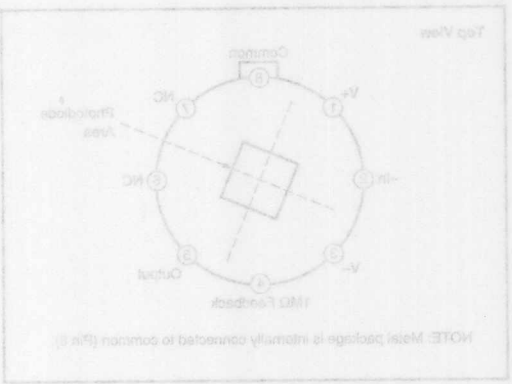
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| OPT301M | 8-Pin TO-99 | 001-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.




NOTE: Metal package is internally connected to common (Pin 8).

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Input Voltage Range (Common Pin) | ±$V_S$ |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | -55°C to +125°C |
| Storage Temperature | -65°C to +125°C |
| Junction Temperature | +125°C |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

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## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| OPT301M | 8-Pin TO-99 | 001-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

# 7 Special Functions

Some analog circuit functions defy classification. In this section you will find a diverse assortment of circuit functions—at least one is bound to be your hidden treasure! Consider some of the possibilities:

**IVC102**—A new, precision FET-input integrating amplifier with on-chip integration capacitors, and low leakage analog switches that convert low-level input current to an output voltage. A lower noise alternative to op amp/resistor transimpedance amplifiers.

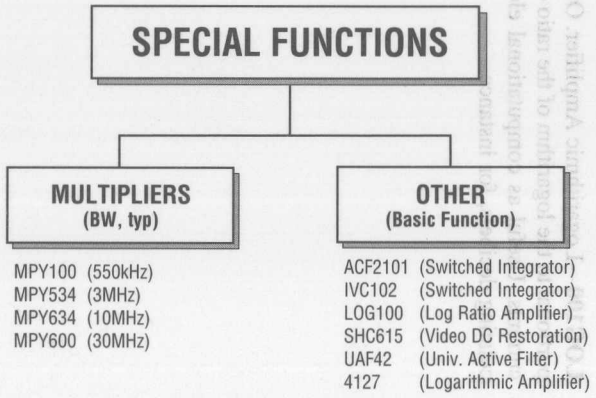
**UAF42**—Universal Analog Filter. Add only external resistors and make a wide range of low-pass, high-pass, band-pass and notch filters.

**ACF2101**—Dual Integrating Transimpedance Amplifier. Integrates input signal currents for a user-determined period of time. Measures tiny currents without using high value resistors.

**MPY634**—Analog Multiplier. Output is equal to the product of two input voltages. Useful in communications (modulation and mixing), power measurement, computation and linearization.

**LOG100**—Logarithmic Amplifier. Output is proportional to the logarithm of the ratio of two input currents. Useful as computational element—calculating decibels, for instance.

# Special Functions




*For Immediate Assistance, Contact Your Local Salesperson*

**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

## MULTIPLIERS/DIVIDERS

| Product | Transfer Function | Error at +25°C max (%) | Temp Coeff (%/°C) | Feed-through (mV) | 1% BW (MHz) | Temp Range[1] | Pkg |
|---|---|---|---|---|---|---|---|
| MPY100 | $[(X_1 - X_2)(Y_1 - Y_2)/10] + Z_2$ | ±0.5 | 0.008 | 30 | 0.07 | Ind | TO-100 |
| MPY534 | $[(X_1 - X_2)(Y_1 - Y_2)/10] + Z_2$ | ±0.25 | 0.008 | 0.05% | 3 | Com | TO-100 |
| MPY600 | $[(X_1 - X_2)(Y_1 - Y_2)/2] + Z_2$ | ±0.025 | 0.02 | 2 | 30 | Ind | DIP |
| MPY634 | $[(X_1 - X_2)(Y_1 - Y_2)/10] + Z_2$ | ±0.5 | 0.015 | 0.15% | 10 | Ind | TO-100, DIP, SOIC |

NOTE: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C.

## OTHER BASIC FUNCTIONS

| Product | Function | Temp Range[1] | Pkg | Description | Comments |
|---|---|---|---|---|---|
| ACF2101 | Switched Integrator | Ind | DIP, SOIC | This is a dual, integrating, transimpedance amplifier that converts an input current to an output voltage by integrating the current for a user determined period of time. Eliminates large feedback resistor of traditional I to V converters. | Includes HOLD and RESET switches and output multiplexer. $V_{OUT} = -\frac{1}{C}\int i_{IN} dt$ |
| IVC102 | Switched Integrator | Ind | DIP, SOIC | Single, integrating amplifier with integrating capacitors and low leakage FET switches. | Ideal for amplifying low level sensors such as photodiodes and ionization chambers. |
| LOG100 | Logarithmic Amplifier | Com | DIP | K Log ($I_1/I_2$) | Optimized for log ratio of current inputs. Specified over six decades of input (1nA to 1mA), 55mV total error, 0.25% log conformity. |
| SHC615 | DC Restoration | XInd | 14-Pin DIP, SOIC | Wide Bandwidth, fast, DC-Restoration circuit for sampling or hum suppression | Bandwidth - OTA: 750kHz<br>Comparator: 280MHz<br>Switching Transients: +1/–7mV<br>Feedthrough Rejection: 100dB |
| UAF42 | Universal Active Filter | Ind | DIP, SOIC | Universal Active Filter which can be configured for a wide range of low-pass, high-pass, and band-pass filters. | Uses classical state variable analog architecture. |
| 4127 | Logarithmic Amplifier | Com | DIP | K Log ($I_1/I_{REF}$) | A versatile part that contains an internal reference and a current inverter. 1% and 0.5% accuracy. |

NOTE: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C.

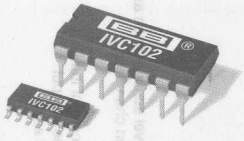
**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

BURR-BROWN®



# IVC102

www.burr-brown.com/databook/IVC102.html

# PRECISION SWITCHED INTEGRATOR TRANSIMPEDANCE AMPLIFIER

## APPLICATIONS

- PRECISION LOW CURRENT MEASUREMENT
- PHOTODIODE MEASUREMENTS
- IONIZATION CHAMBER MEASUREMENTS
- CURRENT/CHARGE-OUTPUT SENSORS
- LEAKAGE CURRENT MEASUREMENT

## FEATURES

- ON-CHIP INTEGRATING CAPACITORS
- GAIN PROGRAMMED BY TIMING
- LOW INPUT BIAS CURRENT: 750fA max
- LOW NOISE
- LOW SWITCH CHARGE INJECTION
- FAST PULSE INTEGRATION
- LOW NONLINEARITY: 0.005% typ
- 14-PIN DIP, SO-14 SURFACE MOUNT

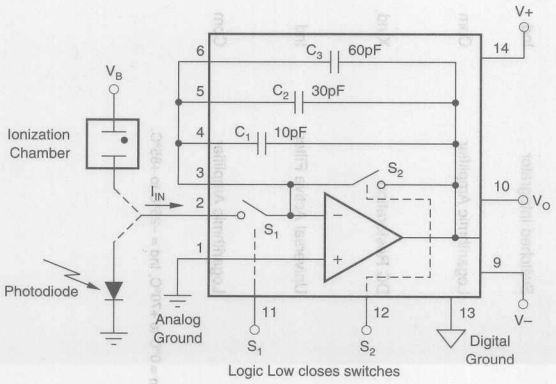
## DESCRIPTION

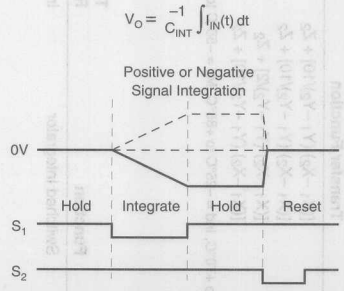
The IVC102 is a precision integrating amplifier with FET op amp, integrating capacitors, and low leakage FET switches. It integrates low-level input current for a user-determined period, storing the resulting voltage on the integrating capacitor. The output voltage can be held for accurate measurement. The IVC102 provides a precision, lower noise alternative to conventional transimpedance op amp circuits that require a very high value feedback resistor.

The IVC102 is ideal for amplifying low-level sensor currents from photodiodes and ionization chambers. The input signal current can be positive or negative.

TTL/CMOS-compatible timing inputs control the integration period, hold and reset functions to set the effective transimpedance gain and to reset (discharge) the integrator capacitor.

Package options include 14-Pin plastic DIP and SO-14 surface-mount packages. Both are specified for the –40°C to 85°C industrial temperature range.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 2kΩ, $C_{INT}$ = $C_1$ + $C_2$ + $C_3$, 1ms integration period[1], unless otherwise specified.

| PARAMETER | CONDITIONS | IVC102P, U MIN | IVC102P, U TYP | IVC102P, U MAX | UNITS |
|---|---|---|---|---|---|
| **TRANSFER FUNCTION** | | | $V_O = -(I_{IN})(T_{INT})/C_{INT}$ | | |
| Gain Error | $C_{INT}$ = $C_1$ + $C_2$ + $C_3$ | | ±5 | +25/–17 | % |
| vs Temperature | | | ±25 | | ppm/°C |
| Nonlinearity | $V_O$ = ±10V | | ±0.005 | | % |
| Input Current Range | | | ±100 | | µA |
| Offset Voltage[2] | $I_{IN}$ = 0, $C_{IN}$ = 50pF | | –5 | ±20 | mV |
| vs Temperature | | | ±30 | | µV/°C |
| vs Power Supply | $V_S$ = +4.75/–10 to +18/–18V | | 150 | 750 | µV/V |
| Droop Rate, Hold Mode | | | –1 | | nV/µs |
| **OP AMP** | | | | | |
| Input Bias Current | $S_1$, $S_2$ Open | | –100 | ±750 | fA |
| vs Temperature | | | See Typical Curve | | |
| Offset Voltage (Op Amp $V_{OS}$) | | | ±0.5 | ±5 | mV |
| vs Temperature | | | ±5 | | µV/°C |
| vs Power Supply | $V_S$ = +4.75/–10 to +18/–18V | | 10 | 100 | µV/V |
| Noise Voltage | f = 1kHz | | 10 | | nV/√Hz |
| **INTEGRATION CAPACITORS** | | | | | |
| $C_1$ + $C_2$ + $C_3$ | | 80 | 100 | 120 | pF |
| vs Temperature | | | ±25 | | ppm/°C |
| $C_1$ | | | 10 | | pF |
| $C_2$ | | | 30 | | pF |
| $C_3$ | | | 60 | | pF |
| **OUTPUT** | | | | | |
| Voltage Range, Positive | $R_L$ = 2kΩ | (V+)–3 | (V+)–1.3 | | V |
| Negative | $R_L$ = 2kΩ | (V–)+3 | (V–)+2.6 | | V |
| Short-Circuit Current | | | ±20 | | mA |
| Capacitive Load Drive | | | 500 | | pF |
| Noise Voltage | | | See Typical Curve | | |
| **DYNAMIC CHARACTERISTIC** | | | | | |
| Op Amp Gain-Bandwidth | | | 2 | | MHz |
| Op Amp Slew Rate | | | 3 | | V/µs |
| Reset | | | | | |
| Slew Rate | | | 3 | | V/µs |
| Settling Time, 0.01% | 10V Step | | 6 | | µs |
| **DIGITAL INPUTS** | (TTL/CMOS Compatible) | | | | |
| $V_{IH}$ (referred to digital ground) | (Logic High) | 2 | | 5.5 | V |
| $V_{IL}$ (referred to digital ground) | (Logic Low) | –0.5 | | 0.8 | V |
| $I_{IH}$ | $V_{IH}$ = 5V | | 2 | | µA |
| $I_{IL}$ | $V_{IL}$ = 0V | | 0 | | µA |
| Switching Time | | | 100 | | ns |
| **POWER SUPPLY** | | | | | |
| Voltage Range: Positive | | +4.75 | +15 | +18 | V |
| Negative | | –10 | –15 | –18 | V |
| Current: Positive | | | 4.1 | 5.5 | mA |
| Negative | | | –1.6 | –2.2 | mA |
| Analog Ground | | | –0.2 | | mA |
| Digital Ground | | | –2.3 | | mA |
| **TEMPERATURE RANGE** | | | | | |
| Operating Range | | –40 | | 85 | °C |
| Storage | | –55 | | 125 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| DIP | | | 100 | | °C/W |
| SO-14 | | | 150 | | °C/W |

NOTES: (1) Standard test timing: 1ms integration, 200µs hold, 100µs reset. (2) Hold mode output voltage after 1ms integration of zero input current. Includes op amp offset voltage, integration of input error current and switch charge injection effects.



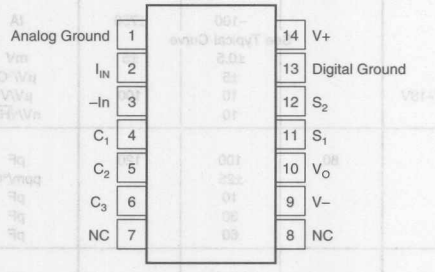
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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, V+ to V– | 36V |
| Logic Input Voltage | V– to V+ |
| Output Short Circuit to Ground | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 10s) | 300°C |

## PIN CONNECTIONS

**Top View** — **14-Pin DIP/ SO-14 Surface Mount**




NC = No Internal Connection
Connect to Analog Ground for Lowest Noise

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| IVC102P | 14-Pin DIP | 010 |
| IVC102U | SO-14 Surface Mount | 235 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®



# LOG100

www.burr-brown.com/databook/LOG100.html

# Precision LOGARITHMIC AND LOG RATIO AMPLIFIER

## FEATURES

- ACCURACY
  0.37% FSO max Total Error
  Over 5 Decades
- LINEARITY
  0.1% max Log Conformity
  Over 5 Decades
- EASY TO USE
  Pin-selectable Gains
  Internal Laser-trimmed Resistors
- WIDE INPUT DYNAMIC RANGE
  6 Decades, 1nA to 1mA
- HERMETIC CERAMIC DIP

## APPLICATIONS

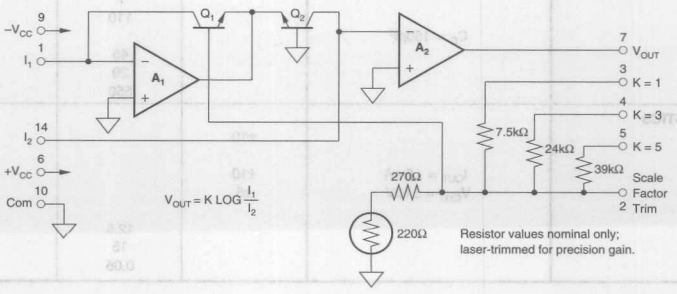
- LOG, LOG RATIO AND ANTILOG COMPUTATIONS
- ABSORBANCE MEASUREMENTS
- DATA COMPRESSION
- OPTICAL DENSITY MEASUREMENTS
- DATA LINEARIZATION
- CURRENT AND VOLTAGE INPUTS

## DESCRIPTION

The LOG100 uses advanced integrated circuit technologies to achieve high accuracy, ease of use, low cost, and small size. It is the logical choice for your logarithmic-type computations. The amplifier has guaranteed maximum error specifications over the full six-decade input range (1nA to 1mA) and for all possible combinations of $I_1$ and $I_2$. Total error is guaranteed so that involved error computations are not necessary.

The circuit uses a specially designed compatible thin-film monolithic integrated circuit which contains amplifiers, logging transistors, and low drift thin-film resistors. The resistors are laser-trimmed for maximum precision. FET input transistors are used for the amplifiers whose low bias currents (1pA typical) permit signal currents as low as 1nA while maintaining guaranteed total errors of 0.37% FSO maximum.

Because scaling resistors are self-contained, scale factors of 1V, 3V or 5V per decade are obtained simply by pin selections. No other resistors are required for log ratio applications. The LOG100 will meet its guaranteed accuracy with no user trimming. Provisions are made for simple adjustments of scale factor, offset voltage, and bias current if enhanced performance is desired.




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## ELECTRICAL

At $T_A$ = +25°C and $\pm V_{CC}$ = ±15V, after 15 minute warm-up, unless otherwise specified.

| PARAMETER | CONDITIONS | LOG100JP MIN | LOG100JP TYP | LOG100JP MAX | UNITS |
|---|---|---|---|---|---|
| **TRANSFER FUNCTION** | | | $V_{OUT}$ = K Log ($I_1/I_2$) | | |
| Log Conformity Error[1] | Either $I_1$ or $I_2$ | | | | |
| Initial | 1nA to 100µA (5 decades) | | 0.04 | 0.1 | % |
| | 1nA to 1mA (6 decades) | | 0.15 | 0.25 | % |
| Over Temperature | 1nA to 100µA (5 decades) | | 0.002 | | %/°C |
| | 1nA to 1mA (6 decades) | | 0.001 | | %/°C |
| K Range[2] | | | 1, 3, 5 | | V/decade |
| Accuracy | | | 0.3 | | % |
| Temperature Coefficient | | | 0.03 | | %/°C |
| **ACCURACY** | | | | | |
| Total Error[3] | K = 1,[4] Current Input Operation | | | | |
| Initial | $I_1$, $I_2$ = 1mA | | | ±55 | mV |
| | $I_1$, $I_2$ = 100µA | | | ±30 | mV |
| | $I_1$, $I_2$ = 10µA | | | ±25 | mV |
| | $I_1$, $I_2$ = 1µA | | | ±20 | mV |
| | $I_1$, $I_2$ = 100nA | | | ±25 | mV |
| | $I_1$, $I_2$ = 10nA | | | ±30 | mV |
| | $I_1$, $I_2$ = 1nA | | | ±37 | mV |
| vs Temperature | $I_1$, $I_2$ = 1mA | | ±0.20 | | mV/°C |
| | $I_1$, $I_2$ = 100µA | | ±0.37 | | mV/°C |
| | $I_1$, $I_2$ = 10µA | | ±0.28 | | mV/°C |
| | $I_1$, $I_2$ = 1µA | | ±0.033 | | mV/°C |
| | $I_1$, $I_2$ = 100nA | | ±0.28 | | mV/°C |
| | $I_1$, $I_2$ = 10nA | | ±0.51 | | mV/°C |
| | $I_1$, $I_2$ = 1nA | | ±1.26 | | mV/°C |
| vs Supply | $I_1$, $I_2$ = 1mA | | ±4.3 | | mV/V |
| | $I_1$, $I_2$ = 100µA | | ±1.5 | | mV/V |
| | $I_1$, $I_2$ = 10µA | | ±0.37 | | mV/V |
| | $I_1$, $I_2$ = 1µA | | ±0.11 | | mV/V |
| | $I_1$, $I_2$ = 100nA | | ±0.61 | | mV/V |
| | $I_1$, $I_2$ = 10nA | | ±0.91 | | mV/V |
| | $I_1$, $I_2$ = 1nA | | ±2.6 | | mV/V |
| **INPUT CHARACTERISTICS** (of Amplifiers $A_1$ and $A_2$) | | | | | |
| Offset Voltage | | | | | |
| Initial | | | ±0.7 | ±5 | mV |
| vs Temperature | | | ±80 | | µV/°C |
| Bias Current | | | | | |
| Initial | | | 1 | 5[5] | pA |
| vs Temperature | | | Doubles Every 10°C | | |
| Voltage Noise | 10Hz to 10kHz, RTI | | 3 | | µVrms |
| Current Noise | 10Hz to 10kHz, RTI | | 0.5 | | pArms |
| **AC PERFORMANCE** | | | | | |
| 3dB Response[6], $I_2$ = 10µA | | | | | |
| 1nA | $C_C$ = 4500pF | | 0.11 | | kHz |
| 1µA | $C_C$ = 150pF | | 38 | | kHz |
| 10µA | $C_C$ = 150pF | | 27 | | kHz |
| 1mA | $C_C$ = 50pF | | 45 | | kHz |
| Step Response[6] | | | | | |
| Increasing | $C_C$ = 150pF | | | | |
| 1µA to 1mA | | | 11 | | µs |
| 100nA to 1µA | | | 7 | | µs |
| 10nA to 100nA | | | 110 | | µs |
| Decreasing | $C_C$ = 150pF | | | | |
| 1mA to 1µA | | | 45 | | µs |
| 1µA to 100nA | | | 20 | | µs |
| 100nA to 10nA | | | 550 | | µs |
| **OUTPUT CHARACTERISTICS** | | | | | |
| Full Scale Output (FSO) | | ±10 | | | V |
| Rated Output | | | | | |
| Voltage | $I_{OUT}$ = ±5mA | ±10 | | | V |
| Current | $V_{OUT}$ = ±10V | ±5 | | | mA |
| Current Limit | | | | | |
| Positive | | | 12.5 | | mA |
| Negative | | | 15 | | mA |
| Impedance | | | 0.05 | | Ω |

# SPECIFICATIONS (CONT)

## ELECTRICAL

At $T_A$ = +25°C and $\pm V_{CC}$ = ±15V, after 15 minute warm-up, unless otherwise specified.

| PARAMETER | CONDITIONS | LOG100JP MIN | LOG100JP TYP | LOG100JP MAX | UNITS |
|---|---|---|---|---|---|
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Rated Voltage | | | ±15 | | VDC |
| Operating Range | Derated Performance | ±12 | | ±18 | VDC |
| Quiescent Current | | | ±7 | ±9 | mA |
| **AMBIENT TEMPERATURE RANGE** | | | | | |
| Specification | | 0 | | +70 | °C |
| Operating Range | Derated Performance | –25 | | +85 | °C |
| Storage | | –40 | | +85 | °C |

NOTES: (1) Log Conformity Error is the peak deviation from the best-fit straight line of the $V_{OUT}$ vs Log $I_{IN}$ curve expressed as a percent of peak-to-peak full scale output. (2) May be trimmed to other values. See Applications section. (3) The worst-case Total Error for any ratio of $I_1/I_2$ is the largest of the two errors when $I_1$ and $I_2$ are considered separately. (4) Total Error at other values of K is K times Total Error for K = 1. (5) Guaranteed by design. Not directly measurable due to amplifier's committed configuration. (6) 3dB and transient response are a function of both the compensation capacitor and the level of input current. See Typical Performance Curves.

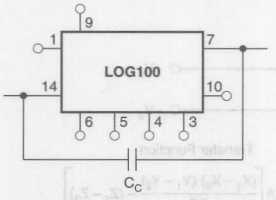
## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply | ±18V |
| Internal Power Dissipation | 600mV |
| Input Current | 10mA |
| Input Voltage Range | ±18V |
| Storage Temperature Range | –40°C to +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Output Short-circuit Duration | Continuous to ground |
| Junction Temperature | 175°C |

## SCALE FACTOR PIN CONNECTIONS

| K, V/DECADE | CONNECTIONS |
|---|---|
| 5 | 5 to 7 |
| 3 | 4 to 7 |
| 1.9 | 4 and 5 to 7 |
| 1 | 3 to 7 |
| 0.85 | 3 and 5 to 7 |
| 0.77 | 3 and 4 to 7 |
| 0.68 | 3 and 4 and 5 to 7 |

## FREQUENCY COMPENSATION



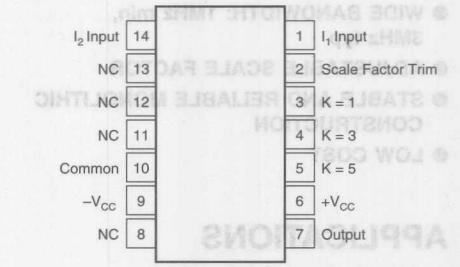

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| LOG100JP | 14-Pin Hermetic Ceramic DIP | 148(2) | 0°C to +70°C |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) During 1994, the package was changed from plastic to hermetic ceramic. Pinout, model number, and specifications remained unchanged. The metal lid of the new package is internally connected to common, pin 10.

## PIN CONFIGURATION

Bottom View




NC = No Connection

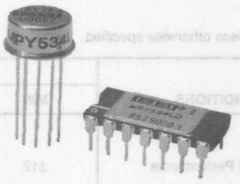
## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integral circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

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BURR-BROWN®



# MPY534

www.burr-brown.com/databook/MPY534.html

# Precision ANALOG MULTIPLIER

## FEATURES

- ±0.25% max 4-QUADRANT ACCURACY
- WIDE BANDWIDTH: 1MHz min, 3MHz typ
- ADJUSTABLE SCALE FACTOR
- STABLE AND RELIABLE MONOLITHIC CONSTRUCTION
- LOW COST

## APPLICATIONS

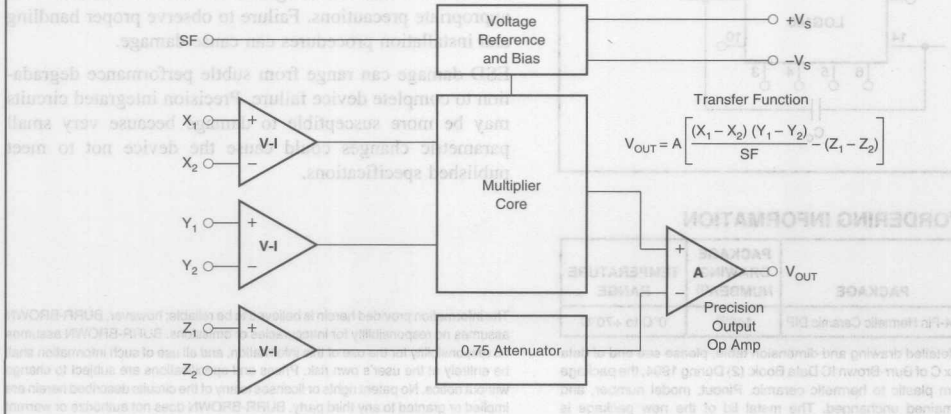
- PRECISION ANALOG SIGNAL PROCESSING
- VIDEO SIGNAL PROCESSING
- VOLTAGE CONTROLLED FILTERS AND OSCILLATORS
- MODULATION AND DEMODULATION
- RATIO AND PERCENTAGE COMPUTATION

## DESCRIPTION

The MPY534 is a high accuracy, general purpose four-quadrant analog multiplier. Its accurately laser trimmed transfer characteristics make it easy to use in a wide variety of applications with a minimum of external parts and trimming circuitry. Its differential X, Y and Z inputs allow configuration as multiplier, squarer, divider, square-rooter and other functions while maintaining high accuracy.

The wide bandwidth of this new design allows accurate signal processing at higher frequencies suitable for video signal processing. It is capable of performing IF and RF frequency mixing, modulation and demodulation with excellent carrier rejection and very simple feedthrough adjustment.

An accurate internal voltage reference provides precise setting of the scale factor. The differential Z input allows user selected scale factors from 0.1 to 10 using external feedback resistors.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C and $V_S$ = ±15VDC, unless otherwise specified.

| PARAMETER | MPY534J | | | MPY534K | | | MPY534L | | | MPY534S | | | MPY534T | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **MULTIPLIER PERFORMANCE** | | | | | | | | | | | | | | | | |
| Transfer Function | | * | | | $\frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z_2$ | | | * | | | * | | | * | | |
| Total Error[1] | | | | | | | | | | | | | | | | |
| (–10V ≤ X, Y ≤ +10V) | | | ±1.0 | | | ±0.5 | | | ±0.25 | | | ±1.0 | | * | | % |
| $T_A$ = min to max | | ±1.5 | | | ±1.0 | | | ±0.5 | | | | ±2.0 | | ±1.0 | | % |
| Total Error vs Temperature | | ±0.022 | | | ±0.015 | | | ±0.008 | | | | ±0.02 | | ±0.01 | | %/°C |
| Scale Factor Error (SF = 10.000V Nominal)[2] | | ±0.25 | | | ±0.1 | | | * | | | ±0.25 | | | * | | % |
| Temperature Coefficient of Scaling Voltage | | ±0.02 | | | ±0.01 | | | ±0.005 | | | ±0.02 | | | ±0.005 | | %/°C |
| Supply Rejection (±15V ±1V) | | * | | | ±0.01 | | | * | | | * | | | * | | % |
| Nonlinearity: | | | | | | | | | | | | | | | | |
| X (X = 20Vp-p, Y = 10V) | | ±0.4 | | | ±0.2 | ±0.3 | | ±0.10 | ±0.12 | | ±0.4 | | | * | * | % |
| Y (Y = 20Vp-p, X = 10V) | | * | | | ±0.01 | ±0.1 | | ±0.005 | * | | * | | | * | * | % |
| Feedthrough[3] | | | | | | | | | | | | | | | | |
| X (Y Nulled, Y = 20Vp-p 50Hz) | | ±0.3 | | | ±0.15 | ±0.3 | | ±0.05 | ±0.12 | | ±0.3 | | | * | * | % |
| Y (X Nulled, Y = 20Vp-p 50Hz) | | * | | | ±0.01 | ±0.1 | | ±0.003 | * | | * | | | * | * | % |
| Output Offset Voltage | | ±5 | ±30 | | ±2 | ±15 | | * | ±10 | | ±5 | ±30 | | * | * | mV |
| Output Offset Voltage Drift | | 200 | | | 100 | | | * | | | | 500 | | | 300 | µV/°C |
| **DYNAMICS** | | | | | | | | | | | | | | | | |
| Small Signal BW, ($V_{OUT}$ = 0.1Vrms) | * | * | | 1 | 3 | | * | * | | * | * | | * | * | | MHz |
| 1% Amplitude Error ($C_{LOAD}$ = 1000pF) | | * | | | 50 | | | * | | | * | | | * | | kHz |
| Slew Rate ($V_{OUT}$ = 20Vp-p) | | * | | | 20 | | | * | | | * | | | * | | V/µs |
| Settling Time (to 1%, $\Delta V_{OUT}$ = 20V) | | * | | | 2 | | | * | | | * | | | * | | µs |
| **NOISE** | | | | | | | | | | | | | | | | |
| Noise Spectral Density: SF = 10V | | * | | | 0.8 | | | * | | | * | | | * | | µV/√Hz |
| Wideband Noise: | | | | | | | | | | | | | | | | |
| f = 10Hz to 5MHz | | * | | | 1 | | | * | | | * | | | * | | mVrms |
| f = 10Hz to 10kHz | | * | | | 90 | | | * | | | * | | | * | | µVrms |
| **OUTPUT** | | | | | | | | | | | | | | | | |
| Output Voltage Swing | * | | | ±11 | | | * | | | * | | | * | | | V |
| Output Impedance (f ≤ 1kHz) | | * | | | 0.1 | | | * | | | * | | | * | | Ω |
| Output Short Circuit Current ($R_L$ = 0, $T_A$ = min to max) | | * | | | 30 | | | * | | | * | | | * | | mA |
| Amplifier Open Loop Gain (f = 50Hz) | | * | | | 70 | | | * | | | * | | | * | | dB |
| **INPUT AMPLIFIERS (X, Y and Z)** | | | | | | | | | | | | | | | | |
| Input Voltage Range | | | | | | | | | | | | | | | | |
| Differential $V_{IN}$ ($V_{CM}$ = 0) | | * | | | ±12 | | | * | | | * | | | * | | V |
| Common-Mode $V_{IN}$ ($V_{DIFF}$ = 0) (see Typical Performance Curves) | | * | | | ±10 | | | * | | | * | | | * | | V |
| Offset Voltage X, Y | | ±5 | ±20 | | ±2 | ±10 | | * | * | | ±5 | ±20 | | * | * | mV |
| Offset Voltage Drift X, Y | | 100 | | | 50 | | | * | | | 100 | | | * | | µV/°C |
| Offset Voltage Z | | ±5 | ±30 | | ±2 | ±15 | | * | ±10 | | ±5 | ±30 | | * | * | mV |
| Offset Voltage Drift Z | | 200 | | | 100 | | | * | | | | 500 | | | 300 | µV/°C |
| CMRR | 60 | 80 | | 70 | 90 | | * | * | | 60 | 80 | | * | * | | dB |
| Bias Current | | * | * | | 0.8 | 2.0 | | * | * | | * | * | | * | * | µA |
| Offset Current | | * | | | 0.1 | | | 0.05 | 0.2 | | * | 2.0 | | * | 2.0 | µA |
| Differential Resistance | | * | | | 10 | | | * | | | * | | | * | | MΩ |
| **DIVIDER PERFORMANCE** | | | | | | | | | | | | | | | | |
| Transfer Function ($X_1 > X_2$) | | * | | | $10V\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$ | | | | | | | | | | | |
| Total Error[1] | | | | | | | | | | | | | | | | |
| (X = 10V, –10V ≤ Z ≤ +10V) | | ±0.75 | | | ±0.35 | | | ±0.2 | | | ±0.75 | | | * | | % |
| (X = 1V, –1V ≤ Z ≤+1V) | | ±2.0 | | | ±1.0 | | | ±0.8 | | | ±2.0 | | | * | | % |
| (0.1V ≤ X ≤ 10V, –10V ≤ Z ≤ 10V) | | ±2.5 | | | ±1.0 | | | ±0.8 | | | ±2.5 | | | * | | % |

## SPECIFICATIONS (CONT)

### ELECTRICAL

At $T_A$ = +25°C and $V_S$ = ±15VDC, unless otherwise specified.

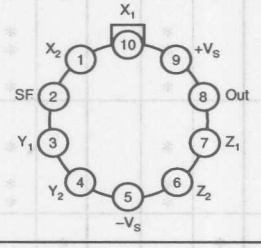
| PARAMETER | MPY534J | | | MPY534K | | | MPY534L | | | MPY534S | | | MPY534T | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **SQUARE PERFORMANCE** | | | | | | | | | | | | | | | | |
| Transfer Function | | * | | | $\frac{(X_1 - X_2)^2}{10V} + Z_2$ | | | * | | | * | | | * | | |
| Total Error (–10V ≤ X ≤ 10V) | | 0.6 | | | ±0.3 | | | ±0.2 | | | ±0.6 | | | * | | % |
| **SQUARE-ROOTER PERFORMANCE** | | | | | | | | | | | | | | | | |
| Transfer Function ($Z_1 \leq Z_2$) | | * | | | $\sqrt{10V(Z_2 - Z_1)} + X_2$ | | | * | | | * | | | * | | |
| Total Error[1] (1V ≤ Z ≤ 10V) | | ±1.0 | | | ±0.5 | | | ±0.25 | | | ±1.0 | | | ±0.5 | | % |
| **POWER SUPPLY** | | | | | | | | | | | | | | | | |
| Supply Voltage: | | | | | | | | | | | | | | | | |
| Rated Performance | | * | | | ±15 | | | * | | | * | | | * | | VDC |
| Operating | * | | * | ±8 | | ±18 | * | | * | * | | ±20 | * | | ±20 | VDC |
| Supply Current, Quiescent | | * | * | | 4 | 6 | | * | * | | * | * | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | | | | | | | | | |
| Operating | * | | * | 0 | | +70 | * | | * | –55 | | +125 | –55 | | +125 | °C |
| Storage | * | | * | –65 | | +150 | * | | * | * | | * | * | | * | °C |

* Specifications same as MPY534K.

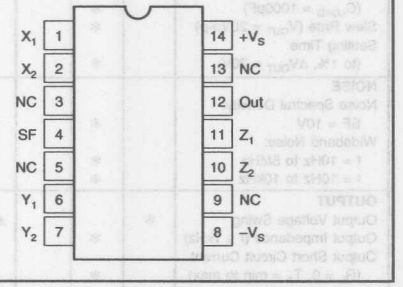
NOTES: (1) Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV). (2) May be reduced to 3V using external resistor between –Vs and SF. (3) Irreducible component due to nonlinearity; excludes effect of offsets.

### PIN CONFIGURATIONS

Top View — TO-100




Top View — DIP




### ABSOLUTE MAXIMUM RATINGS

| PARAMETER | MPY534J, K, L | MPY534S, T |
|---|---|---|
| Power Supply Voltage | ±18 | ±20 |
| Power Dissipation | 500mW | * |
| Output Short-Circuit to Ground | Indefinite | * |
| Input Voltage (all X, Y and Z) | $\pm V_S$ | * |
| Operating Temperature Range | 0°C to +70°C | –55°C to +125°C |
| Storage Temperature Range | –65°C to +150°C | * |
| Lead Temperature (soldering, 10s) | +300°C | * |

* Specification same as for MPY534K.

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| MPY534JD | Ceramic DIP | 169 | 0°C to +70°C |
| MPY534JH | Metal TO-100 | 007 | 0°C to +70°C |
| MPY534KD | Ceramic DIP | 169 | 0°C to +70°C |
| MPY534KH | Metal TO-100 | 007 | 0°C to +70°C |
| MPY534LD | Ceramic DIP | 169 | 0°C to +70°C |
| MPY534LH | Metal TO-100 | 007 | 0°C to +70°C |
| MPY534SD | Ceramic DIP | 169 | –55°C to +125°C |
| MPY534SH | Metal TO-100 | 007 | –55°C to +125°C |
| MPY534TD | Ceramic DIP | 169 | –55°C to +125°C |
| MPY534TH | Metal TO-100 | 007 | –55°C to +125°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

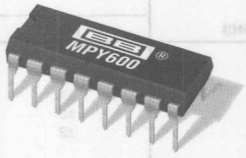
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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BURR-BROWN®




# MPY600

www.burr-brown.com/databook/MPY600.html

# Wide Bandwidth SIGNAL MULTIPLIER

## FEATURES

- WIDE BANDWIDTH:
  75MHz — Current Output
  30MHz — Voltage Output
- LOW NOISE
- LOW FEEDTHROUGH: –60dB (5MHz)
- GROUND-REFERRED OUTPUT
- LOW OFFSET VOLTAGE

## APPLICATIONS

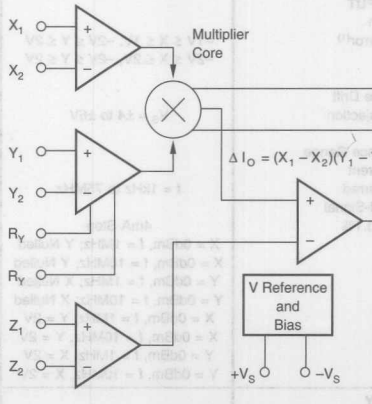
- MODULATOR/DEMODULATOR
- VIDEO SIGNAL PROCESSING
- CRT GEOMETRY CORRECTION
- CRT FOCUS CORRECTION
- VOLTAGE-CONTROLLED CIRCUITS

## DESCRIPTION

The MPY600 is a wide-bandwidth four-quadrant signal multiplier. Its output voltage is equal to the algebraic product of the X and Y input voltages. For signals up to 30MHz, the on-board output op amp provides the complete multiplication function with a low-impedance voltage output. Differential current outputs extend multiplier bandwidth to 75MHz.

The MPY600 offers improved performance compared to common semiconductor modulator or multiplier circuits. It can be used for both two-quadrant (voltage-controlled amplifier) and four-quadrant (double-balanced) applications. While previous devices required cumbersome circuitry for trimming, balance and level-shifting, the MPY600 requires no external components. A single external resistor can be used to program the conversion gain for optimum spurious-free dynamic range. When used as a modulator, carrier feedthrough measures –60dB at 5MHz.

Differential X, Y and Z inputs can be connected in a variety of useful configurations, including squarer, divider, and square-rooter circuits. The MPY600 is available in 16-pin plastic DIP, specified for the industrial temperature range.




$$V_O = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{2V} + Z_2 - Z_1\right]$$

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $V_S = \pm5V$, $T_A = +25°C$, unless otherwise noted.

| SPECIFICATION | CONDITIONS | MPY600AP MIN | MPY600AP TYP | MPY600AP MAX | UNITS |
|---|---|---|---|---|---|
| **INPUTS (X, Y, Z)** | | | | | |
| Full-Scale Differential Input | | | | | |
| $X_1$-$X_2$ | | ±1 | | | V |
| $Y_1$-$Y_2$ | | ±2 | | | V |
| $Z_1$-$Z_2$ | | ±2 | | | V |
| Input Voltage Range | | | ±2.2 | | V |
| Differential Input Range | | | ±2.5 | | V |
| Input Impedance | | | 100 ‖ 1.5 | | kΩ ‖ pF |
| Input Offset Voltage | | | ±0.5 | ±5 | mV |
| Drift | | | 25 | | µV/°C |
| CMRR | $V_{CM} = \pm2V$ | | 70 | | dB |
| PSRR | | | 70 | | dB |
| Input Bias Current (X, Y) | | | +15 | | µA |
| Z Input | | | −15 | | µA |
| **VOLTAGE OUTPUT** | | | | | |
| Transfer Function | | | $V_O = \frac{(X_1-X_2)(Y_1-Y_2)}{2} + Z_2$ | | V |
| Total Multiplier Error[1] | $-1V \le X \le 1V, -2V \le Y \le 2V$ | | ±15 | ±25 | mV |
| | $-2V \le X \le 2V, -2V \le Y \le 2V$ | | ±25 | | mV |
| Gain Error | | | ±1 | | % |
| Gain Temperature Drift | | | ±200 | | ppm/°C |
| Power Supply Rejection | $V_S = \pm4$ to $\pm6V$ | | 70 | | dB |
| Noise | f = 1kHz to 30MHz | | 120 | | nV/ Hz |
| Output Voltage Swing | $R_L = 100\Omega$ | ±2.2 | ±3 | | V |
| Output Current | | ±22 | ±30 | | mA |
| Short-Circuit Limit | | | 50 | | mA |
| Bandwidth | Small Signal | | 30 | | MHz |
| Slew Rate | | | 150 | | V/µs |
| Settling Time to 0.1% | 4V Step | | 150 | | ns |
| Differential Gain Error | 3.58MHz, 0 to 0.7V | | 0.2 | | % |
| Differential Phase Error | 3.58MHz, 0 to 0.7V | | 0.2 | | Degrees |
| Capacitive Load, Max | Stable Operation | | 100 | | pF |
| Feedthrough, X | X = 0dBm, f = 500kHz; Y Nulled | | −65 | | dB |
| | X = 0dBm, f = 5MHz; Y Nulled | | −60 | | dB |
| Feedthrough, Y | Y = 0dBm, f = 500kHz; X Nulled | | −70 | | dB |
| | Y = 0dBm, f = 5MHz; X Nulled | | −50 | | dB |
| Distortion, X | X = 0dBm, f = 500kHz, Y = 2V | | −60 | | dB |
| | X = 0dBm, f = 5MHz, Y = 2V | | −55 | | dB |
| Distortion, Y | Y = 0dBm, f = 500kHz, X = 2V | | −65 | | dB |
| | Y = 0dBm, f = 5MHz, X = 2V | | −55 | | dB |
| **CURRENT OUTPUT** | | | | | |
| Transfer Function | | | $\Delta I_O = (X_1 - X_2)(Y_1 - Y_2)/1000$ | | A |
| Total Multiplier Error[1] | $-1V \le X \le 1V, -2V \le Y \le 2V$ | | ±20 | ±80 | µA |
| | $-2V \le X \le 2V, -2V \le Y \le 2V$ | | ±80 | | µA |
| Gain Error | | | ±1 | | % |
| Gain Temperature Drift | | | ±200 | | ppm/°C |
| Power Supply Rejection | $V_S = \pm4$ to $\pm6V$ | | 50 | | dB |
| Noise, Output | | | 100 | | pA/√Hz |
| Voltage Compliance Range | | | ±2.5 | | V |
| Peak Output Current | | | 5 | | mA |
| Noise, Input-Referred | f = 1kHz to 75MHz | | 50 | | nV/√Hz |
| Bandwidth, Small-Signal | | | 75 | | MHz |
| Settling Time to 0.1% | 4mA Step | | 150 | | ns |
| Feedthrough, X | X = 0dBm, f = 1MHz; Y Nulled | | −65 | | dB |
| | X = 0dBm, f = 10MHz; Y Nulled | | −45 | | dB |
| Feedthrough, Y | Y = 0dBm, f = 1MHz; X Nulled | | −75 | | dB |
| | Y = 0dBm, f = 10MHz; X Nulled | | −55 | | dB |
| Distortion, X | X = 0dBm, f = 1MHz, Y = 2V | | −55 | | dB |
| | X = 0dBm, f = 10MHz, Y = 2V | | −50 | | dB |
| Distortion, Y | Y = 0dBm, f = 1MHz, X = 2V | | −65 | | dB |
| | Y = 0dBm, f = 10MHz, X = 2V | | −50 | | dB |
| **POWER SUPPLY** | | | | | |
| Rated Performance | | | ±5 | | V |
| Operating | | ±4.75 | | ±8 | V |
| Current | | | ±30 | ±35 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specified Temperature Range | | −25 | | +85 | °C |
| Storage Temperature Range | | −40 | | +125 | °C |
| Thermal Resistance, $\theta_{J-A}$ | | | 50 | | °C/W |

NOTE: (1) Deviation from ideal transfer function referred to full scale output. Includes gain, nonlinearity and offset errors.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Input Voltage Range | $\pm V_S$ |
| Op Amp Output Current | 100mA |
| Operating Temperature | +125°C |
| Storage Temperature | +150°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

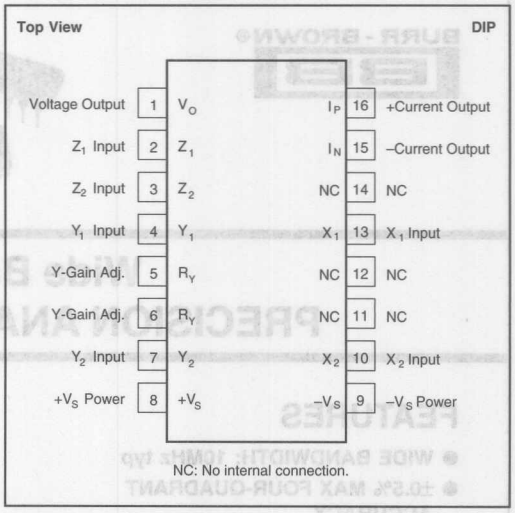
## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| MPY600AP | 16-Pin Plastic DIP | 180 | –25°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN CONFIGURATION

Top View DIP




NC: No internal connection.

## ELECTROSTATIC DISCHARGE SENSITIVITY

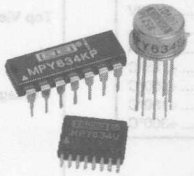
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



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# MPY634

www.burr-brown.com/databook/MPY634.html

# Wide Bandwidth PRECISION ANALOG MULTIPLIER

## FEATURES

- WIDE BANDWIDTH: 10MHz typ
- ±0.5% MAX FOUR-QUADRANT ACCURACY
- INTERNAL WIDE-BANDWIDTH OP AMP
- EASY TO USE
- LOW COST

## APPLICATIONS

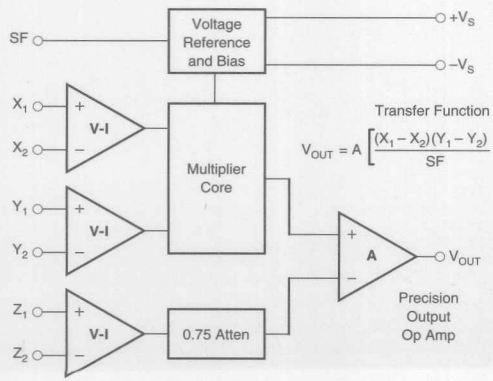
- PRECISION ANALOG SIGNAL PROCESSING
- MODULATION AND DEMODULATION
- VOLTAGE-CONTROLLED AMPLIFIERS
- VIDEO SIGNAL PROCESSING
- VOLTAGE-CONTROLLED FILTERS AND OSCILLATORS

## DESCRIPTION

The MPY634 is a wide bandwidth, high accuracy, four-quadrant analog multiplier. Its accurately laser-trimmed multiplier characteristics make it easy to use in a wide variety of applications with a minimum of external parts, often eliminating all external trimming. Its differential X, Y, and Z inputs allow configuration as a multiplier, squarer, divider, square-rooter, and other functions while maintaining high accuracy.

The wide bandwidth of this new design allows signal processing at IF, RF, and video frequencies. The internal output amplifier of the MPY634 reduces design complexity compared to other high frequency multipliers and balanced modulator circuits. It is capable of performing frequency mixing, balanced modulation, and demodulation with excellent carrier rejection.

An accurate internal voltage reference provides precise setting of the scale factor. The differential Z input allows user-selected scale factors from 0.1 to 10 using external feedback resistors.




Transfer Function

$$V_{OUT} = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right]$$

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132



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# SPECIFICATIONS

At $T_A$ = +25°C and $V_S$ = ±15VDC, unless otherwise noted.

| | MPY634KP/KU | | | MPY634AM | | | MPY634BM | | | MPY634SM | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MODEL | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | UNITS |
| **MULTIPLIER PERFORMANCE** | | | | | | | | | | | | | |
| Transfer Function | | * | | | $\frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z_2$ | | | * | | | * | | |
| Total Error[1] | | | | | | | | | | | | | |
| (–10V ≤ X, Y ≤ +10V) | | | ±2.0 | | | ±1.0 | | | ±0.5 | | | * | % |
| $T_A$ = min to max | | ±2.5 | | | ±1.5 | | | ±1.0 | | | | ±2.0 | % |
| Total Error vs Temperature | | ±0.03 | | | ±0.022 | | | ±0.015 | | | | ±0.02 | %/°C |
| Scale Factor Error | | | | | | | | | | | | | |
| (SF = 10.000V Nominal)[2] | | ±0.25 | | | ±0.1 | | | * | | | * | | % |
| Temperature Coefficient of | | | | | | | | | | | | | |
| Scaling Voltage | | ±0.02 | | | ±0.01 | | | ±0.01 | | | * | | %/°C |
| Supply Rejection (±15V ±1V) | | * | | | ±0.01 | | | * | | | * | | % |
| Nonlinearity | | | | | | | | | | | | | |
| X (X = 20Vp-p, Y = 10V) | | * | | | ±0.4 | | | 0.2 | ±0.3 | | * | | % |
| Y (Y = 20Vp-p, X = 10V) | | * | | | ±0.01 | | | * | ±0.1 | | * | | % |
| Feedthrough[3] | | | | | | | | | | | | | |
| X (Y Nulled, X = 20Vp-p, 50Hz) | | * | | | ±0.3 | | | ±0.15 | ±0.3 | | * | | % |
| Y (X Nulled, Y = 20Vp-p, 50Hz) | | * | | | ±0.01 | | | * | ±0.1 | | * | | % |
| Both Inputs (500kHz, 1Vrms) | | | | | | | | | | | | | |
| Unnulled | 40[4] | 50 | | 45 | 55 | | * | 60 | | * | * | | dB |
| Nulled | 55[4] | 60 | | 55 | 65 | | 60 | 70 | | * | * | | dB |
| Output Offset Voltage | | ±50 | ±100 | | ±5 | ±30 | | * | ±15 | | * | * | mV |
| Output Offset Voltage Drift | | * | | | ±200 | | | ±100 | | | * | ±500 | µV/°C |
| **DYNAMICS** | | | | | | | | | | | | | |
| Small Signal BW, | | | | | | | | | | | | | |
| ($V_{OUT}$ = 0.1Vrms) | 6[4] | * | | 8 | 10 | | * | * | | 6 | * | | MHz |
| 1% Amplitude Error | | | | | | | | | | | | | |
| ($C_{LOAD}$ = 1000pF) | | * | | | 100 | | | * | | | * | | kHz |
| Slew Rate ($V_{OUT}$ = 20Vp-p) | | * | | | 20 | | | * | | | * | | V/µs |
| Settling Time | | | | | | | | | | | | | |
| (to 1%, $\Delta V_{OUT}$ = 20V) | | * | | | 2 | | | * | | | * | | µs |
| **NOISE** | | | | | | | | | | | | | |
| Noise Spectral Density: | | | | | | | | | | | | | |
| SF = 10V | | * | | | 0.8 | | | * | | | * | | µV/√Hz |
| Wideband Noise: | | | | | | | | | | | | | |
| f = 10Hz to 5MHz | | * | | | 1 | | | * | | | * | | mVrms |
| f = 10Hz to 10kHz | | * | | | 90 | | | * | | | * | | µVrms |
| **OUTPUT** | | | | | | | | | | | | | |
| Output Voltage Swing | * | | | ±11 | | | * | | | * | | | V |
| Output Impedance (f ≤ 1kHz) | | * | | | 0.1 | | | * | | | * | | Ω |
| Output Short Circuit Current | | | | | | | | | | | | | |
| ($R_L$ = 0, $T_A$ = min to max) | | * | | | 30 | | | * | | | * | | mA |
| Amplifier Open Loop Gain | | | | | | | | | | | | | |
| (f = 50Hz) | | * | | | 85 | | | * | | | * | | dB |
| **INPUT AMPLIFIERS (X, Y and Z)** | | | | | | | | | | | | | |
| Input Voltage Range | | | | | | | | | | | | | |
| Differential $V_{IN}$ ($V_{CM}$ = 0) | | * | | | ±12 | | | * | | | * | | V |
| Common-Mode $V_{IN}$ ($V_{DIFF}$ = 0) | | * | | | ±10 | | | * | | | * | | V |
| (see Typical Performance Curves) | | | | | | | | | | | | | |
| Offset Voltage X, Y | | ±25 | ±100 | | ±5 | ±20 | | ±2 | ±10 | | * | * | mV |
| Offset Voltage Drift X, Y | | 200 | | | 100 | | | 50 | | | * | | µV/°C |
| Offset Voltage Z | | ±25 | ±100 | | ±5 | ±30 | | ±2 | ±15 | | * | * | mV |
| Offset Voltage Drift Z | | * | | | 200 | | | 100 | | | | 500 | µV/°C |
| CMRR | * | * | | 60 | 80 | | 70 | 90 | | * | * | | dB |
| Bias Current | | * | * | | 0.8 | 2.0 | | * | * | | * | * | µA |
| Offset Current | | * | | | 0.1 | | | * | | | * | 2.0 | µA |
| Differential Resistance | | * | | | 10 | | | * | | | * | | MΩ |
| **DIVIDER PERFORMANCE** | | | | | | | | | | | | | |
| Transfer Function ($X_1 > X_2$) | | * | | | $10V\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$ | | | * | | | * | | |
| Total Error[1] untrimmed | | | | | | | | | | | | | |
| (X = 10V, –10V ≤ Z ≤ +10V) | | 1.5 | | | ±0.75 | | | ±0.35 | | | ±0.75 | | % |
| (X = 1V, –1V ≤ Z ≤ +1V) | | 4.0 | | | ±2.0 | | | ±1.0 | | | * | | % |
| (0.1V≤ X ≤ 10V, –10V ≤ Z ≤ 10V) | | 5.0 | | | ±2.5 | | | ±1.0 | | | * | | % |
| **SQUARE PERFORMANCE** | | | | | | | | | | | | | |
| Transfer Function | | * | | | $\frac{(X_1 - X_2)^2}{10V} + Z_2$ | | | * | | | * | | |
| Total Error (–10V ≤ X ≤ 10V) | | ±1.2 | | | ±0.6 | | | ±0.3 | | | * | | % |

## SPECIFICATIONS (CONT)

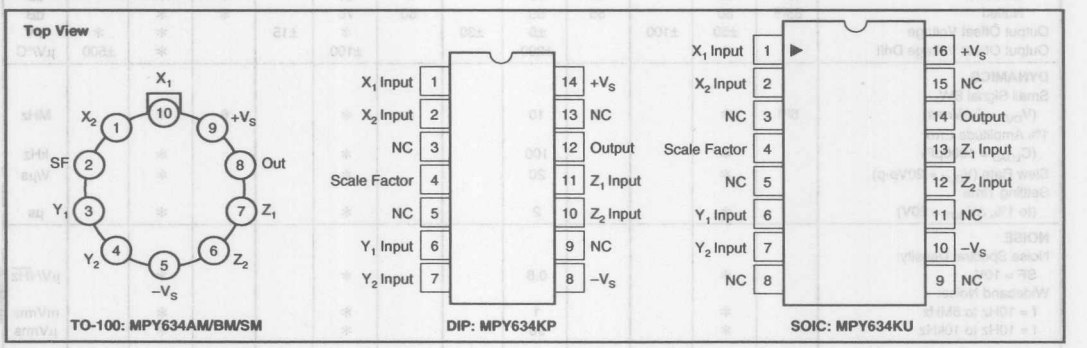
At $T_A$ = +25°C and $V_S$ = ±15VDC, unless otherwise noted.

| MODEL | MPY634KP/KU MIN | MPY634KP/KU TYP | MPY634KP/KU MAX | MPY634AM MIN | MPY634AM TYP | MPY634AM MAX | MPY634BM MIN | MPY634BM TYP | MPY634BM MAX | MPY634SM MIN | MPY634SM TYP | MPY634SM MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **SQUARE-ROOTER PERFORMANCE** | | | | | $\sqrt{10V\,(Z_2 - Z_1)} + X_2$ | | | | | | | | |
| Transfer Function ($Z_1 \leq Z_2$) | | * | | | | | | * | | | * | | |
| Total Error[1] (1V ≤ Z ≤ 10V) | | ±2.0 | | | ±1.0 | | | ±0.5 | | | * | | % |
| **POWER SUPPLY** | | | | | | | | | | | | | |
| Supply Voltage: | | | | | | | | | | | | | |
| Rated Performance | | * | | | ±15 | | | * | | | * | | VDC |
| Operating | * | | * | ±8 | | ±18 | * | | * | * | | ±20 | VDC |
| Supply Current, Quiescent | | * | * | | 4 | 6 | | * | * | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | | | | | | |
| Specification | *[5] | | *[5] | –25 | | +85 | * | | * | –55 | | +125 | °C |
| Storage | –40 | | +85 | –65 | | +150 | * | | * | * | | * | °C |

* Specification same as MPY634AM.

NOTES: (1) Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV). (2) May be reduced to 3V using external resistor between $-V_S$ and SF. (3) Irreducible component due to nonlinearity; excludes effect of offsets. (4) KP grade only. (5) KP grade only. 0°C to +70°C for KU grade.

### PIN CONFIGURATIONS




### ABSOLUTE MAXIMUM RATINGS

| PARAMETER | MPY634AM/BM | MPY634KP/KU | MPY634SM |
|---|---|---|---|
| Power Supply Voltage | ±18 | * | ±20 |
| Power Dissipation | 500mW | * | * |
| Output Short-Circuit to Ground | Indefinite | * | * |
| Input Voltage ( all X, Y and Z) | $\pm V_S$ | * | * |
| Temperature Range: | | | |
| Operating | –25°C/+85°C | * | –55°C/+125°C |
| Storage | –65°C/+150°C | –40°C/+85°C | * |
| Lead Temperature (soldering, 10s) | +300°C | * | * |
| SOIC 'KU' Package | | +260°C | |

* Specification same as for MPY634AM/BM.

### ORDERING INFORMATION

MPY634 ( ) ( )

Basic Model Number

Performance Grade[1]
- K: –25°C to +85°C ('U' package 0°C to +70°C)
- A: –25°C to +85°C
- B: –25°C to +85°C
- S: –55°C to +125°C

Package Code
- M: TO-100 Metal
- P: Plastic 14-pin DIP
- U: 16-pin SOIC

NOTE: (1) Performance grade identifier may not be marked on the SOIC package; a blank denotes "K" grade.

### PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| MPY634KP | 14-Pin PDIP | 010 |
| MPY634KU | 16-Pin SOIC | 211 |
| MPY634AM | TO-100 | 007 |
| MPY634BM | TO-100 | 007 |
| MPY634SM | TO-100 | 007 |

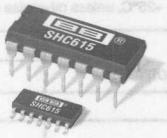
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®



# SHC615

www.burr-brown.com/databook/SHC615.html

# Wide-Bandwidth, DC RESTORATION CIRCUIT

## FEATURES

- PROPAGATION DELAY: 2.2ns
- BANDWIDTH: OTA: 750MHz
  Comparator: 280MHz
- LOW INPUT BIAS CURRENT: –0.3µA
- SAMPLE/HOLD SWITCHING TRANSIENTS: +1/–7mV
- SAMPLE/HOLD FEEDTHROUGH REJECTION: 100dB
- CHARGE INJECTION: 40fC
- HOLD COMMAND DELAY TIME: 3.8ns
- TTL/CMOS HOLD CONTROL

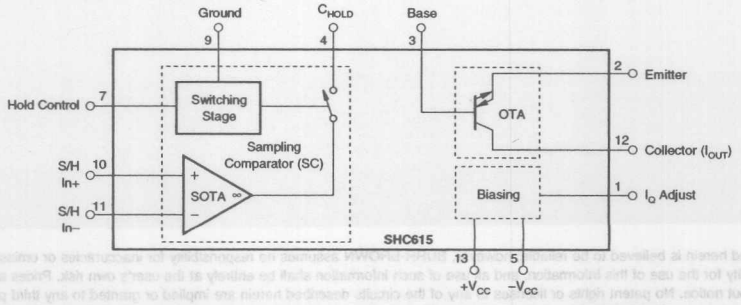
## APPLICATIONS

- BROADCAST/HDTV EQUIPMENT
- TELECOMMUNICATIONS EQUIPMENT
- HIGH-SPEED DATA ACQUISITION
- CAD MONITORS/CCD IMAGE PROCESSING
- NANO SECOND PULSE INTEGRATOR/ PEAK DETECTORS
- PULSE CODE MODULATOR/ DEMODULATOR
- COMPLETE VIDEO DC LEVEL RESTORATION
- SAMPLE/HOLD AMPLIFIER

## DESCRIPTION

The SHC615 is a complete subsystem for very fast and precise DC restoration, offset clamping, and low frequency hum suppression of wideband amplifiers or buffers. Designed to stabilize the performance of video signals, it can also be used as a sample/hold amplifier, high-speed integrator, or peak detector for nanosecond pulses. A wideband Operational Transconductance Amplifier (OTA) with a high-impedance cascode current source output and fast sampling comparator set a new standard for high-speed applications. Both can be used as stand-alone circuits or combined to form a more complex signal processing stage. The self-biased, bipolar OTA can be viewed as an ideal voltage-controlled current source and is optimized for low input bias current. The sampling comparator has two identical high-impedance inputs and a current source output optimized for low output bias current and offset voltage; it can be controlled by a TTL-compatible switching stage within a few nanoseconds. The transconductance of the OTA and sampling comparator can be adjusted by an external resistor, allowing bandwidth, quiescent current, and gain tradeoffs to be optimized.

The SHC615 is available in SO-14 surface mount and 14-pin plastic DIPs, and is specified over the extended temperature range of –40°C to +85°C.




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# DC SPECIFICATIONS

At $V_{CC}$ = ±5V, $R_{LOAD}$ = 100Ω, $R_Q$ = 300Ω, $R_{IN}$ = 150Ω and $T_A$ = +25°C, unless otherwise specified.

| PARAMETER | CONDITIONS | SHC615AP, AU | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **OFFSET VOLTAGE, $V_E$ at $V_B$ = 0** | | | | | |
| Initial | | | 8 | ±40 | mV |
| vs Temperature | | | 40 | | µV/°C |
| vs Supply (tracking) | $V_{CC}$ = ±4.5V to ±5.5V | 50 | 55 | | dB |
| **B-INPUT BIAS CURRENT** | | | | | |
| Initial | | | −0.3 | ±0.9 | µA |
| vs Temperature | | | 1 | | nA/°C |
| **C-OUTPUT BIAS CURRENT, $I_C$ at $V_B$ = 0** | | | | | |
| Initial | | −200 | −77 | +100 | µA |
| **B-INPUT IMPEDANCE** | | | 4.4 | | MΩ |
| **INPUT NOISE** | | | | | |
| Voltage Noise Density, B-to-E | $f_{OUT}$ = 100kHz to 100MHz | | 2.2 | | nV/√Hz |
| Voltage Noise Density, B-to-C | $f_{OUT}$ = 100kHz to 100MHz | | 4.5 | | nV/√Hz |
| **INPUT VOLTAGE RANGE** | | | ±3.4 | | V |
| **OUTPUT** | | | | | |
| Output Voltage Compliance | | | ±3.2 | | V |
| C-Current Output | | ±18 | ±20 | | mA |
| E-Current Output | | ±18 | ±20 | | mA |
| C-Output Impedance | | | 0.5 | | MΩ |
| E-Output Impedance | | | 12 | | Ω |
| Open-Loop Gain | | | 96 | | dB |
| **TRANSCONDUCTANCE** | Small Signal, <200mV | | 70 | | mA/V |

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## DC SPECIFICATIONS (CONT)

At $V_{CC}$ = ±5V, $R_{LOAD}$ = 1kΩ, $R_Q$ = 300Ω, and $T_A$ = +25°C, unless otherwise specified.

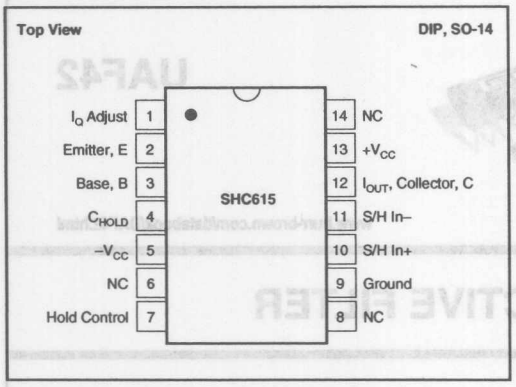
| PARAMETER | CONDITIONS | SHC615AP, AU MIN | SHC615AP, AU TYP | SHC615AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **COMPARATOR** | | | | | |
| **INPUT BIAS CURRENT** | | | | | |
| Initial | | | 1.0 | ±5 | µA |
| vs Temperature | | | –2.3 | | nA/°C |
| **C-OUTPUT BIAS CURRENT** | | | | | |
| Initial | | | ±10 | ±50 | µA |
| vs Temperature | | | ±13 | | nA/°C |
| **INPUT IMPEDANCE** | | | | | |
| Input Impedance | | | 0.2 | | MΩ |
| **INPUT NOISE** | | | | | |
| Voltage Noise Density | $f_{OUT}$ = 100kHz to 100MHz | | 5 | | nV/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | |
| Input Voltage Range | | | ±3.0 | | V |
| Common-Mode Input Range | | | ±3.2 | | V |
| **OUTPUT** | | | | | |
| Output Voltage Compliance | | | ±3.5 | | V |
| C-Current Output | | ±2.5 | ±3.2 | | mA |
| C-Output Impedance | | | 620 ll 2 | | kΩ ll pF |
| Open-Loop Gain | | | 83 | | dB |
| **TRANSCONDUCTANCE** | | | | | |
| Transconductance | | | 22 | | mA/V |
| **HOLD CONTROL** | | | | | |
| Logic 1 Voltage | | +2 | | $+V_{CC}$ +0.6 | V |
| Logic 0 Voltage | | 0 | | 0.8 | V |
| Logic 1 Current | V Hold Control = 5.0V | | 1 | | µA |
| Logic 0 Current | V Hold Control = 0.8V | | 0.05 | | µA |
| **TRANSFER CHARACTERISTICS** | | | | | |
| Charge Injection | Track-To-Hold | | 40 | | fC |
| Feedthrough Rejection | Hold Mode | | –100 | | dB |
| **COMPLETE SHC615** | | | | | |
| **POWER SUPPLY** | | | | | |
| Rated Voltage | | | ±5 | | V |
| Derated Performance | | ±4.5 | | ±5.5 | V |
| Quiescent Current | $R_Q$ = 300Ω | ±12 | ±15 | ±18 | mA |
| Quiescent Current Range | Programmable (Useful Range) | | ±3 to ±36 | | mA |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –40 | | +85 | °C |
| Storage | | –40 | | +125 | °C |

## AC SPECIFICATIONS

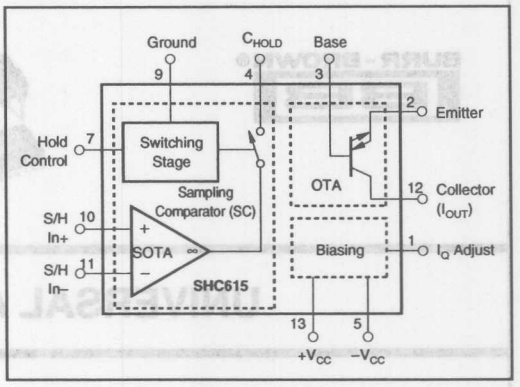
At $V_{CC}$ = ±5V, $R_{LOAD}$ = 100Ω, $R_{SOURCE}$ = 50Ω, $R_Q$ = 300Ω, and $T_A$ = +25°C, unless otherwise specified.

| PARAMETER | CONDITIONS | SHC615AP, AU MIN | SHC615AP, AU TYP | SHC615AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **FREQUENCY DOMAIN** | | | | | |
| **OTA** | | | | | |
| **LARGE-SIGNAL BANDWIDTH** (–3dB), (B-to-E) | $V_{OUT}$ = 5.0Vp-p | | 430 | | MHz |
| | $V_{OUT}$ = 2.8Vp-p | | 540 | | MHz |
| | $V_{OUT}$ = 1.4Vp-p | | 620 | | MHz |
| **SMALL-SIGNAL BANDWIDTH B-TO-E** | $V_{OUT}$ = 0.2Vp-p | | 520 | | MHz |
| **DIFFERENTIAL GAIN (B-TO-E)** | f = 4.43MHz, $V_{OUT}$ = 0.7Vp-p, | | | | |
| | $R_L$ = 150Ω | | 1.8 | | % |
| | $R_L$ = 500Ω | | 0.1 | | % |
| **DIFFERENTIAL PHASE** | f = 4.43MHz, $V_{OUT}$ = 0.7Vp-p, | | | | |
| | $R_L$ = 150Ω | | 0.07 | | ° |
| (B-to-E) | $R_L$ = 500Ω | | 0.01 | | ° |
| **HARMONIC DISTORTION (B-TO-E)** | f = 30MHz, $V_{OUT}$ = 1.4Vp-p | | | | |
| Second Harmonic | | | –50 | | dBc |
| Third Harmonic | | | –46 | | dBc |
| **LARGE SIGNAL BANDWIDTH** (–3dB), (B-to-C) | $V_{OUT}$ = 5.0Vp-p | | 250 | | MHz |
| | $V_{OUT}$ = 2.8Vp-p | | 580 | | MHz |
| | $V_{OUT}$ = 1.4Vp-p | | 750 | | MHz |
| **SMALL SIGNAL BANDWIDTH** B-to-C | $V_{OUT}$ = 0.2Vp-p | | 680 | | MHz |
| **COMPARATOR** | Sample Mode | | | | |
| **BANDWIDTH** (–3dB) | $I_{OUT}$ = 4mAp-p | | 240 | | MHz |
| | $I_{OUT}$ = 2mAp-p | | 270 | | MHz |
| | $I_{OUT}$ = 1mAp-p | | 280 | | MHz |
| **TIME DOMAIN** | | | | | |
| **OTA** | | | | | |
| **RISE TIME** | 2Vp-p Step, 10% to 90% | | | | |
| | B-to-E | | 1.1 | | ns |
| | B-to-C | | 1.2 | | ns |
| **SLEW RATE** | 2Vp-p, B-to-E | | 1800 | | V/µs |
| | B-to-C | | 1700 | | V/µs |
| | 5Vp-p, B-to-E | | 3300 | | V/µs |
| | B-to-C | | 3000 | | V/µs |
| **COMPARATOR** | | | | | |
| **RISE TIME** (Sample Mode) | 10% to 90%, $R_L$ = 50Ω, $I_{OUT}$ = ±2mA, $C_{LOAD}$ = 1pF | | 2.5 | | ns |
| **SLEW RATE** (Sample Mode) | 10% to 90%, $R_L$ = 50Ω, $I_{OUT}$ = ±2mA, $C_{LOAD}$ = 1pF | | 0.95 | | mA/ns |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Propagation Delay Time | $t_{PDH}$, $V_{OD}$ = 200mV | | 2.2 | | ns |
| Propagation Delay Time | $t_{PDL}$, $V_{OD}$ = 200mV | | 2.15 | | ns |
| Delay Time | Sample-to-Hold | | 3.8 | | ns |
| | Hold-to-Sample | | 3.0 | | ns |

## PIN CONFIGURATION




## BLOCK DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage ($\pm V_{CC}$) | ±6V |
| Input Voltage[1] | $\pm V_{CC}$ ±0.7V |
| Operating Temperature | –40°C to +85°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Hold Control | –0.5V to $+V_{CC}$ +0.7V |

NOTE: (1) Inputs are internally diode-clamped to $\pm V_{CC}$.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| SHC615AP | Plastic 14-Pin DIP | 010 | –40°C to +85°C |
| SHC615AU | SO 14-Lead Surface-Mount | 235 | –40°C to +85°C |

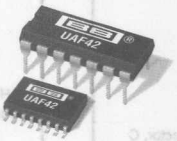
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

BURR-BROWN®



# UAF42

www.burr-brown.com/databook/UAF42.html

# UNIVERSAL ACTIVE FILTER

## FEATURES

- VERSATILE— LOW-PASS, HIGH-PASS BAND-PASS, BAND-REJECT
- SIMPLE DESIGN PROCEDURE
- ACCURATE FREQUENCY AND Q — INCLUDES ON CHIP 1000pF ±0.5% CAPACITORS

## APPLICATIONS

- TEST EQUIPMENT
- COMMUNICATIONS EQUIPMENT
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION SYSTEMS
- MONOLITHIC REPLACEMENT FOR UAF41

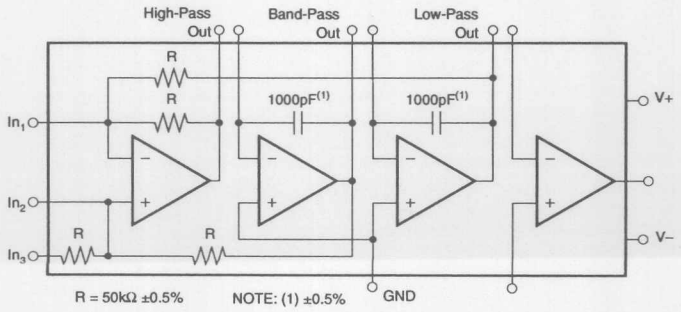
## DESCRIPTION

The UAF42 is a universal active filter which can be configured for a wide range of low-pass, high-pass, and band-pass filters. It uses a classical state-variable analog architecture with an inverting amplifier and two integrators. The integrators include on-chip 1000pF capacitors trimmed to 0.5%. This solves one of the most difficult problems of active filter design—obtaining tight tolerance, low-loss capacitors.

A DOS-compatible filter design program allows easy implementation of many filter types such as Butterworth, Bessel, and Chebyshev. A fourth, uncommitted FET-input op amp (identical to the other three) can be used to form additional stages, or for special filters such as band-reject and Inverse Chebyshev.

The classical topology of the UAF42 forms a time-continuous filter, free from the anomalies and switching noise associated with switched-capacitor filter types.

The UAF42 is available in 14-pin plastic DIP and SOL-16 surface-mount packages, specified for the –25°C to +85°C temperature range.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

| PARAMETER | CONDITIONS | UAF42AP, AU MIN | UAF42AP, AU TYP | UAF42AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **FILTER PERFORMANCE** | | | | | |
| Frequency Range, fn | | | 0 to 100 | | kHz |
| Frequency Accuracy | f = 1kHz | | | 1 | % |
| vs Temperature | | | 0.01 | | %/°C |
| Maximum Q | | | 400 | | — |
| Maximun (Q • Frequency) Product | | | 500 | | kHz |
| Q vs Temperature | $(f_O \bullet Q) < 10^4$ | | 0.01 | | %/°C |
| | $(f_O \bullet Q) < 10^5$ | | 0.025 | | %/°C |
| Q Repeatability | $(f_O \bullet Q) < 10^5$ | | 2 | | % |
| Offset Voltage, Low-Pass Output | | | | ±5 | mV |
| Resistor Accuracy | | | 0.5 | 1% | % |
| **OFFSET VOLTAGE**[1] | | | | | |
| Input Offset Voltage | | | ±0.5 | ±5 | mV |
| vs Temperature | | | ±3 | | µV/°C |
| vs Power Supply | $V_S$ = ±6 to ±18V | 80 | 96 | | dB |
| **INPUT BIAS CURRENT**[1] | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | 10 | 50 | pA |
| Input Offset Current | $V_{CM}$ = 0V | | 5 | | pA |
| **NOISE** | | | | | |
| Input Voltage Noise | | | | | |
| Noise Density: f = 10Hz | | | 25 | | nV/√Hz |
| f = 10kHz | | | 10 | | nV/√Hz |
| Voltage Noise: BW = 0.1 to 10Hz | | | 2 | | µVp-p |
| Input Bias Current Noise | | | | | |
| Noise Density: f = 10kHz | | | 2 | | fA/√Hz |
| **INPUT VOLTAGE RANGE**[1] | | | | | |
| Common-Mode Input Range | | | ±11.5 | | V |
| Common-Mode Rejection | $V_{CM}$ = ±10V | 80 | 96 | | dB |
| **INPUT IMPEDANCE**[1] | | | | | |
| Differential | | | $10^{13}$ ‖ 2 | | Ω ‖ pF |
| Common-Mode | | | $10^{13}$ ‖ 6 | | Ω ‖ pF |
| **OPEN-LOOP GAIN**[1] | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±10V, $R_L$ = 2kΩ | 90 | 126 | | dB |
| **FREQUENCY RESPONSE**[1] | | | | | |
| Slew Rate | | | 10 | | V/µs |
| Gain-Bandwidth Product | G = +1 | | 4 | | MHz |
| Total Harmonic Distortion | G = +1, f = 1kHz | | 0.0004 | | % |
| **OUTPUT**[1] | | | | | |
| Voltage Output | $R_L$ = 2kΩ | ±11 | ±11.5 | | V |
| Short Circuit Current | | | ±25 | | mA |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±15 | | V |
| Operating Voltage Range | | ±6 | | ±18 | V |
| Current | | | ±6 | ±7 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –25 | | +85 | °C |
| Operating | | –25 | | +85 | °C |
| Storage | | –40 | | +125 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | 100 | | °C/W |

* Same as specification for UAF42AP.

NOTES: (1) Specifications apply to uncommitted op amp, $A_4$. The three op amps forming the filter are identical to $A_4$ but are tested as a complete filter.

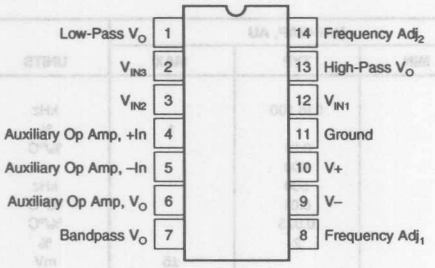


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## PIN CONFIGURATION

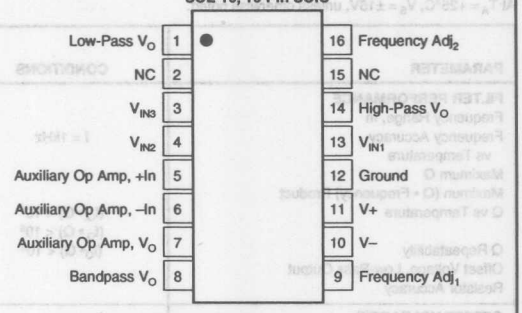
Top View

Plastic DIP, P




U Package

SOL-16, 16-Pin SOIC




NOTE: NC: No Connection. For best performance connect all "NC" pins to ground to minimize inter-lead capacitance.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | ±18V |
| Input Voltage | $\pm V_S$ ±0.7V |
| Output Short Circuit | Continuous |
| Operating Temperature: | |
| Plastic DIP, P; SOIC, U | –40°C to +85°C |
| Storage Temperature: | |
| Plastic DIP, P; SOIC, U | –40°C to +125°C |
| Junction Temperature: | |
| Plastic DIP, P; SOIC, U | +125°C |
| Lead Temperature (soldering, 10s) | +300°C |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| UAF42AP | Plastic 14-pin DIP | 010 | –25°C to +85°C |
| UAF42AU | SOL-16 | 211 | –25°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# 8 References and Regulators

Voltage and current references are used for bridge circuits, calibration standards, D/A and A/D converter reference, sensor excitation and other applications requiring a stable voltage or current reference.

Regulators are used for battery management, distributed power, SCSI-2 termination and any other applications requiring regulated power.

Choose from our complete line of references and regulators which include:

**REF1004-1.2**—1.235V ±4mV bandgap reference that will operate from as little as 10µA in an 8-lead SOIC package.

**REF1004-2.5**—2.500V ±20mV bandgap reference that will operate from as little as 20µA in an 8-lead SOIC package.

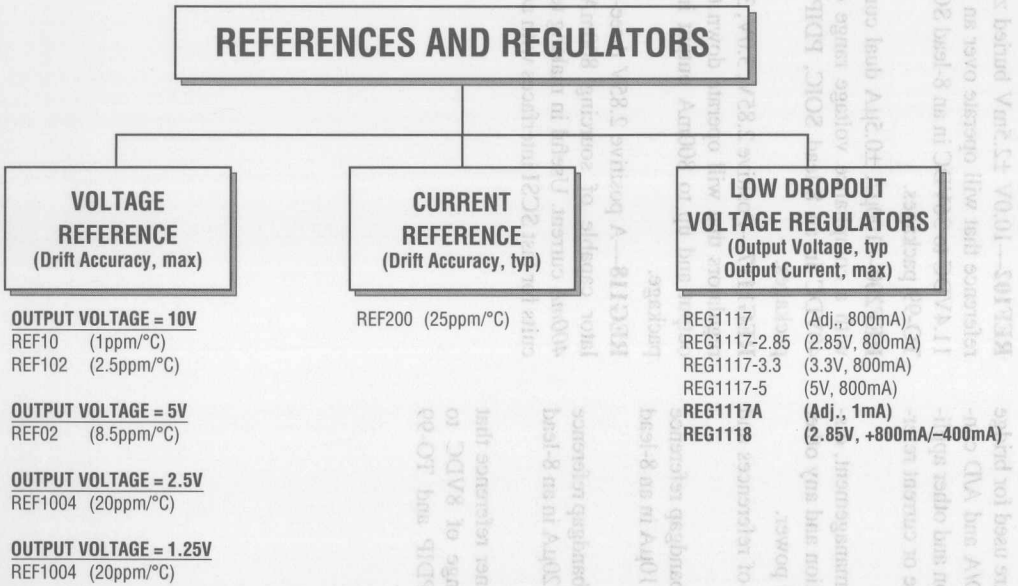
**REF02**—5.0V ±5mV buried zener reference that will operate over an input range of 8VDC to 40VDC in an 8-lead SOIC, PDIP and TO-99 packages.

**REF102**—10.0V ±2.5mV buried zener precision reference that will operate over an input range of 11.4VDC to 36VDC in an 8-lead SOIC, PDIP and TO-99 packages.

**REF200**—100µA ±0.5µA dual current reference with a compliance voltage range of 2.5VDC to 40VDC in an 8-lead SOIC, PDIP AND TO-99 packages.

**REG1117**—Positive 2.85V, 3.0V, 3.3V, and 5.0V regulators that will operate down to 1V input to output and up to 800mA output in an SOT-223 package.

**REG118**—A positive 2.85V three-terminal regulator capable of sourcing 800mA *and sinking 400mA* current. Useful in making termination circuits for fast SCSI interfaces with active negation.




**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPM***

Some specifications have been estimated for comparis
purposes. Refer to data sheets for guaranteed specific



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## VOLTAGE REFERENCE

| Product | Output (V) | Output Current min (mA) | Output Voltage Drift max (±ppm/°C) | Power Supply min, max (V) | Power Supply max (mA) | Temp Range[1] | Cerdip Pkg | Description |
|---|---|---|---|---|---|---|---|---|
| REF02P | +5.00 ±0.015 | 10 | 10 | +7/40 | 1.4 | Ind | PDIP | |
| REF10M | +10.00 ±0.005 | 10 | 1 | +13.5/35 | 4.5 | Com, Mil | TO-99 | Guaranteed Long-Term Stability, ±50ppm/1k hrs |
| REF102 | +10.00 ±0.0025 | 10 | 2.5 | +11.4/36 | 1.4 | Ind, Mil | TO-99, DIP, SOIC | |
| REF1004C | +1.235 ±0.006 | — | 20 | — | 10µA[2] | Com | SOIC | Precision Micropower Voltage Reference |
| REF1004I | +1.235 ±0.01 | — | 20 | — | 10µA[2] | XInd | SOIC | Precision Micropower Voltage Reference |
| REF1004C | +2.50 ±0.013 | — | 20 | — | 20µA[2] | Com | SOIC | Precision Micropower Voltage Reference |
| REF1004I | +2.50 ±0.02 | — | 20 | — | 20µA[2] | XInd | SOIC | Precision Micropower Voltage Reference |

NOTE: (1) Com = 0°C to +70°C. Ind = –25°C to +85°C, Mil = –55°C to +125°C. XInd = –40°C to +85°C. (2) Minimum Operating Current.

## CURRENT REFERENCE

| Product | Output Current (µA) | Voltage Compliance | Drift (max) (ppm/°C) | Pkg | Temp Range[1] | Description |
|---|---|---|---|---|---|---|
| REF200 | Dual 100 ±0.5 | 2.5 V to 40V | 25 | DIP, SO-8 | Ind | Includes 0.5% accurate current mirror. |

NOTE: (1) Ind = –25°C to +85°C.

## LOW DROPOUT VOLTAGE REGULATORS

| Product | Output Voltage (V) typ | Dropout Voltage at 800mA (V) max | Line Regulation (mV) | Load Regulation (mV) max | Quiescent Current (mA) | Temp Range | Pkg | Description |
|---|---|---|---|---|---|---|---|---|
| REG1117 | ADJ. | 1.2 | 0.4% | 0.4% | 10 | Com | SOT-223 | |
| REG1117-2.85 | +2.85 | 1.2 | 7 | 7 | 10 | Com | SOT-223 | +2.85V Voltage Regulator for SCSI-2 Active Termination |
| REG1117-3.3 | +3.3 | 1.2 | 7 | 7 | 10 | Com | SOT-223 | +3.3V Voltage Regulator |
| REG1117-5 | +5 | 1.2 | 10 | 10 | 10 | Com | SOT-223 | +5.0V Voltage Regulator |
| **REG1117A** | **Adj.** | **1.2** | **0.4%** | **0.4%** | **10** | **Com** | **SOT-223** | **Adjustable 1A Voltage Regulator** |
| **REG1118** | **+2.85** | **1.3** | **15** | **20** | **5** | **Com** | **SOT-223** | **+2.85V Voltage Regulator for FAST-20 SCSI Active Negation Termination** |

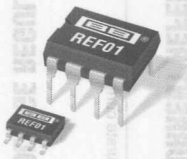
**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

BURR-BROWN®



# REF01

www.burr-brown.com/databook/REF01.html

# +10V Precision VOLTAGE REFERENCE

## FEATURES

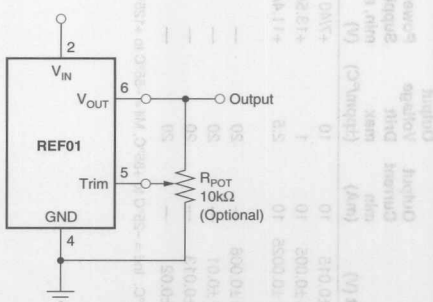
- OUTPUT VOLTAGE: +10V ±0.2% max
- EXCELLENT TEMPERATURE STABILITY: 8.5ppm/°C max (–40°C to +85°C)
- LOW NOISE: 5μVp-p typ (0.1Hz to 10Hz)
- EXCELLENT LINE REGULATION: 0.001%/V max
- EXCELLENT LOAD REGULATION: 0.002%/mA max
- SOURCES 10mA, SINKS 5mA min
- LOW SUPPLY CURRENT: 1.4mA max
- SHORT-CIRCUIT PROTECTED
- WIDE SUPPLY RANGE: 11.4VDC to 40VDC
- PACKAGE OPTIONS: Plastic DIP, SOIC
- EXTENDED INDUSTRIAL TEMPERATURE RANGE: –40°C to +85°C

## APPLICATIONS

- PRECISION REGULATORS
- CONSTANT CURRENT SOURCE/SINK
- DIGITAL VOLTMETERS
- A/D AND D/A CONVERTERS
- PRECISION CALIBRATION STANDARD
- TEST EQUIPMENT

## DESCRIPTION

The REF01 is a high performance, low price, precision pin compatible second source voltage reference. Output accuracy of ±0.2% is a 30% improvement over industry standard REF01s. Output noise is 5μVp-p, which is a 75% decrease in noise over all other REF01s. Line regulation is 0.001%/V max and load regulation is 0.002%/mA max, which far exceeds the performance of our competitors. Quiescent current is a low 1.4mA. REF01 provides extended supply range when compared to industry standard devices. Burr-Brown's REF01 is the best choice for applications which requires improved accuracy, low noise, low power consumption, low drift, and the lowest price. Popular package options are available: Plastic DIP, and SOIC. For guaranteed long-term drift see Burr-Brown's model REF10.




+10V Reference with Trimmed Output

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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C and $V_S$ = +15V power supply, unless otherwise noted.

| PARAMETER | CONDITIONS | REF01A | | | REF01B | | | REF01C | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OUTPUT VOLTAGE ($\Delta V_{OT}$)** | $I_L$ = 0mA | 9.970 | 10.0 | 10.030 | 9.975 | 10.0 | 10.025 | 9.980 | 10.0 | 10.020 | V |
| Change with Temperature[1, 2] | | | | | | | | | | | |
| –40°C to +85°C | | | 0.11 | 0.18 | | 0.06 | 0.11 | | 0.04 | 0.07 | % |
| **OUTPUT VOLTAGE DRIFT[3]** | | | | | | | | | | | |
| –40°C to +85°C ($TCV_O$) | | | 10 | 25 | | 8 | 15 | | 3 | 8.5 | ±ppm/°C |
| **OUTPUT ADJUSTMENT RANGE** | $R_{POT}$ = 10kΩ[6] | ±3 | | | ±3 | | | ±3 | | | % |
| **CHANGE IN $V_O$ TEMP COEFFICIENT WITH OUTPUT ADJUSTMENT** (–55°C to +125°C) | $R_{POT}$ = 10kΩ | | 0.5 | | | 0.5 | | | 0.5 | | ppm/% |
| **OUTPUT VOLTAGE NOISE** | 0.1Hz to 10Hz[5] | | 5 | | | 5 | | | 5 | | µVp-p |
| **LINE REGULATION[4]** | $V_{IN}$ = 11.4V to 36V | | 0.001 | 0.003 | | 0.0007 | 0.002 | | 0.0003 | 0.001 | %/V |
| –40°C to +85°C | | | 0.002 | 0.006 | | 0.001 | 0.004 | | 0.001 | 0.002 | |
| **LOAD REGULATION[4]** | $I_L$ = 0mA to +10mA | | 0.001 | 0.004 | | 0.001 | 0.003 | | 0.001 | 0.002 | %/mA |
| | $I_L$ = 0mA to –5mA | | 0.003 | 0.008 | | 0.002 | 0.006 | | 0.001 | 0.004 | |
| –40°C to +85°C | $I_L$ = 0mA to +10mA | | 0.005 | 0.016 | | 0.004 | 0.012 | | 0.003 | 0.008 | |
| **TURN-ON SETTLING TIME** | To ±0.1% of Final Value | | 5 | | | 5 | | | 5 | | µs |
| **QUIESCENT CURRENT** | No Load | | 1.2 | 1.4 | | 1.2 | 1.4 | | 1.2 | 1.4 | mA |
| **LOAD CURRENT** | | 10 | 21 | | 10 | 21 | | 10 | 21 | | mA |
| **SINK CURRENT** | | –5 | –10 | | * | * | | * | * | | mA |
| **SHORT-CIRCUIT CURRENT** | $V_O$ = 0 | | 30 | | | 30 | | | 30 | | mA |
| **POWER DISSIPATION** | | | 18 | | | 18 | | | 18 | | mW |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification | | | | | | | | | | | |
| REF01A, B, C | | –40 | | +85 | * | | * | * | | * | °C |

NOTES: (1) $\Delta V_{OT}$ is defined as the absolute difference between the maximum output and the minimum output voltage over the specified temperature range expressed as a percentage of 10V: $\Delta V_O = \frac{|V_{MAX} - V_{MIN}|}{10V} \times 100\%$. (2) $\Delta V_{OT}$ specification applies trimmed to +10.000V or untrimmed. (3) $TCV_O$ is defined as $\Delta V_{OT}$ divided by the temperature range. (4) Line and load regulation specifications include the effect of self heating. (5) Sample tested. (6) 10kΩ potentiometer connected between $V_O$ and ground with wiper connected to trim pin. See Figure 3.

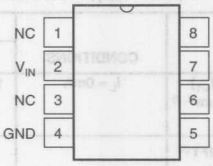
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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Input Voltage | +40V |
| Operating Temperature | |
| P, U | –40°C to +85°C |
| Storage Temperature Range | |
| P, U | –65°C to +125° |
| Output Short Circuit Duration (to Ground or $V_{IN}$) | Indefinite |
| Junction Temperature | –65°C to +150° |
| $\theta_{JA}$ P | 120°C/W |
| U | 80°C/W |
| Lead Temperature (soldering, 60s) | +300°C |

## PIN CONFIGURATIONS

Top View — DIP/SOIC




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE INFORMATION

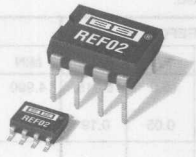
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| REF01AU | 8-Pin SOIC | 182 |
| REF01BU | 8-Pin SOIC | 182 |
| REF01AP | 8-Pin Plastic DIP | 006 |
| REF01BP | 8-Pin Plastic DIP | 006 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

| PRODUCT | $V_{OUT}$ AT 25°C | MAX DRIFT (ppm/°C) | TEMPERATURE | PACKAGE |
|---|---|---|---|---|
| REF01AU | 10V±30mV | ±25 | –40°C to +85°C | 8-Pin SOIC |
| REF01BU | 10V±25mV | ±15 | –40°C to +85°C | 8-Pin SOIC |
| REF01AP | 10V±30mV | ±25 | –40°C to +85°C | 8-Pin Plastic DIP |
| REF01BG | 10V±25mV | ±15 | –40°C to+85°C | 8-Pin Ceramic DIP |
| REF01BP | 10V±25mV | ±15 | –40°C to +85°C | 8-Pin Plastic DIP |

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# REF02

www.burr-brown.com/databook/REF02.html

# +5V Precision VOLTAGE REFERENCE

## FEATURES

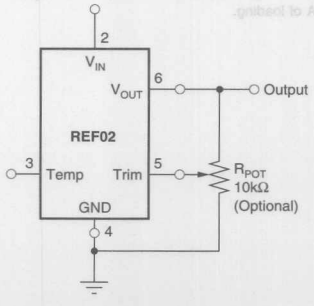
- OUTPUT VOLTAGE: +5V ±0.1% max
- EXCELLENT TEMPERATURE STABILITY: 8.5ppm/°C max (–40°C to +85°C)
- LOW NOISE: 10μVp-p max (0.1Hz to 10Hz)
- EXCELLENT LINE REGULATION: 0.008%/V max
- EXCELLENT LOAD REGULATION: 0.005%/mA max
- LOW SUPPLY CURRENT: 1.4mA max
- SHORT-CIRCUIT PROTECTED
- WIDE SUPPLY RANGE: 8V to 40V
- EXTENDED INDUSTRIAL TEMPERATURE RANGE: –40°C to +85°C
- PACKAGE OPTIONS: Plastic DIP, SOIC

## DESCRIPTION

The REF02 is a precision 5V voltage reference. The drift is laser trimmed to 8.5ppm/°C max over the extended industrial and military temperature range. The REF02 provides a stable 5V output that can be externally adjusted over a ±6% range with minimal effect on temperature stability. REF02 operates from a single supply with an input range of 8V to 40V with a very low current drain of 1mA, and excellent temperature stability due to an improved design. Excellent line and load regulation, low noise, low power, and low cost make the REF02 the best choice whenever a 5V voltage reference is required. All popular package options are available: plastic DIP, and SOIC. The REF02 is an ideal choice for portable instrumentation, temperature transducers, A/D and D/A converters, and digital voltmeter.

## APPLICATIONS

- PRECISION REGULATORS
- CONSTANT CURRENT SOURCE/SINK
- DIGITAL VOLTMETERS
- V/F CONVERTERS
- A/D AND D/A CONVERTERS
- PRECISION CALIBRATION STANDARD
- TEST EQUIPMENT




+5V Reference with Trimmed Output

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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C and $V_{IN}$ = +15V power supply, unless otherwise noted.

| PARAMETER | CONDITIONS | REF02A, R | | | REF02B, S | | | REF02C | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OUTPUT VOLTAGE** | $I_{LOAD}$ = 0mA | 4.985 | 5.0 | 5.015 | 4.990 | * | 5.010 | 4.995 | * | 5.005 | V |
| Change with Temperature[1, 2] ($\Delta V_{OT}$) | | | | | | | | | | | |
| –40°C to +85°C | | | 0.05 | 0.19 | | 0.05 | 0.13 | | 0.05 | 0.11 | % |
| **OUTPUT VOLTAGE DRIFT**[3] | | | | | | | | | | | |
| –40°C to +85°C ($TCV_O$) | | | 4 | 15 | | 4 | 10 | | 4 | 8.5 | ±ppm/°C |
| **OUTPUT ADJUSTMENT RANGE** | $R_{POT}$ = 10kΩ[6] | ±3 | ±6 | | * | * | | * | * | | % |
| **CHANGE IN $V_O$ TEMP COEFFICIENT WITH OUTPUT ADJUSTMENT** (–55°C to +125°C) | $R_{POT}$ = 10kΩ | | 0.7 | | | * | | | * | | ppm/% |
| **OUTPUT VOLTAGE NOISE** | 0.1Hz to 10Hz[5] | | 4 | 10 | | * | * | | * | * | µVp-p |
| **LINE REGULATION**[4] | $V_{IN}$ = 8V to 33V | | 0.006 | 0.010 | | * | * | | 0.004 | 0.008 | %/V |
| –40°C to +85°C | $V_{IN}$ = 8.5V to 33V | | 0.008 | 0.012 | | * | * | | 0.005 | 0.010 | |
| **LOAD REGULATION**[4] | $I_L$ = 0mA to +10mA | | 0.005 | 0.010 | | * | 0.008 | | 0.003 | 0.005 | %/mA |
| –40°C to +85°C | $I_L$ = 0mA to +10mA | | 0.007 | 0.012 | | * | 0.010 | | 0.004 | 0.005 | |
| **TURN-ON SETTLING TIME** | To ±0.1% of Final Value | | 5 | | | * | | | * | | µs |
| **QUIESCENT CURRENT** | No Load | | 1.0 | 1.4 | | * | * | | * | * | mA |
| **LOAD CURRENT (SOURCE)** | | 10 | 21 | | * | * | | * | * | | mA |
| **LOAD CURRENT (SINK)** | | –0.3 | –0.5 | | * | * | | * | * | | mA |
| **SHORT-CIRCUIT CURRENT** | $V_{OUT}$ = 0 | | 30 | | | * | | | * | | mA |
| **POWER DISSIPATION** | No Load | | 15 | 21 | | * | * | | * | * | mW |
| **TEMPERATURE VOLTAGE OUTPUT**[7] | | | 630 | | | * | | | * | | mV |
| **TEMPERATURE COEFFICIENT** of Temperature Pin Voltage –55°C to +125°C | | | 2.1 | | | | | | | | mV/°C |
| **TEMPERATURE RANGE** Specification REF02A, B, C | | –40 | | +85 | * | | * | * | | * | °C |

NOTES: (1) $\Delta V_{OT}$ is defined as the absolute difference between the maximum output and the minimum output voltage over the specified temperature range expressed as a percentage of 5V: $\Delta V_o = \left|\frac{V_{MAX} - V_{MIN}}{5V}\right| \times 100$ (2) $\Delta V_{OT}$ specification applies trimmed to +5.000V or untrimmed. (3) $TCV_O$ is defined as $\Delta V_{OT}$ divided by the temperature range. (4) Line and load regulation specifications include the effect of self heating. (5) Sample tested. (6) 10kΩ potentiometer connected between $V_{OUT}$ and ground with wiper connected to Trim pin. See Figure on page 1. (7) Pin 3 is insensitive to capacitive loading. The temperature voltage will be modified by 7mV for each µA of loading.



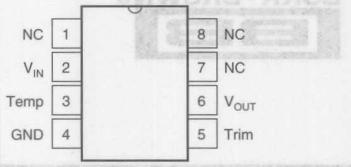
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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Input Voltage | +40V |
| Operating Temperature | |
| G, P, U | –40°C to +85°C |
| Storage Temperature Range | |
| G, P, U | –65°C to +125° |
| M | –65°C to +150° |
| Output Short Circuit Duration (to Ground or $V_{IN}$) | Indefinite |
| Junction Temperature | –65°C to +150° |
| $\theta_{JA}$ P | 120°C/W |
| U | 80°C/W |
| Lead Temperature (soldering, 60s) | +300°C |

## PIN CONFIGURATIONS

Top View DIP/SOIC




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE INFORMATION

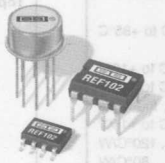
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| REF02AU | SOIC | 182 |
| REF02BU | SOIC | 182 |
| REF02AP | Plastic DIP | 006 |
| REF02BP | Plastic DIP | 006 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

| PRODUCT | $V_{OUT}$ AT 25°C | MAX DRIFT (ppm/°C) | TEMPERATURE | PACKAGE |
|---|---|---|---|---|
| REF02AU | 5V±15mV | ±15 | –40°C to +85°C | SOIC |
| REF02BU | 5V±10mV | ±10 | –40°C to +85°C | SOIC |
| REF02AP | 5V±15mV | ±15 | –40°C to +85°C | Plastic DIP |
| REF02BP | 5V±10mV | ±10 | –40°C to +85°C | Plastic DIP |

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# REF102

www.burr-brown.com/databook/REF102.html

# Precision VOLTAGE REFERENCE

## FEATURES

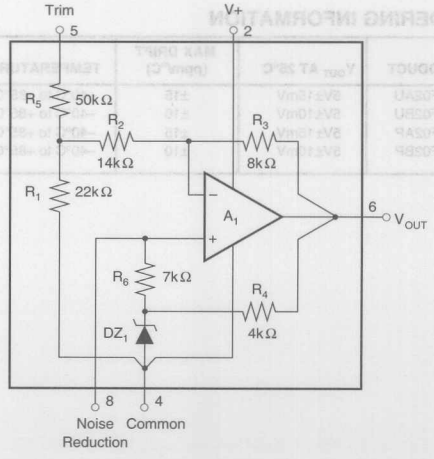
- +10V ±0.0025V OUTPUT
- VERY LOW DRIFT: 2.5ppm/°C max
- EXCELLENT STABILITY: 5ppm/1000hr typ
- EXCELLENT LINE REGULATION: 1ppm/V max
- EXCELLENT LOAD REGULATION: 10ppm/mA max
- LOW NOISE: 5μVp-p typ, 0.1Hz to 10Hz
- WIDE SUPPLY RANGE: 11.4VDC to 36VDC
- LOW QUIESCENT CURRENT: 1.4mA max
- PACKAGE OPTIONS: HERMETIC TO-99, PLASTIC DIP, SOIC

## APPLICATIONS

- PRECISION-CALIBRATED VOLTAGE STANDARD
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETERS
- TEST EQUIPMENT
- PC-BASED INSTRUMENTATION

## DESCRIPTION

The REF102 is a precision 10V voltage reference. The drift is laser-trimmed to 2.5ppm/°C max (CM grade) over the industrial temperature range and 5ppm/°C max (SM grade) over the military temperature range. The REF102 achieves its precision without a heater. This results in low power, fast warm-up, excellent stability, and low noise. The output voltage is extremely insensitive to both line and load variations and can be externally adjusted with minimal effect on drift and stability. Single supply operation from 11.4V to 36V and excellent overall specifications make the REF102 an ideal choice for demanding instrumentation and system reference applications.




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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C and $V_S$ = +15V power supply, unless otherwise noted.

| PARAMETER | CONDITIONS | REF102A, R | | | REF102B, S | | | REF102C, M | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OUTPUT VOLTAGE** | | | | | | | | | | | |
| Initial | $T_A$ = 25°C | 9.99 | | 10.01 | 9.995 | | 10.005 | 9.9975 | | 10.0025 | V |
| vs Temperature [1] | | | | 10 | | | 5 | | | 2.5 | ppm/°C |
| vs Supply (Line Regulation) | $V_S$ = 11.4V to 36V | | | 2 | | | 1 | | | 1 | ppm/V |
| vs Output Current (Load Regulation) | $I_L$ = 0mA to +10mA | | | 20 | | | 10 | | | 10 | ppm/mA |
| | $I_L$ = 0mA to –5mA | | | 40 | | | 20 | | | 20 | ppm/mA |
| vs Time | $T_A$ = 25° | | | | | | | | | | |
| M Package | | | 5 | | | * | | | * | | ppm/1000hr |
| P, U Packages [2] | | | 20 | | | * | | | | | ppm/1000hr |
| Trim Range [3] | | ±3 | | | * | | | * | | | % |
| Capacitive Load, max | | | 1000 | | | * | | | * | | pF |
| **NOISE** | (0.1Hz to 10Hz) | | 5 | | | * | | | * | | µVp-p |
| **OUTPUT CURRENT** | | +10, –5 | | | * | | | * | | | mA |
| **INPUT VOLTAGE RANGE** | | +11.4 | | +36 | * | | * | * | | * | V |
| **QUIESCENT CURRENT** | ($I_{OUT}$ = 0) | | | +1.4 | | | * | | | * | mA |
| **WARM-UP TIME** [4] | (To 0.1%) | | 15 | | | * | | | * | | µs |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification | | | | | | | | | | | |
| REF102A, B, C | | –25 | | +85 | * | | * | * | | * | °C |
| REF102R, S | | –55 | | +125 | * | | * | | | | °C |

* Specifications same as REF102A/R.

NOTES: (1) The "box" method is used to specify output voltage drift vs temperature. See the Discussion of Performance section. (2) Typically 5ppm/1000hrs after 168hr powered stabilization. (3) Trimming the offset voltage affects drift slightly. See Installation and Operating Instructions for details. (4) With noise reduction pin floating. See Typical Performance Curves for details.

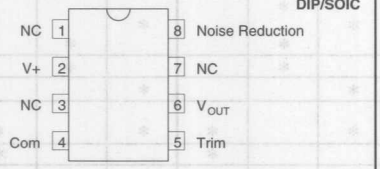


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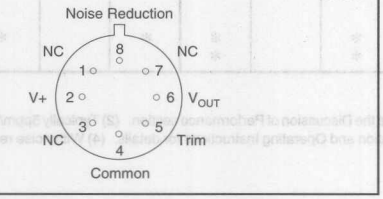
| PRODUCT | PACKAGE | TEMPERATURE RANGE | MAX INITIAL ERROR (mV) | MAX DRIFT (ppm/°C) |
|---|---|---|---|---|
| REF102AU | 8-Pin SOIC | –25°C to +85°C | ±10 | ±10 |
| REF102AP | 8-Pin Plastic DIP | –25°C to +85°C | ±10 | ±10 |
| REF102BP | 8-Pin Plastic DIP | –25°C to +85°C | ±5 | ±5 |
| REF102AM | Metal TO-99 | –25°C to +85°C | ±10 | ±10 |
| REF102BM | Metal TO-99 | –25°C to +85°C | ±5 | ±5 |
| REF102CM | Metal TO-99 | –25°C to +85°C | ±2.5 | ±2.5 |
| REF102RM | Metal TO-99 | –55°C to +125°C | ±10 | ±10 |
| REF102SM | Metal TO-99 | –55°C to +125°C | ±5 | ±5 |

## PIN CONFIGURATIONS

Top View — DIP/SOIC




Top View — TO-99




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

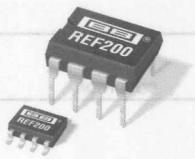
| | |
|---|---|
| Input Voltage | +40V |
| Operating Temperature | |
| P,U | –25°C to +85°C |
| M | –55°C to +125°C |
| Storage Temperature Range | |
| P,U | –40°C to +85°C |
| M | –65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (SOIC, 3s) | +260°C |
| Short-Circuit Protection to Common or V+ | Continuous |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| REF102AU | 8-Pin SOIC | 182 |
| REF102AP | 8-Pin Plastic DIP | 006 |
| REF102BP | 8-Pin Plastic DIP | 006 |
| REF102AM | Metal-TO-99 | 001 |
| REF102BM | Metal-TO-99 | 001 |
| REF102CM | Metal-TO-99 | 001 |
| REF102RM | Metal-TO-99 | 001 |
| REF102SM | Metal-TO-99 | 001 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# REF200

www.burr-brown.com/databook/REF200.html

# DUAL CURRENT SOURCE/CURRENT SINK

## FEATURES

- COMPLETELY FLOATING: No Power Supply or Ground Connections
- HIGH ACCURACY: 100µA ±0.5%
- LOW TEMPERATURE COEFFICIENT: ±25ppm/°C
- WIDE VOLTAGE COMPLIANCE: 2.5V to 40V
- ALSO INCLUDES CURRENT MIRROR

## APPLICATIONS

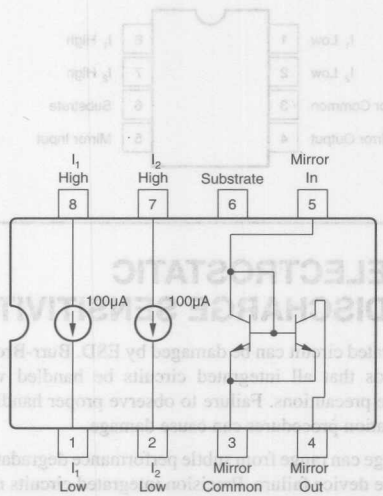
- SENSOR EXCITATION
- BIASING CIRCUITRY
- OFFSETTING CURRENT LOOPS
- LOW VOLTAGE REFERENCES
- CHARGE-PUMP CIRCUITRY
- HYBRID MICROCIRCUITS

## DESCRIPTION

The REF200 combines three circuit building-blocks on a single monolithic chip—two 100µA current sources and a current mirror. The sections are dielectrically isolated, making them completely independent. Also, since the current sources are two-terminal devices, they can be used equally well as current sinks. The performance of each section is individually measured and laser-trimmed to achieve high accuracy at low cost.

The sections can be pin-strapped for currents of 50µA, 100µA, 200µA, 300µA or 400µA. External circuitry can be used to obtain virtually any current. These and many other circuit techniques are shown in the Applications section of this Data Sheet.

The REF200 is available in plastic 8-pin mini-DIP and SOIC packages.






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# SPECIFICATIONS

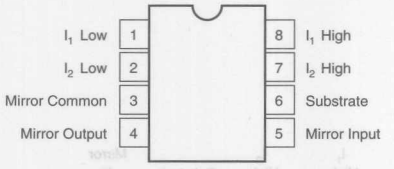
## ELECTRICAL

At $T_A$ = +25°C, $V_S$ = 15V, unless otherwise noted.

| PARAMETER | CONDITION | REF200AP, AU MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **CURRENT SOURCES** | | | | | |
| Current Accuracy | | | ±0.25 | ±1 | % |
| Current Match | | | ±0.25 | ±1 | % |
| Temperature Drift | Specified Temp Range | | 25 | | ppm/°C |
| Output Impedance | 2.5V to 40V | 20 | 100 | | MΩ |
| | 3.5V to 30V | 200 | 500 | | MΩ |
| Noise | BW = 0.1Hz to 10Hz | | 1 | | nAp-p |
| | f = 10kHz | | 20 | | pA/√Hz |
| Voltage Compliance (1%) | $T_{MIN}$ to $T_{MAX}$ | | See Curves | | |
| Capacitance | | | 10 | | pF |
| **CURRENT MIRROR** | I = 100µA Unless Otherwise Noted | | | | |
| Gain | | 0.995 | 1 | 1.005 | |
| Temperature Drift | | | 25 | | ppm/°C |
| Impedance (output) | 2V to 40V | 40 | 100 | | MΩ |
| Nonlinearity | I = 0µA to 250µA | | 0.05 | | % |
| Input Voltage | | | 1.4 | | V |
| Output Compliance Voltage | | | See Curves | | |
| Frequency Response (–3dB) | Transfer | | 5 | | MHz |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –25 | | +85 | °C |
| Operating | | –40 | | +85 | °C |
| Storage | | –40 | | +125 | °C |

## PIN CONFIGURATION

Top View — DIP/SOIC




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Applied Voltage | –6V to +40V |
| Reverse Current | –350µA |
| Voltage Between Any Two Sections | ±80V |
| Operating Temperature | –40°C to +85°C |
| Storage Temperature | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (SOIC 3s) | +260°C |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| REF200AP | 8-Pin Plastic DIP | 006 | –25°C to +85°C |
| REF200AU | 8-Pin SOIC | 182 | –25°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Grade designation "A" may not be marked. Absence of grade designation indicates A grade.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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# REF1004

www.burr-brown.com/databook/REF1004.html

# 1.2V and 2.5V Micropower VOLTAGE REFERENCE

## FEATURES

- INITIAL ACCURACY:
  REF1004-1.2 ±4mV
  REF1004-2.5 ±20mV
- MINIMUM OPERATING CURRENT:
  REF1004-1.2 10µA
  REF1004-2.5 20µA
- EXCELLENT LONG TERM TEMPERATURE STABILITY
- VERY LOW DYNAMIC IMPEDANCE
- OPERATES UP TO 20mA
- PACKAGE: 8-Lead SOIC

## APPLICATIONS

- BATTERY POWERED TEST EQUIPMENT
- PORTABLE MEDICAL INSTRUMENTATION
- PORTABLE COMMUNICATIONS DEVICES
- A/D AND D/A CONVERTERS
- NOTEBOOK AND PALMTOP COMPUTERS

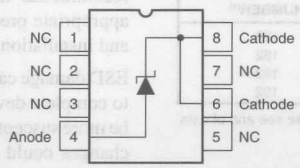
## DESCRIPTION

The REF1004-1.2 and REF1004-2.5 are two terminal bandgap reference diodes designed for high accuracy with outstanding temperature characteristics at low operating currents. Prior to the introduction of the REF1004 Micropower Voltage References, accuracy and stability specifications could only be attained by expensive screening of standard devices. The REF1004 is a cost effective solution when reference voltage accuracy, low power, and long term temperature stability are required.

REF1004 is a drop-in replacement for the LT1004 as well as an upgraded replacement of the LM185/385 series references. The REF1004C is characterized for operation from 0°C to 70°C and the REF1004I is characterized for operation from –40°C to +85°C.

The REF1004 is offered in an 8-lead Plastic SOIC package and shipped in anti-static rails or tape and reel.

Typical Operating Circuit




(Top View)

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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | REF1004-1.2 MIN | REF1004-1.2 TYP | REF1004-1.2 MAX | REF1004-2.5 MIN | REF1004-2.5 TYP | REF1004-2.5 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| REFERENCE VOLTAGE<br>REF1004C(1)<br>REF1004I(2) | $I_R$ = 100µA | <br>1.229<br>1.225 | 1.235<br>1.235<br>1.235 | <br>1.239<br>1.239 | 2.490<br>2.487<br>2.480 | 2.500<br>2.500<br>2.500 | 2.511<br>2.511<br>2.511 | V |
| AVERAGE TEMPERATURE COEFFICIENT | $I_{MIN} \le I_R \le$ 20mA | | 20 | | | 20 | | ppm/°C |
| MINIMUM OPERATION CURRENT(3) | | | 8 | 10 | | 12 | 20 | µA |
| REVERSE BREAKDOWN VOLTAGE CHANGE WITH CURRENT | $I_{MIN} \le I_R \le$ 1mA<br>1mA $\le I_R \le$ 20mA | | | 1<br>1.5(3)<br>10<br>20(3) | | | 1<br>1.5(3)<br>10<br>20(3) | mV |
| REVERSE DYNAMIC IMPEDANCE(3) | $I_R$ = 100µA | | 0.2 | 0.6 | | 0.2 | 0.6 | Ω |
| WIDE BAND NOISE (RMS)<br>10Hz $\le I_R \le$ 10kHz | $I_R$ = 100µA | | 60 | | | 120 | | µV |
| LONG TERM STABILITY<br>$T_A$ = 25°C ± 0.1°C | $I_R$ = 100µA | | 20 | | | 20 | | ppm/KHr |

NOTES: (1) This specification applies over the full operating temperature range of 0°C $\le T_A \le$ 70°C. (2) This specification applies over the full operating temperature range of 40°C $\le T_A \le$ +85°C. (3) Denotes the specifications which apply over the full operating temperature range.

## ORDERING INFORMATION

| PRODUCT | $T_A$ | $V_Z$ | PACKAGE |
|---|---|---|---|
| REF1004C-1.2 | 0°C to +70°C | 1.2V | 8-Lead SOIC |
| REF1004C-2.5 | 0°C to +70°C | 2.5V | 8-Lead SOIC |
| REF1004I-1.2 | –40°C to +85°C | 1.2V | 8-Lead SOIC |
| REF1004I-2.5 | –40°C to +85°C | 2.5V | 8-Lead SOIC |

NOTE: Available in Tape and Reel, Add –TR to Model Number.

## ABSOLUTE MAXIMUM RATINGS

Reverse Breakdown Current ..... 30mA
Forward Current ..... 10mA
Operating Temperature Range
REF1004C ..... 0°C to +70°C
REF1004I ..... –40°C to +85°C
Storage Temperature
REF1004C ..... –65°C to +150°C
REF1004I ..... –65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

## ORDERING INFORMATION

| PRODUCT | PART MARKING |
|---|---|
| REF1004C-1.2 | BBREF0412 |
| REF1004C-2.5 | BBREF0425 |
| REF1004I-1.2 | BBREF0412 |
| REF1004I-2.5 | BBREF0425 |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| REF1004C-1.2 | 8-Pin SOIC | 182 |
| REF1004C-2.5 | 8-Pin SOIC | 182 |
| REF1004I-1.2 | 8-Pin SOIC | 182 |
| REF1004I-2.5 | 8-Pin SOIC | 182 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

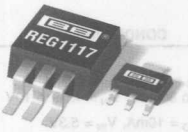
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# REG1117
# REG1117A

www.burr-brown.com/databook/REG1117.html

# 800mA and 1A Low Dropout Positive Regulator 2.85V, 3.3V, 5V, and Adjustable

## FEATURES

- 2.85V, 3.3V, 5V, and ADJUSTABLE VERSIONS
- 2.85V MODEL FOR SCSI-2 ACTIVE TERMINATION
- OUTPUT CURRENT:
  REG1117: 800mA max
  REG1117A: 1A max
- OUTPUT TOLERANCE: ±1% max
- DROPOUT VOLTAGE:
  REG1117: 1.2V max at $I_O$ = 800mA
  REG1117A: 1.3V max at $I_O$ = 1A
- INTERNAL CURRENT LIMIT
- THERMAL OVERLOAD PROTECTION
- SOT-223 AND DDPAK SURFACE MOUNT PACKAGES

## APPLICATIONS

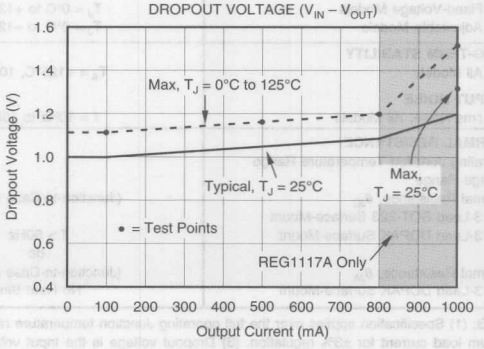
- SCSI-2 ACTIVE TERMINATION
- HAND-HELD DATA COLLECTION DEVICES
- HIGH EFFICIENCY LINEAR REGULATORS
- 5V LINEAR REGULATORS
- BATTERY POWERED INSTRUMENTATION
- BATTERY MANAGEMENT CIRCUITS FOR NOTEBOOK AND PALMTOP PCs

## DESCRIPTION

The REG1117 is a family of three-terminal voltage regulators capable of up to 800mA output. The REG1117 is offered in 2.85V, 3.3V, and 5V fixed output versions as well as an adjustable version. The REG1117A provides 1A of output current in an adjustable version. Output voltage of the adjustable versions is set with two external resistors. The REG1117's low dropout voltage allows its use with as little as 1V input-output voltage differential.

Laser trimming assures excellent output voltage accuracy without adjustment. An NPN output stage allows output stage drive to contribute to the load current for maximum efficiency.

REG1117 (all versions) and REG1117A are packaged in an SOT-223 surface-mount package, suitable for reflow soldering techniques. In addition, REG1117-3.3 and REG1117A are available in a 3-Lead DDPAK surface-mount power package.




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# SPECIFICATIONS

At $T_J$ = +25°C, unless otherwise noted.

| PARAMETER | | CONDITIONS | REG1117, REG1117A MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **OUTPUT VOLTAGE** | | | | | | |
| REG1117-2.85 | | $I_O$ = 10mA, $V_{IN}$ = 4.85V | 2.82 | 2.85 | 2.88 | V |
| | Note 1 | $I_O$ = 0 to 800mA, $V_{IN}$ = 4.05 to 10V | 2.79 | 2.85 | 2.91 | V |
| REG1117-3.3 | | $I_O$ = 10mA, $V_{IN}$ = 5.3V | 3.27 | 3.30 | 3.33 | V |
| | Note 1 | $I_O$ = 0 to 800mA, $V_{IN}$ = 4.8 to 10V | 3.24 | 3.30 | 3.36 | V |
| REG1117-5 | | $I_O$ = 10mA, $V_{IN}$ = 7V | 4.95 | 5.00 | 5.05 | V |
| | Note 1 | $I_O$ = 0 to 800mA, $V_{IN}$ = 6.5 to 10V | 4.90 | 5.00 | 5.10 | V |
| **REFERENCE VOLTAGE** | | | | | | |
| REG1117 (Adjustable) | | $I_O$ = 10mA, $V_{IN} - V_O$ = 2V | 1.238 | 1.250 | 1.262 | V |
| | Note 1 | $I_O$ = 10 to 800mA, $V_{IN} - V_O$ = 1.4 to 10V | 1.225 | 1.250 | 1.280 | V |
| REG1117A (Adjustable) | | $I_O$ = 10mA, $V_{IN} - V_O$ = 2V | 1.238 | 1.250 | 1.262 | V |
| | Note 1 | $I_O$ = 10mA to 1A, $V_{IN} - V_O$ = 1.4 to 10V | 1.225 | 1.250 | 1.280 | V |
| **LINE REGULATION** | | | | | | |
| REG1117-2.85 | Note 1 | $I_O$ = 0, $V_{IN}$ = 4.25 to 10V | | 1 | 7 | mV |
| REG1117-3.3 | Note 1 | $I_O$ = 0, $V_{IN}$ = 4.8 to 10V | | 2 | 7 | mV |
| REG1117-5 | Note 1 | $I_O$ = 0, $V_{IN}$ = 6.5 to 15V | | 3 | 10 | mV |
| REG1117 (Adjustable) | Note 1 | $I_O$ = 10mA, $V_{IN} - V_O$ = 1.5 to 13.75V | | 0.1 | 0.4 | % |
| REG1117A (Adjustable) | Note 1 | $I_O$ = 10mA, $V_{IN} - V_O$ = 1.5 to 13.75V | | 0.1 | 0.4 | % |
| **LOAD REGULATION** | | | | | | |
| REG1117-2.85 | Note 1 | $I_O$ = 0 to 800mA, $V_{IN}$ = 4.25V | | 2 | 10 | mV |
| REG1117-3.3 | Note 1 | $I_O$ = 0 to 800mA, $V_{IN}$ = 4.8V | | 3 | 12 | mV |
| REG1117-5 | Note 1 | $I_O$ = 0 to 800mA, $V_{IN}$ = 6.5V | | 3 | 15 | mV |
| REG1117 (Adjustable) | Note 1, 2 | $I_O$ = 10 to 800mA, $V_{IN} - V_O$ = 3V | | 0.1 | 0.4 | % |
| REG1117A (Adjustable) | Note 1, 2 | $I_O$ = 10mA to 1A, $V_{IN} - V_O$ = 3V | | 0.1 | 0.4 | % |
| **DROPOUT VOLTAGE** | Note 3 | | | | | |
| All Models | Note 1 | $I_O$ = 100mA | | 1.00 | 1.10 | V |
| | Note 1 | $I_O$ = 500mA | | 1.05 | 1.15 | V |
| REG1117 Models | Note 1 | $I_O$ = 800mA | | 1.10 | 1.20 | V |
| REG1117A | | $I_O$ = 1A | | 1.2 | 1.30 | V |
| | Note 1 | $I_O$ = 1A | | 1.2 | 1.55 | V |
| **CURRENT LIMIT** | | | | | | |
| REG1117 Models | | $V_{IN} - V_O$ = 5V | 800 | 950 | 1200 | mA |
| REG1117A | | $V_{IN} - V_O$ = 5V | 1000 | 1250 | 1600 | mA |
| **MINIMUM LOAD CURRENT** | | | | | | |
| Adjustable Models | Note 1, 2 | $V_{IN} - V_O$ = 13.75V | | 1.7 | 5 | mA |
| **QUIESCENT CURRENT** | | | | | | |
| Fixed-Voltage Models | Note 1 | $V_{IN} - V_O$ = 5V | | 4 | 10 | mA |
| **Adjust Pin Current** | Note 1, 2 | $I_O$ = 10mA, $V_{IN} - V_O$ = 1.4 to 10V | | 50 | 120 | µA |
| vs Load Current, REG1117 | Note 1 | $I_O$ = 10mA to 800mA, $V_{IN} - V_O$ = 1.4 to 10V | | 0.5 | 5 | µA |
| vs Load Current, REG1117A | Note 1 | $I_O$ = 10mA to 1A, $V_{IN} - V_O$ = 1.4 to 10V | | 0.5 | 5 | µA |
| **THERMAL REGULATION** | | | | | | |
| All Models | Note 4 | 30ms Pulse | | 0.01 | 0.1 | %/W |
| **RIPPLE REJECTION** | | | | | | |
| All Models | | f = 120Hz, $V_{IN} - V_{OUT}$ = 3V+1$V_{PP}$ Ripple | | 62 | | dB |
| **TEMPERATURE DRIFT** | | | | | | |
| Fixed-Voltage Models | | $T_J$ = 0°C to +125°C | | 0.5 | | % |
| Adjustable Models | | $T_J$ = 0°C to +125°C | | 2 | | % |
| **LONG-TERM STABILITY** | | | | | | |
| All Models | | $T_A$ = +125°C, 1000Hr | | 0.3 | | % |
| **OUTPUT NOISE** | | | | | | |
| rms Noise, All Models | | f = 10Hz to 10kHz | | 0.003 | | % |
| **THERMAL RESISTANCE** | | | | | | |
| Operating Junction Temperature Range | | | 0 | | +125 | °C |
| Storage Range | | | –65 | | +150 | °C |
| Thermal Resistance, $\theta_{JC}$ | | (Junction-to-Case at Tab) | | | | |
| 3-Lead SOT-223 Surface-Mount | | | | 15 | | °C/W |
| 3-Lead DDPAK Surface-Mount | | f > 50Hz | | 2 | | °C/W |
| | | dc | | 3 | | °C/W |
| Thermal Resistance, $\theta_{JA}$ | | (Junction-to-Case at Tab) | | | | |
| 3-Lead DDPAK Surface-Mount | | No Heat Sink | | 65 | | °C/W |

NOTES: (1) Specification applies over the full operating Junction temperature range, 0°C to 125°C. (2) REG1117 and REG1117A adjustable versions require a minimum load current for ±3% regulation. (3) Dropout voltage is the Input voltage minus output voltage that produces a 1% decrease in output voltage. (4) Percentage change in unloaded output voltage before vs after a 30ms power pulse of $I_O$ = 800mA (REG1117 models), $I_O$ = 1A (REG1117A), $V_{IN} - V_O$ = 1.4V (Reading taken 10ms after pulse).

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Power Dissipation | Internally Limited |
| Input Voltage | 15V |
| Operating Junction Temperature Range | 0°C to +125°C |
| Storage Temperature Range | –65°C to +150°C |
| Lead Temperature (soldering, 10s)[2] | +300°C |

NOTE: (1) Stresses above these ratings may cause permanent damage. (2) See "Soldering Methods."

## ORDERING INFORMATION

| PRODUCT[1] | PART MARKING | PACKAGE |
|---|---|---|
| **800mA Current Out** | | |
| REG1117-2.85 | BB11172 | Plastic SOT-223 |
| REG1117-3.3 | BB11174 | Plastic SOT-223 |
| REG1117F-3.3 | REG1117F4 | Plastic 3-Lead DDPAK |
| REG1117-5 | BB11175 | Plastic SOT-223 |
| REG1117 | BB1117 | Plastic SOT-223 |
| **1A Current Out** | | |
| REG1117A | BB1117A | Plastic SOT-223 |
| REG1117FA | REG1117FA | Plastic 3-Lead DDPAK |

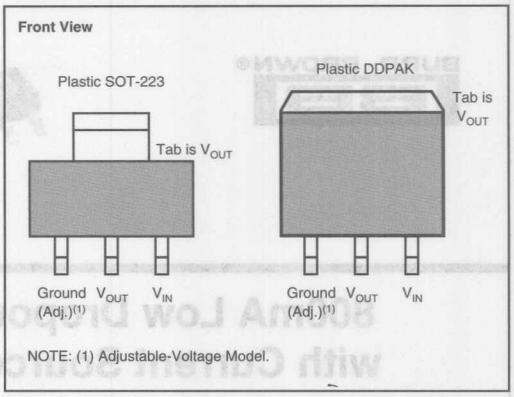
NOTE: (1) Available in Tape and Reel, add –TR to Model Number.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| **800mA Current Out** | | |
| REG1117-2.85 | Plastic SOT-223 | 311 |
| REG1117-3.3 | Plastic SOT-223 | 311 |
| REG1117F-3.3 | Plastic 3-Lead DDPAK | 339 |
| REG1117-5 | Plastic SOT-223 | 311 |
| REG1117 | Plastic SOT-223 | 311 |
| **1A Current Out** | | |
| REG1117A | Plastic SOT-223 | 311 |
| REG1117FA | Plastic 3-Lead DDPAK | 339 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## CONNECTION DIAGRAM



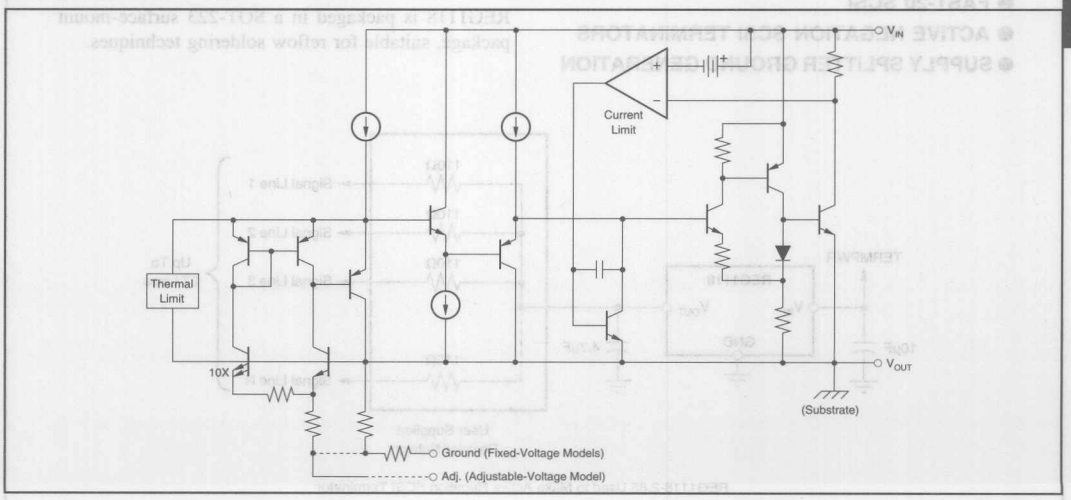

NOTE: (1) Adjustable-Voltage Model.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## SIMPLIFIED SCHEMATIC




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# REG1118

www.burr-brown.com/databook/REG1118.html

# 800mA Low Dropout Positive Regulator with Current Source and Sink Capability

## FEATURES

- SOURCES 800mA, SINKS 400mA
- 2.85V OUTPUT FOR SCSI ACTIVE NEGATION TERMINATION
- 1.3V max DROPOUT VOLTAGE AT $I_O$ = 800mA
- INTERNAL CURRENT LIMIT
- THERMAL OVERLOAD PROTECTION
- SOT-223 SURFACE MOUNT PACKAGE

## APPLICATIONS

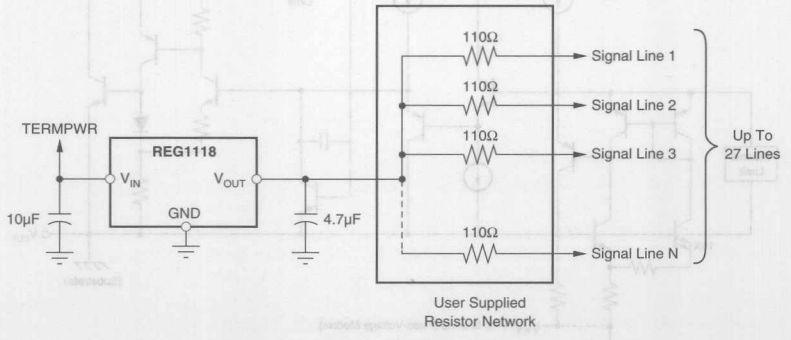
- SCSI-2 AND SCSI-3 DEVICES
- FAST-20 SCSI
- ACTIVE NEGATION SCSI TERMINATORS
- SUPPLY SPLITTER GROUND GENERATION

## DESCRIPTION

The REG1118-2.85 is a three-terminal voltage regulators capable of sourcing up to 800mA and sinking up to 400mA. The sinking capability is important in SCSI applications where active negation line drivers are used. The REG1118-2.85 is useful for making a 27-line Boulay terminator capable of interfacing with active negation drivers required in FAST-20 SCSI applications. The regulator has active current limits for both sink and source currents as well as internal thermal limiting.

Laser trimming assures excellent output voltage accuracy. An NPN output stage allows output stage drive current to contribute to the source load current for maximum efficiency.

REG1118 is packaged in a SOT-223 surface-mount package, suitable for reflow soldering techniques.




REG1118-2.85 Used to Make Active Negation SCSI Terminator

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = 0°C to 70°C, TERMPWR = +5V, unless otherwise noted.

| PARAMETER | CONDITIONS | REG1118-2.85 MIN | REG1118-2.85 TYP | REG1118-2.85 MAX | UNITS |
|---|---|---|---|---|---|
| **OUTPUT VOLTAGE** | | | | | |
| | No Load, $T_A$ = 25°C | 2.82 | 2.85 | 2.88 | V |
| | All Operating Conditions(1) | 2.79 | 2.85 | 2.91 | V |
| **LINE REGULATION(2)** | | | | | |
| | $I_O$ = 0, $V_{IN}$ = 4.75V to 6V | | 0.3 | 4 | mV |
| **LOAD REGULATION(2)** | | | | | |
| | $I_O$ = 0 to 800mA | | 2 | 25 | mV |
| | $I_O$ = –400 to 0mA | | 25 | 60 | mV |
| **DROPOUT VOLTAGE(3)** | $T_A$ = 25°C | | | | |
| | $I_O$ = 100mA | | 0.8 | 1.1 | V |
| | $I_O$ = 800mA | | 1.1 | 1.3 | V |
| **CURRENT LIMIT** | $T_A$ = 25°C | | | | |
| Positive ($I_{SC}$+)(4) | | 800 | 1450 | | mA |
| Negative ($I_{SC}$–) | $V_{OUT}$ = 3.7V | | –750 | –400 | mA |
| **QUIESCENT CURRENT** | $I_O$ = 0 | | 3 | 7 | mA |
| **RIPPLE REJECTION** | $T_A$ = 25°C | | | | |
| | f = 120Hz, $V_{IN} - V_{OUT}$ = 2V, $V_{RIPPLE}$ = 0.5Vp-p | | 56 | | dB |
| **LONG-TERM STABILITY** | | | | | |
| | $T_A$ = +125°C, 1000Hr | | 0.2 | | % |
| **THERMAL SHUTDOWN** | | | | | |
| Junction Temperature Shutdown | | | 150 | | °C |
| Junction Temperature Reset | | | 140 | | °C |
| **THERMAL RESISTANCE** | | | | | |
| Specified Junction Temperature Range | | 0 | | 70 | °C |
| Operating Junction Temperature Range | | 0 | | 125 | °C |
| Storage Range | | –55 | | 125 | °C |
| Thermal Resistance | | | | | |
| $\theta_{JC}$ | (Junction-to-Case at Tab) | | 15 | | °C/W |

NOTES: (1) All operating conditions include the combined effects of load current, input voltage, and temperature over each parameter's full specified range. (2) Load and line regulation are tested at a constant junction temperature by low duty cycle testing. (3) Dropout voltage is defined as the minimum input-to-output voltage that produces a 1% decrease in output voltage. (4) $V_{OUT}$ to ground through 1Ω.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Input Voltage | 7V |
| Output Voltage | –0.2V to (V+) +0.5V |
| Short-Circuit Duration | Indefinite |
| Operating Junction Temperature Range | 0°C to +125°C |
| Storage Temperature Range | –55°C to +125°C |
| Lead Temperature (soldering, 10s)(1) | +300°C |

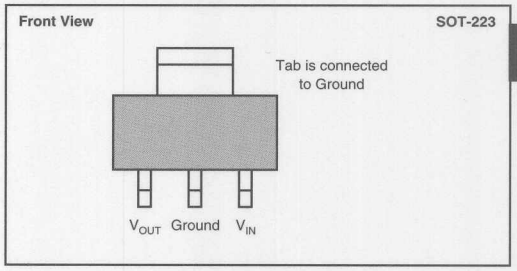
NOTE: (1) See "Soldering Methods."

## PACKAGE/ORDERING INFORMATION

| PRODUCT(1) | PACKAGE | PACKAGE DRAWING NUMBER(2) | PART MARKING |
|---|---|---|---|
| REG1118-2.85 | SOT-223 | 311 | BB11182 |

NOTE: (1) Available in Tape and Reel, add –TR to Model Number. (2) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## CONNECTION DIAGRAM




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

At $T_A$ = 0°C to 70°C, TERMPWR = +5V, unless otherwise noted.

| PARAMETER | CONDITIONS | REG1117-2.85 | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| OUTPUT VOLTAGE | No Load, $T_A$ = 25°C | 2.82 | 2.85 | 2.88 | V |
| | All Operating Conditions[1] | 2.79 | 2.85 | 2.91 | V |
| LINE REGULATION[2] | $I_O$ = 0, $V_{IN}$ = 4.75V to 6V | | 0.3 | 4 | mV |
| LOAD REGULATION[2] | $I_O$ = 0 to 800mA | | 2 | 25 | mV |
| | $I_O$ = −40 to 0mA | | 25 | 60 | mV |
| DROPOUT VOLTAGE[3] | $T_A$ = 25°C | | | | |
| | $I_O$ = 100mA | | 0.9 | 1.1 | V |
| | $I_O$ = 800mA | | 1.1 | 1.3 | V |
| CURRENT LIMIT | $T_A$ = 25°C | | | | |
| Positive ($I_{SC+}$)[4] | | 800 | 1450 | | mA |
| Negative ($I_{SC-}$) | $V_{OUT}$ = 3.7V | | −750 | −400 | mA |
| QUIESCENT CURRENT | $I_O$ = 0 | | 0 | 7 | mA |
| RIPPLE REJECTION | f = 120Hz, $V_{IN}$ − $V_{OUT}$ = 2V, $V_{RIPPLE}$ = 0.5Vp-p | | 56 | | dB |
| LONG-TERM STABILITY | $T_A$ = +125°C, 1000h | | 0.2 | | % |
| THERMAL SHUTDOWN | | | | | |
| Junction Temperature Shutdown | | | 150 | | °C |
| Junction Temperature Reset | | | 140 | | °C |
| THERMAL RESISTANCE | | | | | |
| Specified Junction Temperature Range | | 0 | | 70 | °C |
| Operating Junction Temperature Range | | 0 | | 125 | °C |
| Storage Range | | −65 | | 125 | °C |
| Thermal Resistance | | | | | |
| $\theta_{JC}$ | (Junction-to-Case at Tab) | | 15 | | °C/W |

NOTES: (1) All operating conditions include the combined effects of load current, input voltage, and temperature over each parameter's full specified range. (2) Load and line regulation are tested at a constant junction temperature by low duty cycle testing. (3) Dropout voltage is defined as the minimum input-to-output voltage that produces a 1% decrease in output voltage. (4) $V_{OUT}$ to ground transient.

## ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... 7V
Output Voltage ..... −0.2V to (VIN) +0.6V
Short-Circuit Duration ..... Indefinite
Operating Junction Temperature Range ..... 0°C to +125°C
Storage Temperature Range ..... −65°C to +125°C
Lead Temperature (soldering, 10s)[1] ..... +300°C

NOTE: (1) See "Soldering Methods".

## PACKAGE/ORDERING INFORMATION

| PRODUCT[1] | PACKAGE | PACKAGE DRAWING NUMBER[2] | PART MARKING |
|---|---|---|---|
| REG1117-2.85 | SOT-223 | 311 | 1117-2.8 |

NOTE: (1) Available in Tape and Reel; add –TR to Model Number. (2) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## CONNECTION DIAGRAM

SOT-223




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# Mixed Signal Products

# Mixed Signal Products

*Or, Call Customer Service at 1-800-548-6132 (USA Only)*

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# 2 A/D Converters, Data Acquisition Components

Burr-Brown's analog-to-digital (A/D) converter product line offers a broad selection of resolutions, 12-, 11- and 24-bit for industrial applications, and 16-, 18-, and 24-bit designed especially for audio applications.

**ADS7841** is a complete 4 channel, 12-bit, 200kHz, sample rate serial output interface A/D. The SPI/SSI interface allows a simple and easy interface to micro controllers.

**ADS7843** is a complete 12-bit monolithic sampling A/D designed for 4-wire touch-screen panels. It includes the panel drivers on-chip for simple and easy use.

**ADS7818** is a complete 12-bit, 500kHz, A/D in the smallest package, and with simple and easy to use SPI/SSI interface. It includes S/H, 12-bit A/D, SPI/SSI interface and internal reference.

**ADS1201** is a 130dB dynamic range delta-sigma modulator designed for very hi-resolution applications.

**DDC112** is a 20-bit, 2kHz/channel, dual-channel current input A/D converter with direct photo sensor interface.

The *SpeedPLUS* line of high speed A/D converters continues to grow. It now includes new 8-, 10-, and 12-bit resolution. 5-80MHz sampling converters covering a wide range of applications. All models utilize a leading edge pipeline architecture. SpeedPLUS converters feature a wide dynamic range wideband track/hold, internal or external reference options, low power, flexible input ranges and three-state output drivers.

**ADS900 and ADS901** are 10-bit, 20MHz A/D converters operating down to +2.7V and feature either an internal or external reference. ADS902 is 10-bit, 30MHz A/D, operates from +5V, utilizes an external reference and offers a flexible input range of either 1Vp-p or 2Vp-p. The ADS930 and ADS931 are 8-bit, 30MHz A/D converters that operate from either +3V or +5V supplies and feature an internal or external reference.

**ADS803, ADS804, and ADS805** are a new family of 12-bit, 5-, 10- and 20MHz respectively high dynamic performance A/D converters. All are pin compatible and offer the best combination of high dynamic performance with low power dissipation making them ideal for applications ranging from communications to digital cameras.

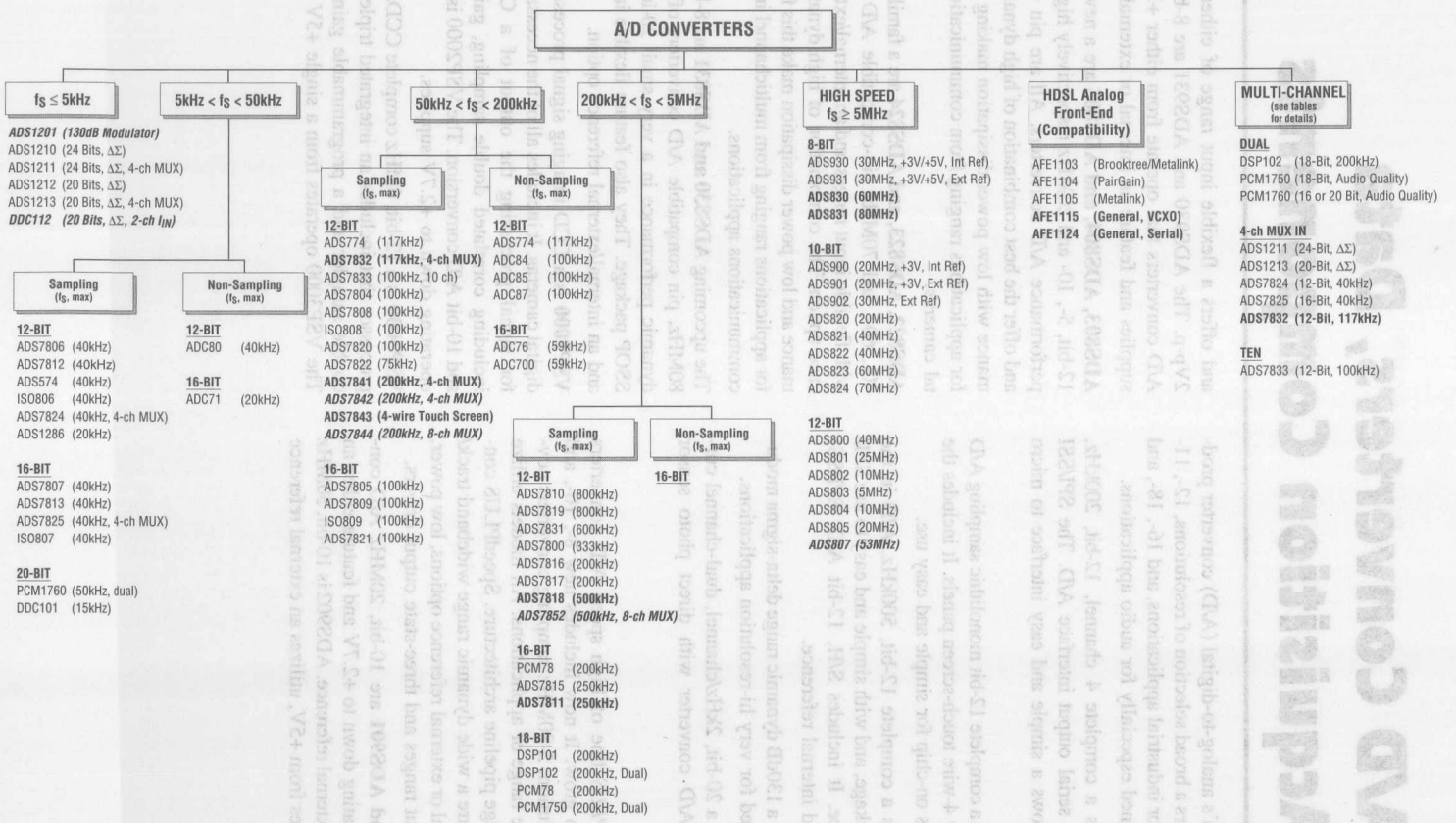
**ADS822, ADS823, and ADS824** are a family of 10-bit, 40-, 60-, and 70MHz pin-compatible A/D converters with flexible input ranges and an internal/external reference option. The combination of high dynamic performance and low power dissipation make this family ideal for applications ranging from multichannel imaging and communications applications.

The upcoming **ADS830 and ADS831** are 8-bit, 60- and 80MHz, pin compatible A/D converters offering high dynamic performance in a very small 20-lead narrow SSOP package. They also feature flexible input ranges and an internal/external reference option.

**VSP2000** is a CCD imaging signal processing IC for digital cameras. It includes all of the necessary features for signal processing the output of a CCD array, including correlated double sampling, gain ranging, and 10-bit A/D conversion. The VSP2000 is capable of operating down to +2.7V supplies.

**VSP3000** is a 12-bit, 6MHz complete CCD/CIS signal processor that includes an integrated triple correlated double sampler and a programmable gain amplifier. The VSP3000 operates from a single +5V supply.

# Analog-to-Digital Converters




**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

*For Immediate Assistance, Contact Your Local Salesperson*

## GENERAL

| Product | Resolution (Bits) | Linearity Error max (%FSR) | NMC[4] | Input Range (V) (see table, pg 34) | Sampling Rate (kHz) | THD (dB, max) | SFDR (dB, min) | Temp Range[1] | Pkg[2] | Serial or Parallel | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC71 | 16 | ±0.003 | 14 | D, E, F, N, R, S | 20 | — | | Ind, Com | TDIP | S, P | Industry Std Pinouts |
| ADC76 | 16 | ±0.003 | 14 | D, E, N, R, S | 60 | — | | Ind, Com | TDIP | S, P | Industry Std Pinouts |
| ADC80AG | 12 | ±0.012 | 12 | D, E, N, R, S | 40 | — | | Ind | TDIP | S, P | Industry Std Pinout and Interface Medium Speed Monolithic |
| ADC84KG | 12 | ±0.012 | 12 | D, E, N, R, S | 100 | — | | Ind | TDIP | S, P | Medium Speed |
| ADC85H | 12 | ±0.012 | 12 | D, E, N, R, S | 100 | — | | Com | TDIP | S, P | Medium Speed |
| ADC87H | 12 | ±0.012 | 12 | D, E, N, R, S | 100 | — | | Mil | TDIP | S, P | Mil Temperature Range |
| ADC700 | 16 | ±0.003 | 14 | D, E, F, N, R, S | 59 | — | | Mil, Ind, Com | TDIP | S, P | Data-Bus Interface |
| ADS574 | 12 | ±0.012 | 12 | E, F, R, S | 40 | — | | Com, Mil | DIP, DDIP, SO | P | Sampling 574 Type |
| ADS800 | 12 | ±0.024 | 12 | Z | 40MHz | | 61* | Com | SOIC, SSOP | P | Sampling, Internal Reference |
| ADS801 | 12 | ±0.024 | 12 | Z | 25MHz | | 61* | Com | SOIC, SSOP | P | Sampling, Internal Reference |
| ADS802 | 12 | ±0.024 | 12 | Z | 10MHz | | 67* | Com | SOIC, SSOP | P | Sampling, Internal Reference |
| ADS803 | 12 | | 12 | FF | 5MHz | | 82* | XInd | SOIC, SSOP | P | Low Power, Ext/Int Ref Option |
| ADS804 | 12 | | 12 | FF | 10MHz | | 80* | XInd | SOIC, SSOP | P | Low Power, Ext/Int Ref Option |
| ADS805 | 12 | | 12 | FF | 20MHz | | 77* | XInd | SOIC, SSOP | P | Low Power, Ext/Int Ref Option |
| ***ADS807*** | ***12*** | | ***12*** | ***FF, HH, II, JJ*** | ***53MHz*** | | ***82**** | ***XInd*** | ***SSOP*** | ***P*** | ***Low Power, Ext/Int Ref Option*** |
| ADS820 | 10 | ±0.097 | 10 | Z | 20MHz | | 63* | Com | SOIC, SSOP | P | Sampling, Internal Reference |
| ADS821 | 10 | ±0.097 | 10 | Z | 40MHz | | 63* | Com | SOIC, SSOP | P | Sampling, Internal Reference |
| ADS822 | 10 | | 10 | FF, GG | 40MHz | | 66* | XInd | SSOP | P | Low Power, Ext/Int Ref Option |
| ADS823 | 10 | | 10 | FF, GG | 60MHz | | 74* | XInd | SSOP | P | Low Power, Ext/Int Ref Option |
| ADS824 | 10 | | 10 | FF, GG | 70MHz | | 68* | XInd | SSOP | P | Low Power, Ext/Int Ref Option |
| **ADS830** | **8** | | **8** | **FF, GG** | **60MHz** | | **73*** | **XInd** | **SSOP** | **P** | **Low Power, Ext/Int Ref Option** |
| **ADS831** | **8** | | **8** | **FF, GG** | **80MHz** | | **65*** | **XInd** | **SSOP** | **P** | **Low Power, Ext/Int Ref Option** |
| ADS900 | 10 | | 10 | CC | 20MHz | | 53* | XInd | SSOP | P | Low Power, Internal Reference |
| ADS901 | 10 | | 10 | CC | 20MHz | | 49* | XInd | SSOP | P | Low Power, External Reference |
| ADS902 | 10 | | 10 | DD | 30MHz | | 60* | XInd | SSOP | P | Low Power, External Reference |
| ADS930 | 8 | | 8 | CC, EE | 30MHz | | 50* | XInd | SSOP | P | Low Power, External Reference |
| ADS931 | 8 | | 8 | CC, EE | 30MHz | | 49* | XInd | SSOP | P | Low Power, External Reference |
| ***ADS1201*** | ***130dB*** | | ***24*** | ***D, S*** | ***Programmable*** | ***—*** | ***—*** | ***XInd*** | ***SOIC*** | ***S*** | ***Single-Channel, ΔΣ, Modulator*** |
| ADS1210 | 24 | ±0.0015 | 24 | D, S | Programmable | — | — | XInd | SOIC, PDIP | S | Single-Channel, ΔΣ, Differential In |
| ADS1211 | 24 | ±0.0015 | 24 | D, S | Programmable | — | — | XInd | SOIC, PDIP, SSOP | S | 4-Channel MUX, ΔΣ, Differential In |
| ADS1212 | 20 | ±0.0015 | 20 | D, S | Programmable | — | — | XInd | PDIP, SOIC | S | Low Power, Single-Channel, ΔΣ |
| ADS1213 | 20 | ±0.0015 | 20 | D, S | Programmable | — | — | XInd | PDIP, SOIC, SSOP | S | Low Power, Four-Channel, ΔΣ |
| ADS1286 | 12 | ±0.024 | 12 | D | 20 | –80 | 86 | XInd | PDIP, SOIC, MSOP | S | Low Power, 1mW Unipolar Input |
| ADS7800 | 12 | ±0.012 | 12 | R, S | 333 | — | 77 | Com, Ind | DIP, SOIC | P | Sampling, Interface |
| ADS7804 | 12 | ±0.012 | 12 | S | 100 | –80 | 80 | XInd | PDIP, SOIC | P | Full Parallel, Pin Compatible to ADS7805 |
| ADS7805 | 16 | ±0.0045 | 16 | S | 100 | –94 | 94 | XInd | PDIP, SOIC | P | Full Parallel, Pin Compatible to ADS7804 |
| ADS7806 | 12 | ±0.012 | 12 | C, D, S | 40 | –80 | 80 | XInd | PDIP, SOIC | S, P | 8-Bit Bytes or Serial, Pin Compatible to ADS7807 |
| ADS7807 | 16 | ±0.0023 | 16 | C, D, S | 40 | –96 | 96 | XInd | PDIP, SOIC | S, P | 8-Bit Bytes or Serial, Pin Compatible to ADS7806 |
| ADS7808 | 12 | ±0.012 | 12 | C, D, E, P, R, S | 100 | –80 | 80 | XInd | PDIP, SOIC | S | Pin Compatible to ADS7809 |

* DENOTES TYPICAL
**BOLD DENOTES NEW PRODUCT**
***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

## GENERAL (CONT)

| Product | Resolution (Bits) | Linearity Error max (%FSR) | NMC[4] | Input Range (see table below) (V) | Sampling Rate (kHz) | THD (dB, max) | SFDR (dB, min) | Temp Range[1] | Pkg[2] | Serial or Parallel | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS7809 | 16 | ±0.006 | 16 | C, D, E, P, R, S | 100 | –96 | 96 | XInd | PDIP, SOIC | S | Pin Compatible to ADS7808 |
| ADS7810 | 12 | ±0.018 | 12 | S | 800 | –77 | 77 | XInd | PDIP, SOIC | P | Sampling, 12-Bit, 800kHz |
| **ADS7811** | **16** | **±0.0045** | **15** | **N** | **250** | | | **XInd** | **PDIP, SOIC** | **P** | **Sampling, w/Internal Reference** |
| ADS7812 | 12 | ±0.012 | 12 | S, AA, R, E, M, P, BB | 40 | –80 | 80 | XInd | PDIP, SO | S | Sampling, pin compatible with ADS7813 |
| ADS7813 | 16 | ±0.0023 | 16 | S, AA, R, E, M, P, BB | 40 | –96 | 96 | XInd | PDIP, SO | S | Sampling, pin compatible with ADS7812 |
| ADS7815 | 16 | ±0.006* | 15 | N | 250 | –96 | 96 | XInd | SOIC | P | Sampling, w/Internal Reference |
| ADS7816 | 12 | ±0.024 | 12 | D | 200 | –84 | 86 | XInd | PDIP, SOIC, MSOP | S | Low Power, 2.5mW, Unipolar Input |
| ADS7817 | 12 | ±0.024 | 12 | J | 200 | –83 | 86 | XInd | PDIP, SOIC, MSOP | S | Low Power, 2.5mW, Bipolar Input |
| **ADS7818** | **12** | **±0.024** | **12** | **O** | **500** | **–78** | **80** | **XInd** | **PDIP, SOIC, MSOP** | **S** | **Low Power, 10mW, Internal Reference** |
| ADS7819 | 12 | 0.018 | 12 | N | 800 | –77 | 77 | XInd | PDIP, SOIC | P | Sampling, 12-Bit, 800kHz |
| ADS7820 | 12 | ±0.01 | 12 | D | 100 | –80 | 80 | XInd | PDIP, SOIC | P | Sampling, pin compatible with ADS7821 |
| ADS7821 | 16 | ±0.006 | 16 | D | 100 | –94 | 94 | Ind | PDIP, SOIC | P | Sampling, pin compatible with ADS7820 |
| ADS7822 | 12 | ±0.024 | 12 | O | 75 | –82 | 86 | XInd | PDIP, SOIC, MSOP | S | Low Power, 0.6mW Unipolar Input |
| ADS7824 | 12 | ±0.01 | 12 | S | 40 | –80 | 80 | XInd | PDIP, SOIC | S, P | Sampling, 4-ch mux input |
| ADS7825 | 16 | ±0.002 | 16 | S | 40 | –90 | 90 | XInd | PDIP, SOIC | S, P | Sampling, 4-ch mux input |
| ADS7831 | 12 | 0.024 | 12 | N | 600 | –77 | 77 | XInd | PDIP, SOIC | P | Low Cost |
| **ADS7832** | **12** | **±0.024** | **12** | **B, D** | **117** | **—** | **—** | **XInd** | **PDIP, LCC** | **P** | **Sampling, 4-ch MUX, Auto Calibration** |
| ADS7833 | 12 | 0.05 | 12 | I, L, M, N | 100 | — | | XInd | PLCC | S | 3-channel, simultaneous sampling |
| **ADS7841** | **12** | **±0.012** | **12** | **D** | **200kHz** | **–76** | **76** | **XInd** | **PDIP, SSOP** | **S** | **Sampling, 4-Channel MUX, Low Power** |
| ***ADS7842*** | ***12*** | ***±0.012*** | ***12*** | ***D*** | ***200kHz*** | ***–76*** | ***76*** | ***XInd*** | ***PDIP, SSOP*** | ***P*** | ***Sampling, 4-Channel MUX, Low Power*** |
| **ADS7843** | **12** | **±0.012** | **12** | **D** | **125kHz** | **—** | **—** | **XInd** | **SSOP** | **S** | **4-Wire Touch-Screen Controller** |
| ***ADS7844*** | ***12*** | ***±0.012*** | ***12*** | ***D*** | ***200*** | ***–76*** | ***76*** | ***XInd*** | ***SSOP*** | ***S*** | ***8-Channel, ALT Source MAX 147*** |
| ***ADS7852*** | ***12*** | ***±0.012*** | ***12*** | ***D*** | ***500*** | ***–76*** | ***76*** | ***XInd*** | ***QSOP*** | ***P*** | ***8-Channel, 2.5V RGF*** |
| DDC101 | 20 | ±2.5ppm[3] | 18 | Current | 15 | — | | Ind | DDIP, SOIC | S | High Accuracy |
| ***DDC112*** | ***20*** | | ***20*** | ***See Data Sheet*** | ***2kHz/Channel*** | **—** | **—** | ***XIND*** | ***SOIC*** | ***S*** | ***Dual Channel, Current Input, ΔΣ*** |
| DSP101 | 18 | 0.003 | — | O | 200 | –90 | | Com | DDIP | S | DSP Compatible, Single Channel |
| DSP102 | 18 | 0.003 | — | O | 200 | –90 | | Com | DDIP | S | DSP Compatible, Dual Channel |
| ISO806 | 12 | ±0.022 | 12 | C, D, S | 40 | –90* | | Ind | PDIP | S | Isolated, Rated 1500Vrms |
| ISO807 | 16 | ±0.0046 | 15 | C, D, S | 40 | –100* | | Ind | PDIP | S | Isolated, Rated 1500Vrms |
| ISO808 | 12 | ±0.022 | 12 | C, D, E, P, R, S | 100 | –90* | | Ind | PDIP | S | Isolated, Rated 1500Vrms |
| ISO809 | 16 | ±0.006 | 15 | C, D, E, P, R, S | 100 | –100* | | Ind | PDIP | S | Isolated, Rated 1500Vrms |

NOTES: (1) Com = 0°C to +70°C, XInd = –40°C to +85°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) DIP = 0.3" wide DIP, DDIP = 0.6" wide DIP, TDIP = 0.9" wide DIP, PLCC = Plastic Leaded Chip Carrier, SO = Small Outline Surface Mount. (3) Linearity errors ±0.025% reading ±2.5ppm FSR. (4) NMC = No Missing Codes.

### KEY FOR A/D CONVERTER INPUT RANGE SPECIFICATION TABLE

| SPECIFICATION CODE | RANGE (V) | SPECIFICATION CODE | RANGE (V) | SPECIFICATION CODE | RANGE (V) |
|---|---|---|---|---|---|
| A | 0 to 1.25 | K | ±1.0 | AA | 0.3125 to 2.8125 |
| B | 0 to 2.5 | L | ±1.25 | BB | 0.5 to 4.5 |
| C | 0 to 4 | M | ±2.0 | CC | 1.0 to 2.0 (S-E) |
| D | 0 to 5 | N | ±2.5 | DD | 1.25 to 3.25 (S-E) |
| E | 0 to 10 | O | ±2.75 | EE | 2 to 4, 2 to 3 (S-E) |
| F | 0 to 20 | P | ±3.33 | FF | 1.5 to 3.5 (S-E) |
| G | 0 to –10 | Q | ±4.0 | GG | 2.0 to 3.0 (S-E) |
| H | ±0.312 | R | ±5.0 | HH | 1.75 to 3.25 (Diff) |
| I | ±0.5 | S | ±10.0 | II | 2.0 to 3.0 (Diff) |
| J | ±0.625 | Z | 1.25 to 3.25 (Diff) | JJ | 1.0 to 4.0 (S-E) |

**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

For Immediate Assistance, Contact Your Local Salesperson

# HDSL, MDSL, SDSL ANALOG FRONT END

**Burr-Brown's Analog Front End products greatly reduce the size and cost of a DSL system by providing all of the active analog circuitry needed to connect a digital signal processor to an external compromise hybrid and line transformer. Functionally, these units are separated into a transmit and a receive section. The transmit section generates, filters, and buffers outgoing 2B1Q data. The receive section echo cancels, filters, and digitizes the symbol data received on the telephone line and passes it to the DSP chip.**

| Product | Design Speed | Minimum Speed | Power | Compatibility | Power Supply | Description |
|---|---|---|---|---|---|---|
| AFE1103 | E1/T1 | 192kbps | 250mW | Brooktree | +5V | Second Sourced By Bt8921 |
| AFE1104 | E1/T1 | 192kbps | 250mW | PairGain | +5V | |
| AFE1105 | E1/T1 | 192kbps | 250mW | Metalink | +5V | |
| **AFE1115** | **E1/T1** | **192kbps** | **250mW** | **General** | **+5V** | **Includes VCXO Circuit** |
| **AFE1124** | **E1/T1** | **64kbps** | **250mW** | **General** | **+5V** | **Serial Interface** |

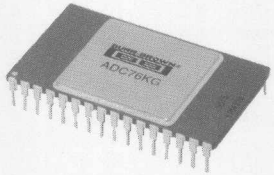


**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

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# ADC76

www.burr-brown.com/databook/ADC76.html

# 16-Bit ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- 16-BIT RESOLUTION
- LINEARITY ERROR: ±0.003% max (KG, BG)
- NO MISSING CODES GUARANTEED FROM –25°C TO +85°C
- 17μs CONVERSION TIME (16-Bit)
- SERIAL AND PARALLEL OUTPUTS

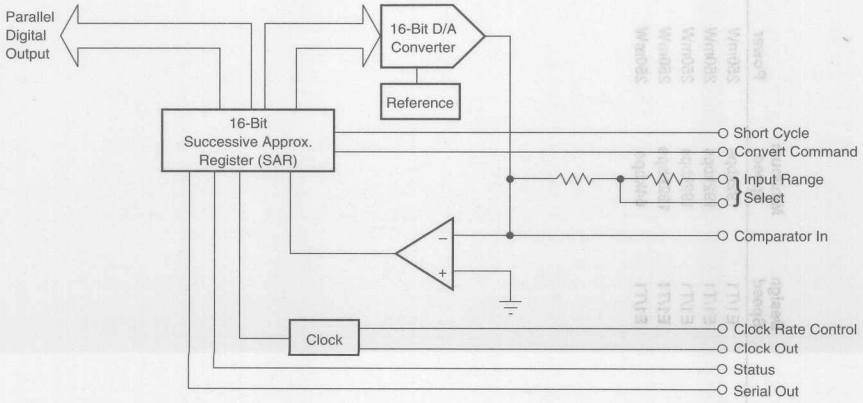
## DESCRIPTION

The ADC76 is a high quality, 16-bit successive approximation analog-to-digital converter. The ADC76 uses state-of-the-art laser-trimmed IC thin-film resistors and is packaged in a hermetic 32-pin dual-in-line package. The converter is complete with internal reference, short cycling capabilities, serial output, and thin-film scaling resistors, which allow selection of analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

It is specified for operation over two temperature ranges: 0°C to +70°C (J, K) and –25°C to +85°C (A, B).

Data is available in parallel and serial form with corresponding clock and status output. All digital inputs and outputs are TTL-compatible.

Power supply voltages are ±15VDC and +5VDC.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

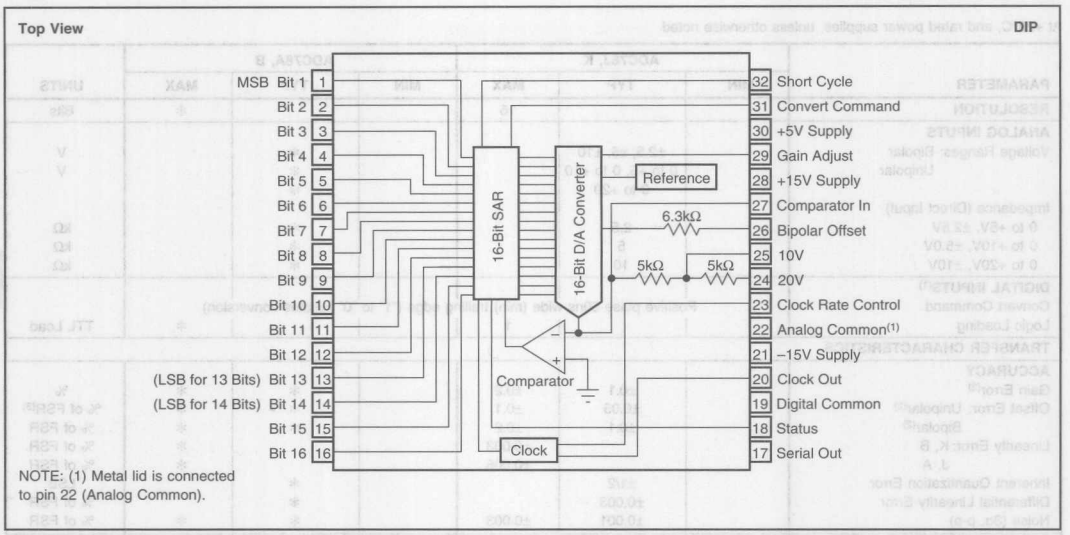
At +25°C, and rated power supplies, unless otherwise noted.

| PARAMETER | ADC76J, K MIN | ADC76J, K TYP | ADC76J, K MAX | ADC76A, B MIN | ADC76A, B TYP | ADC76A, B MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **RESOLUTION** | | | 16 | | | * | Bits |
| **ANALOG INPUTS** | | | | | | | |
| Voltage Ranges: Bipolar | | ±2.5, ±5, ±10 | | | * | | V |
| Unipolar | | 0 to +5, 0 to +10 | | | * | | V |
| | | 0 to +20 | | | * | | |
| Impedance (Direct Input) | | | | | | | |
| 0 to +5V, ±2.5V | | 2.5 | | | * | | kΩ |
| 0 to +10V, ±5.0V | | 5 | | | * | | kΩ |
| 0 to +20V, ±10V | | 10 | | | * | | kΩ |
| **DIGITAL INPUTS**[1] | | | | | | | |
| Convert Command | | Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion) | | | | | |
| Logic Loading | | | 1 | | | * | TTL Load |
| **TRANSFER CHARACTERISTICS** | | | | | | | |
| **ACCURACY** | | | | | | | |
| Gain Error[2] | | ±0.1 | ±0.2 | | * | * | % |
| Offset Error: Unipolar[2] | | ±0.05 | ±0.1 | | * | * | % of FSR[3] |
| Bipolar[2] | | ±0.1 | ±0.2 | | * | * | % of FSR |
| Linearity Error: K, B | | | ±0.003 | | | * | % of FSR |
| J, A | | | ±0.006 | | | * | % of FSR |
| Inherent Quantization Error | | ±1/2 | | | * | | LSB |
| Differential Linearity Error | | ±0.003 | | | * | | % of FSR |
| Noise (3σ, p-p) | | ±0.001 | ±0.003 | | * | * | % of FSR |
| **POWER SUPPLY SENSITIVITY** | | | | | | | |
| ±15VDC | | 0.003 | | | * | | % of FSR/%$V_S$ |
| +5VDC | | 0.001 | | | * | | % of FSR/%$V_S$ |
| **CONVERSION TIME**[4] | | | | | | | |
| 14 Bits | | | 15 | | | * | µs |
| 15 Bits | | | 16 | | | * | µs |
| 16 Bits | | | 17 | | | * | µs |
| **WARM-UP TIME** | 5 | | | * | | | Min |
| **DRIFT** | | | | | | | |
| Gain | | | ±15 | | | * | ppm/°C |
| Offset: Unipolar | | ±2 | ±4 | | * | * | ppm of FSR/°C |
| Bipolar | | | ±10 | | | * | ppm of FSR/°C |
| Linearity | | ±2 | ±3 | | * | * | ppm of FSR/°C |
| No Missing Codes Temp Range | | | | | | | |
| J, A (13-bit) | 0 | | +70 | –25 | | +85 | °C |
| K, B (14-bit) | 0 | | +70 | –25 | | +85 | °C |
| **OUTPUT DIGITAL DATA** | | | | | | | |
| (All codes complementary) | | | | | | | |
| Parallel | | | | | | | |
| Output Codes[5]: Unipolar | | CSB | | | * | | |
| Bipolar | | COB, CTC[6] | | | * | | |
| Output Drive | | | 2 | | | * | TTL Loads |
| Serial Data Code (NRZ) | | CSB, COB | | | * | | |
| Output Drive | | | 2 | | | * | TTL Loads |
| Status | | Logic "1" during conversion | | | * | | |
| Status Output Drive | | | 2 | | | * | TTL Loads |
| Internal Clock: Clock Output Drive | | | 2 | | | * | TTL Loads |
| Frequency[7] | 933 | | 1400 | * | | * | kHz |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | |
| Power Consumption | | 0.655 | | | * | | W |
| Rated Voltage: Analog | ±11.4 | ±15 | ±16 | * | * | * | VDC |
| Digital | +4.75 | +5 | +5.25 | * | * | * | VDC |
| Supply Drain: +15VDC | | +10 | +15 | | * | * | mA |
| –15VDC | | –28 | –35 | | * | * | mA |
| +5VDC | | +17 | +20 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | |
| Specification | 0 | | +70 | –25 | | +85 | °C |
| Storage | –55 | | +125 | * | | * | °C |

*Specification same as ADC76J, K.

NOTES: (1) CMOS/TTL compatible, i.e., Logic "0" = 0.8V, max, Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = 0.4V, max, Logic "1' = 2.4V, min. (2) Adjustable to zero. See "Optional External Gain and Offset Adjustment" section. (3) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (4) Conversion time may be shortened with "Short Cycle" set for lower resolution and with use of Clock Rate Control. See "Optional Conversion Time Adjustment" section. The Clock Rate Control (pin 23) should be connected to Digital Common for specified conversion time. Short Cycle (pin 32) should be left open for 16-bit resolution or connected to the n + 1 digital output for n-bit resolution. For example, connect Short Cycle to Bit 15 (pin 15) for 14-bit resolution. For resolutions less than 16 bits, pin 32 should also be tied to +5V through a 2kΩ resistor. (5) See Table I. CSB = Complementary Straight Binary, COB = Complementary Offset Binary, CTC = Complementary Two's Complement. (6) CTC coding obtained by inverting MSB (pin 1). (7) Adjustable with Clock Rate Control from approximately 933kHz to 1.4MHz.

## PIN CONFIGURATION




NOTE: (1) Metal lid is connected to pin 22 (Analog Common).

## ABSOLUTE MAXIMUM SPECIFICATIONS

| | |
|---|---|
| $+V_{CC}$ to Common | 0V to +16.5V |
| $-V_{CC}$ to Common | 0V to –16.5V |
| $+V_{DD}$ to Common | 0V to +7V |
| Analog Common to Digital Common | ±0.5V |
| Logic Inputs to Common | 0V to $V_{DD}$ |
| Maximum Power Dissipation | 1000mW |
| Lead Temperature (soldering, 10s) | 300°C |

## ORDERING INFORMATION

| PRODUCT | LINEARITY ERROR max (% of FSR) | TEMPERATURE RANGE |
|---|---|---|
| ADC76AG | ±0.006 | –25°C to +85°C |
| ADC76BG | ±0.003 | –25°C to +85°C |
| ADC76JG | ±0.006 | 0°C to +70°C |
| ADC76KG | ±0.003 | 0°C to +70°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ADC76JG | 32-Pin Hermetic DIP | 172-5 |
| ADC76KG | 32-Pin Hermetic DIP | 172-5 |
| ADC76AG | 32-Pin Hermetic DIP | 172-5 |
| ADC76BG | 32-Pin Hermetic DIP | 172-5 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# ADC80

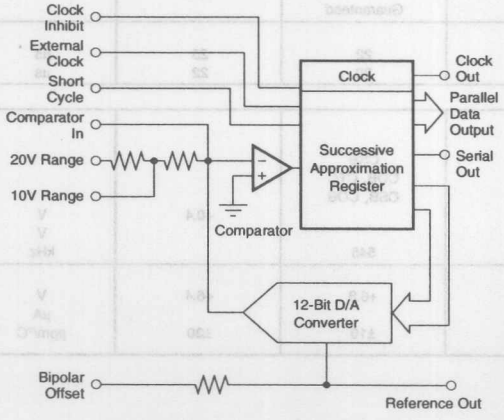
www.burr-brown.com/databook/ADC80.html



# General Purpose ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- INDUSTRY-STANDARD 12-BIT ADC
- ±0.012% LINEARITY
- 25µs max CONVERSION TIME
- ±12V OR ±15V OPERATION
- NO MISSING CODES: –25°C to +85°C
- HERMETIC 32-PIN PACKAGE
- PARALLEL AND SERIAL OUTPUTS
- 595mW max DISSIPATION




## DESCRIPTION

The ADC80 is a 12-bit successive-approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom designed for freedom from latch-up and optimum AC performance. It is complete with a comparator, a monolithic 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, and a CMOS logic chip containing the successive approximation register (SAR), clock, and all other associated logic functions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial endpoint accuracies of better than ±0.12% (±1/2LSB).

The maximum conversion time of 25µs makes the ADC80 ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 40kHz. In addition, the ADC80 may be short-cycled for faster conversion speed with reduced resolution, and an external clock may be used to synchronize the converter to the system clock or to obtain higher speed operation.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC80 operates equally well with either ±15V or ±12V analog power supplies, and also requires use of a +5V logic power supply. However, unlike many ADC-type products, a +5V analog power supply is not required. It is packaged in a hermetic 32-pin side-brazed ceramic dual-in-line package.

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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $\pm V_{CC}$ = 12V or 15V, $V_{DD}$ = +5V, unless otherwise specified.

| PARAMETER | ADC80AG MIN | ADC80AG TYP | ADC80AG MAX | UNITS |
|---|---|---|---|---|
| **RESOLUTION** | | | | |
| ADC80AG-12, ADC80-AGZ-12[1] | | | 12 | Bits |
| ADC80AG-10 | | | 10 | Bits |
| **INPUT** | | | | |
| **ANALOG** | | | | |
| Voltage Ranges: Unipolar | | 0 to +5, 0 to +10 | | V |
| Bipolar | | ±2.5, ±5, ±10 | | V |
| Impedance: 0 to +5V, ±2.5V | 2.45 | 2.5 | 2.55 | kΩ |
| 0 to +10V, +5V | 4.9 | 5 | 5.1 | kΩ |
| ±10V | 9.8 | 10 | 10.2 | kΩ |
| **DIGITAL** | | | | |
| Logic Characteristics (Over specification temperature range) | | | | |
| $V_{IH}$ (Logic "1") | 2 | | 5.5 | V |
| $V_{IL}$ (Logic "0") | –0.3 | | +0.8 | V |
| $I_{IH}$ ($V_{IN}$ = +2.7V) | | | –150 | µA |
| $I_{IL}$ ($V_{IN}$ = +0.4V) | | | 500 | µA |
| Convert Command Pulse Width[2] | 100 | | 2000 | ns |
| **TRANSFER CHARACTERISTICS** | | | | |
| **ACCURACY** | | | | |
| Gain Error[2] | | ±0.1 | ±0.3 | % of FSR[4] |
| Offset Error[3]: Unipolar | | ±0.05 | ±0.2 | % of FSR |
| Bipolar | | ±0.1 | ±0.3 | % of FSR |
| Linearity Error: ADC80AG-12, ADC80AGZ-12 | | | ±0.012 | % of FSR |
| ADC80AG-10 | | | ±0.048 | % of FSR |
| Differential Linearity Error | | ±1/2 | ±3/4 | LSB |
| Inherent Quantization Error | | ±1/2 | | LSB |
| **POWER SUPPLY SENSITIVITY** | | | | |
| 11.4V ≤ $\pm V_{CC}$ ≤ 16.5V | | ±0.003 | ±0.009 | % of FSR/%$V_{CC}$ |
| +4.5V ≤ $V_{DD}$ ≤ +5.5V | | ±0.002 | ±0.005 | % of FSR/%$V_{DD}$ |
| **DRIFT** | | | | |
| Total Accuracy, Bipolar[5] | | ±10 | ±23 | ppm/°C |
| Gain | | ±15 | ±30 | ppm/°C |
| Offset: Unipolar | | ±3 | | ppm of FSR/°C |
| Bipolar | | ±7 | ±15 | ppm of FSR/°C |
| Linearity Error Drift | | ±1 | ±3 | ppm of FSR/°C |
| Differential Linearity over Temperature Range | | | ±3/4 | LSB |
| No Missing Code Temperature Range | –25 | | +85 | °C |
| Monotonicity Over Temperature Range | | Guaranteed | | |
| **CONVERSION TIME[6]** | | | | |
| ADC80AG-12, ADC80-AGZ-12 | 15 | 22 | 25 | µs |
| ADC80AG-10 | 13 | 20 | 22 | µs |
| **OUTPUT** | | | | |
| **DIGITAL** (Bits 1-12 , Clock Out, Status, Serial Out) | | | | |
| Output Codes[7] | | | | |
| Parallel: Unipolar | | CSB | | |
| Bipolar | | COB, CTC | | |
| Serial (NRZ)[8] | | CSB, COB | | |
| Logic Levels: Logic 0 ($I_{SINK}$ ≤ 3.2mA) | | | +0.4 | V |
| Logic 1 ($I_{SOURCE}$ ≤ 80µA) | +2.4 | | | V |
| Internal Clock Frequency | | 545 | | kHz |
| **INTERNAL REFERENCE VOLTAGE** | | | | |
| Voltage | +6.2 | +6.3 | +6.4 | V |
| Source Current Available for External Loads[9] | 200 | | | µA |
| Temperature Coefficient | | ±10 | ±30 | ppm/°C |

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# SPECIFICATIONS (CONT)

## ELECTRICAL

At $T_A$ = +25°C, $\pm V_{CC}$ = 12V or 15V, $V_{DD}$ = +5V, unless otherwise specified.

| PARAMETER | ADC80AG MIN | ADC80AG TYP | ADC80AG MAX | UNITS |
|---|---|---|---|---|
| **POWER SUPPLY REQUIREMENTS** (For all models) | | | | |
| Voltage: $\pm V_{CC}$ | ±11.4 | ±15 | ±16.5 | V |
| $V_{DD}$ | +4.5 | +5 | +5.5 | V |
| Current: $+I_{CC}$ | | 5 | 8.5 | mA |
| $-I_{CC}$ | | 21 | 26 | mA |
| $I_{DD}$ | | 11 | 15 | mA |
| Power Dissipation ($\pm V_{CC}$ = 15V) | | 450 | 595 | mW |
| Thermal Resistance, $\theta_{JA}$ | | 50 | | °C/W |
| **TEMPERATURE RANGE** (Ambient) | | | | |
| Specification | –25 | | +85 | °C |
| Operating (derated specs) | –55 | | +125 | °C |
| Storage | –65 | | +150 | °C |

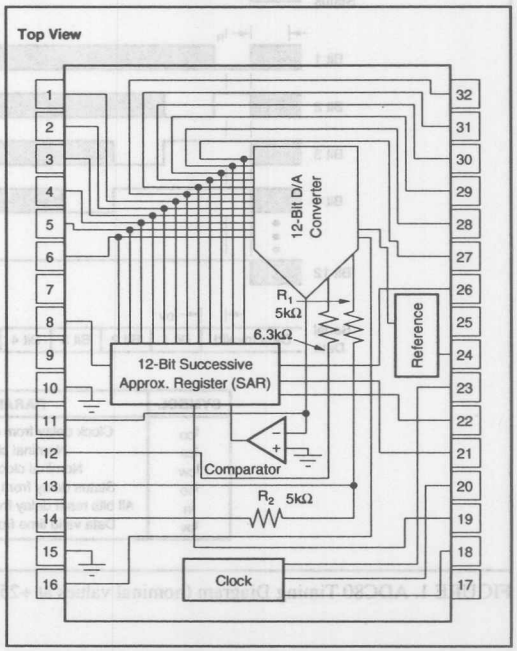
NOTES: (1) ADC80AGZ-12 is not recommended for new designs. Standard ADC80AG-12 now meets the extended power supply range of the ADC80AGZ-12. (2) Accurate conversion will be obtained with any convert command pulse width of greater than 100ns; however, it must be limited to 2µs (max) to assure the specified conversion time. (3) Gain and offset errors are adjustable to zero. See "Optional External Gain and Offset Adjustment" section. (4) FSR means Full-Scale Range and is 20V for ±10V range, 10V for ±5V and 0 to +10V ranges, etc. (5) Includes drift due to linearity, gain, and offset drifts. (6) Conversion time is specified using internal clock. For operation with an external clock see "Clock Options" section. This converter may also be short-cycled to less than 12-bit resolution for shorter conversion time: see "Short Cycle Feature" section. (7) CSB means Complementary Straight Binary, COB means Complementary Offset Binary, and CTC means Complementary Two's Complement coding. See Table 1 for additional information. (8) NRZ means Non-Return-to-Zero coding. (9) External loading must be constant during conversion, and must not exceed 200µA for guaranteed specification.

## PIN ASSIGNMENTS

| PIN | DESCRIPTION | PIN | DESCRIPTION |
|---|---|---|---|
| 1 | Bit 6 | 32 | Bit 7 |
| 2 | Bit 5 | 31 | Bit 8 |
| 3 | Bit 4 | 30 | Bit 9 |
| 4 | Bit 3 | 29 | Bit 10 (LSB-10 Bits) |
| 5 | Bit 2 | 28 | Bit 11 |
| 6 | Bit 1 (MSB) | 27 | Bit 12 (LSB-12 Bits) |
| 7 | NC(1) | 26 | Serial Out |
| 8 | Bit 1 ($\overline{\text{MSB}}$) | 25 | $-V_{CC}$ |
| 9 | +5V Digital Supply | 24 | Reference Out (+6.3V) |
| 10 | Digital Common(2) | 23 | Clock Out |
| 11 | Comparator In | 22 | Status |
| 12 | Bipolar Offset | 21 | Short Cycle |
| 13 | $R_1$ 10V Range | 20 | Clock Inhibit |
| 14 | $R_2$ 20V Range | 19 | External Clock |
| 15 | Analog Common | 18 | Convert Command |
| 16 | Gain Adjust | 17 | $+V_{CC}$ |

NOTE: (1) +5V applied to pin 7 has no effect on circuit. (2) Metal lid of package is connected to pin 10.

## CONNECTION DIAGRAM




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_{CC}$ to Analog Common | 0 to +16.5V |
| $-V_{CC}$ to Analog Common | 0 to –16.5V |
| $V_{DD}$ to Digital Common | 0 to +7V |
| Analog Common to Digital Common | ±0.5V |
| Logic Inputs (Convert Command, Clock In) to Digital Common | –0.3V to $+V_{DD}$ +0.5V |
| Analog Inputs (Analog In, Bipolar Offset) to Analog Common | ±16.5V |
| Reference Output | Indefinite Short to Common, Momentary Short to $V_{CC}$ |
| Lead Temperature, (soldering, 10s) | +300°C |

**CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.**

**Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.**

## ORDERING INFORMATION

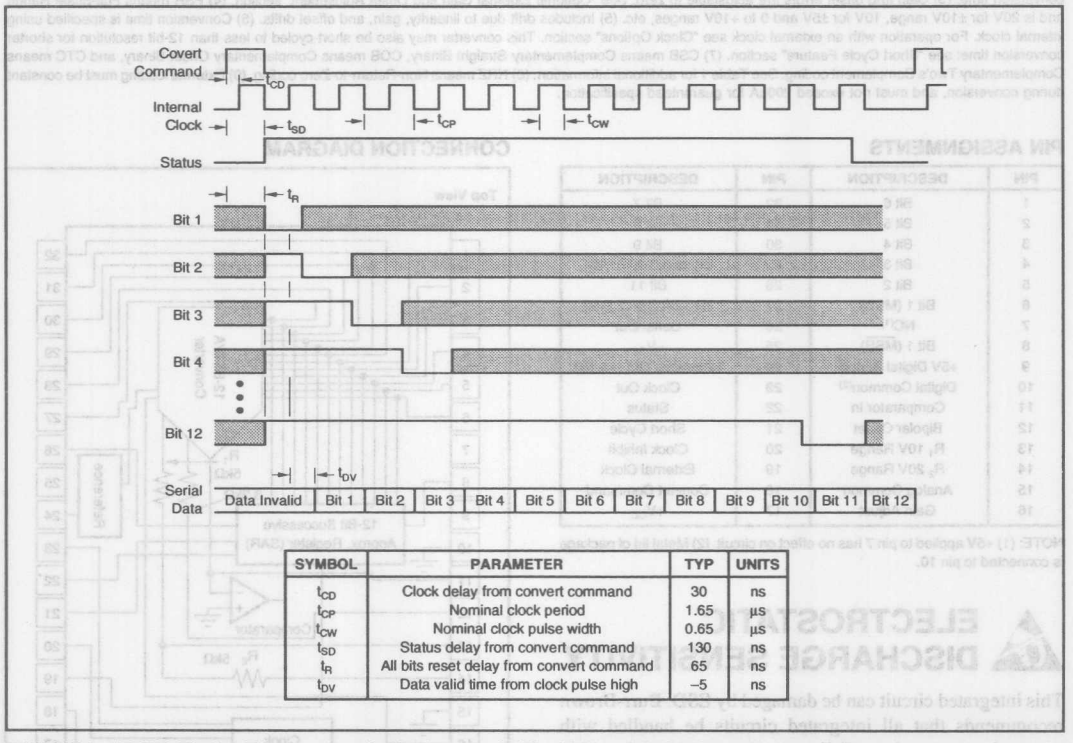
| PRODUCT | RESOLUTION (Bits) |
|---|---|
| ADC80AG-10 | 10 |
| ADC80G-12 | 12 |
| ADC80GZ-12[1] | 12 |

NOTE: (1) ADC80AGZ-12 is not recommended for new designs. Standard ADC80AG-12 now meets the extended power supply range of the ADC80AGZ-12.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| ADC80AG-10 | 32-Pin Hermetic | 172 |
| ADC80G-12 | 32-Pin Hermetic | 172 |
| ADC80AZ-12[1] | 32-Pin Hermetic | 172 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

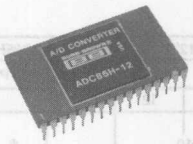



| SYMBOL | PARAMETER | TYP | UNITS |
|---|---|---|---|
| $t_{CD}$ | Clock delay from convert command | 30 | ns |
| $t_{CP}$ | Nominal clock period | 1.65 | µs |
| $t_{CW}$ | Nominal clock pulse width | 0.65 | µs |
| $t_{SD}$ | Status delay from convert command | 130 | ns |
| $t_R$ | All bits reset delay from convert command | 65 | ns |
| $t_{DV}$ | Data valid time from clock pulse high | –5 | ns |

FIGURE 1. ADC80 Timing Diagram (nominal values at +25°C with internal clock).

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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# ADC84
# ADC85H
# ADC87H

www.burr-brown.com/databook/ADC84.html

# IC ANALOG-TO-DIGITAL CONVERTERS

## FEATURES

- INDUSTRY STANDARD 12-BIT A/D CONVERTERS
- COMPLETE WITH CLOCK AND INPUT BUFFER
- HIGH SPEED CONVERSION: 10µs (max)
- REDUCED CHIP COUNT—HIGH RELIABILITY
- LOWER POWER DISSIPATION: 450MW (typ)
- ±0.012% max LINEARITY ERROR
- THREE TEMPERATURE RANGES:
  0°C to +70°C—ADC84
  –25°C to +85°C—ADC85H
  –55°C to +125°C—ADC87H
- NO MISSING CODES OVER FULL TEMPERATURE RANGE
- PARALLEL AND SERIAL OUTPUTS
- ±12V OR ±15V POWER SUPPLY OPERATION
- HERMETIC 32-PIN CERAMIC SIDE-BRAZED DIP

## DESCRIPTION

ADC84, ADC85H, and ADC87H analog-to-digital converters utilize state-of-the-art IC and laser-trimmed thin-film components, and are packaged in a 32-pin hermetic side-brazed package.

They are complete with internal reference and input buffer amplifier. Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, offering initial accuracies of better than ±0.012% (±1/2LSB).

The fast 10µs conversion speed for 12-bit resolution makes these ADCs excellent for a wide range of applications where system throughput sampling rates of 100kHz are required. In addition, they may be short cycled and the clock rate control may be used to obtain faster conversion speeds at lower resolutions.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are CMOS/TTL-compatible. Power supply voltages are ±12VDC or ±15VDC and +5VDC.

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

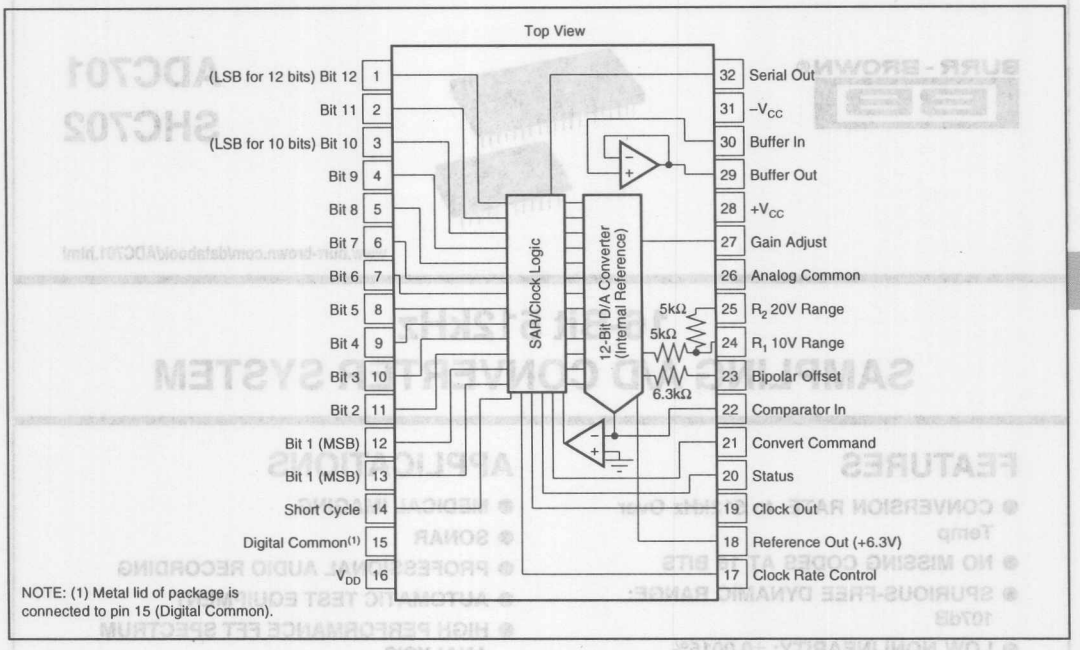
Specified at +25°C and rated supplies, unless otherwise noted.

| PARAMETER | ADC84KG-12[1] MIN | ADC84KG-12[1] TYP | ADC84KG-12[1] MAX | ADC85H-12 MIN | ADC85H-12 TYP | ADC85H-12 MAX | ADC87H-12 MIN | ADC87H-12 TYP | ADC87H-12 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| **RESOLUTION** | | | 12 | | | * | | | * | Bits |
| **ANALOG INPUTS** | | | | | | | | | | |
| Voltage Ranges: Bipolar | | ±2.5, ±5, ±10 | | | * | | | * | | V |
| Unipolar | | 0 to +5, 0 to +10 | | | * | | | * | | V |
| Impedance (Direct Input): 0 to +5V, ±2.5V | 2.45 | 2.5 | 2.55 | * | * | * | * | * | * | kΩ |
| 0 to +10V, ±5V | 4.9 | 5 | 5.1 | * | * | * | * | * | * | kΩ |
| ±10V | 9.8 | 10 | 10.2 | * | * | * | * | * | * | kΩ |
| Buffer Amplifier: Impedance | 100 | | | * | | | * | | | MΩ |
| Bias Current | | 50 | | | * | | | * | | nA |
| Settling Time to 0.01% for 20V Step[2] | | 2 | | | * | | | * | | µs |
| **DIGITAL INPUTS[3]** | | | | | | | | | | |
| Convert Command | | Positive pulse 50ns (min), trailing edge initiates conversion | | | | | | | | |
| Logic Loading | | 1 | | | * | | | * | | TTL Load |
| **TRANSFER CHARACTERISTICS** | | | | | | | | | | |
| **ACCURACY** | | | | | | | | | | |
| Gain Error [4] | | ±0.1 | ±0.25 | | * | * | | * | * | % |
| Offset Error[4]: Unipolar | | ±0.05 | ±0.2 | | * | * | | * | * | % of FSR[5] |
| Bipolar | | ±0.1 | ±0.25 | | * | * | | * | * | % of FSR |
| Linearity Error[6] | | | ±0.012 | | | * | | | * | % of FSR |
| Inherent Quantization Error | | ±0.5 | | | * | | | * | | LSB |
| Differential Linearity Error | | ±0.5 | | | * | | | * | | LSB |
| No Missing Codes Temperature Range | 0 | | +70 | –25 | | +85 | –55 | | +125 | °C |
| **POWER SUPPLY SENSITIVITY** | | | | | | | | | | |
| Gain and Offset: ±15V | | ±0.004 | | | * | | | * | | % of FSR/%$V_S$ |
| +5V | | ±0.001 | | | * | | | * | | % of FSR/%$V_S$ |
| **DRIFT** | | | | | | | | | | |
| Gain | | ±30 | | | | ±15 | | | ±15 | ppm/°C |
| Offset: Unipolar | | ±3 | | | ±3 | | | | ±5 | ppm of FSR/°C |
| Bipolar | | ±15 | | | | ±7 | | | ±10 | ppm of FSR/°C |
| Linearity | | ±3 | | | | ±2 | | | ±2 | ppm of FSR/°C |
| Monotonicity | | Guaranteed | | | * | | | * | | |
| **CONVERSION TIME** | | 10 | | | | * | | | * | µs |
| **DIGITAL OUTPUT[3]** | | | | | | | | | | |
| (All Modes Complementary) | | | | | | | | | | |
| Parallel Output Codes: Unipolar | | CSB | | | * | | | * | | |
| Bipolar | | COB, CTC | | | * | | | * | | |
| Output Drive | | 2 | | | * | | | * | | TTL Loads |
| Serial Data Codes (NRZ) | | CSB, COB | | | * | | | * | | |
| Output Drive | | 2 | | | * | | | * | | TTL Loads |
| Status | | Logic "1" During Conversion | | | * | | | * | | |
| Output Drive | | 2 | | | * | | | * | | TTL Loads |
| Internal Clock: Output Drive | | 2 | | | * | | | * | | TTL Loads |
| Frequency[7] | | 1.35 | | | * | | | * | | MHz |
| **INTERNAL REFERENCE VOLTAGE** | | | | | | | | | | |
| Reference Output | +6.2 | +6.3 | +6.4 | * | * | * | * | * | * | V |
| Max. External Current with No Degradation | | | 200 | | | * | | | * | µA |
| Tempco of Drift | | | ±20 | | ±5 | ±10 | | ±5 | ±10 | ppm/°C |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | | | |
| Rated Supply Voltages | | +5, ±12 or ±15 | | | * | | | * | | V |
| Supply Ranges: $V_{DD}$ | +4.75 | | +5.25 | * | | * | * | | * | V |
| $\pm V_{CC}$ | ±11.4 | | ±16.5 | * | | * | * | | * | V |
| Supply Drain: $+I_{CC}$ | | | 20 | | | * | | | * | mA |
| $-I_{CC}$ | | | 25 | | | * | | | * | mA |
| $I_{DD}$ | | | 10 | | | * | | | * | mA |
| Total Power Dissipation | | 450 | 725 | | * | * | | * | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | | | |
| Specification | 0 | | +70 | –25 | | +85 | –55 | | +125 | °C |
| Operating (with Derated Specs) | –25 | | +85 | –55 | | +125 | | | | °C |
| Storage | –65 | | +150 | * | | * | * | | * | °C |

* Specification is the same as ADC84KG-12.

NOTES: (1) Model ADC84KG-10 is the same as model ADC84KG-12 except for the following: (a) Resolution: 10 bits (max), (b) Linearity Error: ±0.048% of FSR (max), (c) Conversion Time: 6µs (max), (d) Internal Clock Frequency: 1.9MHz (typ). (2) If the buffer is used, delay Convert Command until amplifier settles. (3) DTL/TTL compatible. For digital inputs Logic "0" = 0.8V (max) and Logic "1" = 2.0V (min). For digital outputs Logic "0" = 0.4V (max) and Logic "1" = 2.4V (min). (4) Adjustable to zero. (5) FSR means Full Scale Range. (6) The error shown is the same as ±1/2LSB max linearity error in % of FSR. (7) Internal clock is externally adjustable.

## CONNECTION DIAGRAM — ADC84, 85H, 87H




NOTE: (1) Metal lid of package is connected to pin 15 (Digital Common).

## ORDERING INFORMATION

| PRODUCT | RESOLUTION (Bits) | TEMPERATURE RANGE |
|---|---|---|
| ADC84KG-10 | 10 | 0°C to +70°C |
| ADC84KG-12 | 12 | 0°C to +70°C |
| ADC85H-12 | 12 | –25°C to +85°C |
| ADC87H-12 | 12 | –55°C to +125°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ADC84KG-10 | Case Ceramic DIP | 172-5 |
| ADC84KG-12 | Case Ceramic DIP | 172-5 |
| ADC85H-12 | 32-Pin Side-brazed | 172-5 |
| ADC87H-12 | 32-Pin Side-brazed | 172-5 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

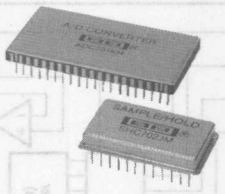
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# ADC701
# SHC702

www.burr-brown.com/databook/ADC701.html

# 16-Bit 512kHz SAMPLING A/D CONVERTER SYSTEM

## FEATURES

- CONVERSION RATE: to 512kHz Over Temp
- NO MISSING CODES AT 16 BITS
- SPURIOUS-FREE DYNAMIC RANGE: 107dB
- LOW NONLINEARITY: ±0.0015%
- SELECTABLE INPUT RANGES: ±5V, ±10V, 0 to +10V, 0 to +5V, –10V to 0
- LOW POWER DISSIPATION: 2.8W Typical Including Sample/Hold
- METAL AND CERAMIC DIP PACKAGES

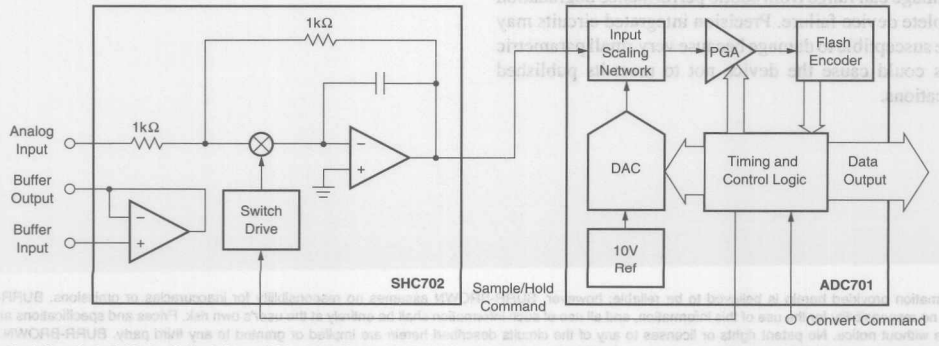
## APPLICATIONS

- MEDICAL IMAGING
- SONAR
- PROFESSIONAL AUDIO RECORDING
- AUTOMATIC TEST EQUIPMENT
- HIGH PERFORMANCE FFT SPECTRUM ANALYSIS
- ULTRASOUND SIGNAL PROCESSING
- HIGH SPEED DATA ACQUISITION
- REPLACES DISCRETE MODULAR ADCs

## DESCRIPTION

The ADC701 is a very high speed 16-bit analog-to-digital converter based on a three-step subranging architecture. Outstanding dynamic performance is achieved with the SHC702 companion sample/hold amplifier. Both devices use hybrid construction for applications where reliability, small size, and low power consumption are especially important.

Excellent linearity and stability are assured through use of a new ultra-precise monolithic D/A converter and a low-drift reference circuit. Custom monolithic op amps provide very high bandwidth and low noise in all sections of the analog signal path. Logic is CMOS/TTL compatible and is designed for maximum flexibility.




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# SPECIFICATIONS

## ELECTRICAL (ADC701 ONLY)

At $T_A$ = +25°C, 500kHz sampling rate, $\pm V_{CC}$ = ±15V, $\pm V_{DD1}$ = ±5V, $+V_{DD2}$ = +5V, and five-minute warmup in a convection environment, unless otherwise noted.

| PARAMETER | CONDITIONS | ADC701JH MIN | ADC701JH TYP | ADC701JH MAX | ADC701KH MIN | ADC701KH TYP | ADC701KH MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **RESOLUTION** | | | | 16 | | | * | Bits |
| **INPUTS** | | | | | | | | |
| **ANALOG** | | | | | | | | |
| Voltage Ranges | Unipolar | | 0 to +5, 0 to +10, −10 to 0 | | | | | V |
| | Bipolar | | ±5, ±10 | | | | | V |
| Resistance | 0 to +5V Range | 2.45 | 2.5 | 2.55 | * | * | * | kΩ |
| | 0 to +10V, −10 to 0, ±5V Ranges | 4.9 | 5 | 5.1 | * | * | * | kΩ |
| | ±10V Range | 9.8 | 10 | 10.2 | * | * | * | kΩ |
| Capacitance | All Ranges | | 5 | | | * | | pF |
| **DIGITAL** | | | | | | | | |
| Logic Family | | | TTL-Compatible CMOS | | | | | |
| Convert Command | Start Conversion | | Rising Edge | | | | | |
| Pulse Width | t = Conversion Period | 50 | | t − 50 | * | | * | ns |
| **TRANSFER CHARACTERISTICS** | | | | | | | | |
| **ACCURACY** | | | | | | | | |
| Gain Error[1] | 0 to +10V Range | | ±0.03 | ±0.1 | | * | * | % |
| | ±10V Range | | ±0.03 | ±0.1 | | * | * | % |
| Power Supply Sensitivity of Gain | All Ranges, All Supplies | | ±0.005 | ±0.1 | | * | * | %/V |
| Input Offset Error[1] | 0 to +10V Range | | ±1 | ±3 | | * | * | mV |
| | ±10V Range | | ±5 | ±10 | | * | * | mV |
| Power Supply Sensitivity of Offset | All Ranges, All Supplies | | ±0.006 | ±0.1 | | * | * | %FSR/V |
| Integral Linearity Error[2] | | | ±0.002 | ±0.003 | | ±0.0012 | * | %FSR[3] |
| Differential Linearity Error[2] | | | ±0.0006 | ±0.0012 | | * | * | %FSR |
| No Missing Codes | | | Guaranteed | | | Guaranteed | | |
| Noise | $R_{SOURCE} \leq 50\Omega$ | | 0.6 | | | * | | LSB rms |
| **CONVERSION CHARACTERISTICS** | | | | | | | | |
| Sample Rate | Unadjusted | DC | | 512 | * | | * | kHz |
| Conversion Time[4] | Unadjusted | | 1.45 | 1.5 | | * | * | µs |
| **OUTPUTS** | | | | | | | | |
| **DIGITAL** | | | | | | | | |
| Logic Family | | | TTL-Compatible CMOS | | | | | |
| Data Coding | Unipolar Ranges | | Straight Binary | | | | | |
| | Bipolar Ranges | | Offset Binary | | | | | |
| Logic "0" Levels ($V_{OL}$) | $I_{OL} \leq 3.2mA$ | | 0.1 | 0.4 | | * | * | V |
| Logic "1" Levels ($V_{OH}$) | $I_{OH} \leq 80\mu A$ | 4 | 4.9 | | * | * | | V |
| Data Valid Setup Time Before Strobe | Both Edges | 28 | 37 | | * | * | | ns |
| **INTERNAL REFERENCE** | | | | | | | | |
| Voltage | $R_{LOAD} \geq 5k\Omega$ | +9.995 | +10.000 | +10.005 | * | * | * | V |
| Current Available to External Loads | | 2 | 5 | | * | * | | mA |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | |
| Supply Voltages: $+V_{CC}$ | Operating | +14.25 | +15 | +15.75 | * | * | * | V |
| $-V_{CC}$ | | −14.25 | −15 | −15.75 | * | * | * | V |
| $+V_{DD1}$ | | +4.75 | +5 | +5.25 | * | * | * | V |
| $-V_{DD1}$ | | −4.25 | −5 | −6 | * | * | * | V |
| $+V_{DD2}$ | | +4.25 | +5 | +5.25 | * | * | * | V |
| Supply Currents: $+I_{CC}$ | Operating | | 25 | 30 | | * | * | mA |
| $-I_{CC}$ | | | 33 | 45 | | * | * | mA |
| $+I_{DD1}$ | | | 45 | 55 | | * | * | mA |
| $-I_{DD1}$ | | | 37 | 50 | | * | * | mA |
| $+I_{DD2}$ | | | 133 | 150 | | * | * | mA |
| Power Dissipation | Nominal Voltages | | 1.95 | 2.3 | | * | * | W |
| **PERFORMANCE OVER TEMPERATURE** | | | | | | | | |
| Specification Temperature Range | $T_A$ Min to $T_A$ Max | +15 | | +55 | 0 | | +70 | °C |
| Gain Error | All Ranges | | ±10 | ±15 | | * | * | ppm/°C |
| Input Offset Error | All Unipolar Ranges | | ±1 | ±5 | | * | * | ppm FSR/°C |
| | All Bipolar Ranges | | ±1 | ±5 | | * | * | ppm FSR/°C |
| Integral Linearity Error[2] | | | ±0.2 | | | * | ±0.5 | ppm/°C |
| Differential Linearity Error[2] | | | ±0.05 | | | * | ±0.3 | ppm/°C |
| No Missing Codes | | | Typical | | | Guaranteed | | |
| Reference Output Drift | | | ±3 | | | * | | ppm/°C |
| Drift of Conversion Time | Unadjusted | | +3 | +4 | | * | * | ns/°C |
| Sample Rate | Unadjusted | DC | | 512 | * | | * | kHz |

* Same specifications as ADC701JH.

## ELECTRICAL (SHC702 ONLY)

At $T_A$ = +25°C, 500kHz sampling rate, $\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, and five-minute warmup in a convection environment, unless otherwise noted.

| PARAMETER | CONDITIONS | SHC702JM MIN | SHC702JM TYP | SHC702JM MAX | UNITS |
|---|---|---|---|---|---|
| **INPUTS** (Without Input Buffer) | | | | | |
| **ANALOG** | | | | | |
| Voltage Range | | ±10.25 | ±11 | | V |
| Resistance | | 0.98 | 1 | 1.02 | kΩ |
| Capacitance | | | 3 | | pF |
| **DIGITAL** | | | | | |
| Logic Family | | | LSTTL | | |
| Input Loading | | | 2 | | LSTTL Loads |
| **TRANSFER CHARACTERISTICS** | | | | | |
| **ACCURACY** | | | | | |
| Gain | $R_{SOURCE}$ = 0Ω | | −1 | | V/V |
| Gain Error | $R_{SOURCE}$ = 0Ω | | ±0.02 | ±0.1 | % |
| Linearity Error | Sample Mode | | ±0.0003 | | %FSR |
| Offset Error | Sample Mode | | ±0.5 | ±3 | mV |
| Charge Offset (Pedestal) Error | Sample/Hold Mode, $R_{SOURCE} \leq 50\Omega$ | | ±0.5 | ±5 | mV |
| Droop Rate | Hold Mode | | ±0.2 | ±2 | µV/µs |
| Dynamic Nonlinearity | Sample/Hold Mode | | ±0.0005 | | %FSR |
| Power Supply Sensitivity | Offset Plus Charge Offset, All Supplies | | ±0.003 | | %FSR/V |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Acquisition Time | 10V Step to ±150µV | | 600 | | ns |
| | 5V Step to ±150µV | | 500 | | ns |
| Sample-to-Hold Settling Time[5] | to ±150µV | | 120 | | ns |
| Aperture Delay Time | | | 20 | | ns |
| Aperture Uncertainty (Jitter) | | | 10 | 25 | ps rms |
| Slew Rate | | | 150 | | V/µs |
| Small Signal Bandwidth | $V_{IN}$ = ±1V | | 3.1 | | MHz |
| Full-Power Bandwidth | $V_{IN}$ = ±10V | | 2 | | MHz |
| Feedthrough Rejection | Hold Mode, 10Vp-p Square Wave Input | | 0.001 | | % |
| **OUTPUT** | | | | | |
| Voltage Range | $R_{LOAD} \geq 1k\Omega$ | ±10.25 | ±11 | | V |
| Output Current | | ±40 | | | mA |
| Short Circuit Protection | $R_{LOAD}$ = 0Ω | | Indefinite | | |
| Output Impedance | DC | | 0.01 | 0.1 | Ω |
| **INPUT BUFFER CHARACTERISTICS** | | | | | |
| **INPUT** | | | | | |
| Impedance | | | $10^{13}$ \|\| 3 | | Ω \|\| pF |
| Bias Current | $V_{IN}$ = ±10V | | ±2 | ±15 | pA |
| Offset Voltage | $R_{SOURCE} \leq 10k\Omega$ | | ±0.3 | ±1.5 | mV |
| Voltage Range | | ±10.25 | ±11 | | V |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Slew Rate | | 20 | 35 | | V/µs |
| Full-Power Bandwidth | $V_{IN}$ = ±10V | | 570 | | kHz |
| Settling Time | 10V Step to ±150µV | | 1.7 | | µs |
| **OUTPUT** | | | | | |
| Output Current | | ±15 | ±20 | | mA |
| Short Circuit Protection | $R_{LOAD}$ = 0Ω | | Indefinite | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage: $+V_{CC}$ | Operating | +13.5 | +15 | +16.5 | V |
| $-V_{CC}$ | | −13.5 | −15 | −16.5 | V |
| $+V_{DD1}$ | | +4.75 | +5 | +5.25 | V |
| Current: $+I_{CC}$ | Operating | | 33 | 40 | mA |
| $-I_{CC}$ | | | 18 | 25 | mA |
| $+I_{DD1}$ | | | 5 | 10 | mA |
| Power Dissipation | Nominal Voltages | | 790 | 950 | mW |
| **PERFORMANCE OVER TEMPERATURE** | | | | | |
| Specification Temperature Range | $T_A$ Min to $T_A$ Max | 0 | | +70 | °C |
| Sample/Hold Gain Error | $R_{SOURCE}$ = 0Ω | | ±1 | ±5 | ppm/°C |
| Sample/Hold Offset Error | $R_{SOURCE} \leq 50\Omega$ | | ±10 | ±30 | µV/°C |
| Sample/Hold Charge Offset Error | $R_{SOURCE} \leq 50\Omega$ | | ±10 | ±80 | µV/°C |
| Droop Rate | | | | ±50 | µV/µs |
| Buffer Offset Error | $R_{SOURCE} \leq 10k\Omega$ | | ±3 | ±15 | µV/°C |

NOTES: (1) Adjustable to zero. Tested and guaranteed for 0 to +10V and ±10V ranges only. (2) Peak-to-peak based on 99.9% of all codes. (3) FSR means full-scale range and depends on the input range selected. (4) ADC conversion time is defined as the time that the Sample/Hold must remain in the Hold mode; i.e., the duration of the Sample/Hold command. This time must be added to the Sample/Hold acquisition time to obtain the total system throughput time. (5) Given for reference only — this time overlaps with the ADC701 conversion time and does not affect system throughput rate.

# SPECIFICATIONS

## ELECTRICAL (COMBINED ADC701/SHC702)

At $T_A$ = +25°C, 500kHz sampling rate, $\pm V_{CC}$ = ±15V, $\pm V_{DD1}$ = ±5V, $+V_{DD2}$ = +5V, and five-minute warmup in a convection environment, ±5V input range, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Sample Rate | Unadjusted | DC | | 512 | kHz |
| Dynamic Nonlinearity | | | ±0.002 | | %FSR |
| Total Harmonic Distortion (THD) | $f_{IN}$ = 20kHz (–0.3dB) | | –103 | | dB |
| | $f_{IN}$ = 199kHz (–0.2dB) | | –82 | | dB |
| Spurious-Free Dynamic Range (SFDR) | $f_{IN}$ = 20kHz (–0.3dB) | | 107 | | dB |
| | $f_{IN}$ = 199kHz (–12dB) | | 94 | | dB |
| Two-Tone Intermodulation Distortion (IMD) | $f_1$ = 195kHz (–6.5dB), $f_2$ = 200kHz (–6.5dB) | | –81 | | dBC |
| | $f_1$ = 195kHz (–12.5dB), $f_2$ = 200kHz (–12.5dB) | | –86 | | dBC |
| Signal-to-Noise Ratio (SNR) | $f_{IN}$ = 5kHz (–0.5dB) | | 93 | | dB |
| Total Power Dissipation | Operating | | 2.8 | 3.25 | W |

## ADC701 PIN ASSIGNMENTS

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---|---|---|---|
| 1 | Bit 1/9 (Bit 1 = MSB) | 40 | $-V_{DD1}$ (–5V) Analog |
| 2 | Bit 2/10 | 39 | Common (Analog) |
| 3 | Bit 3/11 | 38 | $+V_{DD1}$ (+5V) Analog |
| 4 | Bit 4/12 | 37 | Reference (Gain) Adjust |
| 5 | Bit 5/13 | 36 | +10V Reference Output(2) |
| 6 | Bit 6/14 | 35 | Common (Reference) |
| 7 | Bit 7/15 | 34 | DNC |
| 8 | Bit 8/16 | 33 | Common (Analog) |
| 9 | Clip Detect Output | 32 | +10V Reference Input(2) |
| 10 | $+V_{DD2}$ (+5V) Digital | 31 | Input D (1) |
| 11 | Common (Digital) | 30 | Input C (1) |
| 12 | Data Strobe | 29 | Common (Signal) |
| 13 | High/Low Byte Select | 28 | Input B (1) |
| 14 | Convert Command | 27 | Input A (1) |
| 15 | Sample/Hold Control(3) | 26 | $-V_{CC}$ (–15V) Analog |
| 16 | Common (Digital) | 25 | Common (Power) |
| 17 | Common (Digital) | 24 | $+V_{CC}$ (+15V) Analog |
| 18 | Clock Adjust | 23 | DNC(4) |
| 19 | Common (Digital) | 22 | Offset Adjust |
| 20 | $+V_{DD2}$ (+5V) Digital | 21 | Offset Adjust |

NOTES: (1) Refer to Input Connection Table. (2) Reference Input is normally connected to Reference Output, unless an external 10V reference is used. (3) Sample/Hold Control goes high to activate Hold mode. (4) DNC = Do Not Connect.

## PACKAGING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ADC701JH | Ceramic | 230 |
| ADC701KH | Ceramic | 230 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ADC701 ORDERING INFORMATION

ADC701 ( ) H

Basic Model Number

Performance Grade Code
- K: 0°C to +70°C Ambient Temperature
- J: +15°C to +55°C Ambient Temperature

Package Code
- H: Metal and Ceramic

## ADC701 ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $\pm V_{CC}$ | ±18V |
| $\pm V_{DD1}$, $+V_{DD2}$ | ±7V, +7V |
| Analog Input | $\pm V_{CC}$ |
| Logic Input | –0.5V to ($+V_{DD2}$ + 0.3V) |
| Logic Output | ±25mA |
| Case Temperature | +150°C |
| Junction Temperature | +165°C |
| Storage Temperature | –65°C to +165°C |
| Power Dissipation | 3W |

Stresses above these ratings may permanently damage the device.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ADC701 OUTPUT CODING

| INPUT LEVEL (Exact Center of Code) | NOMINAL INPUT VOLTAGE TO ADC701 (Multiply by –1 for SHC702 Input Voltage) 0–10V RANGE (1LSB ≈153µV) | ±10V RANGE (1LSB ≈05µV | ±5V RANGE (1LSB ≈153µV) | OUTPUT CODE (1 = Logic High) MSB LSB | CLIP DETECT |
|---|---|---|---|---|---|
| Underrange | < –76µV | < –10.000153V | < –5.000076V | 0000 0000 0000 0000 | 1 |
| –FS | 0V | –10V | –5V | 0000 0000 0000 0000 | 0 |
| –FS + 1LSB | +153µV | –9.999695V | –4.999847V | 0000 0000 0000 0001 | 0 |
| –3/4FS | +1.25V | –7.5V | –3.75V | 0010 0000 0000 0000 | 0 |
| –1/2FS | +2.5V | –5V | –2.5V | 0100 0000 0000 0000 | 0 |
| –1/4FS | +3.75V | –2.5V | –1.25V | 0110 0000 0000 0000 | 0 |
| –1LSB | +4.999847V | –305µV | –153µV | 0111 1111 1111 1111 | 0 |
| Mid-Scale | +5V | 0V | 0V | 1000 0000 0000 0000 | 0 |
| +1LSB | +5.000153V | +305µV | +153µV | 1000 0000 0000 0001 | 0 |
| +1/4FS | +6.25V | +2.5V | +1.25V | 1010 0000 0000 0000 | 0 |
| +1/2FS | +7.5V | +5V | +2.5V | 1100 0000 0000 0000 | 0 |
| +3/4FS | +8.75V | +7.5V | +3.75V | 1110 0000 0000 0000 | 0 |
| +FS –2LSB | +9.999695V | +9.99939V | +4.999695V | 1111 1111 1111 1110 | 0 |
| +FS – 1LSB | +9.999847V | +9.999695V | +4.999847V | 1111 1111 1111 1111 | 0 |
| Overrange | > +9.999924V | > +9.999847V | > +4.999924V | 1111 1111 1111 1111 | 1 |

## SHC702 PIN ASSIGNMENTS

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---|---|---|---|
| 1 | Sample/Hold Output | 24 | $+V_{CC}$ (+15V) Analog |
| 2 | NC(3) | 23 | Common (Power) |
| 3 | NC | 22 | $-V_{CC}$ (–15V) Analog |
| 4 | NC | 21 | Common (Analog) |
| 5 | NC | 20 | NC |
| 6 | NC | 19 | NC |
| 7 | NC | 18 | NC |
| 8 | NC | 17 | Buffer Amp Input(2) |
| 9 | $+V_{DD1}$ (+5V) Analog | 16 | NC |
| 10 | Common (Digital) | 15 | Common (Signal) |
| 11 | $\overline{\text{Hold}}$ Input(1) | 14 | Buffer Amp Output |
| 12 | Hold Input(1) | 13 | Analog Input |

NOTES: (1) Hold mode is activated only when pin 12 is low and pin 11 is high. For normal use with ADC701, pin 12 is grounded and pin 11 is connected to ADC701 Sample/Hold control (ADC701 pin 15). (2) If the buffer amp is not used, pin 17 should be grounded. (3) NC = No Internal Connection.

## PACKAGING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| SHC702JM | 24-Pin | 037 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## SHC702 ORDERING INFORMATION

SHC702 J M

Basic Model Number
Performance Grade Code
J: 0°C to +70°C Ambient Temperature
Package Code
M: Metal

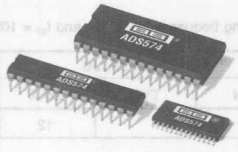
## SHC702 ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $\pm V_{cc}$ | ±18V |
| $+V_{DD1}$ | +7V |
| Analog and Buffer Inputs | $\pm V_{CC}$ |
| Outputs | Indefinite Short to Common |
| Logic Inputs | –0.5V to ($+V_{DD1}$ + 0.3V) |
| Case Temperature | +150°C |
| Junction Temperature | +165°C |
| Storage Temperature | –65°C to +165°C |
| Power Dissipation | 1.5W |

Stresses above these ratings may permanently damage the device.

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BURR-BROWN®



# ADS574

www.burr-brown.com/databook/ADS574.html



# Microprocessor-Compatible Sampling CMOS ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- REPLACES ADC574 FOR NEW DESIGNS
- COMPLETE SAMPLING A/D WITH REFERENCE, CLOCK AND MICROPROCESSOR INTERFACE
- FAST ACQUISITION AND CONVERSION: 25µs max
- ELIMINATES EXTERNAL SAMPLE/HOLD IN MOST APPLICATIONS
- GUARANTEED AC AND DC PERFORMANCE
- SINGLE +5V SUPPLY OPERATION
- LOW POWER: 100mW max
- PACKAGE OPTIONS: 0.6" and 0.3" DIPs, SOIC

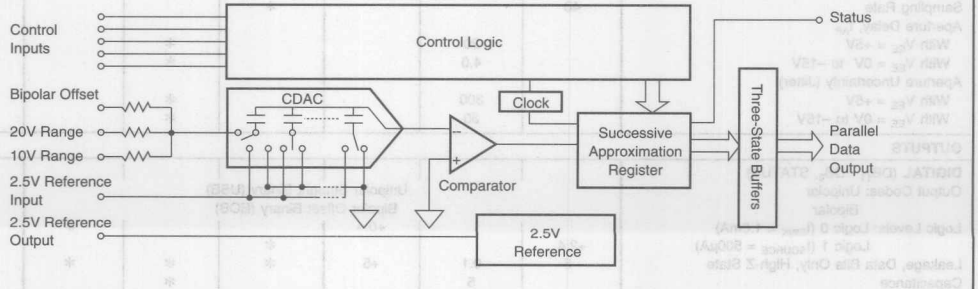
## DESCRIPTION

The ADS574 is a 12-bit successive approximation analog-to-digital converter using an innovative capacitor array (CDAC) implemented in low-power CMOS technology. This is a drop-in replacement for ADC574 models in most applications, with internal sampling, much lower power consumption, and capability to operate from a single +5V supply.

The ADS574 is complete with internal clock, microprocessor interface, three-state outputs, and internal scaling resistors for input ranges of 0V to +10V, 0V to +20V, ±5V, or ±10V. The maximum throughput time for 12-bit conversions is 25µs over the full operating temperature range, including both acquisition and conversion.

Complete user control over the internal sampling function facilitates elimination of external sample/hold amplifiers in most existing designs.

The ADS574 requires +5V, with –12V or –15V optional, depending on usage. No +15V supply is required. Available packages include 0.3" or 0.6" wide 28-pin plastic DIPs and 28-lead SOICs.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

## ELECTRICAL

At $T_A = T_{MIN}$ to $T_{MAX}$, $V_{DD}$ = +5V, $V_{EE}$ = –15V to +5V, sampling frequency of 40kHz, and $f_{IN}$ = 10kHz, unless otherwise specified.

| | ADS574JE, JP, JU | | | ADS574KE, KP, KU | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **RESOLUTION** | | | 12 | | | * | Bits |
| **INPUTS** | | | | | | | |
| **ANALOG** | | | | | | | |
| Voltage Ranges: Unipolar | | | 0 to +10, 0 to +20 | | | | V |
| Bipolar | | | ±5, ±10 | | | | V |
| Impedance: 0 to +10V, ±5V | 15 | 21 | | * | * | | kΩ |
| ±10V, 0V to +20V | 60 | 84 | | * | * | | kΩ |
| **DIGITAL** (CE, $\overline{CS}$, R/$\overline{C}$, $A_0$, 12/$\overline{8}$) | | | | | | | |
| Voltages: Logic 1 | +2.0 | | +5.5 | * | | * | V |
| Logic 0 | –0.5 | | +0.8 | * | | * | V |
| Current | –5 | 0.1 | +5 | * | * | * | µA |
| Capacitance | | 5 | | | * | | pF |
| **TRANSFER CHARACTERISTICS** | | | | | | | |
| **DC ACCURACY** | | | | | | | |
| At +25°C | | | | | | | |
| Linearity Error | | | ±1 | | | ±1/2 | LSB |
| Unipolar Offset Error (adjustable to zero) | | | ±2 | | | * | LSB |
| Bipolar Offset Error (adjustable to zero) | | | ±10 | | | ±4 | LSB |
| Full-Scale Calibration Error [1] (adjustable to zero) | | | ±0.25 | | | * | % of FS [2] |
| No Missing Codes Resolution (Diff. Linearity) | 12 | | | 12 | | | Bits |
| $T_{MIN}$ to $T_{MAX}$ [3] | | | | | | | |
| Linearity Error | | | ±1 | | | ±1/2 | LSB |
| Full-Scale Calibration Error | | | ±0.47 | | | ±0.37 | % of FS |
| Unipolar Offset | | | ±4 | | | ±3 | LSB |
| Bipolar Offset | | | ±12 | | | ±5 | LSB |
| No Missing Codes Resolution | 12 | | | 12 | | | Bits |
| **AC ACCURACY** [4] | | | | | | | |
| Spurious Free Dynamic Range | 73 | 78 | | 76 | * | | dB |
| Total Harmonic Distortion | | –77 | –72 | | * | –75 | dB |
| Signal-to-Noise Ratio | 69 | 72 | | 71 | * | | dB |
| Signal-to-(Noise + Distortion) Ratio | 68 | 71 | | 70 | * | | dB |
| Intermodulation Distortion ($F_{IN1}$ = 10kHz, $F_{IN2}$ = 11.5kHz) | | –75 | | | * | | |
| **TEMPERATURE COEFFICIENTS** [5] | | | | | | | |
| Unipolar Offset | | ±1 | | | * | | ppm/°C |
| Bipolar Offset | | ±2 | | | * | | ppm/°C |
| Full-Scale Calibration | | ±12 | | | * | | ppm/°C |
| **POWER SUPPLY SENSITIVITY** | | | | | | | |
| Change in Full-Scale Calibration[6] | | | | | | | |
| +4.75V < $V_{DD}$ < +5.25V | | | ±1/2 | | | * | LSB |
| **CONVERSION TIME** (Including Acquisition Time) | | | | | | | |
| $t_{AQ}$ + $t_C$ at 25°C: | | | | | | | |
| 8-Bit Cycle | | 16 | 18 | | * | * | µs |
| 12-Bit Cycle | | 22 | 25 | | * | * | µs |
| 12-Bit Cycle, $T_{MIN}$ to $T_{MAX}$ | | 22 | 25 | | * | * | µs |
| **SAMPLING DYNAMICS** | | | | | | | |
| Sampling Rate | 40 | | | * | | | kHz |
| Aperture Delay, $t_{AP}$ | | | | | | | |
| With $V_{EE}$ = +5V | | 20 | | | * | | ns |
| With $V_{EE}$ = 0V to –15V | | 4.0 | | | * | | µs |
| Aperture Uncertainty (Jitter) | | | | | | | |
| With $V_{EE}$ = +5V | | 300 | | | * | | ps, rms |
| With $V_{EE}$ = 0V to –15V | | 30 | | | * | | ns, rms |
| **OUTPUTS** | | | | | | | |
| **DIGITAL** ($DB_{11}$ - $DB_0$, STATUS) | | | | | | | |
| Output Codes: Unipolar | | | Unipolar Straight Binary (USB) | | | | |
| Bipolar | | | Bipolar Offset Binary (BOB) | | | | |
| Logic Levels: Logic 0 ($I_{SINK}$ = 1.6mA) | | | +0.4 | | | * | V |
| Logic 1 ($I_{SOURCE}$ = 500µA) | +2.4 | | | * | | | V |
| Leakage, Data Bits Only, High-Z State | –5 | 0.1 | +5 | * | * | * | µA |
| Capacitance | | 5 | | | * | | pF |

# SPECIFICATIONS (CONT)

## ELECTRICAL

At $T_A = T_{MIN}$ to $T_{MAX}$, $V_{DD}$ = +5V, $V_{EE}$ = –15V to +5V, sampling frequency of 40kHz, and $f_{IN}$ = 10kHz, unless otherwise specified.

| PARAMETER | ADS574JE, JP, JU | | | ADS574KE, KP, KU | | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INTERNAL REFERENCE VOLTAGE** | | | | | | | |
| Voltage | +2.4 | +2.5 | +2.6 | * | * | * | V |
| Source Current Available for External Loads | 0.5 | | | * | | | mA |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | |
| Voltage: $V_{EE}$ (7) | –16.5 | | $V_{DD}$ | * | | * | V |
| $V_{DD}$ | +4.5 | | +5.5 | * | | * | V |
| Current: $I_{EE}$ (7) ($V_{EE}$ = –15V) | | –1 | | | * | | mA |
| $I_{DD}$ | | +13 | +20 | | * | * | mA |
| Power Dissipation ($T_{MIN}$ to $T_{MAX}$) ($V_{EE}$ = 0V to +5V) | | 65 | 100 | | * | * | mW |
| **TEMPERATURE RANGE** | | | | | | | |
| Specification | 0 | | +70 | * | | * | °C |
| Operating: | –40 | | +85 | * | | * | °C |
| Storage | –65 | | +150 | * | | * | °C |

* Same specification as ADS574JE, JP, JU.

NOTES: (1) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C. (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. (3) Maximum error at $T_{MIN}$ and $T_{MAX}$. (4) Based on using $V_{EE}$ = +5V, which starts a conversion immediately upon a convert command. Using $V_{EE}$ = 0V to –15V makes the ADS574/ADS774 emulate standard ADC574 operation. In this mode, the internal sample/hold acquires the input signal after receiving the convert command, and does not assume that the input level has been stable before the convert command arrives. (5) Using internal reference. (6) This is worst case change in accuracy from accuracy with a +5V supply. (7) $V_{EE}$ is optional, and is only used to set the mode for the internal sample/hold. When $V_{EE}$ = –15V, $I_{EE}$ = –1mA typ; when $V_{EE}$ = 0V, $I_{EE}$ = ±5µA typ; when $V_{EE}$ = +5V, $I_{EE}$ = +167µA typ.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $V_{EE}$ to Digital Common | $+V_{DD}$ to –16.5V |
| $V_{DD}$ to Digital Common | 0V to +7V |
| Analog Common to Digital Common | ±1V |
| Control Inputs (CE, $\overline{CS}$, $A_0$, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common | –0.5V to $V_{DD}$ +0.5V |
| Analog Inputs (Ref In, Bipolar Offset, $10V_{IN}$) to Analog Common | ±16.5V |
| $20V_{IN}$ to Analog Common | ±24V |
| Ref Out | Indefinite Short to Common, Momentary Short to $V_{DD}$ |
| Max Junction Temperature | +165°C |
| Power Dissipation | 1000mW |
| Lead Temperature (soldering,10s) | +300°C |
| Thermal Resistance, $\theta_{JA}$ : Plastic DIPs | 100°C/W |
| SOIC | 100°C/W |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

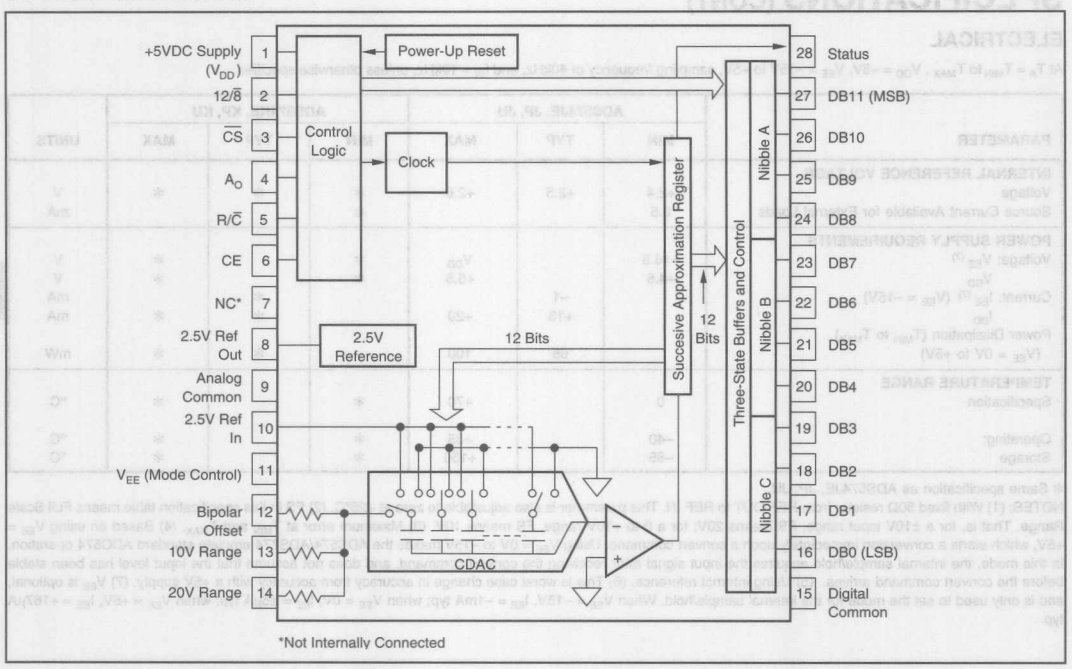
## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | SINAD(2) | TEMPERATURE RANGE | LINEARITY ERROR (LSB) |
|---|---|---|---|---|---|
| ADS574JE | 0.3" Plastic DIP | 246 | 68 | 0°C to +70°C | ±1 |
| ADS574KE | 0.3" Plastic DIP | 246 | 70 | 0°C to +70°C | ±1/2 |
| ADS574JP | 0.6" Plastic DIP | 215 | 68 | 0°C to +70°C | ±1 |
| ADS574KP | 0.6" Plastic DIP | 215 | 70 | 0°C to +70°C | ±1/2 |
| ADS574JU | SOIC | 217 | 68 | 0°C to +70°C | ±1 |
| ADS574KU | SOIC | 217 | 70 | 0°C to +70°C | ±1/2 |

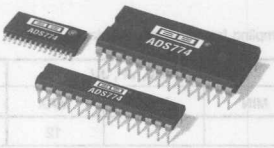
NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) SINAD is Signal-to-(Noise and Distortion) expressed in dB.

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## CONNECTION DIAGRAM



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# ADS774

www.burr-brown.com/databook/ADS774.html

# Microprocessor-Compatible Sampling CMOS ANALOG-to-DIGITAL CONVERTER

## FEATURES

- REPLACES ADC574, ADC674 AND ADC774 FOR NEW DESIGNS
- COMPLETE SAMPLING A/D WITH REFERENCE, CLOCK AND MICROPROCESSOR INTERFACE
- FAST ACQUISITION AND CONVERSION: 8.5µs max OVER TEMPERATURE
- ELIMINATES EXTERNAL SAMPLE/HOLD IN MOST APPLICATIONS
- GUARANTEED AC AND DC PERFORMANCE
- SINGLE +5V SUPPLY OPERATION
- LOW POWER: 120mW max
- PACKAGE OPTIONS: 0.6" and 0.3" DIPs, SOIC

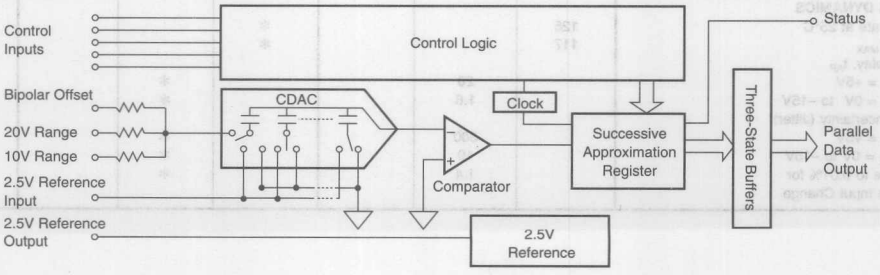
## DESCRIPTION

The ADS774 is a 12-bit successive approximation analog-to-digital converter using an innovative capacitor array (CDAC) implemented in low-power CMOS technology. This is a drop-in replacement for ADC574, ADC674, and ADC774 models in most applications, with internal sampling, much lower power consumption, and the ability to operate from a single +5V supply.

The ADS774 is complete with internal clock, microprocessor interface, three-state outputs, and internal scaling resistors for input ranges of 0V to +10V, 0V to +20V, ±5V, or ±10V. The maximum throughput time is 8.5µs over the full operating temperature range, including both acquisition and conversion.

Complete user control over the internal sampling function facilitates elimination of external sample/hold amplifiers in most existing designs.

The ADS774 requires +5V, with –15V optional. No +15V supply is required. Available packages include 0.3" or 0.6" wide 28-pin plastic DIP and 28-pin SOICs.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

## SPECIFICATIONS

### ELECTRICAL

At $T_A = T_{MIN}$ to $T_{MAX}$, $V_{DD} = +5V$, $V_{EE} = -15V$ to $+5V$, sampling frequency of 117kHz, $f_{IN} = 10kHz$; unless otherwise specified.

| PARAMETER | ADS774JE, JP, JU | | | ADS774KE, KP, KU | | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | 12 | | | * | Bits |
| **INPUTS** | | | | | | | |
| **ANALOG** | | | | | | | |
| Voltage Ranges: Unipolar | | | 0 to +10, 0 to +20 | | | | V |
| Bipolar | | | ±5, ±10 | | | | V |
| Impedance: 0 to +10V, ±5V | 8.5 | 12 | | * | * | | kΩ |
| ±10V, 0V to +20V | 35 | 50 | | * | * | | kΩ |
| **DIGITAL** (CE, $\overline{CS}$, R/$\overline{C}$, $A_0$, 12/$\overline{8}$) | | | | | | | |
| Voltages: Logic 1 | +2.0 | | +5.5 | * | | * | V |
| Logic 0 | –0.5 | | +0.8 | * | | * | V |
| Current | –5 | 0.1 | +5 | * | * | * | µA |
| Capacitance | | 5 | | | * | | pF |
| **TRANSFER CHARACTERISTICS** | | | | | | | |
| **DC ACCURACY** | | | | | | | |
| At +25°C | | | | | | | |
| Linearity Error | | | ±1 | | | ±1/2 | LSB |
| Unipolar Offset Error (adjustable to zero) | | | ±2 | | | * | LSB |
| Bipolar Offset Error (adjustable to zero) | | | ±10 | | | ±4 | LSB |
| Full-Scale Calibration Error (1) (adjustable to zero) | | | ±0.25 | | | * | % of FS (2) |
| No Missing Codes Resolution | 12 | | | 12 | | | Bits |
| $T_{MIN}$ to $T_{MAX}$ (3) | | | | | | | |
| Linearity Error | | | ±1 | | | ±1/2 | LSB |
| Full-Scale Calibration Error | | | ±0.47 | | | ±0.37 | % of FS |
| Unipolar Offset | | | ±4 | | | ±3 | LSB |
| Bipolar Offset | | | ±12 | | | ±5 | LSB |
| No Missing Codes Resolution | 12 | | | 12 | | | Bits |
| **AC ACCURACY** (4) | | | | | | | |
| Spurious Free Dynamic Range | 73 | 78 | | 76 | * | | dB |
| Total Harmonic Distortion | | –77 | –72 | | * | –75 | dB |
| Signal-to-Noise Ratio | 69 | 72 | | 71 | * | | dB |
| Signal-to-(Noise + Distortion) Ratio | 68 | 71 | | 70 | * | | dB |
| Intermodulation Distortion | | –75 | | | * | | |
| ($F_{IN1}$ = 20kHz, $F_{IN2}$ = 23kHz) | | | | | | | |
| **TEMPERATURE COEFFICIENTS** (5) | | | | | | | |
| Unipolar Offset | | ±1 | | | * | | ppm/°C |
| Bipolar Offset | | ±2 | | | * | | ppm/°C |
| Full-Scale Calibration | | ±12 | | | * | | ppm/°C |
| **POWER SUPPLY SENSITIVITY** | | | | | | | |
| Change in Full-Scale Calibration(6) | | | | | | | |
| +4.75V < $V_{DD}$ < +5.25V | | | | | | | |
| Max Change | | | ±1/2 | | | * | LSB |
| **CONVERSION TIME** (Including Acquisition Time) | | | | | | | |
| $t_{AQ} + t_C$ at 25°C: | | | | | | | |
| 8-Bit Cycle | | 5.5 | 5.9 | | * | * | µs |
| 12-Bit Cycle | | 7.5 | 8 | | * | * | µs |
| 12-Bit Cycle, $T_{MIN}$ to $T_{MAX}$: | | 8 | 8.5 | | * | * | µs |
| **SAMPLING DYNAMICS** | | | | | | | |
| Sampling Rate at 25°C | 125 | | | * | | | kHz |
| $T_{MIN}$ to $T_{MAX}$ | 117 | | | * | | | kHz |
| Aperture Delay, $t_{AP}$ | | | | | | | |
| With $V_{EE}$ = +5V | | 20 | | | * | | ns |
| With $V_{EE}$ = 0V to –15V | | 1.6 | | | * | | µs |
| Aperture Uncertainty (Jitter) | | | | | | | |
| With $V_{EE}$ = +5V | | 300 | | | * | | ps, rms |
| With $V_{EE}$ = 0V to –15V | | 10 | | | * | | ns, rms |
| Settling time to 0.01% for Full-Scale Input Change | | 1.4 | | | * | | µs |

# SPECIFICATIONS (CONT)

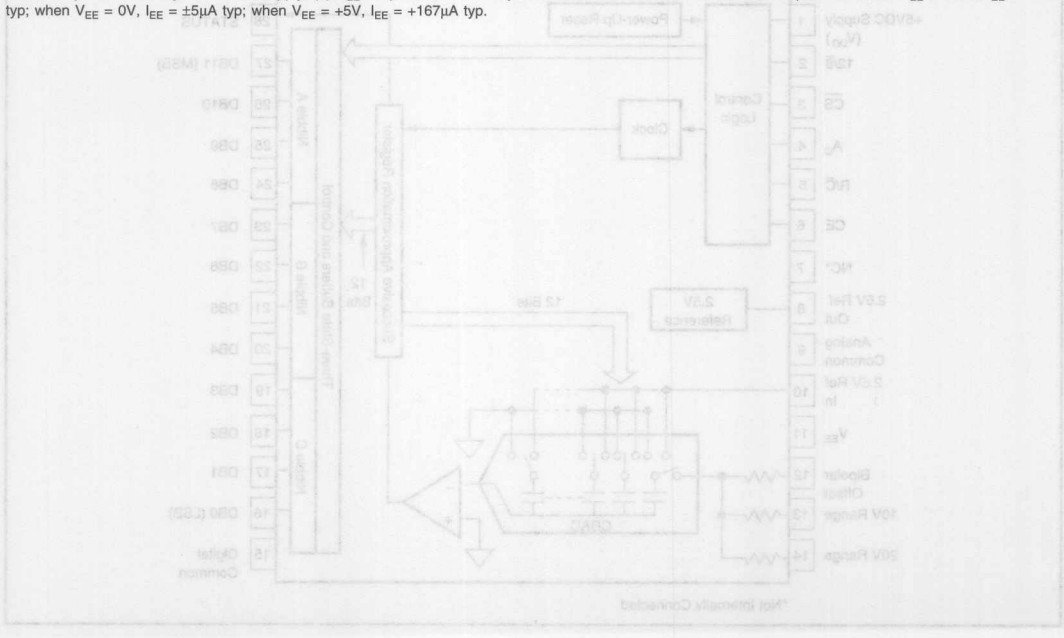
## ELECTRICAL

At $T_A = T_{MIN}$ to $T_{MAX}$, $V_{DD}$ = +5V, $V_{EE}$ = –15V to +5V, sampling frequency of 117kHz, $f_{IN}$ = 10kHz; unless otherwise specified.

| PARAMETER | ADS774JE, JP, JU | | | ADS774KE, KP, KU | | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OUTPUTS** | | | | | | | |
| **DIGITAL** ($DB_{11}$ - $DB_0$, STATUS) | | | | | | | |
| Output Codes: Unipolar | | | Unipolar Straight Binary (USB) | | | | |
| Bipolar | | | Bipolar Offset Binary (BOB) | | | | |
| Logic Levels: Logic 0 ($I_{SINK}$ = 1.6mA) | | | +0.4 | | | * | V |
| Logic 1 ($I_{SOURCE}$ = 500µA) | +2.4 | | | * | | | V |
| Leakage, Data Bits Only, High-Z State | –5 | 0.1 | +5 | * | * | * | µA |
| Capacitance | | 5 | | | * | | pF |
| **INTERNAL REFERENCE VOLTAGE** | | | | | | | |
| Voltage | +2.4 | +2.5 | +2.6 | * | * | * | V |
| Source Current Available for External Loads | 0.5 | | | * | | | mA |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | |
| Voltage: $V_{EE}$ (7) | –16.5 | | $V_{DD}$ | * | | * | V |
| $V_{DD}$ | +4.5 | | +5.5 | * | | * | V |
| Current: $I_{EE}$ (7) ($V_{EE}$ = –15V) | | –1 | | | * | | mA |
| $I_{DD}$ | | +15 | +24 | | * | * | mA |
| Power Dissipation ($T_{MIN}$ to $T_{MAX}$) ($V_{EE}$ = 0V to +5V) | | 75 | 120 | | * | * | mW |
| **TEMPERATURE RANGE** | | | | | | | |
| Specification | 0 | | +70 | * | | * | °C |
| Operating: | –40 | | +85 | * | | * | °C |
| Storage Temperature Range | –65 | | +150 | * | | * | °C |

* Same specification as ADS774JE, JP, JU.

NOTES: (1) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C. (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. (3) Maximum error at $T_{MIN}$ and $T_{MAX}$. (4) Based on using $V_{EE}$ = +5V, which is the Control Mode. See the section "S/H Control Mode and ADC774 Emulation Mode." (5) Using internal reference. (6) This is worst case change in accuracy from accuracy with a +5V supply. (7) $V_{EE}$ is optional, and is only used to set the mode for the internal sample/hold. When $V_{EE}$ = –15V, $I_{EE}$ = –1mA typ; when $V_{EE}$ = 0V, $I_{EE}$ = ±5µA typ; when $V_{EE}$ = +5V, $I_{EE}$ = +167µA typ.



The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $V_{EE}$ to Digital Common | $+V_{DD}$ to −16.5V |
| $V_{DD}$ to Digital Common | 0V to +7V |
| Analog Common to Digital Common | ±1V |
| Control Inputs (CE, $\overline{CS}$, $A_0$, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common | −0.5V to $V_{DD}$ +0.5V |
| Analog Inputs (Ref In, Bipolar Offset, $10V_{IN}$) to Analog Common | ±16.5V |
| $20V_{IN}$ to Analog Common | ±24V |
| Ref Out | Indefinite Short to Common, Momentary Short to $V_{DD}$ |
| Max Junction Temperature | +165°C |
| Power Dissipation | 1000mW |
| Lead Temperature (soldering,10s) | +300°C |
| Thermal Resistance, $\theta_{JA}$ : Plastic DIPs | 100°C/W |
| SOIC | 100°C/W |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

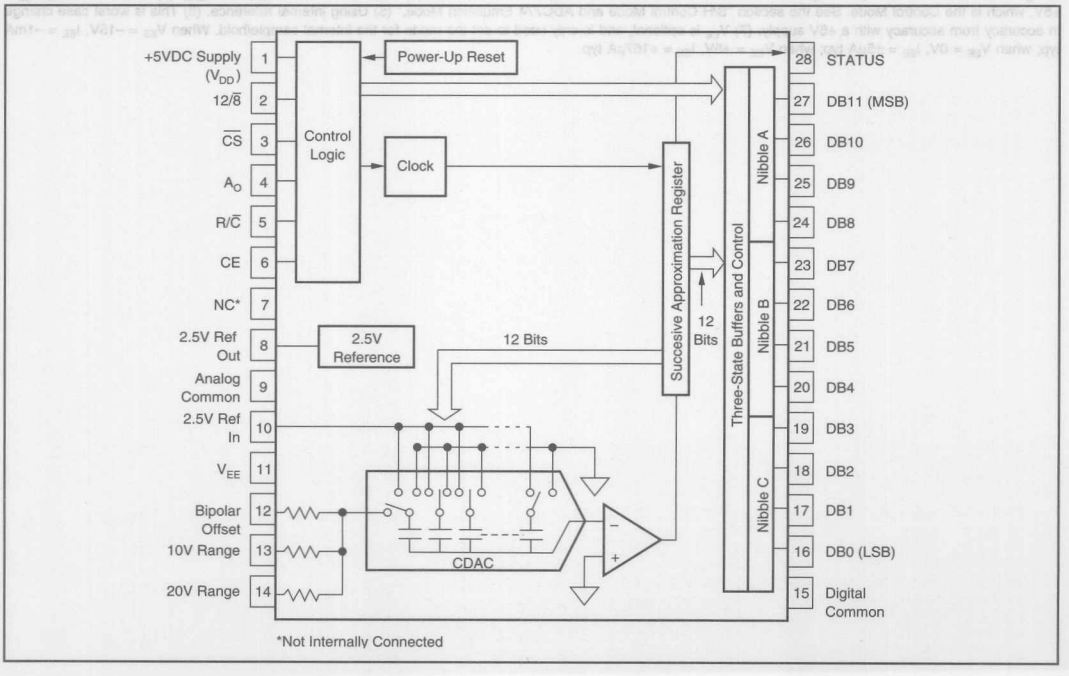
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

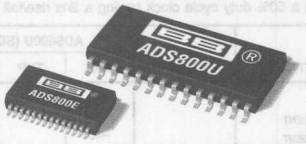
| PRODUCT | SINAD[1] | TEMPERATURE RANGE | LINEARITY ERROR | PACKAGE | PACKAGE DRAWING NUMBER[2] |
|---|---|---|---|---|---|
| ADS774JE | 68dB | 0°C to +70°C | ±1LSB | 28-Pin 0.3" Plastic DIP | 246 |
| ADS774KE | 70dB | 0°C to +70°C | ±1/2LSB | 28-Pin 0.3" Plastic DIP | 246 |
| ADS774JP | 68dB | 0°C to +70°C | ±1LSB | 28-Pin 0.6" Plastic DIP | 215 |
| ADS774KP | 70dB | 0°C to +70°C | ±1/2LSB | 28-Pin 0.6" Plastic DIP | 215 |
| ADS774JU | 68dB | 0°C to +70°C | ±1LSB | 28-Lead SOIC | 217 |
| ADS774KU | 70dB | 0°C to +70°C | ±1/2LSB | 28-Lead SOIC | 217 |

NOTES: (1) SINAD is Signal-to-(Noise + Distortion) expressed in dB. (2) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## CONNECTION DIAGRAM



BURR-BROWN®




# ADS800

www.burr-brown.com/databook/ADS800.html

## SpeedPlus™ 12-Bit, 40MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- LOW POWER: 390mW
- INTERNAL REFERENCE
- WIDEBAND TRACK/HOLD: 65MHz
- SINGLE +5V SUPPLY
- PACKAGE: 28-Lead SOIC and 28-Lead SSOP

## APPLICATIONS

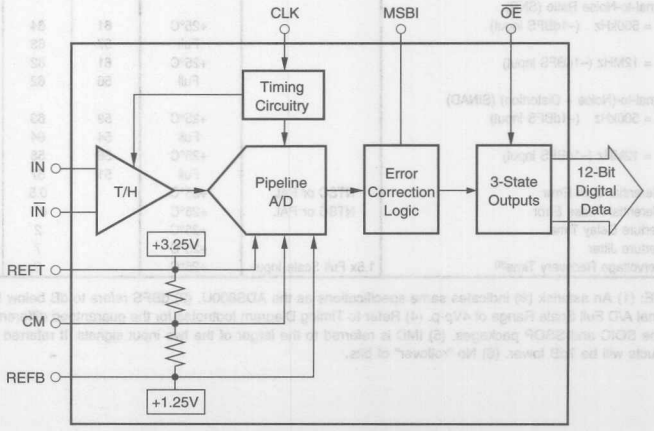
- IF AND BASEBAND DIGITIZATION
- DIGITAL COMMUNICATIONS
- ULTRASOUND IMAGING
- GAMMA CAMERAS
- TEST INSTRUMENTATION
- CCD IMAGING
  - Copiers
  - Scanners
  - Cameras
- VIDEO DIGITIZING

## DESCRIPTION

The ADS800 is a low power, monolithic 12-bit, 40MHz analog-to-digital converter utilizing a small geometry CMOS process. This COMPLETE converter includes a 12-bit quantizer, wideband track/hold, reference and three-state outputs. It operates from a single +5V power supply and can be configured to accept either differential or single-ended input signals.

The ADS800 employs digital error correction to provide excellent Nyquist differential linearity performance for demanding imaging applications. Its low distortion, high SNR and high oversampling capability give it the extra margin needed for telecommunications, test instrumentation and video applications.

This high performance A/D converter is specified over temperature for AC and DC performance at a 40MHz sampling rate. The ADS800 is available in 28-lead SOIC and SSOP packages.




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# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

| PARAMETER | CONDITIONS | TEMP | ADS800U (SOIC) MIN | ADS800U (SOIC) TYP | ADS800U (SOIC) MAX | ADS800E (SSOP) MIN | ADS800E (SSOP) TYP | ADS800E (SSOP) MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Resolution | | | | 12 | | | * | | Bits |
| Specified Temperature Range | $T_{AMBIENT}$ | | 0 | | +70 | *[1] | | * | °C |
| Operating Temperature Range | $T_{AMBIENT}$ | | –40 | | +85 | * | | * | °C |
| **ANALOG INPUT** | | | | | | | | | |
| Differential Full Scale Input Range | Both Inputs, 180° Out of Phase | | +1.25 | | +3.25 | * | | * | V |
| Common-Mode Voltage | | | | +2.25 | | | * | | V |
| Analog Input Bandwidth (–3dB) | | | | | | | | | |
| Small Signal | –20dBFS[2] Input | +25°C | | 400 | | | * | | MHz |
| Full Power | 0dBFS Input | +25°C | | 65 | | | * | | MHz |
| Input Impedance | | | | 1.25 ll 4 | | | * | | MΩ ll pF |
| **DIGITAL INPUT** | | | | | | | | | |
| Logic Family | | | | TTL/HCT Compatible CMOS | | | TTL/HCT Compatible CMOS | | |
| Convert Command | Start Conversion | | | Falling Edge | | | Falling Edge | | |
| **ACCURACY[3]** | | | | | | | | | |
| Gain Error | | +25°C | | ±0.4 | ±1.5 | | * | * | % |
| | | Full | | ±0.6 | ±2.5 | | * | * | % |
| Gain Drift | | | | ±95 | | | * | | ppm/°C |
| Power Supply Rejection of Gain | Delta +$V_S$ = ±5% | +25°C | | 0.01 | 0.15 | | * | * | %FSR/% |
| Input Offset Error | | Full | | ±2.6 | ±3.5 | | * | * | % |
| Power Supply Rejection of Offset | Delta +$V_S$ = ±5% | +25°C | | 0.02 | 0.15 | | * | * | %FSR/% |
| **CONVERSION CHARACTERISTICS** | | | | | | | | | |
| Sample Rate | | | 10k | | 40M | * | | * | Sample/s |
| Data Latency | | | | 6.5 | | | * | | Convert Cycle |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | | |
| Differential Linearity Error | | | | | | | | | |
| f = 500kHz | $t_H$ = 13ns[4] | +25°C | | ±0.6 | ±1.0 | | * | | LSB |
| | | Full | | ±0.8 | | | * | | LSB |
| f = 12MHz | | +25°C | | ±0.4 | ±1.0 | | ±0.7 | | LSB |
| | | Full | | ±0.5 | | | ±0.8 | | LSB |
| No Missing Codes | $t_H$ = 13ns[4] | +25°C | | Guaranteed | | | Guaranteed | | LSB |
| Integral Linearity Error at f = 500kHz | | Full | | ±1.9 | | | * | | LSB |
| Spurious-Free Dynamic Range (SFDR) | | | | | | | | | |
| f = 500kHz (–1dBFS input) | | +25°C | 65 | 72 | | * | * | | dBFS |
| | | Full | 60 | 66 | | * | * | | dBFS |
| f = 12MHz (–1dBFS input) | | +25°C | 58 | 61 | | * | * | | dBFS |
| | | Full | 55 | 61 | | * | * | | dBFS |
| Two-Tone Intermodulation Distortion (IMD)[5] | | | | | | | | | |
| f = 4.4MHz and 4.5MHz (–7dBFS each tone) | | +25°C | | –63 | | | * | | dBc |
| | | Full | | –62 | | | * | | dBc |
| Signal-to-Noise Ratio (SNR) | | | | | | | | | |
| f = 500kHz (–1dBFS input) | | +25°C | 61 | 64 | | 59 | * | | dB |
| | | Full | 57 | 63 | | * | * | | dB |
| f = 12MHz (–1dBFS input) | | +25°C | 61 | 62 | | 59 | * | | dB |
| | | Full | 56 | 62 | | * | * | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | | | | | | | | | |
| f = 500kHz (–1dBFS input) | | +25°C | 59 | 63 | | 57 | * | | dB |
| | | Full | 54 | 64 | | * | * | | dB |
| f = 12MHz (–1dBFS input) | | +25°C | 56 | 58 | | 54 | * | | dB |
| | | Full | 51 | 57 | | * | * | | dB |
| Differential Gain Error | NTSC or PAL | +25°C | | 0.5 | | | * | | % |
| Differential Phase Error | NTSC or PAL | +25°C | | 0.1 | | | * | | degrees |
| Aperture Delay Time | | +25°C | | 2 | | | * | | ns |
| Aperture Jitter | | +25°C | | 7 | | | * | | ps rms |
| Overvoltage Recovery Time[6] | 1.5x Full Scale Input | +25°C | | 2 | | | * | | ns |

NOTE: (1) An asterisk (*) indicates same specifications as the ADS800U. (2) dBFS refers to dB below Full Scale. (3) Percentage accuracies are referred to the internal A/D Full Scale Range of 4Vp-p. (4) Refer to Timing Diagram footnotes for the guaranteed differential linearity performance and no missing codes condition for the SOIC and SSOP packages. (5) IMD is referred to the larger of the two input signals. If referred to the peak envelope signal (≈0dB), the intermodulation products will be 7dB lower. (6) No "rollover" of bits.

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## SPECIFICATIONS (CONT)

At $T_A$ = +25°C, $V_S$ = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

| PARAMETER | CONDITIONS | TEMP | ADS800U (SOIC) MIN | ADS800U (SOIC) TYP | ADS800U (SOIC) MAX | ADS800E (SSOP) MIN | ADS800E (SSOP) TYP | ADS800E (SSOP) MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| **OUTPUTS** | | | | | | | | | |
| Logic Family | | | | TTL/HCT Compatible CMOS | | | TTL/HCT Compatible CMOS | | |
| Logic Coding | | | | SOB or BTC | | | SOB or BTC | | |
| Logic Levels | Logic Selectable<br>Logic "LO", $C_L$ = 15pF max | Full | 0 | | 0.4 | * | | * | V |
| | Logic "HI", $C_L$ = 15pF max | Full | +2.5 | | $+V_S$ | * | | * | V |
| 3-State Enable Time | | | | 20 | 40 | | * | * | ns |
| 3-State Disable Time | | Full | | 2 | 10 | | * | * | ns |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | | |
| Supply Voltage: $+V_S$ | Operating | Full | +4.75 | +5.0 | +5.25 | * | * | * | V |
| Supply Current: $+I_S$ | Operating | +25°C | | 78 | 93 | | * | * | mA |
| | Operating | Full | | 78 | 97 | | * | * | mA |
| Power Consumption | Operating | +25°C | | 390 | 465 | | * | * | mW |
| | Operating | Full | | 390 | 485 | | * | * | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | | |
| 28-Lead SOIC | | | | 75 | | | | | °C/W |
| 28-Lead SSOP | | | | | | | 50 | | °C/W |

* Specifications same as ADS800U.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Analog Input | 0V to ($+V_S$ + 300mV) |
| Logic Input | 0V to ($+V_S$ + 300mV) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +125°C |
| External Top Reference Voltage (REFT) | +3.4V Max |
| External Bottom Reference Voltage (REFB) | +1.1V Min |

NOTE: (1) Stresses above these ratings may permanently damage the device.

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS800U | 28-Lead SOIC | 217 | –40°C to +85°C |
| ADS800E | 28-Lead SSOP | 324 | –40°C to +85°C |

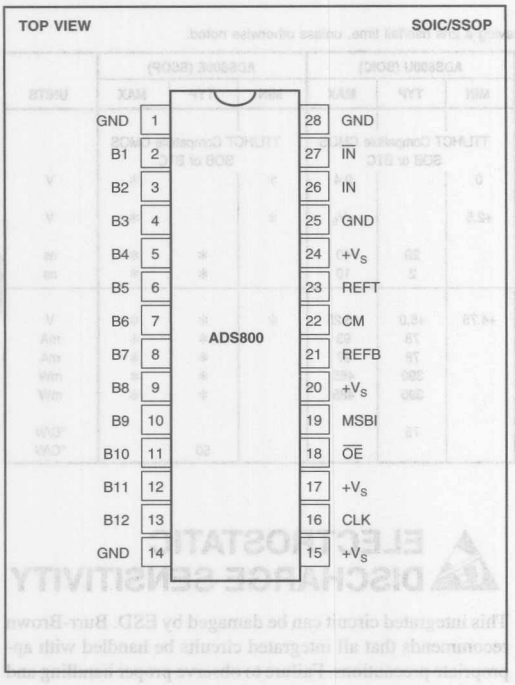
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

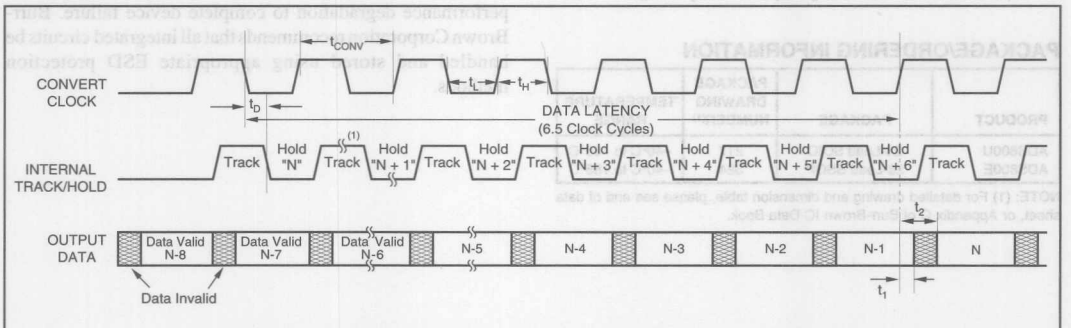
## PIN CONFIGURATION




## PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | GND | Ground |
| 2 | B1 | Bit 1, Most Significant Bit |
| 3 | B2 | Bit 2 |
| 4 | B3 | Bit 3 |
| 5 | B4 | Bit 4 |
| 6 | B5 | Bit 5 |
| 7 | B6 | Bit 6 |
| 8 | B7 | Bit 7 |
| 9 | B8 | Bit 8 |
| 10 | B9 | Bit 9 |
| 11 | B10 | Bit 10 |
| 12 | B11 | Bit 11 |
| 13 | B12 | Bit 12, Least Significant Bit |
| 14 | GND | Ground |
| 15 | $+V_S$ | +5V Power Supply |
| 16 | CLK | Convert Clock Input, 50% Duty Cycle |
| 17 | $+V_S$ | +5V Power Supply |
| 18 | $\overline{OE}$ | HI: High Impedance State. LO or Floating: Normal Operation. Internal pull-down resistors. |
| 19 | MSBI | Most Significant Bit Inversion, HI: MSB inverted for complementary output. LO or Floating: Straight output. Internal pull-down resistors. |
| 20 | $+V_S$ | +5V Power Supply |
| 21 | REFB | Bottom Reference Bypass. For external bypassing of internal +1.25V reference. |
| 22 | CM | Common-Mode Voltage. It is derived by (REFT + REFB)/2. |
| 23 | REFT | Top Reference Bypass. For external bypassing of internal +3.25V reference. |
| 24 | $+V_S$ | +5V Power Supply |
| 25 | GND | Ground |
| 26 | IN | Input |
| 27 | $\overline{IN}$ | Complementary Input |
| 28 | GND | Ground |

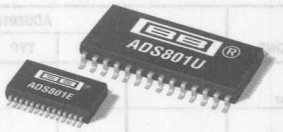
## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 25 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 12 | 12.5 | | ns |
| $t_H$ | Clock Pulse High | 12(2) | 12.5 | | ns |
| $t_D$ | Aperture Delay | | 2 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12.5 | ns |

NOTE: (1) "§" indicates the portion of the waveform that will stretch out at slower sample rates. (2) $t_H$ must be 13ns minimum if no missing codes is desired only for the conditions of $t_{CONV}$ ≤28ns and $f_{IN}$ <2MHz for the SOIC package. For best performance in the SSOP package, $t_H$ must be 13ns minimum for all input frequencies and $t_{CONV}$ ≤28ns. Refer to the Clock Requirements for a possible clock skew circuit for this condition.

BURR-BROWN®




# ADS801

www.burr-brown.com/databook/ADS801.html

## SpeedPlus™ 12-Bit, 25MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- NO MISSING CODES
- LOW POWER: 270mW
- INTERNAL REFERENCE
- WIDEBAND TRACK/HOLD: 65MHz
- SINGLE +5V SUPPLY
- PACKAGE: 28-Lead SOIC and 28-Lead SSOP

## APPLICATIONS

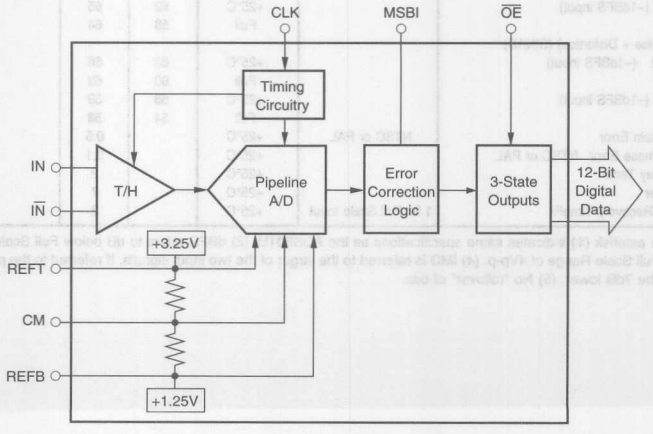
- IF AND BASEBAND DIGITIZATION
- DIGITAL COMMUNICATIONS
- TEST INSTRUMENTATION
- CCD IMAGING
  - Copiers
  - Scanners
  - Cameras
- VIDEO DIGITIZING
- GAMMA CAMERAS

## DESCRIPTION

The ADS801 is a low power, monolithic 12-bit, 25MHz analog-to-digital converter utilizing a small geometry CMOS process. This COMPLETE converter includes a 12-bit quantizer, wideband track/hold, reference, and three-state outputs. It operates from a single +5V power supply and can be configured to accept either single-ended or differential input signals.

The ADS801 employs digital error correction to provide excellent Nyquist differential linearity performance for demanding imaging applications. Its low distortion, high SNR and high oversampling capability give it the extra margin needed for telecommunications, instrumentation and video applications.

This high performance A/D converter is specified over temperature for AC and DC performance at a 25MHz sampling rate. The ADS820 is available in 28-lead SOIC and 28-lead SSOP packages.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = +5V, Sampling Rate = 25MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

| PARAMETER | CONDITIONS | TEMP | ADS801U MIN | ADS801U TYP | ADS801U MAX | ADS801E MIN | ADS801E TYP | ADS801E MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Resolution | | | | 12 | | | 12 | | Bits |
| Specified Temperature Range | $T_{AMBIENT}$ | | –40 | | +85 | *[1] | | * | °C |
| **ANALOG INPUT** | | | | | | | | | |
| Differential Full Scale Input Range | Both Inputs, 180° Out of Phase | | +1.25 | | +3.25 | * | | * | V |
| Common-Mode Voltage | | | | +2.25 | | | * | | V |
| Analog Input Bandwidth (–3dB) | | | | | | | | | |
| Small Signal | –20dBFS[2] Input | +25°C | | 400 | | | * | | MHz |
| Full Power | 0dBFS Input | +25°C | | 65 | | | * | | MHz |
| Input Impedance | | | | 1.25 II 4 | | | * | | MΩ II pF |
| **DIGITAL INPUT** | | | | | | | | | |
| Logic Family | | | | TTL/HCT Compatible CMOS | | | TTL/HCT Compatible CMOS | | |
| Convert Command | Start Conversion | | | Falling Edge | | | Falling Edge | | |
| **ACCURACY[3]** | | | | | | | | | |
| Gain Error | | +25°C | | ±0.6 | ±1.5 | | * | * | % |
| | | Full | | ±1.0 | ±2.5 | | * | * | % |
| Gain Tempco | | | | ±85 | | | * | | ppm/°C |
| Power Supply Rejection of Gain | Delta +$V_S$ = ±5% | +25°C | | 0.03 | 0.15 | | * | * | %FSR/% |
| Input Offset Error | | Full | | ±2.1 | ±3.0 | | * | * | % |
| Power Supply Rejection of Offset | Delta +$V_S$ = ±5% | +25°C | | 0.05 | 0.15 | | * | * | %FSR/% |
| **CONVERSION CHARACTERISTICS** | | | | | | | | | |
| Sample Rate | | | 10k | | 25M | * | | * | Sample/s |
| Data Latency | | | | 6.5 | | | * | | Convert Cycle |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | | |
| Differential Linearity Error | | | | | | | | | |
| f = 500kHz | | +25°C | | ±0.3 | ±1.0 | | ±0.4 | * | LSB |
| | | 0°C to +85°C | | ±0.4 | ±1.0 | | ±0.5 | * | LSB |
| f = 10MHz | | +25°C | | ±0.3 | ±1.0 | | ±0.4 | * | LSB |
| | | 0°C to +85°C | | ±0.4 | ±1.0 | | ±0.5 | * | LSB |
| No Missing Codes | | 0°C to +85°C | | Guaranteed | | | Guaranteed | | LSB |
| Integral Linearity Error at f = 500kHz | | Full | | ±1.7 | | | * | | LSB |
| Spurious-Free Dynamic Range (SFDR) | | | | | | | | | |
| f = 500kHz (–1dBFS input) | | +25°C | 63 | 77 | | * | | * | dBFS |
| | | Full | 62 | 73 | | * | | * | dBFS |
| f = 10MHz (–1dBFS input) | | +25°C | 57 | 61 | | * | | * | dBFS |
| | | Full | 55 | 61 | | * | | * | dBFS |
| Two-Tone Intermodulation Distortion (IMD)[4] | | | | | | | | | |
| f = 4.4MHz and 4.5MHz (–7dBFS each tone) | | +25°C | | –64 | | | * | | dBc |
| | | Full | | –63 | | | * | | dBc |
| Signal-to-Noise Ratio (SNR) | | | | | | | | | |
| f = 500kHz (–1dBFS input) | | +25°C | 64 | 66 | | 62 | 64 | | dB |
| | | Full | 61 | 64 | | 59 | * | | dB |
| f = 10MHz (–1dBFS input) | | +25°C | 62 | 65 | | * | * | | dB |
| | | Full | 58 | 64 | | * | * | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | | | | | | | | | |
| f = 500kHz (–1dBFS input) | | +25°C | 63 | 66 | | 61 | 64 | | dB |
| | | Full | 60 | 63 | | 58 | * | | dB |
| f = 10MHz (–1dBFS input) | | +25°C | 56 | 59 | | * | * | | dB |
| | | Full | 54 | 58 | | * | * | | dB |
| Differential Gain Error | NTSC or PAL | +25°C | | 0.5 | | | * | | % |
| Differential Phase Error NTSC or PAL | | +25°C | | 0.1 | | | * | | degrees |
| Aperture Delay Time | | +25°C | | 2 | | | * | | ns |
| Aperture Jitter | | +25°C | | 7 | | | * | | ps rms |
| Overvoltage Recovery Time[5] | 1.5x Full Scale Input | +25°C | | 2 | | | * | | ns |

NOTE: (1) An asterisk (*) indicates same specifications as the ADS801U. (2) dBFS refers to dB below Full Scale. (3) Percentage accuracies are referred to the internal A/D Full Scale Range of 4Vp-p. (4) IMD is referred to the larger of the two input signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 7dB lower. (5) No "rollover" of bits.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## SPECIFICATIONS (CONT)

At $T_A$ = +25°C, $V_S$ = +5V, Sampling Rate = 25MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

| PARAMETER | CONDITIONS | TEMP | ADS801U MIN | ADS801U TYP | ADS801U MAX | ADS801E MIN | ADS801E TYP | ADS801E MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| **OUTPUTS** | | | | | | | | | |
| Logic Family | | | | TTL/HCT Compatible CMOS | | | TTL/HCT Compatible CMOS | | |
| Logic Coding | Logic Selectable | | | Falling Edge | | | Falling Edge | | |
| Logic Levels | Logic "LO", $C_L$ = 15pF max | Full | 0 | | 0.4 | * | | * | V |
| | Logic "HI", $C_L$ = 15pF max | Full | +2.5 | | $+V_S$ | * | | * | V |
| 3-State Enable Time | | | | 20 | 40 | | * | * | ns |
| 3-State Disable Time | | Full | | 2 | 10 | | * | * | ns |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | | |
| Supply Voltage: $+V_S$ | Operating | Full | +4.75 | +5.0 | +5.25 | * | * | * | V |
| Supply Current: $+I_S$ | Operating | +25°C | | 54 | 65 | | * | * | mA |
| | Operating | Full | | 54 | 68 | | * | * | mA |
| Power Consumption | Operating | +25°C | | 270 | 325 | | * | * | mW |
| | Operating | Full | | 270 | 340 | | * | * | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | | |
| 28-Lead SOIC | | | | 75 | | | * | | °C/W |
| 28-Lead SSOP | | | | 50 | | | * | | °C/W |

* Specifications same as ADS801U.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Analog Input | 0V to ($+V_S$ + 300mV) |
| Logic Input | 0V to ($+V_S$ + 300mV) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +125°C |
| External Top Reference Voltage (REFT) | +3.4V Max |
| External Bottom Reference Voltage (REFB) | +1.1V Min |

NOTE: Stresses above these ratings may permanently damage the device.

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS801U | 28-Lead SOIC | 217 | –40°C to +85°C |
| ADS801E | 28-Lead SSOP | 324 | –40°C to +85°C |

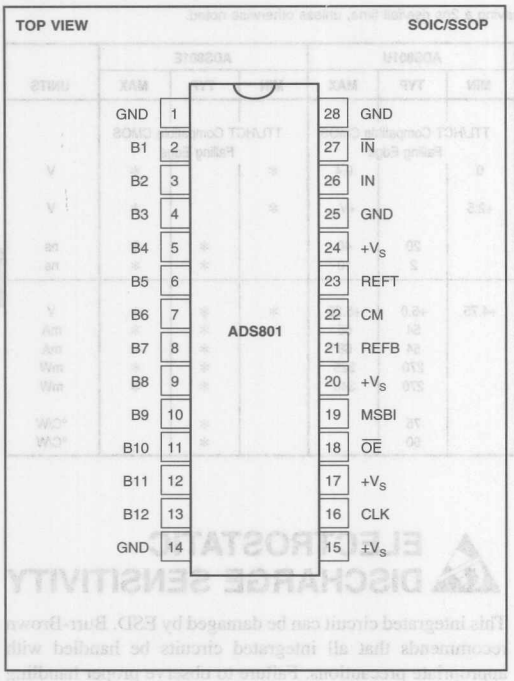
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

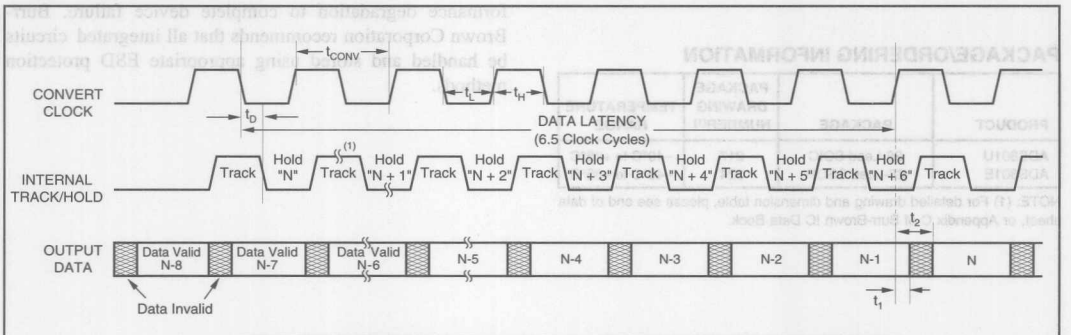
## PIN CONFIGURATION




## PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | GND | Ground |
| 2 | B1 | Bit 1, Most Significant Bit |
| 3 | B2 | Bit 2 |
| 4 | B3 | Bit 3 |
| 5 | B4 | Bit 4 |
| 6 | B5 | Bit 5 |
| 7 | B6 | Bit 6 |
| 8 | B7 | Bit 7 |
| 9 | B8 | Bit 8 |
| 10 | B9 | Bit 9 |
| 11 | B10 | Bit 10 |
| 12 | B11 | Bit 11 |
| 13 | B12 | Bit 12, Least Significant Bit |
| 14 | GND | Ground |
| 15 | $+V_S$ | +5V Power Supply |
| 16 | CLK | Convert Clock Input, 50% Duty Cycle |
| 17 | $+V_S$ | +5V Power Supply |
| 18 | $\overline{OE}$ | HI: High Impedance State. LO or Floating: Normal Operation. Internal pull-down resistors. |
| 19 | MSBI | Most Significant Bit Inversion, HI: MSB inverted for complementary output. LO or Floating: Straight output. Internal pull-down resistors. |
| 20 | $+V_S$ | +5V Power Supply |
| 21 | REFB | Bottom Reference Bypass. For external bypassing of internal +1.25V reference. |
| 22 | CM | Common-Mode Voltage. It is derived by (REFT + REFB)/2. |
| 23 | REFT | Top Reference Bypass. For external bypassing of internal +3.25V reference. |
| 24 | $+V_S$ | +5V Power Supply |
| 25 | GND | Ground |
| 26 | IN | Input |
| 27 | $\overline{IN}$ | Complementary Input |
| 28 | GND | Ground |

## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 40 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 19 | 20 | | ns |
| $t_H$ | Clock Pulse High | 19 | 20 | | ns |
| $t_D$ | Aperture Delay | | 2 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12.5 | ns |

NOTE: (1) " ⟆ " indicates the portion of the waveform that will stretch out at slower sample rates.

BURR-BROWN®




# ADS802

www.burr-brown.com/databook/ADS802.html

## SpeedPLUS™ 12-Bit, 10MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- NO MISSING CODES
- LOW POWER: 250mW
- INTERNAL REFERENCE
- WIDEBAND TRACK/HOLD: 65MHz
- SINGLE +5V SUPPLY

## APPLICATIONS

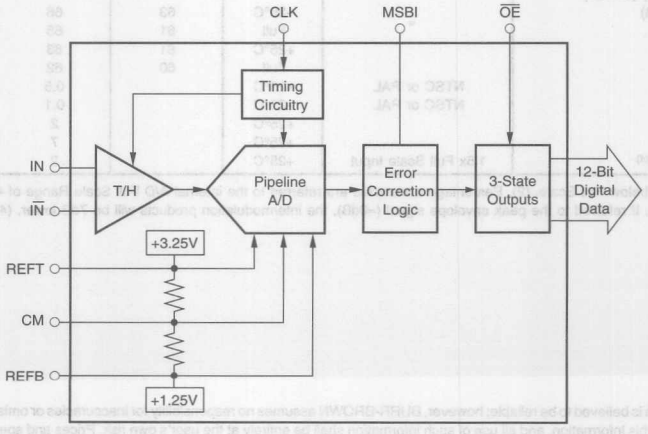
- IF AND BASEBAND DIGITIZATION
- DATA ACQUISITION CARDS
- TEST INSTRUMENTATION
- CCD IMAGING
  - Copiers
  - Scanners
  - Cameras
- VIDEO DIGITIZING
- GAMMA CAMERAS

## DESCRIPTION

The ADS802 is a low power, monolithic 12-bit, 10MHz analog-to-digital converter utilizing a small geometry CMOS process. This COMPLETE converter includes a 12-bit quantizer, wideband track/hold, reference and three-state outputs. It operates from a single +5V power supply and can be configured to accept either differential or single-ended input signals.

The ADS802 employs digital error correction in order to provide excellent Nyquist differential linearity performance for demanding imaging applications. Its low distortion, high SNR, and high oversampling capability give it the extra margin needed for telecommunications, test instrumentation and video applications.

This high performance A/D converter is specified for AC and DC performance at a 10MHz sampling rate. The ADS802 is available in 28-lead SOIC and SSOP packages.




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# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = +5V, and Sampling Rate = 10MHz, with a 50% duty cycle clock having 2ns rise/fall time, unless otherwise noted.

| PARAMETER | CONDITIONS | TEMP | ADS802U, E MIN | ADS802U, E TYP | ADS802U, E MAX | UNITS |
|---|---|---|---|---|---|---|
| Resolution | | | | 12 | | Bits |
| Specified Temperature Range | $T_{AMBIENT}$ | | –40 | | +85 | °C |
| **ANALOG INPUT** | | | | | | |
| Differential Full Scale Input Range | Both Inputs | | +1.25 | | +3.25 | V |
| Common-Mode Voltage | | | | +2.25 | | V |
| Analog Input Bandwidth (–3dB) | | | | | | |
| Small Signal | –20dBFS[1] Input | +25°C | | 400 | | MHz |
| Full Power | 0dBFS Input | +25°C | | 65 | | MHz |
| Input Impedance | | | | 1.25 ll 4 | | MΩ ll pF |
| **DIGITAL INPUT** | | | | | | |
| Logic Family | | | | TTL/HCT Compatible CMOS | | |
| Convert Command | Start Conversion | | | Falling Edge | | |
| **ACCURACY[2]** | | | | | | |
| Gain Error | | +25°C | | ±0.6 | ±1.5 | % |
| | | Full | | ±1.0 | ±2.5 | % |
| Gain Tempco | | | | ±85 | | ppm/°C |
| Power Supply Rejection of Gain | Delta +$V_S$ = ±5% | +25°C | | 0.03 | 0.1 | %FSR/% |
| Input Offset Error | | Full | | ±2.1 | ±3.0 | % |
| Power Supply Rejection of Offset | Delta +$V_S$ = ±5% | +25°C | | 0.05 | 0.1 | %FSR/% |
| **CONVERSION CHARACTERISTICS** | | | | | | |
| Sample Rate | | | 10k | | 10M | Sample/s |
| Data Latency | | | | 6.5 | | Convert Cycle |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Differential Linearity Error | | | | | | |
| f = 500kHz | | +25°C | | ±0.3 | ±1.0 | LSB |
| | | 0°C to +85°C | | ±0.4 | ±1.0 | LSB |
| f = 5MHz | | +25°C | | ±0.4 | ±1.0 | LSB |
| | | 0°C to +85°C | | ±0.4 | ±1.0 | LSB |
| No Missing Codes | | 0°C to +85°C | | Guaranteed | | LSB |
| Integral Linearity Error at f = 500kHz | Best Fit | 0°C to +85°C | | ±1.7 | ±2.75 | LSB |
| Spurious-Free Dynamic Range (SFDR) | | | | | | |
| f = 500kHz (–1dBFS input) | | +25°C | 67 | 77 | | dBFS |
| | | Full | 66 | 75 | | dBFS |
| f = 5MHz (–1dBFS input) | | +25°C | 63 | 67 | | dBFS |
| | | Full | 62 | 66 | | dBFS |
| Two-Tone Intermodulation Distortion (IMD)[3] | | | | | | |
| f = 4.4MHz and 4.5MHz (–7dBFS each tone) | | +25°C | | –65 | | dBc |
| | | Full | | –64 | | dBc |
| Signal-to-Noise Ratio (SNR) | | | | | | |
| f = 500kHz (–1dBFS input) | | +25°C | 65 | 67 | | dB |
| | | Full | 64 | 67 | | dB |
| f = 5MHz (–1dBFS input) | | +25°C | 64 | 66 | | dB |
| | | Full | 62 | 66 | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | | | | | | |
| f = 500kHz (–1dBFS input) | | +25°C | 63 | 66 | | dB |
| | | Full | 61 | 65 | | dB |
| f = 5MHz (–1dBFS input) | | +25°C | 61 | 63 | | dB |
| | | Full | 60 | 62 | | dB |
| Differential Gain Error | NTSC or PAL | +25°C | | 0.5 | | % |
| Differential Phase Error | NTSC or PAL | +25°C | | 0.1 | | degrees |
| Aperture Delay Time | | +25°C | | 2 | | ns |
| Aperture Jitter | | +25°C | | 7 | | ps rms |
| Overvoltage Recovery Time[4] | 1.5x Full Scale Input | +25°C | | 2 | | ns |

NOTE: (1) dBFS refers to dB below Full Scale. (2). Percentage accuracies are referred to the internal A/D Full Scale Range of 4Vp-p. (3) IMD is referred to the larger of the two input signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 7dB lower. (4) No "rollover" of bits.

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## SPECIFICATIONS (CONT)

At $T_A$ = +25°C, $V_S$ = +5V, and Sampling Rate = 10MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

| PARAMETER | CONDITIONS | TEMP | ADS802U, E MIN | ADS802U, E TYP | ADS802U, E MAX | UNITS |
|---|---|---|---|---|---|---|
| **OUTPUTS** | | | | | | |
| Logic Family | | | | TTL/HCT Compatible CMOS | | |
| Logic Coding | Logic Selectable | | | SOB or BTC | | |
| Logic Levels | Logic "LO" | Full | 0 | | 0.4 | V |
| | Logic "HI" | Full | 2.0 | | $+V_S$ | V |
| 3-State Enable Time | | Full | | 20 | 40 | ns |
| 3-State Disable Time | | Full | | 2 | 10 | ns |
| **POWER SUPPLY REQUIREMENTS** | | | | | | |
| Supply Voltage: $+V_S$ | Operating | Full | +4.75 | +5.0 | +5.25 | V |
| Supply Current: $+I_S$ | Operating | +25°C | | 50 | 62 | mA |
| | Operating | Full | | 52 | 62 | mA |
| Power Consumption | Operating | +25°C | | 250 | 310 | mW |
| | Operating | Full | | 260 | 310 | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | | |
| 28-Lead SOIC | | | | 75 | | °C/W |
| 28-Lead SSOP | | | | 50 | | °C/W |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Analog Input | 0V to ($+V_S$ + 300mV) |
| Logic Input | 0V to ($+V_S$ + 300mV) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +125°C |
| External Top Reference Voltage (REFT) | +3.4V Max |
| External Bottom Reference Voltage (REFB) | +1.1V Min |

NOTE: Stresses above these ratings may permanently damage the device.

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS802U | 28-Lead SOIC | 217 | –40°C to +85°C |
| ADS802E | 28-Lead SSOP | 324 | –40°C to +85°C |

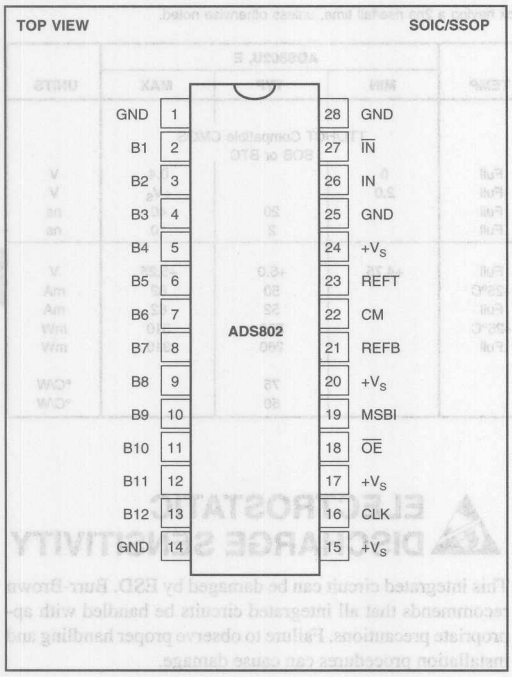
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

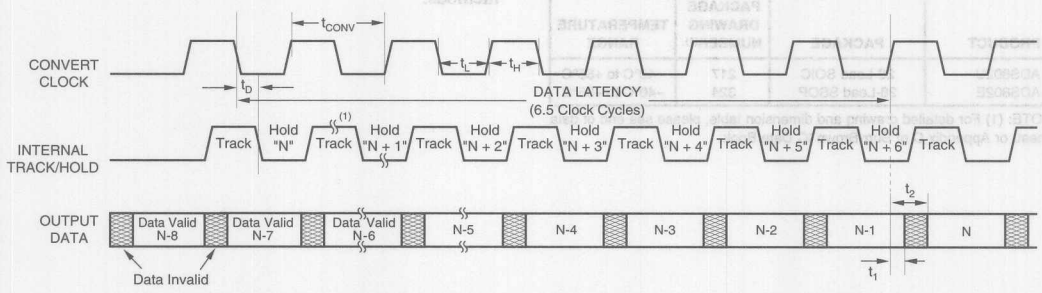
## PIN CONFIGURATION




## PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | GND | Ground |
| 2 | B1 | Bit 1, Most Significant Bit |
| 3 | B2 | Bit 2 |
| 4 | B3 | Bit 3 |
| 5 | B4 | Bit 4 |
| 6 | B5 | Bit 5 |
| 7 | B6 | Bit 6 |
| 8 | B7 | Bit 7 |
| 9 | B8 | Bit 8 |
| 10 | B9 | Bit 9 |
| 11 | B10 | Bit 10 |
| 12 | B11 | Bit 11 |
| 13 | B12 | Bit 12, Least Significant Bit |
| 14 | GND | Ground |
| 15 | $+V_S$ | +5V Power Supply |
| 16 | CLK | Convert Clock Input, 50% Duty Cycle |
| 17 | $+V_S$ | +5V Power Supply |
| 18 | $\overline{OE}$ | HI: High Impedance State. LO or Floating: Normal Operation. Internal pull-down resistors. |
| 19 | MSBI | Most Significant Bit Inversion, HI: MSB inverted for complementary output. LO or Floating: Straight output. Internal pull-down resistors. |
| 20 | $+V_S$ | +5V Power Supply |
| 21 | REFB | Bottom Reference Bypass. For external bypassing of internal +1.25V reference. |
| 22 | CM | Common-Mode Voltage. It is derived by (REFT + REFB)/2. |
| 23 | REFT | Top Reference Bypass. For external bypassing of internal +3.25V reference. |
| 24 | $+V_S$ | +5V Power Supply |
| 25 | GND | Ground |
| 26 | IN | Input |
| 27 | $\overline{IN}$ | Complementary Input |
| 28 | GND | Ground |

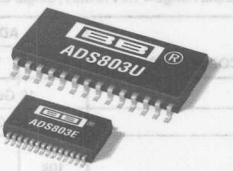
## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 100 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 48 | 50 | | ns |
| $t_H$ | Clock Pulse High | 48 | 50 | | ns |
| $t_D$ | Aperture Delay | | 2 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12.5 | ns |

NOTE: (1) " § " indicates the portion of the waveform that will stretch out at slower sample rates.

BURR-BROWN®




# ADS803

www.burr-brown.com/databook/ADS803.html

## SpeedPLUS™ 12-Bit, 5MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- HIGH SFDR: 82dB at NYQUIST
- HIGH SNR: 69dB
- LOW POWER: 115mW
- SMALL 28-LEAD SSOP AND SOIC PACKAGES
- LOW DLE: 0.25LSB
- FLEXIBLE INPUT RANGE
- OVER-RANGE INDICATOR

## APPLICATIONS

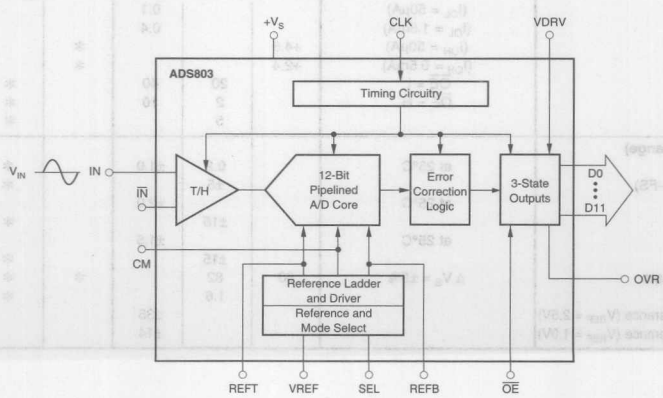
- IF AND BASEBAND DIGITIZATION
- CCD IMAGING SCANNERS
- TEST INSTRUMENTATION

## DESCRIPTION

The ADS803 is a high-speed, high dynamic range, 12-bit pipelined analog-to-digital converter. This converter includes a high-bandwidth track/hold that gives excellent spurious performance up to and beyond the Nyquist rate. This high-bandwidth, linear track/hold minimizes harmonics and has low jitter, leading to excellent SNR performance. The ADS803 is also pin-compatible with the 10MHz ADS804 and the 20MHz ADS805.

The ADS803 provides an internal reference and can be programmed for a 2Vp-p input range for the best spurious performance and ease of driving. Alternatively, the 5Vp-p input range can be used for the lowest input referred noise of 0.09 LSBs rms giving superior imaging performance. There is also a capability to set the input range in between the 2Vp-p and 5Vp-p input ranges or to use external reference. The ADS803 also provides an overrange indicator flag to indicate an input range that exceeds the full scale input range of the converter. This flag can be used to reduce the gain of the front end gain-ranging circuitry.

The ADS803 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for communications, medical imaging, video and test instrumentation applications. The ADS803 is available in 28-lead SSOP and SOIC packages.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = Full Specified Temperature Range, $V_S$ = +5V, Specified Input Range = 1.5V to 3.5V, Single-ended Input and Sampling Rate = 5MHz, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS803U | | | ADS803E | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | 12 Guaranteed | | | *[1] | | Bits |
| **SPECIFIED TEMPERATURE RANGE** | | | –40 to +85 | | | –40 to +85 | | °C |
| **CONVERSION CHARACTERISTICS** | | | | | | | | |
| Sample Rate | | 10k | | 5M | * | | * | Samples/s |
| Data Latency | | | 6 | | | * | | Clk Cycles |
| **ANALOG INPUT** | | | | | | | | |
| Single-Ended Input Range | | 1.5 | | 3.5 | * | | * | V |
| Standard Optional Single-Ended Input Range | | 0 | | 5 | * | | * | V |
| Common-Mode Voltage | | | 2.5 | | | * | | V |
| Standard Optional Common-Mode Voltage | | | 1 | | | * | | V |
| Input Capacitance | | | 20 | | | * | | pF |
| Track-Mode Input Bandwidth | –3dBFS Input | | 270 | | | * | | MHz |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | |
| Differential Linearity Error (Largest Code Error) | | | | | | | | |
| f = 500kHz | | | ±0.25 | ±0.75 | | * | * | LSB |
| No Missing Codes | | | Guaranteed | | | Guaranteed | | |
| Spurious Free Dynamic Range[2] | | | | | | | | |
| f = 2.48MHz (–1dB input) | | 75 | 82 | | * | * | | dBFS |
| Two-Tone Intermodulation Distortion[4] | | | 74 | | | * | | dBc |
| f = 1.8M and 1.9M (–7dBFS each tone) | | | | | | | | |
| Signal-to-Noise Ratio (SNR) | | | | | | | | |
| f = 2.48MHz (–1dB input) | | 67 | 69 | | * | * | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | | | | | | | | |
| f = 2.48MHz (–1dB input) | | 66 | 68 | | * | * | | dB |
| Effective Number of Bits at 2.48MHz[5] | | | 11 | | | * | | Bits |
| Input Referred Noise | 0V to 5V Input | | 0.09 | | | * | | LSBs rms |
| | 1.5V to 3.5V Input | | 0.23 | | | * | | LSBs rms |
| Integral Nonlinearity Error | | | | | | | | |
| f = 500kHz | | | ±1 | ±2 | | * | * | LSB |
| Aperture Delay Time | | | 1 | | | * | | ns |
| Aperture Jitter | | | 4 | | | * | | ps rms |
| Overvoltage Recovery Time | 1.5 x FS Input | | 2 | | | * | | ns |
| Full-Scale Step Acquisition Time | | | 50 | | | * | | ns |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Family | | | CMOS Compatible | | | CMOS Compatible | | |
| Convert Command | Start Conversion | | Rising Edge of Convert Clock | | | Rising Edge of Convert Clock | | |
| High Level Input Current ($V_{IN}$ = 5V)[6] | | | | 100 | | | * | µA |
| Low Level Input Current ($V_{IN}$ = 0V) | | | | ±10 | | | * | µA |
| High Level Input Voltage | | +3.5 | | | * | | | V |
| Low Level Input Voltage | | | | +1.0 | | | * | V |
| Input Capacitance | | | 5 | | | * | | pF |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Logic Family | | | TTL/HCT Logic Compatible CMOS | | | TTL/HCT Logic Compatible CMOS | | V |
| Logic Coding | | | Straight Offset Binary | | | Straight Offset Binary | | |
| Low Output Voltage | ($I_{OL}$ = 50µA) | | | 0.1 | | | * | V |
| Low Output Voltage | ($I_{OL}$ = 1.6mA) | | | 0.4 | | | * | V |
| High Output Voltage | ($I_{OH}$ = 50µA) | +4.5 | | | * | | | V |
| High Output Voltage | ($I_{OH}$ = 0.5mA) | +2.4 | | | * | | | V |
| 3-State Enable Time | $\overline{OE}$ = L | | 20 | 40 | | * | * | ns |
| 3-State Disable Time | $\overline{OE}$ = H | | 2 | 10 | | * | * | ns |
| Output Capacitance | | | 5 | | | * | | pF |
| **ACCURACY (5Vp-p Input Range)** | | | | | | | | |
| Zero Error (Referred to –FS) | at 25°C | | 0.2 | ±1.0 | | * | * | %FS |
| Zero Error Drift (Referred to –FS) | | | ±5 | | | * | | ppm/°C |
| Gain Error[7] | at 25°C | | | ±2.0 | | | * | %FS |
| Gain Error Drift[7] | | | ±15 | | | * | | ppm/°C |
| Gain Error[8] | at 25°C | | | ±1.5 | | | * | %FS |
| Gain Error Drift[8] | | | ±15 | | | * | | ppm/°C |
| Power Supply Rejection of Gain | $\Delta V_S$ = ±5% | 60 | 82 | | * | * | | dB |
| Reference Input Resistance | | | 1.6 | | | * | | kΩ |
| Internal Voltage Reference Tolerance ($V_{REF}$ = 2.5V) | | | | ±35 | | | * | mV |
| Internal Voltage Reference Tolerance ($V_{REF}$ = 1.0V) | | | | ±14 | | | * | mV |

## SPECIFICATIONS (CONT)

At $T_A$ = Full Specified Temperature Range, $V_S$ = +5V, Specified Input Range = 1.5V to 3.5V, Single-ended Input and Sampling Rate = 5MHz, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS803U | | | ADS803E | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | |
| Supply Voltage: $+V_S$ | Operating | +4.7 | +5.0 | 5.3 | * | * | * | V |
| Supply Current: $+I_S$ | Operating | | 23 | 27 | | * | * | mA |
| Power Dissipation | Operating | | 116 | 135 | | * | * | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| 28-Lead SOIC | | | 75 | | | | | °C/W |
| 28-Lead SSOP | | | | | | 50 | | °C/W |

NOTES: (1) An asterisk (*) indicates same specifications as the ADS803U. (2) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (3) dBFS means dB relative to full scale. (4) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (5) Effective number of bits (ENOB) is defined by (SINAD – 1.76)/6.02. (6) Internal 50kΩ pull-down resistor. (7) Includes internal reference. (8) Excludes internal reference.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Analog Input | (–0.3V) to ($+V_S$ +0.3V) |
| Logic Input | (–0.3V) to ($+V_S$ +0.3V) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +150°C |

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS803U | 28-Lead SOIC | 217 | –40°C to +85°C |
| ADS803E | 28-Lead SSOP | 324 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade of the SO-8 and DIP packages will be marked with a "B" by pin 8.

### DEMO BOARD ORDERING INFORMATION

| PRODUCT | DEMO BOARD |
|---|---|
| ADS803U | DEM-ADS80xU |

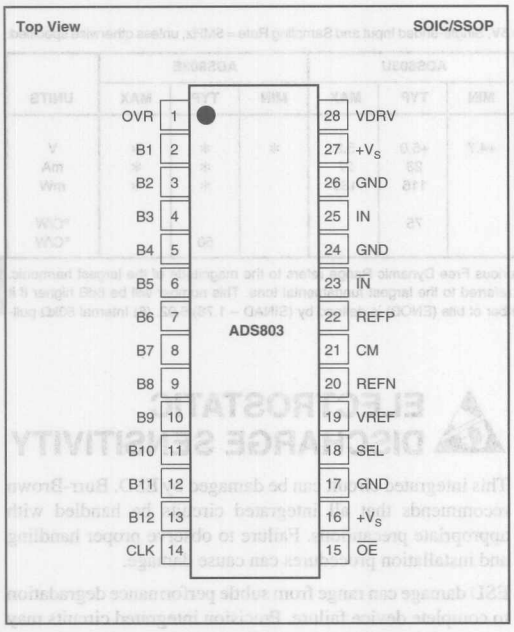
### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

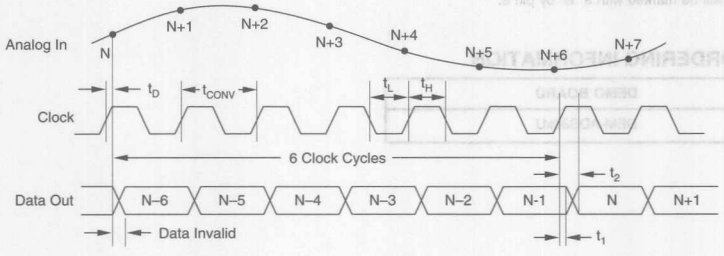
## PIN CONFIGURATION




## PIN DESCRIPTIONS

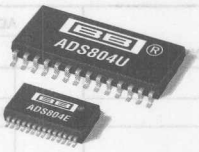
| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | OVR | Over Range Indicator |
| 2 | B1 | Data Bit 1 (MSB) |
| 3 | B2 | Data Bit 2 |
| 4 | B3 | Data Bit 3 |
| 5 | B4 | Data Bit 4 |
| 6 | B5 | Data Bit 5 |
| 7 | B6 | Data Bit 6 |
| 8 | B7 | Data Bit 7 |
| 9 | B8 | Data Bit 8 |
| 10 | B9 | Data Bit 9 |
| 11 | B10 | Data Bit 10 |
| 12 | B11 | Data Bit 11 |
| 13 | B12 | Data Bit 12 (LSB) |
| 14 | CLK | Convert Clock Input |
| 15 | $\overline{OE}$ | Output Enable |
| 16 | $+V_S$ | +5V Supply |
| 17 | GND | Ground |
| 18 | SEL | Input Range Select |
| 19 | VREF | Reference Voltage Select |
| 20 | REFB | Bottom Reference |
| 21 | CM | Common-Mode Voltage |
| 22 | REFT | Top Reference |
| 23 | $\overline{IN}$ | Complementary Analog Input |
| 24 | GND | Analog Ground |
| 25 | IN | Analog Input (+) |
| 26 | GND | Analog Ground |
| 27 | $+V_S$ | +5V Supply |
| 28 | VDRV | Output Driver Voltage |

## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 200 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 96 | 99 | | ns |
| $t_H$ | Clock Pulse High | 96 | 99 | | ns |
| $t_D$ | Aperture Delay | | 3 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12 | ns |

BURR-BROWN®




# ADS804

**DEMO BOARD AVAILABLE**

www.burr-brown.com/databook/ADS804.html

## SpeedPlus™ 12-Bit, 10MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- HIGH SFDR: 80dB at NYQUIST
- HIGH SNR: 69dB
- LOW POWER: 180mW
- SMALL 28-PIN SSOP AND SOIC PACKAGES
- LOW DLE: ±0.3LSB
- FLEXIBLE INPUT RANGE
- OVERRANGE INDICATOR

## APPLICATIONS

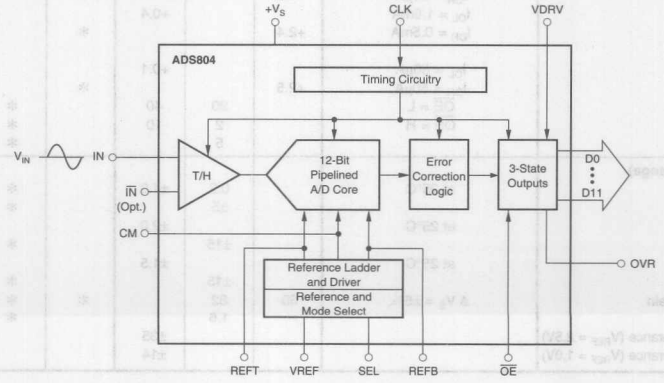
- IF AND BASEBAND DIGITIZATION
- CCD IMAGING
- SCANNERS
- TEST INSTRUMENTATION

## DESCRIPTION

The ADS804 is a high-speed, high dynamic range, 12-bit pipelined analog-to-digital converter. This converter includes a high-bandwidth track/hold that gives excellent spurious performance up to and beyond the Nyquist rate. This high-bandwidth, linear track/hold minimizes harmonics and has low jitter, leading to excellent SNR performance. The ADS804 is also pin-compatible with the 5MHz ADS803 and the 20MHz ADS805.

The ADS804 provides an internal reference and can be programmed for a 2Vp-p input range for the best spurious performance and ease of driving. Alternatively, the 5Vp-p input range can be used for the lowest input referred noise of 0.09 LSBs rms giving superior imaging performance. There is also a capability to set the input range in between the 2Vp-p and 5Vp-p input ranges or to use external reference. The ADS804 also provides an overrange indicator flag to indicate an input range that exceeds the full scale input range of the converter. This flag can be used to reduce the gain of the front end gain-ranging circuitry.

The ADS804 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for communications, medical imaging, video and test instrumentation applications. The ADS804 is available in 28-pin SSOP and SOIC packages.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = Full Specified Temperature Range, $V_S$ = +5V, Specified Single-ended Input Range = 1.5V to 3.5V, Sampling Rate = 10MHz, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS804U MIN | ADS804U TYP | ADS804U MAX | ADS804E MIN | ADS804E TYP | ADS804E MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **RESOLUTION** | | | 12 | | | ✻[1] | | Bits |
| **SPECIFIED TEMPERATURE RANGE** | | | –40 to +85 | | | –40 to +85 | | °C |
| **CONVERSION CHARACTERISTICS** | | | | | | | | |
| Sample Rate | | 10k | | 10M | ✻ | | ✻ | Samples/s |
| Data Latency | | | 6 | | | ✻ | | Clk Cycles |
| **ANALOG INPUT** | | | | | | | | |
| Single-Ended Input Range | 2Vp-p | 1.5 | | 3.5 | ✻ | | ✻ | V |
| Single-Ended Input Range (Optional) | 5Vp-p | 0 | | 5 | ✻ | | ✻ | V |
| Common-Mode Voltage | | | +2.5 | | | ✻ | | V |
| Input Impedance | | | 1.25 ‖ 16 | | | ✻ | | MΩ ‖ pF |
| Track-Mode Input Bandwidth | –3dBFS Input | | 270 | | | ✻ | | MHz |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | |
| Differential Linearity Error (Largest Code Error) | | | | | | | | |
| f = 500kHz | | | ±0.3 | ±0.75 | | ✻ | ✻ | LSB |
| No Missing Codes | | | Guaranteed | | | Guaranteed | | |
| Spurious Free Dynamic Range[2] | | | | | | | | |
| f = 4.8MHz | | 73 | 80 | | ✻ | ✻ | | dBFS |
| Two-Tone Intermodulation Distortion[4] | | | | | | | | |
| f = 3.5MHz and 4.0MHz (–7dBFS each tone) | | | 76 | | | ✻ | | dBc |
| Signal-to-Noise Ratio (SNR) | | | | | | | | |
| f = 4.8MHz | | 66.5 | 69 | | ✻ | ✻ | | dBFS |
| Signal-to-(Noise + Distortion) (SINAD) | | | | | | | | |
| f = 4.8MHz | | 65 | 68 | | ✻ | ✻ | | dBFS |
| Effective Number of Bits at 4.8MHz[5] | | | 11 | | | ✻ | | Bits |
| Input Referred Noise | 0V to 5V Input | | 0.09 | | | ✻ | | LSBs rms |
| | 1.5V to 3.5V Input | | 0.23 | | | ✻ | | LSBs rms |
| Integral Nonlinearity Error | | | | | | | | |
| f = 500kHz | | | ±1 | ±2 | | ✻ | ✻ | LSB |
| Aperture Delay Time | | | 1 | | | ✻ | | ns |
| Aperture Jitter | | | 4 | | | ✻ | | ps rms |
| Overvoltage Recovery Time | 1.5 x FS Input | | 2 | | | ✻ | | ns |
| Full-Scale Step Acquisition Time | | | 30 | | | ✻ | | ns |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Family | | | CMOS Compatible | | | CMOS Compatible | | |
| Convert Command | Start Conversion | | Rising Edge of Convert Clock | | | Rising Edge of Convert Clock | | |
| High Level Input Current ($V_{IN}$ = 5V)[6] | | | | 100 | | | ✻ | µA |
| Low Level Input Current ($V_{IN}$ = 0V) | | | | 10 | | | ✻ | µA |
| High Level Input Voltage | | +3.5 | | | ✻ | | | V |
| Low Level Input Voltage | | | | +1.0 | | | ✻ | V |
| Input Capacitance | | | 5 | | | ✻ | | pF |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Logic Family | | | TTL/HCT Compatible CMOS | | | TTL/HCT Compatible CMOS | | V |
| Convert Command | | | Straight Offset Binary | | | Straight Offset Binary | | |
| Output Voltages, $V_{DRV}$ = +5V | | | | | | | | |
| Low-Level | $I_{OL}$ = 50µA | | | +0.1 | | | ✻ | V |
| High-Level | $I_{OH}$ = 50µA | +4.6 | | | ✻ | | | V |
| Low-Level | $I_{OL}$ = 1.6mA | | | +0.4 | | | ✻ | V |
| High-Level | $I_{OH}$ = 0.5mA | +2.4 | | | ✻ | | | V |
| Output Voltages, $V_{DRV}$ = +3V | | | | | | | | |
| Low-Level | $I_{OL}$ = 50µA | | | +0.1 | | | ✻ | V |
| High-Level | $I_{OH}$ = 50µA | +2.5 | | | ✻ | | | V |
| 3-State Enable Time | $\overline{OE}$ = L | | 20 | 40 | | ✻ | ✻ | ns |
| 3-State Enable Time | $\overline{OE}$ = H | | 2 | 10 | | ✻ | ✻ | ns |
| Output Capacitance | | | 5 | | | ✻ | | pF |
| **ACCURACY (5Vp-p Input Range)** | | | | | | | | |
| Zero Error (Referred to –FS) | at 25°C | | 0.2 | ±1.0 | | ✻ | ✻ | %FS |
| Zero Error Drift | | | ±5 | | | ✻ | | ppm/°C |
| Gain Error[7] | at 25°C | | | ±2.0 | | | ✻ | %FS |
| Gain Error Drift[7] | | | ±15 | | | ✻ | | ppm/°C |
| Gain Error[8] | at 25°C | | | ±1.5 | | | ✻ | %FS |
| Gain Error Drift[8] | | | ±15 | | | ✻ | | ppm/°C |
| Power Supply Rejection of Gain | $\Delta V_S$ = ±5% | 60 | 82 | | ✻ | ✻ | | dB |
| Reference Input Resistance | | | 1.6 | | | ✻ | | kΩ |
| Internal Voltage Reference Tolerance ($V_{REF}$ = 2.5V) | | | | ±35 | | | ✻ | mV |
| Internal Voltage Reference Tolerance ($V_{REF}$ = 1.0V) | | | | ±14 | | | ✻ | mV |

## SPECIFICATIONS (CONT)

At $T_A$ = Full Specified Temperature Range, $V_S$ = +5V, Specified Single-ended Input Range = 1.5V to 3.5V, Sampling Rate = 10MHz, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS804U | | | ADS804E | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | |
| Supply Voltage: $+V_S$ | | +4.7 | +5.0 | +5.3 | * | * | * | V |
| Supply Current: $+I_S$ | | | 36 | 40 | | * | * | mA |
| Power Dissipation | | | 180 | 200 | | * | * | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| 28-Pin SOIC | | | 75 | | | | | °C/W |
| 28-Pin SSOP | | | | | | 50 | | °C/W |

NOTES: (1) An asterisk (*) indicates same specifications as the ADS804U. (2) Spurious Free Dynamic Range difference in dB between the rms input amplitude to the peak spar level in the output frequency spectrum. (3) dBFS means dB relative to full scale. (4) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (5) Effective number of bits (ENOB) is defined by (SINAD – 1.76)/6.02. (6) Internal 50kΩ pull-down resistor. (7) Includes internal reference. (8) Excludes internal reference.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$, $V_{DRV}$ | +6V |
| Analog Input | (–0.3V) to ($+V_S$ +0.3V) |
| Logic Input | (–0.3V) to ($+V_S$ +0.3V) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +150°C |

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS804U | 28-Pin SOIC | 217 | –40°C to +85°C |
| ADS804E | 28-Pin SSOP | 324 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### DEMO BOARD ORDERING INFORMATION

| PRODUCT | DEMO BOARD |
|---|---|
| ADS804U | DEM-ADS80xU |

### ELECTROSTATIC DISCHARGE SENSITIVITY

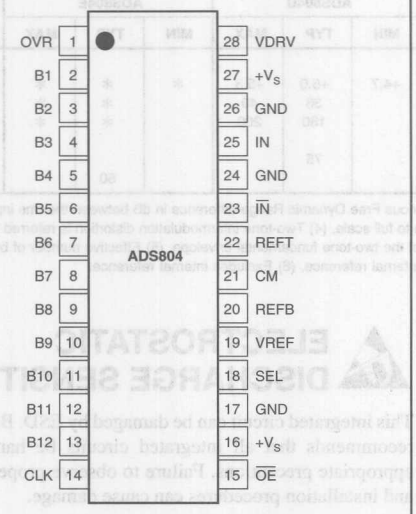
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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## PIN CONFIGURATION

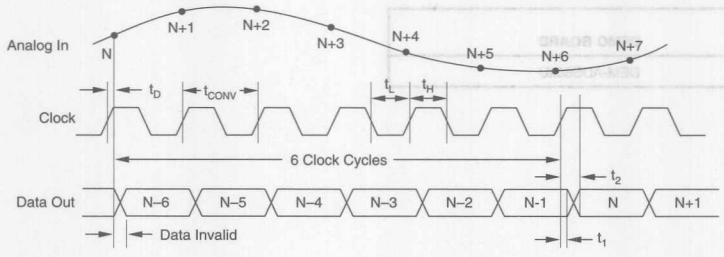
Top View SOIC/SSOP




## PIN DESCRIPTIONS

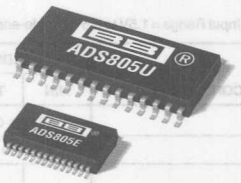
| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | OVR | Over Range Indicator (See Application Section) |
| 2 | B1 | Data Bit 1(D11) (MSB) |
| 3 | B2 | Data Bit 2 (D10) |
| 4 | B3 | Data Bit 3 (D9) |
| 5 | B4 | Data Bit 4 (D8) |
| 6 | B5 | Data Bit 5 (D7) |
| 7 | B6 | Data Bit 6 (D6) |
| 8 | B7 | Data Bit 7 (D5) |
| 9 | B8 | Data Bit 8 (D4) |
| 10 | B9 | Data Bit 9 (D3) |
| 11 | B10 | Data Bit 10 (D2) |
| 12 | B11 | Data Bit 11 (D1) |
| 13 | B12 | Data Bit 12 (D0) (LSB) |
| 14 | CLK | Convert Clock Input |
| 15 | $\overline{OE}$ | Output Enable. H-High Impedance State. L-Low or floating, normal operation (Internal pull-down resistor) |
| 16 | $+V_S$ | +5V Supply |
| 17 | GND | Ground |
| 18 | SEL | Input Range Select (See Application Section) |
| 19 | VREF | Reference Voltage Select (I/O) |
| 20 | REFB | Bottom Reference |
| 21 | CM | Common-Mode Voltage |
| 22 | REFT | Top Reference |
| 23 | $\overline{IN}$ | Analog Input (–) |
| 24 | GND | Ground |
| 25 | IN | Analog Input (+) |
| 26 | GND | Ground |
| 27 | $+V_S$ | +5V Supply |
| 28 | VDRV | Output Driver Voltage (See Application Section) |

## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 100 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 48 | 49 | | ns |
| $t_H$ | Clock Pulse High | 48 | 49 | | ns |
| $t_D$ | Aperture Delay | | 2 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12 | ns |

BURR - BROWN®




# ADS805

www.burr-brown.com/databook/ADS805.html

## SpeedPlus™ 12-Bit, 20MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- HIGH SFDR: 74dB at 9.8MHz $f_{IN}$
- HIGH SNR: 68dB
- LOW POWER: 300mW
- SMALL 28-LEAD SSOP AND SOIC PACKAGES
- LOW DLE: 0.25LSB
- FLEXIBLE INPUT RANGE
- OVER-RANGE INDICATOR

## APPLICATIONS

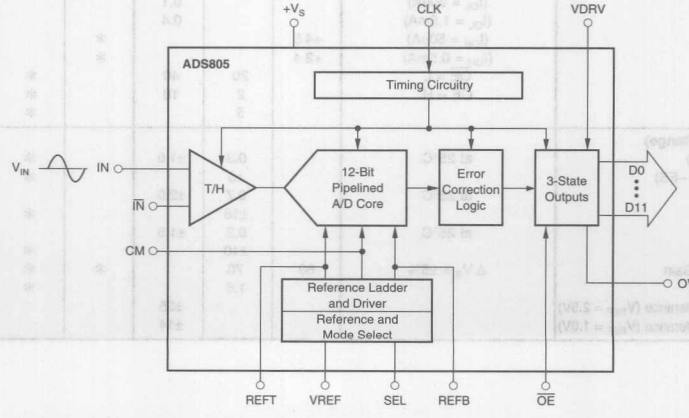
- STUDIO CAMERAS
- IF AND BASEBAND DIGITIZATION
- COPIERS
- TEST INSTRUMENTATION

## DESCRIPTION

The ADS805 is a 20MHz, high dynamic range, 12-bit pipelined analog-to-digital converter. This converter includes a high-bandwidth track/hold that gives excellent spurious performance up to and beyond the Nyquist rate. This high-bandwidth, linear track/hold minimizes harmonics and has low jitter, leading to excellent SNR performance. The ADS805 is also pin-compatible with the 10MHz ADS804 and the 5MHz ADS803.

The ADS805 provides an internal reference or an external reference can be used. ADS805 can be programmed for a 2Vp-p input range which is the easiest to drive with a single op amp and provides the best spurious performance. Alternatively, the 5Vp-p input range can be used for the lowest input referred noise of 0.09 LSBs rms giving superior imaging performance. There is also the capability to set the input range between 2Vp-p and 5Vp-p, either single-ended or differential. The ADS805 also provides an overrange flag that indicates when the input signal has exceeded the converter's full scale range. This flag can also be used to reduce the gain of the front end signal conditioning circuitry.

The ADS805 employs digital error techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for communications, medical imaging, video and test instrumentation applications. The ADS805 is available in 28-lead SSOP and SOIC packages.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = Full Specified Temperature Range, $V_S$ = +5V, Specified Input Range = 1.5V to 3.5V, Single-ended Input and Sampling Rate = 20MHz, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS805U | | | ADS805E | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | 12 Bits Guaranteed | | | *[1] | | Bits |
| **SPECIFIED TEMPERATURE RANGE** | | | –40 to +85 | | | –40 to +85 | | °C |
| **CONVERSION CHARACTERISTICS** | | | | | | | | |
| Sample Rate | | 10k | | 20M | * | | * | Samples/s |
| Data Latency | | | 6 | | | * | | Clk Cycles |
| **ANALOG INPUT** | | | | | | | | |
| Standard Single-Ended Input Range | | 1.5 | | 3.5 | * | | * | V |
| Optional Single-Ended Input Range | | 0 | | 5 | * | | * | V |
| Standard Common-Mode Voltage | | | 2.5 | | | * | | V |
| Standard Optional Common-Mode Voltage | | | 1 | | | * | | V |
| Input Capacitance | | | 20 | | | * | | pF |
| Track-Mode Input Bandwidth | –3dBFS Input | | 270 | | | * | | MHz |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | |
| Differential Linearity Error (Largest Code Error) | | | | | | | | |
| f = 500kHz | | | ±0.25 | ±0.75 | | * | * | LSB |
| No Missing Codes | | | Guaranteed | | | Guaranteed | | |
| Spurious Free Dynamic Range[2] | | | | | | | | |
| f = 9.8MHz | | 70 | 74 | | * | * | | dBFS |
| Two-Tone Intermodulation Distortion[4] | | | | | | | | |
| f = 7.7MHz and 7.9MHz (–7dB each tone) | | | –70 | | | * | | dBc |
| Signal-to-Noise Ratio (SNR) | | | | | | | | |
| f = 9.8MHz | | 63 | 68 | | * | * | | dBFS |
| Signal-to-(Noise + Distortion) (SINAD) | | | | | | | | |
| f = 9.8MHz | | 62 | 66 | | * | * | | dBFS |
| Effective Number of Bits at 9.8MHz[5] | | | 10.7 | | | * | | Bits |
| Input Referred Noise | 0V to 5V Input | | 0.09 | | | * | | LSBs rms |
| | 1.5V to 3.5V Input | | 0.23 | | | * | | LSBs rms |
| Integral Nonlinearity Error | | | | | | | | |
| f = 500kHz | | | ±1 | ±2 | | * | * | LSB |
| Aperture Delay Time | | | 3 | | | * | | ns |
| Aperture Jitter | | | 4 | | | * | | ps rms |
| Overvoltage Recovery Time | 1.5X FS Input | | 2 | | | * | | ns |
| Full-Scale Step Acquisition Time | | | 20 | | | 20 | | ns |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Family | | | CMOS Compatible | | | CMOS Compatible | | |
| Convert Command | Start Conversion | | Rising Edge of Convert Clock | | | Rising Edge of Convert Clock | | |
| High Level Input Current ($V_{IN}$ = 5V)[6] | | | | ±100 | | | * | µA |
| Low Level Input Current ($V_{IN}$ = 0V) | | | | 10 | | | * | µA |
| High Level Input Voltage | | +3.5 | | | * | | | V |
| Low Level Input Voltage | | | | +1.0 | | * | | V |
| Input Capacitance | | | 5 | | | * | | pF |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Logic Family | | | TTL/HCT Compatible CMOS | | | TTL/HCT Compatible CMOS | | V |
| Logic Coding | | | Straight Offset Binary | | | Straight Offset Binary | | |
| Low Output Voltage | ($I_{OL}$ = 50µA) | | | 0.1 | | | * | V |
| Low Output Voltage | ($I_{OL}$ = 1.6mA) | | | 0.4 | | | * | V |
| High Output Voltage | ($I_{OH}$ = 50µA) | +4.5 | | | * | | | V |
| High Output Voltage | ($I_{OH}$ = 0.5mA) | +2.4 | | | * | | | V |
| 3-State Enable Time | $\overline{OE}$ = L | | 20 | 40 | | * | * | ns |
| 3-State Disable Time | $\overline{OE}$ = H | | 2 | 10 | | * | * | ns |
| Output Capacitance | | | 5 | | | * | | pF |
| **ACCURACY (5Vp-p Input Range)** | | | | | | | | |
| Zero Error (Referred to –FS) | at 25°C | | 0.3 | ±1.0 | | * | * | %FS |
| Zero Error Drift (Referred to –FS) | | | ±5 | | | * | | ppm/°C |
| Gain Error[7] | at 25°C | | 0.7 | ±2.0 | | | * | %FS |
| Gain Error Drift[7] | | | ±18 | | | * | | ppm/°C |
| Gain Error[8] | at 25°C | | 0.2 | ±1.5 | | | * | %FS |
| Gain Error Drift[8] | | | ±10 | | | * | | ppm/°C |
| Power Supply Rejection of Gain | $\Delta V_S$ = ±5% | 60 | 70 | | * | * | | dB |
| Reference Input Resistance | | | 1.6 | | | * | | kΩ |
| Internal Voltage Reference Tolerance ($V_{REF}$ = 2.5V) | | | | ±35 | | | * | mV |
| Internal Voltage Reference Tolerance ($V_{REF}$ = 1.0V) | | | | ±14 | | | * | mV |

## SPECIFICATIONS (CONT)

At $T_A$ = Full Specified Temperature Range, $V_S$ = +5V, Specified Input Range = 1.5V to 3.5V, Single-ended Input and Sampling Rate = 20MHz, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS805U MIN | ADS805U TYP | ADS805U MAX | ADS805E MIN | ADS805E TYP | ADS805E MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | |
| Supply Voltage: $+V_S$ | Operating | +4.75 | +5.0 | +5.25 | * | * | * | V |
| Supply Current: $+I_S$ | Operating | | 60 | 69 | | * | * | mA |
| Power Dissipation | Operating | | 300 | 345 | | * | * | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| 28-Lead SOIC | | | 75 | | | | | °C/W |
| 28-Lead SSOP | | | | | | 50 | | °C/W |

NOTES: (1) An asterisk (*) indicates same specifications as the ADS805U. (2) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (3) dBFS means dB relative to full scale. (4) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (5) Effective number of bits (ENOB) is defined by (SINAD – 1.76)/6.02. (6) Internal 50kΩ pull down resistor. (7) Includes internal reference. (8) Excludes internal reference.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Analog Input | (–0.3V) to ($+V_S$ +0.3V) |
| Logic Input | (–0.3V) to ($+V_S$ +0.3V) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +150°C |

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS805U | 28-Lead SOIC | 217 | –40°C to +85°C |
| ADS805E | 28-Lead SSOP | 324 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### DEMO BOARD ORDERING INFORMATION

| PRODUCT | DEMO BOARD |
|---|---|
| ADS805U | DEM-ADS80xU |

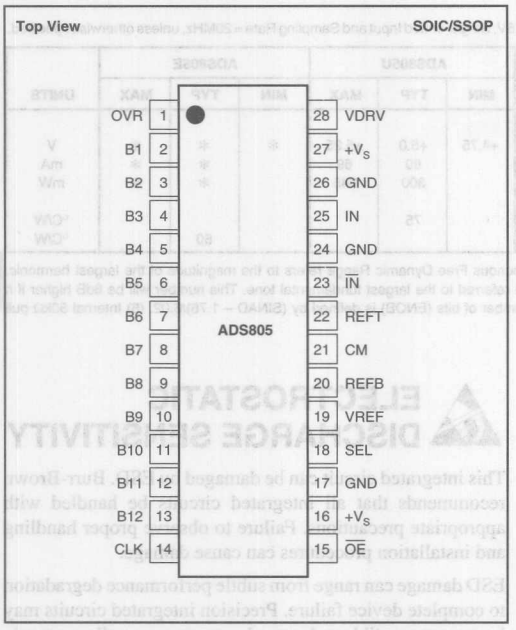
### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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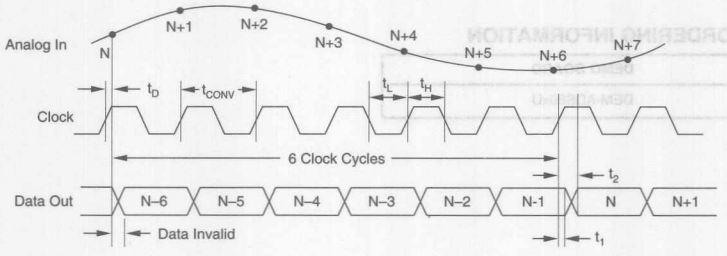
## PIN CONFIGURATION




## PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | OVR | Over Range Indicator |
| 2 | B1 | Data Bit 1 (D11) (MSB) |
| 3 | B2 | Data Bit 2 (D10) |
| 4 | B3 | Data Bit 3 (D9) |
| 5 | B4 | Data Bit 4 (D8) |
| 6 | B5 | Data Bit 5 (D7) |
| 7 | B6 | Data Bit 6 (D6) |
| 8 | B7 | Data Bit 7 (D5) |
| 9 | B8 | Data Bit 8 (D4) |
| 10 | B9 | Data Bit 9 (D3) |
| 11 | B10 | Data Bit 10 (D2) |
| 12 | B11 | Data Bit 11 (D1) |
| 13 | B12 | Data Bit 12 (D0) (LSB) |
| 14 | CLK | Convert Clock Input |
| 15 | $\overline{OE}$ | Output Enable |
| 16 | $+V_S$ | +5V Supply |
| 17 | GND | Ground |
| 18 | SEL | Input Range Select |
| 19 | VREF | Reference Voltage Select |
| 20 | REFB | Bottom Reference |
| 21 | CM | Common-Mode Voltage |
| 22 | REFT | Top Reference |
| 23 | $\overline{IN}$ | Complementary Analog Input |
| 24 | GND | Ground |
| 25 | IN | Analog Input (+) |
| 26 | GND | Ground |
| 27 | $+V_S$ | +5V Supply |
| 28 | VDRV | Output Driver Voltage |

## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 50 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 24 | 25 | | ns |
| $t_H$ | Clock Pulse High | 24 | 25 | | ns |
| $t_D$ | Aperture Delay | | 3 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12 | ns |

BURR-BROWN®




# ADS806

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

www.burr-brown.com/databook/ADS806.html

# SpeedPlus™ 12-Bit, 50MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- HIGH SFDR: 73dB
- HIGH SNR: 67dB
- LOW POWER: 380mW
- SMALL 28-LEAD SSOP PACKAGE
- FLEXIBLE INPUT RANGE
- OVER-RANGE INDICATOR

## APPLICATIONS

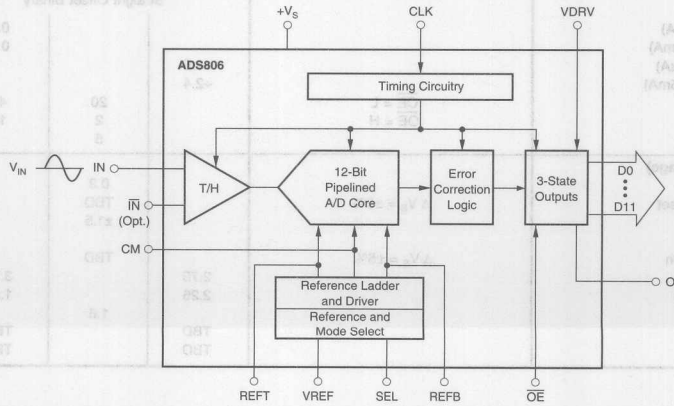
- IF AND BASEBAND DIGITIZATION
- HIGH-END IMAGING
- ULTRA SOUND IMAGING
- TEST INSTRUMENTATION

## DESCRIPTION

The ADS806 is a high-speed, high dynamic range, 12-bit pipelined analog-to-digital converter. This converter includes a high-bandwidth track/hold that gives excellent spurious performance up to and beyond the Nyquist rate, This high-bandwidth, linear track/hold minimizes harmonics and has low jitter, leading to excellent SNR performance. The ADS806 is also pin-compatible with the 20MHz ADS805, the 10MHz ADS804 and the 5MHz ADS803.

The ADS806 provides an internal reference and can be programmed for a 2Vp-p input range for the best spurious performance and ease of driving. Alternatively, the 5Vp-p input range can be used for the lowest input referred noise, giving superior imaging performance. There is also a capability to set the input range in between the 2Vp-p and 5Vp-p input ranges or to use external reference. The ADS806 also provides an overrange indicator flag to indicate an input range that exceeds the full scale input range of the converter. This flag can be used to reduce the gain of the front end gain-ranging circuitry.

The ADS806 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for communications, medical imaging, video and test instrumention applications. The ADS806 is available in a 28-lead SSOP package.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

## SPECIFICATIONS—PRELIMINARY

At $T_A$ = Full Specified Temperature Range, $V_S$ = +5V, Specified Input Range = 1.5V to 3.5V, Single-ended Input and Sampling Rate = 50MHz, unless otherwise noted.

| PARAMETER | COMMENTS | ADS806E MIN | ADS806E TYP | ADS806E MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | 12 Bits Guaranteed | | Bits |
| **SPECIFIED TEMPERATURE RANGE** | | | –40 to +85 | | °C |
| **CONVERSION CHARACTERISTICS** | | | | | |
| Sample Rate | | 10k | | 50M | Samples/s |
| Data Latency | | | 6 | | Clk Cycles |
| **ANALOG INPUT** | | | | | |
| Single-Ended Input Range | 2Vp-p | 1.5 | | 3.5 | V |
| Single-Ended Input Range (Optional) | 5Vp-p | 0 | | 5 | V |
| Common-Mode Voltage | | | +2.5 | | V |
| Input Impedance | | | 1.25 ll 16 | | MΩ ll pF |
| Track-Mode Input Bandwidth | –3dBFS Input | | 270 | | MHz |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Differential Linearity Error (Largest Code Error) | | | | | |
| f = 12MHz | | | ±0.25 | ±0.75 | LSB |
| No Missing Codes | | | Guaranteed | | |
| Spurious Free Dynamic Range[1] | | | | | |
| f = 12MHz (–1dB input) | | 68 | 73 | | dBFS[2] |
| Two-Tone Intermodulation Distortion[3] | | | | | |
| f = 3.5MHz and 4.0MHz (–7dB each tone) | | | 76 | | dBc |
| Signal-to-Noise Ratio (SNR) | | | | | |
| f = 12MHz (–1dB input) | | 63 | 67 | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | | | | | |
| f = 12MHz (–1dB input) | | 62 | 66 | | dB |
| Effective Number of Bits at 12MHz[4] | | | TBD | | Bits |
| Input Referred Noise | 0V to 5V Input | | TBD | | LSBs rms |
| | 1.5V to 3.5V Input | | TBD | | LSBs rms |
| Integral Nonlinearity Error | | | | | |
| f = 500kHz | | | ±1 | ±2 | LSB |
| Aperture Delay Time | | | 1 | | ns |
| Aperture Jitter | | | 1.2 | | ps rms |
| Analog Input Bandwidth | | | | | |
| Small Signal | –20dBFS Input | | 350 | | MHz |
| Full Power | 0dBFS Input | | 100 | | MHz |
| Overvoltage Recovery Time | 1.5 x FS Input | | 2 | | ns |
| Full-Scale Step Acquisition Time | | | TBD | | ns |
| **DIGITAL INPUTS** | | | | | |
| Logic Family | | | TTL/HCT Compatible CMOS | | |
| Convert Command | Start Conversion | | Rising Edge of Convert Clock | | |
| High Level Input Current ($V_{IN}$ = 5V) | | | | ±10 | µA |
| Low Level Input Current ($V_{IN}$ = 0V) | | | | ±10 | µA |
| High Level Input Voltage | | +3.5 | | | V |
| Low Level Input Voltage | | | | +1.0 | V |
| Input Capacitance | | | 5 | | pF |
| **DIGITAL OUTPUTS** | | | | | |
| Logic Family | | | TTL/HCT Compatible CMOS | | |
| Logic Coding | | | Straight Offset Binary | | |
| Low Output Voltage ($I_{OL}$ = 50µA) | | | | 0.1 | V |
| Low Output Voltage, ($I_{OL}$ = 1.6mA) | | | | 0.4 | V |
| High Output Voltage ($I_{OH}$ = 50µA) | | +4.5 | | | V |
| High Output Voltage, ($I_{OH}$ = 0.5mA) | | +2.4 | | | V |
| 3-State Enable Time | $\overline{OE}$ = L | | 20 | 40 | ns |
| 3-State Disable Time | $\overline{OE}$ = H | | 2 | 10 | ns |
| Output Capacitance | | | 5 | | pF |
| **ACCURACY (5Vp-p Input Range)** | | | | | |
| Zero Error | | | 0.3 | | %FS |
| Power Supply Rejection of Offset | $\Delta V_S$ = ±5% | | TBD | | dB |
| Gain Error[5] | | | ±1.5 | | %FS |
| Gain Error[6] | | | | | |
| Power Supply Rejection of Gain | $\Delta V_S$ = ±5% | | TBD | | dB |
| External REFP Voltage Range | | 2.75 | | 3.75 | V |
| External REFN Voltage Range | | 2.25 | | 1.25 | V |
| Reference Input Resistance | | | 1.6 | | kΩ |
| REFT Tolerance | | TBD | | TBD | mV |
| REFB Tolerance | | TBD | | TBD | mV |

## SPECIFICATIONS—PRELIMINARY (CONT)

At $T_A$ = Full Specified Temperature Range, $V_S$ = +5V, Specified Input Range = 1.5V to 3.5V, Single-ended Input and Sampling Rate = 50MHz, unless otherwise specified.

| PARAMETER | COMMENTS | ADS806E MIN | ADS806E TYP | ADS806E MAX | UNITS |
|---|---|---|---|---|---|
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Supply Voltage: $+V_S$ | Operating | +4.75 | +5.0 | +5.25 | V |
| Supply Current: $+I_S$ | Operating | | 76 | 62 | mA |
| Power Dissipation | Operating | | 380 | | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| 28-Lead SSOP | | | 50 | | °C/W |

NOTES: (1) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to full scale. (3) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (4) Effective number of bits (ENOB) is defined by (SINAD – 1.76)/6.02. (5) Includes internal reference. (6) Excludes internal reference.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Analog Input | (–0.3V) to ($+V_S$ +0.3V) |
| Logic Input | (–0.3V) to ($+V_S$ +0.3V) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +150°C |

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| ADS806E | 28-Lead SSOP | 324 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

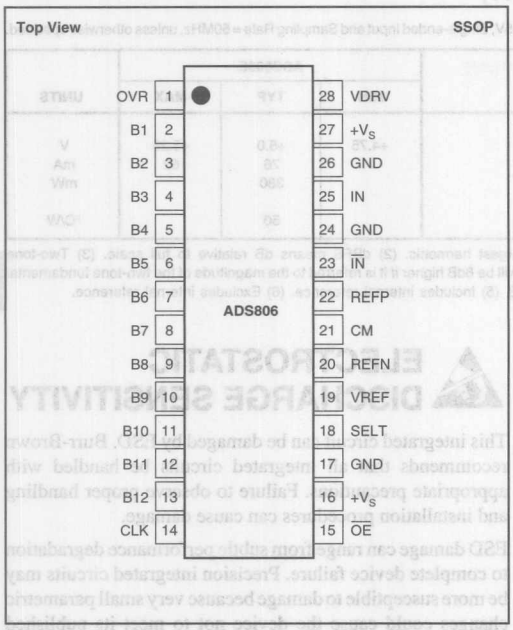
### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

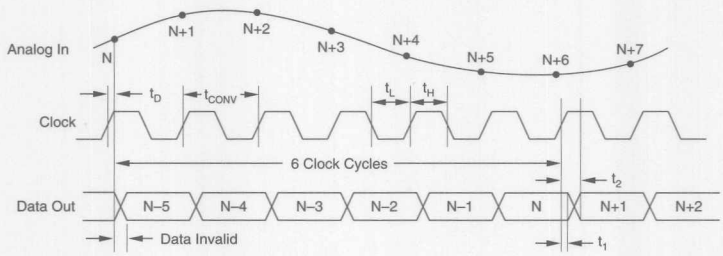
## PIN CONFIGURATION




## PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | OVR | Over Range Indicator |
| 2 | B1 | Data Bit 1, (D11, MSB) |
| 3 | B2 | Data Bit 2, (D10) |
| 4 | B3 | Data Bit 3, (D9) |
| 5 | B4 | Data Bit 4, (D8) |
| 6 | B5 | Data Bit 5, (D7) |
| 7 | B6 | Data Bit 6, (D6) |
| 8 | B7 | Data Bit 7, (D5) |
| 9 | B8 | Data Bit 8, (D4) |
| 10 | B9 | Data Bit 9, (D3) |
| 11 | B10 | Data Bit 10, (D2) |
| 12 | B11 | Data Bit 11, (D1) |
| 13 | B12 | Data Bit 12, (D0, LSB) |
| 14 | CLK | Convert Clock Input |
| 15 | $\overline{OE}$ | Output Enable |
| 16 | $+V_S$ | +5V Supply |
| 17 | GND | Ground |
| 18 | SEL | Input Range Select |
| 19 | VREF | Reference Voltage Select |
| 20 | REFB | Bottom Reference |
| 21 | CM | Common-Mode Voltage |
| 22 | REFT | Top Reference |
| 23 | $\overline{IN}$ | Complementary Analog Input |
| 24 | GND | Analog Ground |
| 25 | IN | Analog Input (+) |
| 26 | GND | Analog Ground |
| 27 | $+V_S$ | +5V Supply |
| 28 | VDRV | Output Driver Voltage |

## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 20 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 9.8 | 10 | | ns |
| $t_H$ | Clock Pulse High | 9.8 | 10 | | ns |
| $t_D$ | Aperture Delay | | 2 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12 | ns |

BURR-BROWN®

# ADS807

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

www.burr-brown.com/databook/ADS807.html



## SpeedPLUS™ 12-Bit, 53MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- SPURIOUS FREE DYNAMIC RANGE: 82dB at 10MHz $f_{IN}$
- HIGH SNR: 67.5dB (2Vp-p), 69dB (3Vp-p)
- LOW POWER: 324mW
- INTERNAL/EXTERNAL REFERENCE OPTION
- LOW DNL: 0.5LSB
- FLEXIBLE INPUT RANGE: 2Vp-p to 3Vp-p
- 28-LEAD SSOP PACKAGE

## APPLICATIONS

- COMMUNICATIONS IF PROCESSING
- MEDICAL IMAGING
- TEST EQUIPMENT
- COMMUNICATIONS
- VIDEO DIGITIZING
- CCD DIGITIZING

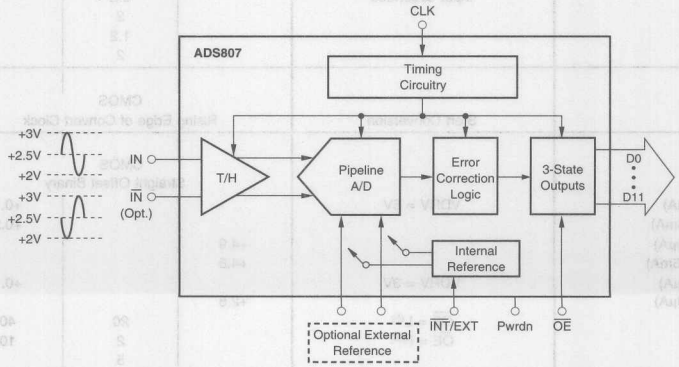
## DESCRIPTION

The ADS807 is a high-speed, high dynamic range, 12-bit pipelined analog-to-digital converter. This converter includes a high-bandwidth track/hold that gives excellent spurious performance up to and beyond the Nyquist rate. The differential nature of this track/hold and A/D circuitry minimizes third-order harmonics and give excellent common-mode noise immunity.

The ADS807 provides for setting the full-scale range of the converter without any external bandgap reference circuitry. There is an option to disable the internal reference, thereby allowing low-drive external references to be used. This feature can be important in multichannel applications such as ultrasound medical imaging where the gain and offset matching of each converter is important.

The ADS807 also provides an overrange indicator flag to indicate an input range that exceeds the full-scale input range of the converter. This flag can be used to reduce the gain of the front end gain-ranging circuitry. There is also an output enable pin to allow for testability on a PC board.

The ADS807 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for communications, medical imaging, video and test instrumentation applications. The ADS807 is available in a 28-lead SSOP package.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

## SPECIFICATIONS—PRELIMINARY

At $T_A$ = full specified temperature range, $V_S$ = +5V, differential input range = 2V to 3V for each input, sampling rate = 53MHz, unless otherwise noted.

| PARAMETER | CONDITIONS | ADS807E MIN | ADS807E TYP | ADS807E MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | 12 Guaranteed | | Bits |
| Specified Temperature Range | Ambient Air | –40 | | +85 | °C |
| **ANALOG INPUT** | | | | | |
| Full Scale Input Range (Differential) | 2Vp-p, INT or EXT Ref | 2 | | 3 | V |
| Full Scale Input Range (Single-Ended) | 2Vp-p, INT or EXT Ref | 1.5 | | 3.5 | V |
| Optional Full Scale Input Range (Differential) | 3Vp-p, External Ref | 1.75 | | 3.25 | V |
| Optional Full Scale Input Range (Single-Ended) | 3Vp-p, External Ref | 1 | | 4 | V |
| Analog Input Bias Current | | | 1 | | µA |
| Analog Input Bandwidth | | | 270 | | MHz |
| Input Impedance | | | 1.25 ll 10 | | MΩ ll pF |
| **CONVERSION CHARACTERISTICS** | | | | | |
| Sample Rate | | 10k | | 53M | Samples/s |
| Data Latency | | | 5 | | Clock Cycles |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Differential Linearity Error (largest code error) | | | | | |
| f = 1MHz | | | ±0.5 | ±1.0 | LSB |
| f = 10MHz | | | ±0.5 | ±1.0 | LSB |
| No Missing Codes | | | Guaranteed | | |
| Integral Nonlinearity Error, f = 1MHz | | | ±0.5 | ±2.0 | LSBs |
| Spurious Free Dynamic Range[1] | | | | | |
| f = 1MHz (–1dB input) | | | 85 | | dBFS[2] |
| f = 10MHz (–1dB input) | | | 82 | | dBFS |
| f = 20MHz (–1dB input) | | | 80 | | dBFS |
| f = 40MHz (undersampling) | | | 76 | | dBFS |
| f = 1MHz to 10MHz, $f_S$ = 40MHz | 2Vp-p, Single-Ended Input | 63 | 69 | | dBFS |
| Two-Tone Intermodulation Distortion[3] | | | | | |
| f = 4.5MHz and 5.5MHz (–7dB each tone) | | | 77 | | dBc |
| Signal-to-Noise Ratio (SNR) | | | | | |
| f = 1MHz (–1dB input) | 2Vp-p | | 67.5 | | dB |
| f = 10MHz (–1dB input) | 2Vp-p | | 67.5 | | dB |
| f = 20MHz (–dB input) | 2Vp-p | | 67.3 | | dB |
| f = 40MHz (undersampling) | 2Vp-p | | 67 | | dB |
| f = 1MHz to 10MHz, $f_S$ = 40MHz | 2Vp-p | 63 | 67.5 | | dB |
| f = 1MHz to 10MHz, $f_S$ = 40MHz | 2Vp-p, Single-Ended Input | 63 | 67 | | dB |
| f = 1MHz (–1dB input) | 3Vp-p | | 69 | | dB |
| f = 10MHz (–1dB input) | 3Vp-p | | 69 | | dB |
| Signal-to-(Noise + Distortion) (SINAD)[4] | | | | | |
| f = 1MHz (–1dBFS input) | 2Vp-p | | 67 | | dB |
| f = 10MHz (–1dBFS input) | 2Vp-p | | 67 | | dB |
| f = 20MHz (–1dBFS input) | 2Vp-p | | 67 | | dB |
| f = 1MHz to 10MHz, $f_S$ = 40MHz | 2Vp-p | 63 | 67 | | dB |
| f = 1MHz to 10MHz, $f_S$ = 40MHz | 2Vp-p, Single-Ended Input | 60 | 64 | | dB |
| f = 1MHz (–1dBFS input) | 3Vp-p | | 68.5 | | dB |
| f = 10MHz (–dBFS Input) | 3Vp-p | | 68.5 | | dB |
| Output Noise | Input Grounded | | 0.2 | | LSBs rms |
| Aperture Delay Time | | | 2 | | ns |
| Aperture Jitter | | | 1.2 | | ps rms |
| Overvoltage Recovery Time | | | 2 | | ns |
| **DIGITAL INPUT** | | | | | |
| Logic Family | | | CMOS | | |
| Convert Command | Start Conversion | | Rising Edge of Convert Clock | | |
| **DIGITAL OUTPUTS** | | | | | |
| Logic Family | | | CMOS | | |
| Logic Coding | | | Straight Offset Binary | | |
| Low Output Voltage ($I_{OL}$ = 50µA) | VDRV = 5V | | | +0.1 | V |
| Low Output Voltage, ($I_{OL}$ = 1.6mA) | | | | +0.2 | V |
| High Output Voltage, ($I_{OH}$ = 50µA) | | +4.9 | | | V |
| High Output Voltage, ($I_{OH}$ = 0.5mA) | | +4.8 | | | V |
| Low Output Voltage, ($I_{OL}$ = 50µA) | VDRV = 3V | | | +0.1 | V |
| High Output Voltage, ($I_{OH}$ = 50µA) | | +2.8 | | | V |
| 3-State Enable Time | $\overline{OE}$ = L[5] | | 20 | 40 | ns |
| 3-State Disable Time | $\overline{OE}$ = H[5] | | 2 | 10 | ns |
| Output Capacitance | | | 5 | | pF |

## SPECIFICATIONS—PRELIMINARY (CONT)

At $T_A$ = full specified temperature range, $V_S$ = +5V, differential input range = 2V to 3V for each input, sampling rate = 53MHz, unless otherwise noted.

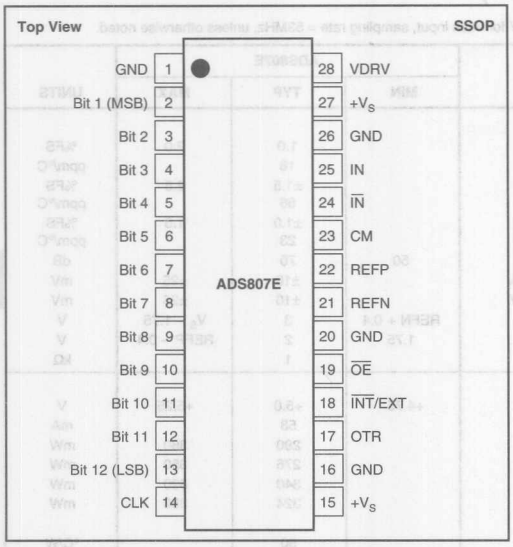
| PARAMETER | CONDITIONS | ADS807E MIN | ADS807E TYP | ADS807E MAX | UNITS |
|---|---|---|---|---|---|
| **ACCURACY (Internal Reference, 2Vp-p, Unless Otherwise Noted)** | | | | | |
| Zero Error (Referred to –FS) | at 25°C | | 1.0 | 2.0 | %FS |
| Zero Error Drift (Referred to –FS) | | | 16 | | ppm/°C |
| Gain Error[6] | at 25°C | | ±1.5 | 2.5 | %FS |
| Gain Error Drift[6] | | | 66 | | ppm/°C |
| Gain Error[7] | at 25°C | | ±1.0 | 1.5 | %FS |
| Gain Error Drift[7] | | | 23 | | ppm/°C |
| Power Supply Rejection of Gain | $\Delta V_S$ = ±5% | 50 | 70 | | dB |
| REFT Tolerance | Deviation from Ideal 3.3V | | ±10 | ±25 | mV |
| REFB Tolerance | Deviation From Ideal 2V | | ±10 | ±25 | mV |
| External REFP Voltage Range | | REFN + 0.4 | 3 | $V_S$ – 1.75 | V |
| External REFN Voltage Range | | 1.75 | 2 | REFP – 0.4 | V |
| Reference Input Resistance | | | 1 | | kΩ |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Supply Voltage: $+V_S$ | Operating | +4.75 | +5.0 | +5.25 | V |
| Supply Current: $+I_S$ | Operating | | 58 | | mA |
| Power Dissipation: VDRV = 5V | External Reference | | 290 | 360 | mW |
| VDRV = 3V | External Reference | | 276 | 350 | mW |
| VDRV = 5V | Internal Reference | | 340 | 390 | mW |
| VDRV = 3V | Internal Reference | | 324 | 380 | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| 28-Lead SSOP | | | 50 | | °C/W |

NOTES: (1) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to Full Scale. (3) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (4) Effective number of bits (ENOB) is defined by (SINAD – 1.76)/6.02. (5) A 50kΩ pull-down resistor is inserted internally on $\overline{OE}$ pin. (6) Includes internal reference. (7) Excludes internal reference.



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## PIN CONFIGURATION




## PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | GND | Ground |
| 2 | Bit 1 | Data Bit 1 (MSB) |
| 3 | Bit 2 | Data Bit 2 |
| 4 | Bit 3 | Data Bit 3 |
| 5 | Bit 4 | Data Bit 4 |
| 6 | Bit 5 | Data Bit 5 |
| 7 | Bit 6 | Data Bit 6 |
| 8 | Bit 7 | Data Bit 7 |
| 9 | Bit 8 | Data Bit 8 |
| 10 | Bit 9 | Data Bit 9 |
| 11 | Bit 10 | Data Bit 10 |
| 12 | Bit 11 | Data Bit 11 |
| 13 | Bit 12 | Data Bit 12 (LSB) |
| 14 | CLK | Convert Clock |
| 15 | $+V_S$ | +5V Supply |
| 16 | GND | Ground |
| 17 | OTR | Out of Range Indicator |
| 18 | INT/EXT | Reference Select: HI = External<br>LO = Internal or Floating |
| 19 | OE | Output Enable |
| 20 | GND | Ground |
| 21 | REFN | Bottom Reference/Bypass |
| 22 | REFP | Top Reference/Bypass |
| 23 | CM | Common-Mode Voltage Output |
| 24 | IN | Complementary Analog Input |
| 25 | IN | Analog Input |
| 26 | GND | Ground |
| 27 | $+V_S$ | +5V Supply |
| 28 | VDRV | Logic Driver Supply Voltage |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Analog Input | (–0.3V) to ($+V_S$ + 0.3V) |
| Logic Input | (–0.3V) to ($+V_S$ + 0.3V) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +150°C |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS807E | 28-Lead SSOP | 324 | –40°C to +85°C |

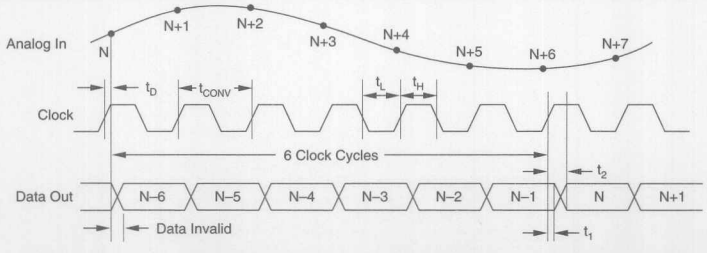
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 18.87 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 9.4 | $t_{CONV}/2$ | | ns |
| $t_H$ | Clock Pulse High | 9.4 | $t_{CONV}/2$ | | ns |
| $t_D$ | Aperture Delay | | 2 | | ns |
| $t_1$(1) | Data Hold Time, $C_L$ = 0pF | 2.7 | | | ns |
| $t_2$(1) | New Data Delay Time, $C_L$ = 15pF max | | | 12 | ns |

NOTE: (1) $t_1$ and $t_2$ times are valid for VDRV voltages of +2.7V to +5V.

BURR-BROWN®




# ADS820

www.burr-brown.com/databook/ADS820.html

## SpeedPlus™ 10-Bit, 20MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- NO MISSING CODES
- INTERNAL REFERENCE
- LOW DIFFERENTIAL LINEARITY ERROR: 0.2LSB
- LOW POWER: 195mW
- HIGH SNR: 60dB
- WIDEBAND TRACK/HOLD: 65MHz
- PACKAGES: 28-Lead SOIC and 28-Lead SSOP

## APPLICATIONS

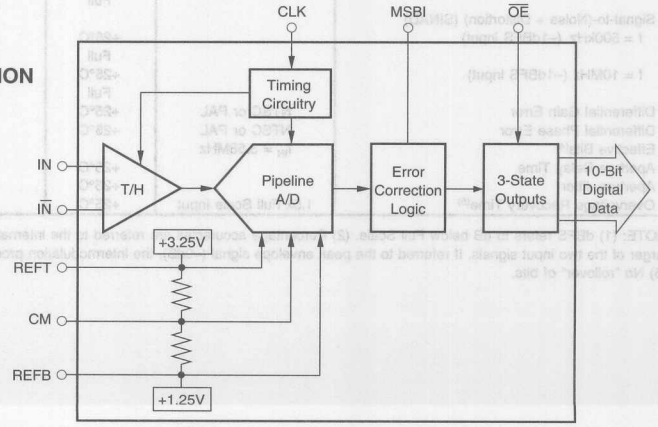
- SET-TOP BOXES
- CABLE MODEMS
- VIDEO DIGITIZING
- CCD IMAGING
  - Camcorders
  - Copiers
  - Scanners
  - Security Cameras
- IF AND BASEBAND DIGITIZATION

## DESCRIPTION

The ADS820 is a low power, monolithic 10-bit, 20MHz analog-to-digital converter utilizing a small geometry CMOS process. This COMPLETE converter includes a 10-bit quantizer with internal track/hold, reference, and a power down feature. It operates from a single +5V power supply and can be configured to accept either differential or single-ended input signals.

The ADS820 employs digital error correction to provide excellent Nyquist differential linearity performance for demanding imaging applications. Its low distortion, high SNR and high oversampling capability give it the extra margin needed for telecommunications and video applications.

This high performance converter is specified for AC and DC performance at a 20MHz sampling rate. The ADS820 is available in 28-lead SOIC and SSOP packages.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = +5V, Sampling Rate = 20MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

| PARAMETER | CONDITIONS | TEMP | ADS820U, E | | | UNITS |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Resolution | | | | 10 | | Bits |
| Specified Temperature Range | $T_{AMBIENT}$ | | –40 | | +85 | °C |
| **ANALOG INPUT** | | | | | | |
| Differential Full Scale Input Range | | | +1.25 | | +3.25 | V |
| Common-Mode Voltage | | | | 2.25 | | V |
| Analog Input Bandwidth (–3dB) | | | | | | |
| Small Signal | –20dBFS(1) Input | +25°C | | 400 | | MHz |
| Full Power | 0dB Input | +25°C | | 65 | | MHz |
| Input Impedance | | | | 1.25 ll 4 | | MΩ ll pF |
| **DIGITAL INPUT** | | | | | | |
| Logic Family | | | | TTL/HCT Compatible CMOS | | |
| Convert Command | Start Conversion | | | Falling Edge | | |
| **ACCURACY(2)** | | | | | | |
| Gain Error | | +25°C | | ±0.6 | ±1.5 | % |
| | | Full | | ±1.0 | ±2.5 | % |
| Gain Tempco | | | | ±85 | | ppm/°C |
| Power Supply Rejection of Gain | Delta $+V_S$ = ±5% | +25°C | | 0.01 | 0.1 | %FSR/% |
| Input Offset Error | | Full | | ±2.1 | ±3.0 | % |
| Power Supply Rejection of Offset | Delta $+V_S$ = ±5% | +25°C | | 0.02 | 0.1 | %FSR/% |
| **CONVERSION CHARACTERISTICS** | | | | | | |
| Sample Rate | | | 10k | | 20M | Sample/s |
| Data Latency | | | | 6.5 | | Convert Cycle |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Differential Linearity Error | | | | | | |
| f = 500kHz | | +25°C | | ±0.15 | ±1.0 | LSB |
| | | Full | | ±0.15 | ±1.0 | LSB |
| f = 10MHz | | +25°C | | ±0.2 | ±1.0 | LSB |
| | | Full | | ±0.2 | ±1.0 | LSB |
| No Missing Codes | | Full | | Guaranteed | | |
| Integral Linearity Error at f = 500kHz | | Full | | ±0.5 | ±2.0 | LSB |
| Spurious-Free Dynamic Range (SFDR) | | | | | | |
| f = 500kHz (–1dBFS input) | | +25°C | 67 | 77 | | dBFS |
| | | Full | 64 | 74 | | dBFS |
| f = 10MHz (–1dBFS input) | | +25°C | 59 | 63 | | dBFS |
| | | Full | 57 | 62 | | dBFS |
| Two-Tone Intermodulation Distortion (IMD)(3) | | | | | | |
| f = 4.4MHz and 4.5MHz (referred to –1dBFS envelope) | | +25°C | | –61 | | dBc |
| | | Full | | –60 | | dBc |
| Signal-to-Noise Ratio (SNR) | | | | | | |
| f = 500kHz (–1dBFS input) | | +25°C | 58 | 60.5 | | dB |
| | | Full | 56 | 60 | | dB |
| f = 10MHz (–1dBFS input) | | +25°C | 58 | 60 | | dB |
| | | Full | 56 | 60 | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | | | | | | |
| f = 500kHz (–1dBFS input) | | +25°C | 58 | 60.5 | | dB |
| | | Full | 55 | 60 | | dB |
| f = 10MHz (–1dBFS input) | | +25°C | 56 | 58 | | dB |
| | | Full | 54 | 57 | | dB |
| Differential Gain Error | NTSC or PAL | +25°C | | 0.5 | | % |
| Differential Phase Error | NTSC or PAL | +25°C | | 0.1 | | degrees |
| Effective Bits(4) | $f_{IN}$ = 3.58MHz | | | 9.5 | | Bits |
| Aperture Delay Time | | +25°C | | 2 | | ns |
| Aperture Jitter | | +25°C | | 7 | | ps rms |
| Overvoltage Recovery Time(5) | 1.5x Full Scale Input | +25°C | | 2 | | ns |

NOTE: (1) dBFS refers to dB below Full Scale. (2) Percentage accuracies are referred to the internal A/D Full Scale Range of 4Vp-p. (3) IMD is referred to the larger of the two input signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 7dB lower. (4) Based on (SINAD – 1.76)/6.02. (5) No "rollover" of bits.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## SPECIFICATIONS (CONT)

At $T_A$ = +25°C, $V_S$ = +5V, Sampling Rate = 20MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

| PARAMETER | CONDITIONS | TEMP | ADS820U, E MIN | ADS820U, E TYP | ADS820U, E MAX | UNITS |
|---|---|---|---|---|---|---|
| **OUTPUTS** | | | | | | |
| Logic Family | | | | TTL/HCT Compatible CMOS | | |
| Logic Coding | Logic Selectable | | | SOB or BTC | | V |
| Logic Levels | Logic "LO", $C_L$ = 15pF | Full | 0 | | 0.4 | V |
| | Logic "HI", $C_L$ = 15pF | Full | 2.5 | | $+V_S$ | V |
| 3-State Enable Time | | | | 20 | 40 | ns |
| 3-State Disable Time | | Full | | 2 | 10 | ns |
| **POWER SUPPLY REQUIREMENTS** | | | | | | |
| Supply Voltage: $+V_S$ | Operating | Full | +4.75 | +5 | +5.25 | V |
| Supply Current: $+I_S$ | Operating | +25°C | | 39 | 47 | mA |
| | Operating | Full | | 40 | 55 | mA |
| Power Consumption | Operating | +25°C | | 195 | 235 | mW |
| | Operating | Full | | 200 | 275 | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | | |
| 28-Lead SOIC | | | | 75 | | °C/W |
| 28-Lead SSOP | | | | 50 | | °C/W |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Analog Input | 0V to ($+V_S$ + 300mV) |
| Logic Input | 0V to ($+V_S$ + 300mV) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +125°C |
| External Top Reference Voltage (REFT) | +3.4V Max |
| External Bottom Reference Voltage (REFB) | +1.1V Min |

NOTE: Stresses above these ratings may permanently damage the device.

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS820U | 28-Lead SOIC | 217 | –40°C to +85°C |
| ADS820E | 28-Lead SSOP | 324 | –40°C to +85°C |

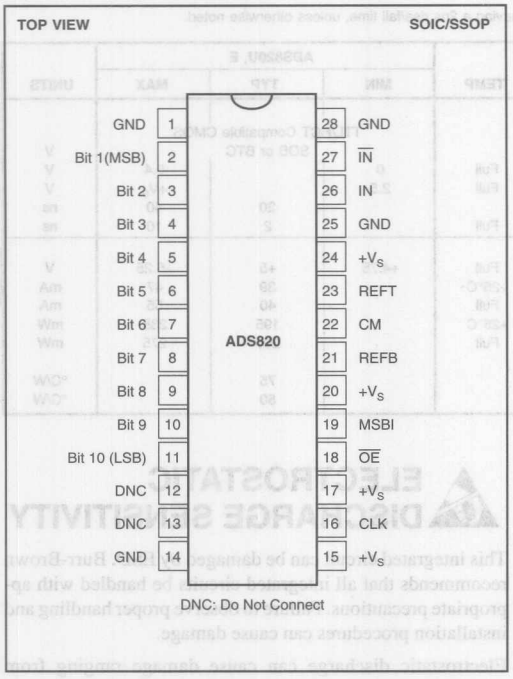
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

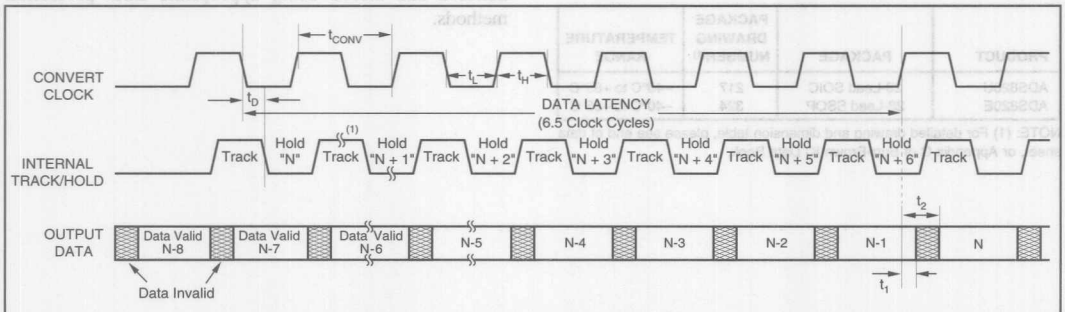
## PIN CONFIGURATION




## PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | GND | Ground |
| 2 | B1 | Bit 1, Most Significant Bit |
| 3 | B2 | Bit 2 |
| 4 | B3 | Bit 3 |
| 5 | B4 | Bit 4 |
| 6 | B5 | Bit 5 |
| 7 | B6 | Bit 6 |
| 8 | B7 | Bit 7 |
| 9 | B8 | Bit 8 |
| 10 | B9 | Bit 9 |
| 11 | B10 | Bit 10, Least Significant Bit |
| 12 | DNC | Do not connect. |
| 13 | DNC | Do not connect. |
| 14 | GND | Ground |
| 15 | $+V_S$ | +5V Power Supply |
| 16 | CLK | Convert Clock Input, 50% Duty Cycle |
| 17 | $+V_S$ | +5V Power Supply |
| 18 | $\overline{OE}$ | HI: High Impedance State. LO or Floating: Normal Operation. Internal pull-down resistor. |
| 19 | MSBI | Most Significant Bit Inversion, HI: MSB inverted for complementary output. LO or Floating: Straight output. Internal pull-down resistor. |
| 20 | $+V_S$ | +5V Power Supply |
| 21 | REFB | Bottom Reference Bypass. For external bypassing of internal +1.25V reference. |
| 22 | CM | Common-Mode Voltage. It is derived by (REFT + REFB)/2. |
| 23 | REFT | Top Reference Bypass. For external bypassing of internal +3.25V reference. |
| 24 | $+V_S$ | +5V Power Supply |
| 25 | GND | Ground |
| 26 | IN | Input |
| 27 | $\overline{IN}$ | Complementary Input |
| 28 | GND | Ground |

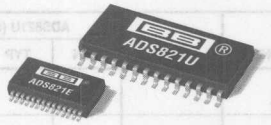
## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 50 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 24 | 25 | | ns |
| $t_H$ | Clock Pulse High | 24 | 25 | | ns |
| $t_D$ | Aperture Delay | | 2 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12.5 | ns |

NOTE: (1) " § " indicates the portion of the waveform that will stretch out at slower sample rates.

BURR-BROWN®




# ADS821

www.burr-brown.com/databook/ADS821.html

## SpeedPLUS™ 10-Bit, 40MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- NO MISSING CODES
- INTERNAL REFERENCE
- LOW POWER: 380mW
- HIGH SNR: 58dB
- INTERNAL TRACK/HOLD
- PACKAGE: 28-Lead SOIC and SSOP

## APPLICATIONS

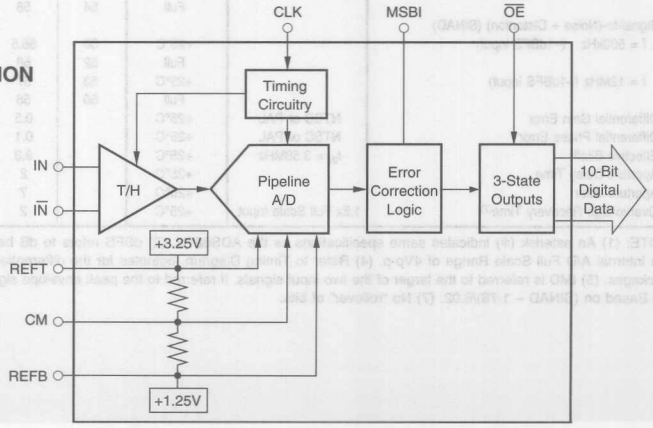
- VIDEO DIGITIZING
- ULTRASOUND IMAGING
- GAMMA CAMERAS
- SET-TOP BOXES
- CABLE MODEMS
- CCD IMAGING
  - Color Copiers
  - Scanners
  - Camcorders
  - Security Cameras
  - Fax Machines
- IF AND BASEBAND DIGITIZATION
- TEST INSTRUMENTATION

## DESCRIPTION

The ADS821 is a low power, monolithic 10-bit, 40MHz analog-to-digital converter utilizing a small geometry CMOS process. This COMPLETE converter includes a 10-bit quantizer with internal track/hold, reference, and a power down feature. It operates from a single +5V power supply and can be configured to accept either differential or single-ended input signals.

The ADS821 employs digital error correction to provide excellent Nyquist differential linearity performance for demanding imaging applications. Its low distortion, high SNR and high oversampling capability give it the extra margin needed for telecommunications and video applications.

This high performance converter is specified for AC and DC performance at a 40MHz sampling rate. The ADS821 is available in 28-lead SOIC and SSOP packages.




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# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

| PARAMETER | CONDITIONS | TEMP | ADS821U (SOIC) MIN | ADS821U (SOIC) TYP | ADS821U (SOIC) MAX | ADS821E (SSOP) MIN | ADS821E (SSOP) TYP | ADS821E (SSOP) MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Resolution | | | | 10 | | | * | | Bits |
| Specified Temperature Range | $T_{AMBIENT}$ | | –40 | | +85 | *(1) | | * | °C |
| **ANALOG INPUT** | | | | | | | | | |
| Differential Full Scale Input Range | | | +1.25 | | +3.25 | * | | * | V |
| Common-Mode Voltage | | | | +2.25 | | | * | | V |
| Analog Input Bandwidth (–3dB) | | | | | | | | | |
| Small Signal | –20dBFS(2) Input | +25°C | | 400 | | | * | | MHz |
| Full Power | 0dBFS Input | +25°C | | 65 | | | * | | MHz |
| Input Impedance | | | | 1.25 ll 4 | | | * | | MΩ ll pF |
| **DIGITAL INPUT** | | | | | | | | | |
| Logic Family | | | | TTL/HCT Compatible CMOS | | | TTL/HCT Compatible CMOS | | |
| Convert Command | Start Conversion | | | Falling Edge | | | Falling Edge | | |
| **ACCURACY(3)** | | | | | | | | | |
| Gain Error | | +25°C | | ±0.6 | ±1.5 | | * | * | % |
| | | Full | | ±1.1 | ±2.5 | | * | * | % |
| Gain Drift | | | | ±85 | | | * | | ppm/°C |
| Power Supply Rejection of Gain | Delta $+V_S$ = ±5% | +25°C | | 0.01 | 0.15 | | * | * | %FSR/% |
| Input Offset Error | | Full | | ±2.1 | ±3.5 | | * | * | % |
| Power Supply Rejection of Offset | Delta $+V_S$ = ±5% | +25°C | | 0.02 | 0.15 | | * | * | %FSR/% |
| **CONVERSION CHARACTERISTICS** | | | | | | | | | |
| Sample Rate | | | 10k | | 40M | * | | * | Sample/s |
| Data Latency | | | | 6.5 | | | * | | Convert Cycle |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | | |
| Differential Linearity Error | $t_H$ = 13ns(4) | | | | | | | | |
| f = 500kHz | | +25°C | | ±0.5 | ±1.0 | | * | * | LSB |
| | | 0°C to +70°C | | ±0.6 | ±1.0 | | * | * | LSB |
| f = 12MHz | | +25°C | | ±0.5 | ±1.0 | | * | * | LSB |
| | | 0°C to +70°C | | ±0.6 | ±1.0 | | * | * | LSB |
| No Missing Codes | | 0°C to +70°C | | Guaranteed | | | * | | |
| Integral Linearity Error at f = 500kHz | | 0°C to +70°C | | ±0.5 | ±2.0 | | * | * | LSB |
| Spurious-Free Dynamic Range (SFDR) | | | | | | | | | |
| f = 500kHz (–1dBFS input) | | +25°C | 60 | 70 | | * | * | | dBFS |
| | | Full | 54 | 67 | | * | * | | dBFS |
| f = 12MHz (–1dBFS input) | | +25°C | 58 | 63 | | * | * | | dBFS |
| | | Full | 54 | 62 | | * | * | | dBFS |
| Two-Tone Intermodulation Distortion (IMD)(5) | | | | | | | | | |
| f = 4.4MHz and 4.5MHz (–7dBFS each tone) | | +25°C | | –61 | | | * | | dBc |
| | | Full | | –60 | | | * | | dBc |
| Signal-to-Noise Ratio (SNR) | | | | | | | | | |
| f = 500kHz (–1dBFS input) | | +25°C | 57 | 59 | | 55 | * | | dB |
| | | Full | 55 | 59 | | 53 | * | | dB |
| f = 12MHz (–1dBFS input) | | +25°C | 56 | 58 | | 54 | * | | dB |
| | | Full | 54 | 58 | | 52 | * | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | | | | | | | | | |
| f = 500kHz (–1dBFS input) | | +25°C | 56 | 58.5 | | * | * | | dB |
| | | Full | 52 | 58 | | * | * | | dB |
| f = 12MHz (–1dBFS input) | | +25°C | 53 | 57 | | * | * | | dB |
| | | Full | 50 | 56 | | * | * | | dB |
| Differential Gain Error | NTSC or PAL | +25°C | | 0.5 | | | * | | % |
| Differential Phase Error | NTSC or PAL | +25°C | | 0.1 | | | * | | degrees |
| Effective Bits(6) | $f_{IN}$ = 3.58MHz | +25°C | | 9.3 | | | * | | Bits |
| Aperture Delay Time | | +25°C | | 2 | | | * | | ns |
| Aperture Jitter | | +25°C | | 7 | | | * | | ps rms |
| Overvoltage Recovery Time(7) | 1.5x Full Scale Input | +25°C | | 2 | | | * | | ns |

NOTE: (1) An asterisk (*) indicates same specifications as the ADS821U. (2) dBFS refers to dB below Full Scale. (3) Percentage accuracies are referred to the internal A/D Full Scale Range of 4Vp-p. (4) Refer to Timing Diagram footnotes for the differential linearity performance conditions for the SOIC and SSOP packages. (5) IMD is referred to the larger of the two input signals. If referred to the peak envelope signal (≈0dB), the intermodulation products will be 7dB lower. (6) Based on (SINAD – 1.76)/6.02. (7) No "rollover" of bits.

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## SPECIFICATIONS (CONT)

At $T_A$ = +25°C, $V_S$ = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

| PARAMETER | CONDITIONS | TEMP | ADS821U (SOIC) MIN | ADS821U (SOIC) TYP | ADS821U (SOIC) MAX | ADS821E (SSOP) MIN | ADS821E (SSOP) TYP | ADS821E (SSOP) MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| **OUTPUTS** | | | | | | | | | |
| Logic Family | | | | TTL/HCT Compatible CMOS | | | TTL/HCT Compatible CMOS | | |
| Logic Coding | | | | SOB or BTC | | | SOB or BTC | | |
| Logic Levels | Logic Selectable | | | | | | | | |
| | Logic "LO", $C_L$ = 15pF max | Full | 0 | | 0.4 | * | | * | V |
| | Logic "HI", $C_L$ = 15pF max | Full | +2.5 | | $+V_S$ | * | | * | V |
| 3-State Enable Time | | | | 20 | 40 | | * | * | ns |
| 3-State Disable Time | | Full | | 2 | 10 | | * | * | ns |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | | |
| Supply Voltage: $+V_S$ | Operating | Full | +4.75 | +5 | +5.25 | * | * | * | V |
| Supply Current: $+I_S$ | Operating | +25°C | | 76 | 88 | | * | * | mA |
| | Operating | Full | | 78 | 90 | | * | * | mA |
| Power Consumption | Operating | +25°C | | 380 | 440 | | * | * | mW |
| | Operating | Full | | 390 | 450 | | * | * | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | 75 | | | 50 | | °C/W |

* Specifications same as ADS821U.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Analog Input | 0V to ($+V_S$ + 300mV) |
| Logic Input | 0V to ($+V_S$ + 300mV) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +125°C |
| External Top Reference Voltage (REFT) | +3.4V max |
| External Bottom Reference Voltage (REFB) | +1.1V min |

NOTE: Stresses above these ratings may permanently damage the device.

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS821U | 28-Lead SOIC | 217 | –40°C to +85°C |
| ADS821E | 28-Lead SSOP | 324 | –40°C to +85°C |

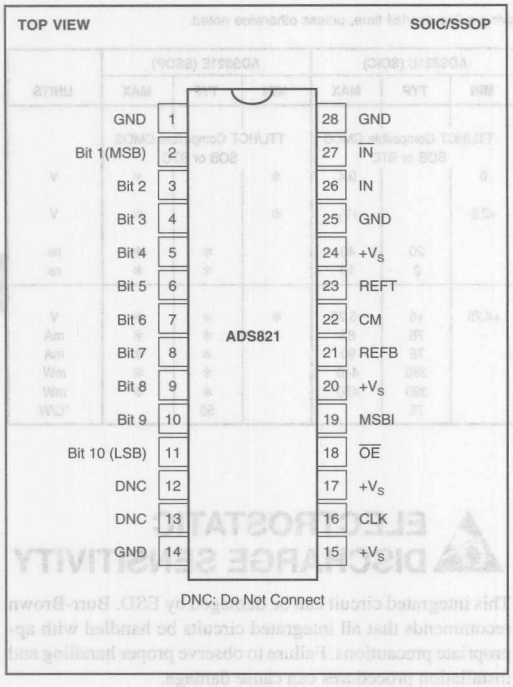
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

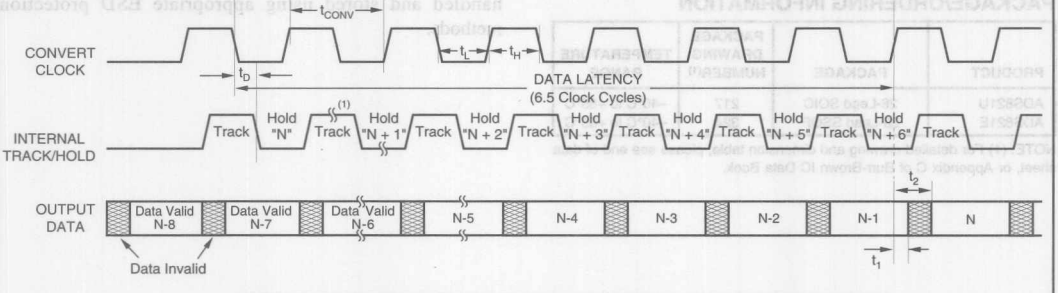
## PIN CONFIGURATION




## PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | GND | Ground |
| 2 | B1 | Bit 1, Most Significant Bit |
| 3 | B2 | Bit 2 |
| 4 | B3 | Bit 3 |
| 5 | B4 | Bit 4 |
| 6 | B5 | Bit 5 |
| 7 | B6 | Bit 6 |
| 8 | B7 | Bit 7 |
| 9 | B8 | Bit 8 |
| 10 | B9 | Bit 9 |
| 11 | B10 | Bit 10, Least Significant Bit |
| 12 | DNC | Do not connect. |
| 13 | DNC | Do not connect. |
| 14 | GND | Ground |
| 15 | $+V_S$ | +5V Power Supply |
| 16 | CLK | Convert Clock Input, 50% Duty Cycle |
| 17 | $+V_S$ | +5V Power Supply |
| 18 | $\overline{OE}$ | HI: High Impedance State. LO or Floating: Normal Operation. Internal pull-down resistor. |
| 19 | MSBI | Most Significant Bit Inversion, HI: MSB inverted for complementary output. LO or Floating: Straight output. Internal pull-down resistor. |
| 20 | $+V_S$ | +5V Power Supply |
| 21 | REFB | Bottom Reference Bypass. For external bypassing of internal +1.25V reference. |
| 22 | CM | Common-Mode Voltage. It is derived by (REFT + REFB)/2. |
| 23 | REFT | Top Reference Bypass. For external bypassing of internal +3.25V reference. |
| 24 | $+V_S$ | +5V Power Supply |
| 25 | GND | Ground |
| 26 | IN | Input |
| 27 | $\overline{IN}$ | Complementary Input |
| 28 | GND | Ground |

## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 25 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 12 | 12.5 | | ns |
| $t_H$ | Clock Pulse High | 12(2) | 12.5 | | ns |
| $t_D$ | Aperture Delay | | 2 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12.5 | ns |

NOTE: (1) "§" indicates the portion of the waveform that will stretch out at slower sample rates. (2) $t_H$ must be 13ns minimum if no missing codes is desired only for the conditions of $t_{CONV}$ ≤28ns and $f_{IN}$ <2MHz for the SOIC package. For best performance in the SSOP package, $t_H$ must be 13ns minimum for all input frequencies and $t_{CONV}$ ≤28ns. Refer to the Clock Requirements for a possible clock skew circuit for this condition.

BURR-BROWN®




# ADS822

www.burr-brown.com/databook/ADS822.html

## SpeedPLUS™ 10-Bit, 40MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- HIGH SNR: 60dB
- HIGH SFDR: 72dBFS
- LOW POWER: 190mW
- INTERNAL/EXTERNAL REFERENCE OPTION
- SINGLE-ENDED OR FULLY DIFFERENTIAL ANALOG INPUT
- PROGRAMMABLE INPUT RANGE
- LOW DNL: 0.5LSB
- SINGLE +5V SUPPLY OPERATION
- +3V DIGITAL OUTPUT CAPABILITY
- POWER DOWN: 20mW
- 28-LEAD SSOP PACKAGE

## APPLICATIONS

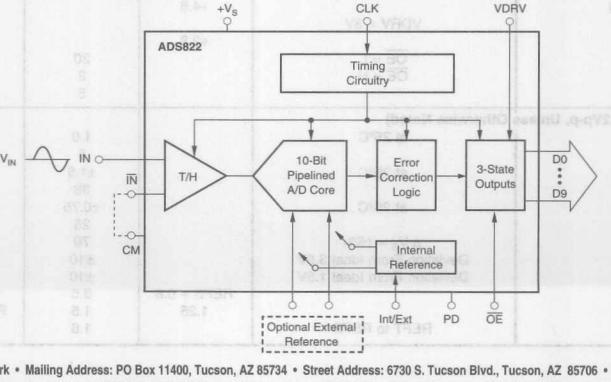
- MEDICAL IMAGING
- TEST EQUIPMENT
- COMPUTER SCANNERS
- COMMUNICATIONS
- VIDEO DIGITIZING

## DESCRIPTION

The ADS822 is a pipeline, CMOS analog-to-digital converter that operates from a single +5V power supply. This converter provides excellent performance with a single-ended input and can be operated with a differential input for added spurious performance. This high performance converter includes a 10-bit quantizer, high bandwidth track/hold. And a high accuracy internal reference. It also allows for the user to disable the internal reference and utilize external references. This external reference option provides excellent gain and offset matching when used in multi-channel applications or in applications where full scale range adjustment is required.

The ADS822 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for medical imaging, communications, video, test instrumentation. The ADS822 offers power dissipation of 190mW and also provides a power down mode, thus reducing power dissipation to only 20mW.

The ADS822 is specified at a maximum sampling frequency of 40MHz and a single-ended input range of 1.5V to 3.5V. The ADS822 is available in a 28-lead SSOP package and is pin-for-pin compatible with the 10-bit, 60MHz ADS823 and the 10-bit, 70MHz ADS824, providing an upgrade path to higher sampling frequencies.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = full specified temperature range, $V_S$ = +5V, single-ended input range = 1.5V to 3.5V, and sampling rate = 40MHz, external reference, unless otherwise noted.

| PARAMETER | CONDITIONS | ADS822E MIN | ADS822E TYP | ADS822E MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | 10 Guaranteed | | Bits |
| **SPECIFIED TEMPERATURE RANGE** | Ambient Air | | –40 to +85 | | °C |
| **ANALOG INPUT** | | | | | |
| Standard Single-Ended Input Range | 2Vp-p | 1.5 | | 3.5 | V |
| Optional Single-Ended Input Range | 1Vp-p | 2 | | 3 | V |
| Common-Mode Range | | | 2.5 | | V |
| Optional Differential Input Range | 2Vp-p | 2 | | 3 | V |
| Analog Input Bias Current | | | 1 | | µA |
| Input Impedance | | | 1.25 ll 10 | | MΩ ll pF |
| Track-Mode Input Bandwidth | –3dBFS Input | | 300 | | MHz |
| **CONVERSION CHARACTERISTICS** | | | | | |
| Sample Rate | | 10k | | 40M | Samples/s |
| Data Latency | | | 5 | | Clk Cyc |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Differential Linearity Error (largest code error) | | | | | |
| f = 1MHz | | | ±0.25 | ±1.0 | LSB |
| f = 10MHz | | | ±0.5 | | LSB |
| No Missing Codes | | | Guaranteed | | |
| Integral Nonlinearity Error, f = 1MHz | | | ±0.5 | ±2.0 | LSBs |
| Spurious Free Dynamic Range[1] | Referred to Full Scale | | | | |
| f = 1MHz | | | 72 | | dBFS[2] |
| f = 10MHz | | 63 | 66 | | dBFS |
| Two-Tone Intermodulation Distortion[3] | | | | | |
| f = 9.5MHz and 9.9MHz (–7dB each tone) | | | –67 | | dBc |
| Signal-to-Noise Ratio (SNR) | Referred to Full Scale | | | | |
| f = 1MHz | | | 60 | | dB |
| f = 10MHz | | 57 | 60 | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | Referred to Full Scale | | | | |
| f = 1MHz | | | 59 | | dB |
| f = 10MHz | | 56 | 58 | | dB |
| Effective Number of Bits[4], f = 1MHz | | | 9.5 | | Bits |
| Output Noise | Input Tied to Common-Mode | | 0.2 | | LSBs rms |
| Aperture Delay Time | | | 3 | | ns |
| Aperture Jitter | | | 1.2 | | ps rms |
| Overvoltage Recovery Time | | | 2 | | ns |
| Full-Scale Step Acquisition Time | | | 5 | | ns |
| **DIGITAL INPUTS** | | | | | |
| Logic Family | | | CMOS Compatible | | |
| Convert Command | Start Conversion | | Rising Edge of Convert Clock | | |
| High Level Input Current[5] ($V_{IN}$ = $5V_{DD}$) | | | | 100 | µA |
| Low Level Input Current ($V_{IN}$ = 0V) | | | | 10 | µA |
| High Level Input Voltage | | +3.5 | | | V |
| Low Level Input Voltage | | | | +1.0 | V |
| Input Capacitance | | | 5 | | pF |
| **DIGITAL OUTPUTS** | | | | | |
| Logic Family | | | CMOS Compatible | | |
| Logic Coding | | | Straight Offset Binary | | |
| Low Output Voltage ($I_{OL}$ = 50µA) | VDRV = 5V | | | +0.1 | V |
| Low Output Voltage, ($I_{OL}$ = 1.6mA) | | | | +0.2 | V |
| High Output Voltage, ($I_{OH}$ = 50µA) | | +4.9 | | | V |
| High Output Voltage, ($I_{OH}$ = 0.5mA) | | +4.8 | | | V |
| Low Output Voltage, ($I_{OL}$ = 50µA) | VDRV = 3V | | | +0.1 | V |
| High Output Voltage, ($I_{OH}$ = 50µA) | | +2.8 | | | V |
| 3-State Enable Time | $\overline{OE}$ = L | | 20 | 40 | ns |
| 3-State Disable Time | $\overline{OE}$ = H | | 2 | 10 | ns |
| Output Capacitance | | | 5 | | pF |
| **ACCURACY (Internal Reference, 2Vp-p, Unless Otherwise Noted)** | | | | | |
| Zero Error (Referred to –FS) | at 25°C | | 1.0 | 3.0 | %FS |
| Zero Error Drift (Referred to –FS) | | | 5 | | ppm/°C |
| Gain Error[6] | at 25°C | | ±1.5 | ±2.5 | %FS |
| Gain Error Drift[6] | | | 38 | | ppm/°C |
| Gain Error[7] | at 25°C | | ±0.75 | ±1.5 | %FS |
| Gain Error Drift[7] | | | 25 | | ppm/°C |
| Power Supply Rejection of Gain | Δ $V_S$ = ±5% | | 70 | | dB |
| REFT Tolerance | Deviation From Ideal 3.5V | | ±10 | ±25 | mV |
| REFB Tolerance | Deviation From Ideal 1.5V | | ±10 | ±25 | mV |
| External REFT Voltage Range | | REFB + 0.8 | 3.5 | $V_S$ – 1.25 | V |
| External REFB Voltage Range | | 1.25 | 1.5 | REFT – 0.8 | V |
| Reference Input Resistance | REFT to REFB | | 1.6 | | kΩ |

## SPECIFICATIONS (CONT)

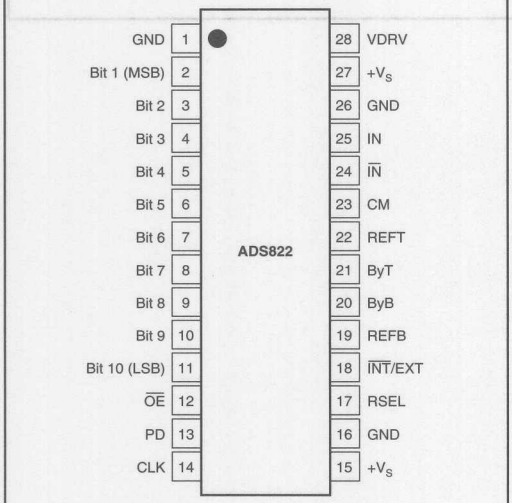
At $T_A$ = full specified temperature range, $V_S$ = +5V, single-ended input range = 1.5V to 3.5V, and sampling rate = 40MHz, external reference, unless otherwise noted.

| PARAMETER | CONDITIONS | ADS822E MIN | ADS822E TYP | ADS822E MAX | UNITS |
|---|---|---|---|---|---|
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Supply Voltage: $+V_S$ | Operating | +4.75 | +5.0 | +5.25 | V |
| Supply Current: $+I_S$ | Operating (External Reference) | | 40 | | mA |
| Power Dissipation: VDRV = 5V | External Reference | | 200 | 230 | mW |
| VDRV = 3V | External Reference | | 190 | | mW |
| VDRV = 5V | Internal Reference | | 250 | | mW |
| VDRV = 3V | Internal Reference | | 240 | | mW |
| Power Down | Operating | | 20 | | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| 28-Lead SSOP | | | 50 | | °C/W |

NOTES: (1) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to Full Scale. (3) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (4) Effective number of bits (ENOB) is defined by (SINAD – 1.76)/6.02. (5) A 50kΩ pull-down resistor is inserted internally on $\overline{OE}$ pin. (6) Includes internal reference. (7) Excludes internal reference.

### PIN CONFIGURATION

Top View SSOP




### PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | GND | Ground |
| 2 | Bit 1 | Data Bit 1 (D9) (MSB) |
| 3 | Bit 2 | Data Bit 2 (D8) |
| 4 | Bit 3 | Data Bit 3 (D7) |
| 5 | Bit 4 | Data Bit 4 (D6) |
| 6 | Bit 5 | Data Bit 5 (D5) |
| 7 | Bit 6 | Data Bit 6 (D4) |
| 8 | Bit 7 | Data Bit 7 (D3) |
| 9 | Bit 8 | Data Bit 8 (D2) |
| 10 | Bit 9 | Data Bit 9 (D1) |
| 11 | Bit 10 | Data Bit 10 (D0) (LSB) |
| 12 | $\overline{OE}$ | Output Enable: HI: High Impedance State LO or floating: Normal Operation (Internal Pull-down Resistor) |
| 13 | PD | Power Down: HI = Enable; LO = Disable |
| 14 | CLK | Convert Clock Input |
| 15 | $+V_S$ | +5V Supply |
| 16 | GND | Ground |
| 17 | RSEL | Input Range Select: HI = 2V; LO = 1V |
| 18 | $\overline{INT}$/EXT | Reference Select: HI = External, LO = Internal |
| 19 | REFB | Bottom Reference |
| 20 | ByB | Bottom Ladder Bypass |
| 21 | ByT | Top Ladder Bypass |
| 22 | REFT | Top Reference |
| 23 | CM | Common-Mode Voltage Output |
| 24 | $\overline{IN}$ | Complementary Input (–) |
| 25 | IN | Analog Input (+) |
| 26 | GND | Analog Ground |
| 27 | $+V_S$ | +5V Supply |
| 28 | VDRV | Output Logic Driver Supply Voltage |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Analog Input | –0.3V to ($+V_S$ + 0.3V) |
| Logic Input | –0.3V to ($+V_S$ + 0.3V) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +150°C |

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS822E | 28-Lead SSOP | 324 | –40°C to +85°C |

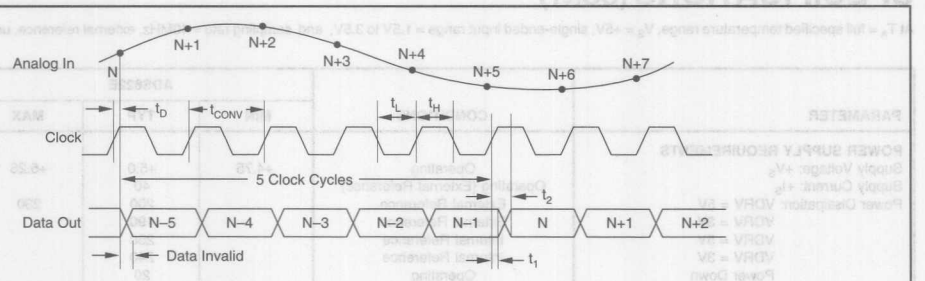
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 25 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 11.5 | 12.5 | | ns |
| $t_H$ | Clock Pulse High | 11.5 | 12.5 | | ns |
| $t_D$ | Aperture Delay | | 3 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12 | ns |

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# ADS823

www.burr-brown.com/databook/ADS823.html

## SpeedPLUS™ 10-Bit, 60MHz Sampling ANALOG-TO-DIGITAL CONVERTER



## FEATURES

- HIGH SNR: 60dB
- HIGH SFDR: 74dB
- LOW POWER: 265mW
- INTERNAL/EXTERNAL REFERENCE OPTION
- SINGLE-ENDED OR DIFFERENTIAL ANALOG INPUT
- PROGRAMMABLE INPUT RANGE
- LOW DNL: 0.25LSB
- SINGLE +5V SUPPLY OPERATION
- +3V DIGITAL OUTPUT CAPABILITY
- POWER DOWN: 20mW
- 28-LEAD SSOP PACKAGE

## APPLICATIONS

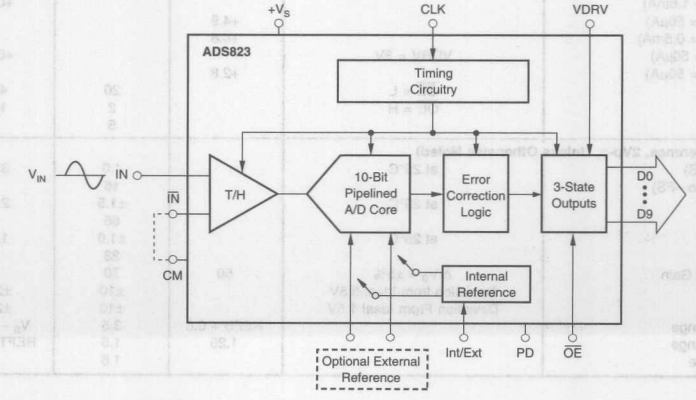
- MEDICAL IMAGING
- COMMUNICATIONS
- CCD IMAGING
- VIDEO DIGITIZING
- TEST EQUIPMENT

## DESCRIPTION

The ADS823 is a pipeline, CMOS analog-to-digital converter that operates from a single +5V power supply. This converter provides excellent performance with a single-ended input and can be operated with a differential input for added spurious performance. This high performance converter includes a 10-bit quantizer, high bandwidth track/hold, and a high accuracy internal reference. It also allows for the user to disable the internal reference and utilize external references. This external reference option provides excellent gain and offset matching when used in multi-channel applications or in applications where full scale range adjustment is required.

The ADS823 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for medical imaging, communications, video, and test instrumentation. The ADS823 offers power dissipation of 265mW and also provides a power down mode, thus reducing power dissipation to only 20mW.

The ADS823 is specified at a maximum sampling frequency of 60MHz and a single-ended input range of 1.5V to 3.5V. The ADS823 is available in a 28-lead SSOP package and is pin compatible with the 10-bit, 40MHz ADS822 and the 10-bit, 75MHz ADS824.




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# SPECIFICATIONS

At $T_A$ = full specified temperature range, single-ended input range = 1.5V to 3.5V, sampling rate = 60MHz, external reference, unless otherwise noted.

| PARAMETER | CONDITIONS | ADS823E MIN | ADS823E TYP | ADS823E MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | 10 Guaranteed | | Bits |
| **SPECIFIED TEMPERATURE RANGE** | Ambient Air | | –40 to +85 | | °C |
| **ANALOG INPUT** | | | | | |
| Standard Single-Ended Input Range | 2Vp-p | 1.5 | | 3.5 | V |
| Optional Single-Ended Input Range | 1Vp-p | 2 | | 3 | V |
| Common-Mode Voltage | | | 2.5 | | V |
| Optional Differential Input Range | 2Vp-p | 2 | | 3 | V |
| Analog Input Bias Current | | | 1 | | µA |
| Input Impedance | | | 1.25 ll 10 | | MΩ ll pF |
| Track-Mode Input Bandwidth | –3dBFS Input | | 300 | | MHz |
| **CONVERSION CHARACTERISTICS** | | | | | |
| Sample Rate | | 10k | | 60M | Samples/s |
| Data Latency | | | 5 | | Clk Cyc |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Differential Linearity Error (largest code error) | | | | | |
| f = 1MHz | | | ±0.25 | ±1.0 | LSB |
| f = 10MHz | | | ±0.25 | | LSB |
| No Missing Codes | | | Guaranteed | | |
| Integral Nonlinearity Error, f = 1MHz | | | ±0.5 | ±1.5 | LSBs |
| Spurious Free Dynamic Range[1] | | | | | |
| f = 1MHz | | | 74 | | dBFS[2] |
| f = 10MHz | | 67 | 74 | | dBFS |
| Two-Tone Intermodulation Distortion[3] | | | | | |
| f = 9.5MHz and 9.9MHz (–7dB each tone) | | | 64 | | dBc |
| Signal-to-Noise Ratio (SNR) | Referred to Full Scale Sinewave | | | | |
| f = 1MHz | | | 60 | | dB |
| f = 10MHz | | 57 | 60 | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | Referred to Full Scale Sinewave | | | | |
| f = 1MHz | | | 59 | | dB |
| f = 10MHz | | 56 | 59 | | dB |
| Effective Number of Bits[4], f = 1MHz | | | 9.5 | | Bits |
| Output Noise | Input Grounded | | 0.2 | | LSBs rms |
| Aperture Delay Time | | | 3 | | ns |
| Aperture Jitter | | | 1.2 | | ps rms |
| Overvoltage Recovery Time[4] | | | 2 | | ns |
| Full-Scale Step Acquisition Time | | | 5 | | ns |
| **DIGITAL INPUTS** | | | | | |
| Logic Family | | | CMOS Compatible | | |
| Convert Command | Start Conversion | | Rising Edge of Convert Clock | | |
| High Level Input Current[5] ($V_{IN}$ = 5V) | | | | +100 | µA |
| Low Level Input Current ($V_{IN}$ = 0V) | | | | +10 | µA |
| High Level Input Voltage | | +3.5 | | | V |
| Low Level Input Voltage | | | | +1.0 | V |
| Input Capacitance | | | 5 | | pF |
| **DIGITAL OUTPUTS** | | | | | |
| Logic Family | | | CMOS Compatible | | |
| Logic Coding | | | Straight Offset Binary | | |
| Low Output Voltage ($I_{OL}$ = 50µA) | VDRV = 5V | | | +0.1 | V |
| Low Output Voltage, ($I_{OL}$ = 1.6mA) | | | | +0.2 | V |
| High Output Voltage, ($I_{OH}$ = 50µA) | | +4.9 | | | V |
| High Output Voltage, ($I_{OH}$ = 0.5mA) | | +4.8 | | | V |
| Low Output Voltage, ($I_{OL}$ = 50µA) | VDRV = 3V | | | +0.1 | V |
| High Output Voltage, ($I_{OH}$ = 50µA) | | +2.8 | | | V |
| 3-State Enable Time | $\overline{OE}$ = L | | 20 | 40 | ns |
| 3-State Disable Time | $\overline{OE}$ = H | | 2 | 10 | ns |
| Output Capacitance | | | 5 | | pF |
| **ACCURACY (Internal Reference, 2Vp-p, Unless Otherwise Noted)** | | | | | |
| Zero Error (Referred to –FS) | at 25°C | | 1.0 | 3.0 | %FS |
| Zero Error Drift (Referred to –FS) | | | 16 | | ppm/°C |
| Gain Error[6] | at 25°C | | ±1.5 | 2.5 | %FS |
| Gain Error Drift[6] | | | 66 | | ppm/°C |
| Gain Error[7] | at 25°C | | ±1.0 | 1.5 | %FS |
| Gain Error Drift[7] | | | 23 | | ppm/°C |
| Power Supply Rejection of Gain | $\Delta V_S$ = ±5% | 50 | 70 | | dB |
| REFT Tolerance | Deviation from Ideal 3.5V | | ±10 | ±25 | mV |
| REFB Tolerance | Deviation From Ideal 1.5V | | ±10 | ±25 | mV |
| External REFT Voltage Range | | REFB + 0.8 | 3.5 | $V_S$ – 1.25 | V |
| External REFB Voltage Range | | 1.25 | 1.5 | REFT – 0.8 | V |
| Reference Input Resistance | | | 1.6 | | kΩ |

## SPECIFICATIONS (CONT)

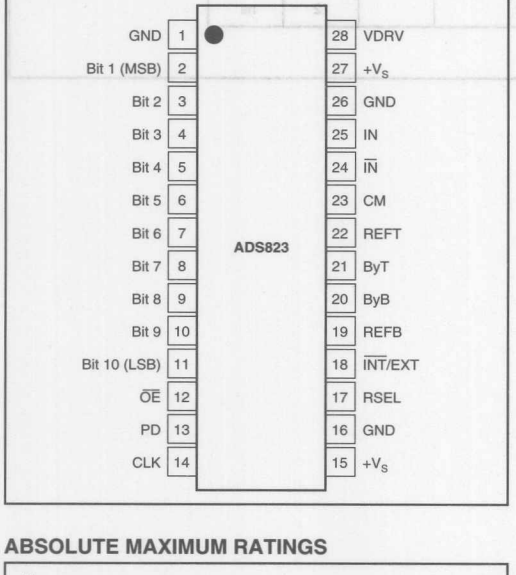
At $T_A$ = full specified temperature range, single-ended input range = 1.5V to 3.5V, sampling rate = 60MHz, external reference, unless otherwise noted.

| PARAMETER | CONDITIONS | ADS823E MIN | ADS823E TYP | ADS823E MAX | UNITS |
|---|---|---|---|---|---|
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Supply Voltage: $+V_S$ | Operating | +4.75 | +5.0 | +5.25 | V |
| Supply Current: $+I_S$ | Operating | | 55 | | mA |
| Power Dissipation: VDRV = 5V | External Reference | | 275 | 335 | mW |
| VDRV = 3V | External Reference | | 265 | | mW |
| VDRV = 5V | Internal Reference | | 295 | 350 | mW |
| VDRV = 3V | Internal Reference | | 285 | | mW |
| Power Down | Operating | | 20 | | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| 28-Lead SSOP | | | 50 | | °C/W |

NOTES: (1) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to Full Scale. (3) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (4) Effective number of bits (ENOB) is defined by (SINAD – 1.76)/6.02. (5) A 50kΩ pull-down resistor is inserted internally on $\overline{OE}$ pin. (6) Includes internal reference. (7) Excludes internal reference.

### PIN CONFIGURATION

Top View SSOP




### PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | GND | Ground |
| 2 | Bit 1 | Data Bit 1 (D9) (MSB) |
| 3 | Bit 2 | Data Bit 2 (D8) |
| 4 | Bit 3 | Data Bit 3 (D7) |
| 5 | Bit 4 | Data Bit 4 (D6) |
| 6 | Bit 5 | Data Bit 5 (D5) |
| 7 | Bit 6 | Data Bit 6 (D4) |
| 8 | Bit 7 | Data Bit 7 (D3) |
| 9 | Bit 8 | Data Bit 8 (D2) |
| 10 | Bit 9 | Data Bit 9 (D1) |
| 11 | Bit 10 | Data Bit 10 (D0) (LSB) |
| 12 | $\overline{OE}$ | Output Enable. HI: High Impedance State. LO or floating: Normal Operation (Internal Pull-down Resistor) |
| 13 | PD | Power Down: HI = Power Down; LO = Normal |
| 14 | CLK | Convert Clock Input |
| 15 | $+V_S$ | +5V Supply |
| 16 | GND | Ground |
| 17 | RSEL | Input Range Select: HI = 2V; LO = 1V |
| 18 | $\overline{INT}$/EXT | Reference Select: HI = External; LO = Internal |
| 19 | REFB | Bottom Reference |
| 20 | ByB | Bottom Ladder Bypass |
| 21 | ByT | Top Ladder Bypass |
| 22 | REFT | Top Reference |
| 23 | CM | Common-Mode Voltage Output |
| 24 | $\overline{IN}$ | Complementary Input (–) |
| 25 | IN | Analog Input (+) |
| 26 | GND | Ground |
| 27 | $+V_S$ | +5V Supply |
| 28 | VDRV | Output Logic Driver Supply Voltage |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Analog Input | –0.3V to ($+V_S$ + 0.3V) |
| Logic Input | –0.3V to ($+V_S$ + 0.3V) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +150°C |

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS823E | 28-Lead SSOP | 324 | –40°C to +85°C |

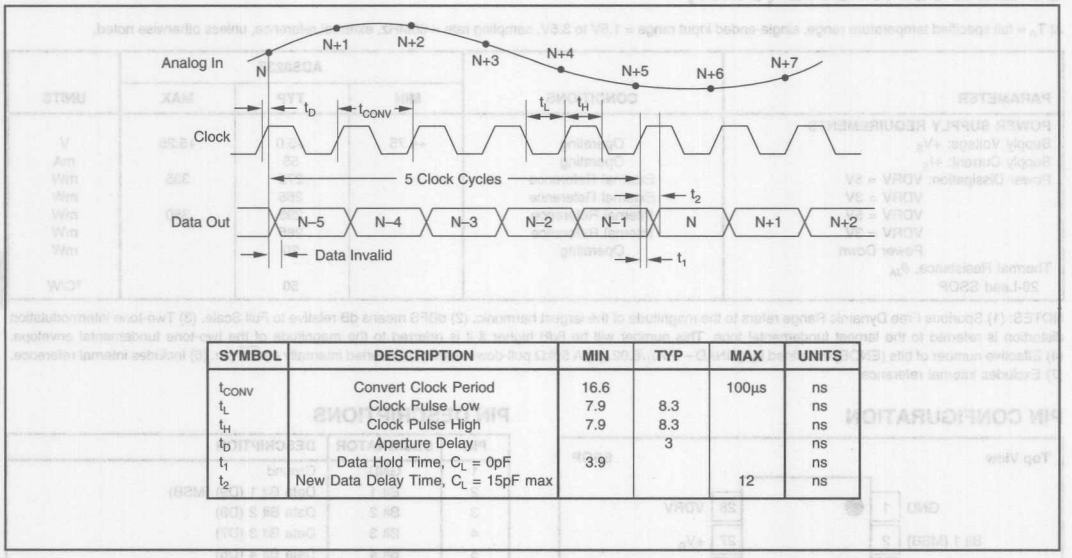
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 16.6 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 7.9 | 8.3 | | ns |
| $t_H$ | Clock Pulse High | 7.9 | 8.3 | | ns |
| $t_D$ | Aperture Delay | | 3 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12 | ns |

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BURR-BROWN®



# ADS824

www.burr-brown.com/databook/ADS824.html

## SpeedPLUS™ 10-Bit, 70MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- HIGH SNR: 59dB
- HIGH SFDR: 70dB
- LOW POWER: 315mW
- INTERNAL/EXTERNAL REFERENCE OPTION
- SINGLE-ENDED OR DIFFERENTIAL ANALOG INPUT
- PROGRAMMABLE INPUT RANGE: 1Vp-p or 2Vp-p
- LOW DNL: 0.3LSB
- SINGLE +5V SUPPLY OPERATION
- +3V DIGITAL OUTPUT CAPABILITY
- POWER DOWN: 20mW
- 28-LEAD SSOP PACKAGE

## APPLICATIONS

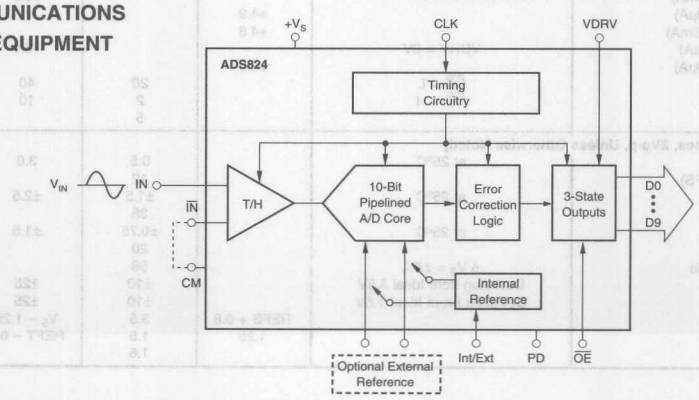
- MEDICAL IMAGING
- HDTV VIDEO DIGITIZING
- COMMUNICATIONS
- TEST EQUIPMENT

## DESCRIPTION

The ADS824 is a pipeline, CMOS analog-to-digital converter that operates from a single +5V power supply. This converter provides excellent performance with a single-ended input and can be operated with a differential input for added spurious performance. This high performance converter includes a 10-bit quantizer, high bandwidth track/hold, and a high accuracy internal reference. It also allows for the user to disable the internal reference and utilize external references. This external reference option provides excellent gain and offset matching when used in multi-channel applications or in applications where full scale range adjustment is required.

The ADS824 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for medical imaging, communications, video, and test instrumentation. The ADS824 offers power dissipation of 315mW and also provides a power-down mode, thus reducing power dissipation to only 20mW.

The ADS824 is specified at a maximum sampling frequency of 70MHz and a single-ended input range of 1.5V to 3.5V. The ADS824 is available in a 28-lead SSOP package and is pin compatible with the 10-bit, 40MHz ADS822 and the 10-bit, 60MHz ADS823.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = full specified temperature range, single-ended input range = 1.5V to 3.5V, sampling rate = 70MHz, external reference, unless otherwise noted.

| PARAMETER | CONDITIONS | ADS824E MIN | ADS824E TYP | ADS824E MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | 10 Guaranteed | | Bits |
| **SPECIFIED TEMPERATURE RANGE** | Ambient Air | | –40 to +85 | | °C |
| **ANALOG INPUT** | | | | | |
| Standard Single-Ended Input Range | 2Vp-p | 1.5 | | 3.5 | V |
| Optional Single-Ended Input Range | 1Vp-p | 2 | | 3 | V |
| Common-Mode Voltage | | | 2.5 | | V |
| Optional Differential Input Range | 2Vp-p | 2 | | 3 | V |
| Analog Input Bias Current | | | 1 | | µA |
| Track-Mode Input Bandwidth | –3dBFS | | 300 | | MHz |
| Input Impedance | | | 1.25 ll 10 | | MΩ ll pF |
| **CONVERSION CHARACTERISTICS** | | | | | |
| Sample Rate | | 10k | | 70M | Samples/s |
| Data Latency | | | 5 | | Clk Cyc |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Differential Linearity Error (largest code error) | | | | | |
| f = 1MHz | | | ±0.3 | ±1.0 | LSB |
| f = 10MHz | | | ±0.3 | | LSB |
| No Missing Codes | | | Guaranteed | | |
| Integral Nonlinearity Error, f = 1MHz | | | ±0.5 | ±2.0 | LSBs |
| Spurious Free Dynamic Range[1] | Referred to Full Scale | | | | |
| f = 1MHz | | | 70 | | dBFS[2] |
| f = 10MHz | | 60 | 68 | | dBFS |
| Two-Tone Intermodulation Distortion[3] | | | | | |
| f = 4.5MHz and 5.5MHz (–7dB each tone) | | | –63.4 | | dBc |
| Signal-to-Noise Ratio (SNR) | Referred to Full Scale | | | | |
| f = 1MHz | | | 59 | | dB |
| f = 10MHz | | 55 | 59 | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | Referred to Full Scale | | | | |
| f = 1MHz | | | 58 | | dB |
| f = 10MHz | | 50 | 58 | | dB |
| Effective Number of Bits[4], f = 1MHz | | | 9.3 | | Bits |
| Output Noise | Input Grounded | | 0.2 | | LSBs rms |
| Aperture Delay Time | | | 3 | | ns |
| Aperture Jitter | | | 1.2 | | ps rms |
| Overvoltage Recovery Time | | | 2 | | ns |
| Full-Scale Step Acquisition Time | | | 5 | | ns |
| **DIGITAL INPUTS** | | | | | |
| Logic Family | | | CMOS Compatible | | |
| Convert Command | Start Conversion | | Rising Edge of Convert Clock | | |
| High Level Input Current[5] ($V_{IN}$ = 5V) | | | | 100 | µA |
| Low Level Input Current ($V_{IN}$ = 0V) | | | | 10 | µA |
| High Level Input Voltage | | +3.5 | | | V |
| Low Level Input Voltage | | | | +1.0 | V |
| Input Capacitance | | | 5 | | pF |
| **DIGITAL OUTPUTS** | | | | | |
| Logic Family | | | CMOS Compatible | | |
| Logic Coding | | | Straight Offset Binary | | |
| Low Output Voltage ($I_{OL}$ = 50µA) | VDRV = 5V | | | +0.1 | V |
| Low Output Voltage, ($I_{OL}$ = 1.6mA) | | | | +0.2 | V |
| High Output Voltage, ($I_{OH}$ = 50µA) | | +4.9 | | | V |
| High Output Voltage, ($I_{OH}$ = 0.5mA) | | +4.8 | | | V |
| Low Output Voltage, ($I_{OL}$ = 50µA) | VDRV = 3V | | | +0.1 | V |
| High Output Voltage, ($I_{OH}$ = 50µA) | | +2.8 | | | V |
| 3-State Enable Time | $\overline{OE}$ = L | | 20 | 40 | ns |
| 3-State Disable Time | $\overline{OE}$ = H | | 2 | 10 | ns |
| Output Capacitance | | | 5 | | pF |
| **ACCURACY (Internal Reference, 2Vp-p, Unless Otherwise Noted)** | | | | | |
| Zero Error (Referred to –FS) | at 25°C | | 0.5 | 3.0 | %FS |
| Zero Error Drift (Referred to –FS) | | | 12 | | ppm/°C |
| Gain Error[6] | at 25°C | | ±1.5 | ±2.5 | %FS |
| Gain Error Drift[6] | | | 38 | | ppm/°C |
| Gain Error[7] | at 25°C | | ±0.75 | ±1.5 | %FS |
| Gain Error Drift[7] | | | 20 | | ppm/°C |
| Power Supply Rejection of Gain | $\Delta V_S$ = ±5% | | 68 | | dB |
| REFT Tolerance | Deviation from Ideal 3.5V | | ±10 | ±25 | mV |
| REFB Tolerance | Deviation From Ideal 1.5V | | ±10 | ±25 | mV |
| External REFT Voltage Range | | REFB + 0.8 | 3.5 | $V_S$ – 1.25 | V |
| External REFB Voltage Range | | 1.25 | 1.5 | REFT – 0.8 | V |
| Reference Input Resistance | | | 1.6 | | kΩ |

## SPECIFICATIONS (CONT)

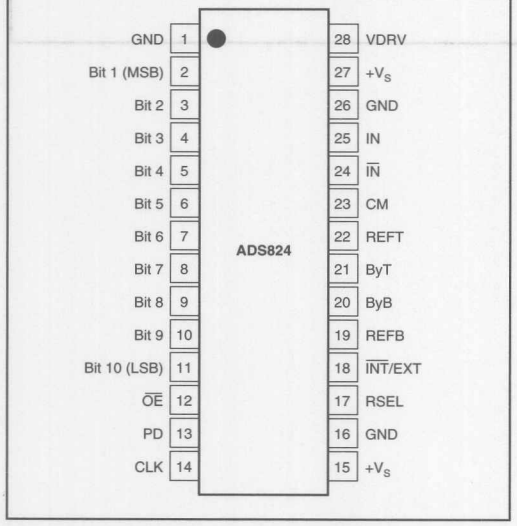
At $T_A$ = full specified temperature range, single-ended input range = 1.5V to 3.5V, sampling rate = 70MHz, external reference, unless otherwise noted.

| PARAMETER | CONDITIONS | ADS824E MIN | ADS824E TYP | ADS824E MAX | UNITS |
|---|---|---|---|---|---|
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Supply Voltage: $+V_S$ | Operating | +4.75 | +5.0 | +5.25 | V |
| Supply Current: $+I_S$ | Operating | | 66 | | mA |
| Output Driver Supply Current (VDRV) | | | 9 | | mA |
| Power Dissipation: VDRV = 5V | External Reference | | 330 | 375 | mW |
| VDRV = 3V | External Reference | | 315 | | mW |
| VDRV = 5V | Internal Reference | | 345 | | mW |
| VDRV = 3V | Internal Reference | | 335 | | mW |
| Power Down | Operating | | 20 | | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| 28-Lead SSOP | | | | | °C/W |

NOTES: (1) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to Full Scale. (3) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (4) Effective number of bits (ENOB) is defined by (SINAD – 1.76)/6.02. (5) A 50kΩ pull-down resistor is inserted internally. (6) Includes internal reference. (7) Excludes internal reference.

### PIN CONFIGURATION

Top View SSOP




### PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | GND | Ground |
| 2 | Bit 1 | Data Bit 1 (D9) (MSB) |
| 3 | Bit 2 | Data Bit 2 (D8) |
| 4 | Bit 3 | Data Bit 3 (D7) |
| 5 | Bit 4 | Data Bit 4 (D6) |
| 6 | Bit 5 | Data Bit 5 (D5) |
| 7 | Bit 6 | Data Bit 6 (D4) |
| 8 | Bit 7 | Data Bit 7 (D3) |
| 9 | Bit 8 | Data Bit 8 (D2) |
| 10 | Bit 9 | Data Bit 9 (D1) |
| 11 | Bit 10 | Data Bit 10 (D0) (LSB) |
| 12 | $\overline{OE}$ | Output Enable. HI: High Impedance State. LO or floating: Normal Operation (Internal Pull-down Resistor) |
| 13 | PD | Power Down: HI = Power Down; LO = Normal |
| 14 | CLK | Convert Clock Input |
| 15 | $+V_S$ | +5V Supply |
| 16 | GND | Ground |
| 17 | RSEL | Input Range Select: HI = 2Vp-p; LO = 1Vp-p |
| 18 | $\overline{INT}$/EXT | Reference Select: HI = External; LO = Internal |
| 19 | REFB | Bottom Reference |
| 20 | ByB | Bottom Ladder Bypass |
| 21 | ByT | Top Ladder Bypass |
| 22 | REFT | Top Reference |
| 23 | CM | Common-Mode Voltage Output |
| 24 | $\overline{IN}$ | Complementary Input (–) |
| 25 | IN | Analog Input (+) |
| 26 | GND | Ground |
| 27 | $+V_S$ | +5V Supply |
| 28 | VDRV | Output Logic Driver Supply Voltage |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Analog Input | –0.3V to ($+V_S$ + 0.3V) |
| Logic Input | –0.3V to ($+V_S$ + 0.3V) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +150°C |

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS824E | 28-Lead SSOP | 324 | –40°C to +85°C |

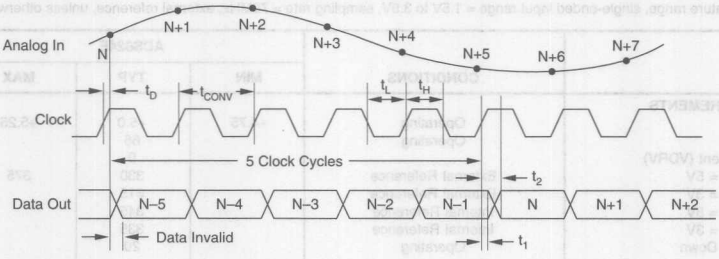
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 13.4 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 6.4 | 6.7 | | ns |
| $t_H$ | Clock Pulse High | 6.4 | 6.7 | | ns |
| $t_D$ | Aperture Delay | | 3 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12 | ns |

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# ADS830

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
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www.burr-brown.com/databook/ADS830.html

# SpeedPLUS™ 8-Bit, 60MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- HIGH SNR: 49.5dB
- INTERNAL/EXTERNAL REFERENCE OPTION
- SINGLE-ENDED OR DIFFERENTIAL ANALOG INPUT
- PROGRAMMABLE INPUT RANGE: 1Vp-p/2Vp-p
- LOW POWER: 180mW
- LOW DNL: 0.5LSB
- SINGLE +5V SUPPLY OPERATION
- 20-PIN SSOP PACKAGE
- POWER DOWN: 20mW

## APPLICATIONS

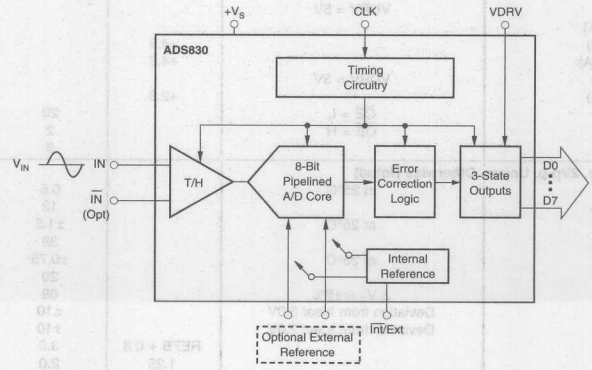
- MEDICAL IMAGING
- VIDEO DIGITIZING
- COMMUNICATIONS
- DISK-DRIVE CONTROL

## DESCRIPTION

The ADS830 is a pipeline, CMOS analog-to-digital converter that operates from a single +5V power supply. This converter provides excellent performance with a single-ended input and can be operated with a differential input for added spurious performance. This high performance converter includes an 8-bit quantizer, high bandwidth track/hold, and a high accuracy internal reference. It also allows for the user to disable the internal reference and utilize external references. This external reference option provides excellent gain and offset matching when used in multi-channel applications or in applications where DC full scale range adjustment is required.

The ADS830 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for medical imaging, communications, video, and test instrumentation. The ADS830 offers power dissipation of 180mW and also provides a power-down mode, thus reducing power dissipation to only 20mW.

The ADS830 is specified at a maximum sampling frequency of 60MHz and a single-ended input range of 1.5V to 3.5V. The ADS830 is available in a 20-pin SSOP package and is pin-for-pin compatible with the 8-bit, 80MHz ADS831.




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## SPECIFICATIONS—PRELIMINARY

At $T_A$ = full specified temperature range, single-ended input range = 1.5V to 3.5V, sampling rate = 60MHz, external reference, unless otherwise noted.

| PARAMETER | CONDITIONS | ADS830E MIN | ADS830E TYP | ADS830E MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | 8 Guaranteed | | Bits |
| **SPECIFIED TEMPERATURE RANGE** | Ambient Air | | –40 to +85 | | °C |
| **ANALOG INPUT** | | | | | |
| Standard Single-Ended Input Range | 2Vp-p | 1.5 | | 3.5 | V |
| Optional Single-Ended Input Range | 1Vp-p | 2 | | 3 | V |
| Common-Mode Voltage | | | 2.5 | | V |
| Optional Differential Input Range | 2Vp-p | 2 | | 3 | V |
| Analog Input Bias Current | | | 1 | | µA |
| Input Impedance | | | 1.25 ll 10 | | MΩ ll pF |
| Track-Mode Input Bandwidth | –3dBFS | | 300 | | MHz |
| **CONVERSION CHARACTERISTICS** | | | | | |
| Sample Rate | | 10k | | 60M | Samples/s |
| Data Latency | | | 4 | | Clk Cyc |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Differential Linearity Error (Largest Code Error) | | | | | |
| f = 1MHz | | | ±0.5 | ±1.0 | LSB |
| f = 10MHz | | | ±0.5 | ±1.0 | LSB |
| No Missing Codes | | | Guaranteed | | |
| Integral Nonlinearity Error, f = 1MHz | | | ±0.5 | ±2.0 | LSBs |
| Spurious Free Dynamic Range[1] | | | | | |
| f = 1MHz (–1dB input) | | | 75 | | dBFS[2] |
| f = 10MHz (–1dB input) | | 67 | 73 | | dBFS |
| Two-Tone Intermodulation Distortion[3] | | | | | |
| f = 4.5MHz and 5.5MHz (–7dB each tone) | | | 68 | | dBc |
| Signal-to-Noise Ratio (SNR) | Referred to Full Scale | | | | |
| f = 1MHz | | | 49.5 | | dB |
| f = 10MHz | | 46 | 49.5 | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | Referred to Full Scale | | | | |
| f = 1MHz | | | 48 | | dB |
| f = 3.58MHz | | | 48 | | dB |
| f = 10MHz | | 45 | 48 | | dB |
| Effective Number of Bits[4], f = 1MHz | | | 7.7 | | Bits |
| Differential Gain Error | NTSC, PAL | | 0.2 | | % |
| Differential Phase Error | NTSC, PAL | | 0.2 | | degrees |
| Output Noise | Input Tied to Common-Mode | | 0.2 | | LSBs rms |
| Aperture Delay Time | | | 3 | | ns |
| Aperture Jitter | | | 1.2 | | ps rms |
| Overvoltage Recovery Time | | | 2 | | ns |
| Full-Scale Step Acquisition Time | | | TBD | | ns |
| **DIGITAL INPUTS** | | | | | |
| Logic Family | | | CMOS | | |
| Convert Command | Start Conversion | | Rising Edge of Convert Clock | | |
| High Level Input Current[5] ($V_{IN}$ = 5V) | | | | 100 | µA |
| Low Level Input Current ($V_{IN}$ = 0V) | | | | 10 | µA |
| High Level Input Voltage | | +3.5 | | | V |
| Low Level Input Voltage | | | | +1.0 | V |
| Input Capacitance | | | 5 | | pF |
| **DIGITAL OUTPUTS** | | | | | |
| Logic Family | | | CMOS | | |
| Logic Coding | | | Straight Offset Binary | | |
| Low Output Voltage ($I_{OL}$ = 50µA) | VDRV = 5V | | | +0.1 | V |
| Low Output Voltage, ($I_{OL}$ = 1.6mA) | | | | +0.2 | V |
| High Output Voltage, ($I_{OH}$ = 50µA) | | +4.9 | | | V |
| High Output Voltage, ($I_{OH}$ = 0.5mA) | | +4.8 | | | V |
| Low Output Voltage, ($I_{OL}$ = 50µA) | VDRV = 3V | | | +0.1 | V |
| High Output Voltage, ($I_{OH}$ = 50µA) | | +2.8 | | | V |
| 3-State Enable Time | $\overline{OE}$ = L | | 20 | 40 | ns |
| 3-State Disable Time | $\overline{OE}$ = H | | 2 | 10 | ns |
| Output Capacitance | | | 5 | | pF |
| **ACCURACY (Internal Reference, 2Vp-p, Unless Otherwise Noted)** | | | | | |
| Zero Error (Referred to –FS) | at 25°C | | 0.5 | 1 | %FS |
| Zero Error Drift (Referred to –FS) | | | 12 | | ppm/°C |
| Gain Error[6] | at 25°C | | ±1.5 | ±2.5 | %FS |
| Gain Error Drift[6] | | | 38 | | ppm/°C |
| Gain Error[7] | at 25°C | | ±0.75 | ±1.5 | %FS |
| Gain Error Drift[7] | | | 20 | | ppm/°C |
| Power Supply Rejection of Gain | $\Delta V_S$ = ±5% | | 68 | | dB |
| REFT Tolerance | Deviation from Ideal 3.0V | | ±10 | ±25 | mV |
| REFB Tolerance | Deviation from Ideal 2.0V | | ±10 | ±25 | mV |
| External REFT Voltage Range | | REFB + 0.8 | 3.0 | $V_S$ – 1.25 | V |
| External REFB Voltage Range | | 1.25 | 2.0 | REFT – 0.8 | V |
| Reference Input Resistance | REFT to REF3 | | 800 | | kΩ |

## SPECIFICATIONS—PRELIMINARY

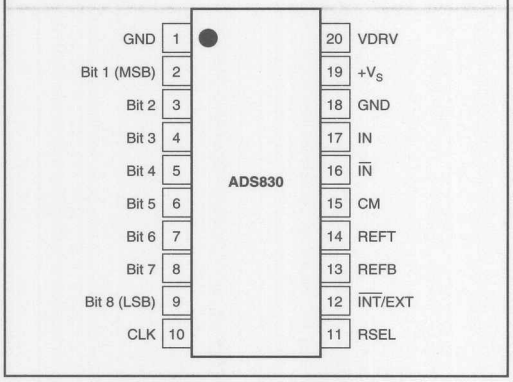
At $T_A$ = full specified temperature range, single-ended input range = 1.5V to 3.5V, sampling rate = 60MHz, external reference, unless otherwise noted.

| PARAMETER | CONDITIONS | ADS830E MIN | ADS830E TYP | ADS830E MAX | UNITS |
|---|---|---|---|---|---|
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Supply Voltage: $+V_S$ | Operating | +4.75 | +5.0 | +5.25 | V |
| Supply Current: $+I_S$ | Operating | | | | mA |
| Power Dissipation: VDRV = 5V | External Reference | | 190 | | mW |
| VDRV = 3V | External Reference | | 180 | | mW |
| VDRV = 5V | Internal Reference | | 210 | | mW |
| VDRV = 3V | Internal Reference | | 200 | | mW |
| Power Down | Operating | | 20 | | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| 20-Pin SSOP | | | | | °C/W |

NOTES: (1) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to Full Scale. (3) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (4) Effective number of bits (ENOB) is defined by (SINAD – 1.76)/6.02. (5) A 50kΩ pull-down resistor is inserted internally. (6) Includes internal reference. (7) Excludes internal reference.

### PIN CONFIGURATION

Top View SSOP




### PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | GND | Ground |
| 2 | Bit 1 | Data Bit 1 (D7) (MSB) |
| 3 | Bit 2 | Data Bit 2 (D6) |
| 4 | Bit 3 | Data Bit 3 (D5) |
| 5 | Bit 4 | Data Bit 4 (D4) |
| 6 | Bit 5 | Data Bit 5 (D3) |
| 7 | Bit 6 | Data Bit 6 (D2) |
| 8 | Bit 7 | Data Bit 7 (D1) |
| 9 | Bit 8 | Data Bit 8 (D0) (LSB) |
| 10 | CLK | Convert Clock |
| 11 | RSEL | Input Range Select: HI = 2V; LO = 1V |
| 12 | INT/EXT | Reference Select: HI = External; LO = Internal |
| 13 | REFB | Bottom Reference |
| 14 | REFT | Top Reference |
| 15 | CM | Common-Mode Voltage Output |
| 16 | IN | Complementary Input |
| 17 | IN | Analog Input |
| 18 | GND | Ground |
| 19 | +VS | +5V Supply |
| 20 | VDRV | Output Logic Drive Supply Voltage |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Analog Input | –0.3V to ($+V_S$ + 0.3V) |
| Logic Input | –0.3V to ($+V_S$ + 0.3V) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +150°C |

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS830E | 20-Pin SSOP | 349 | –40°C to +85°C |

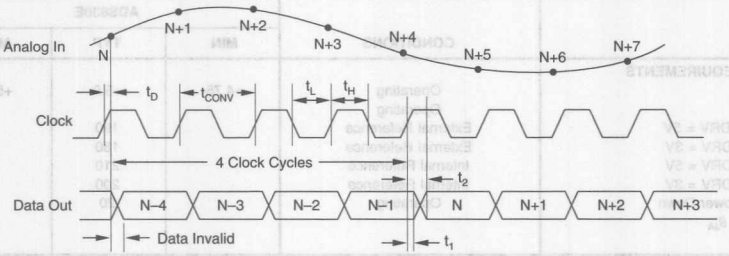
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 16.6 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 7.3 | 8.3 | | ns |
| $t_H$ | Clock Pulse High | 7.3 | 8.3 | | ns |
| $t_D$ | Aperture Delay | | 3 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12 | ns |

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# ADS831

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

www.burr-brown.com/databook/ADS831.html

## SpeedPLUS™ 8-Bit, 80MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- HIGH SNR: 48.5dB
- INTERNAL/EXTERNAL REFERENCE OPTION
- SINGLE-ENDED OR DIFFERENTIAL ANALOG INPUT
- PROGRAMMABLE INPUT RANGE: 1Vp-p/2Vp-p
- LOW POWER: 265mW
- LOW DNL: 0.5LSB
- SINGLE +5V SUPPLY OPERATION
- 20-PIN SSOP PACKAGE
- POWER DOWN: 20mW

## APPLICATIONS

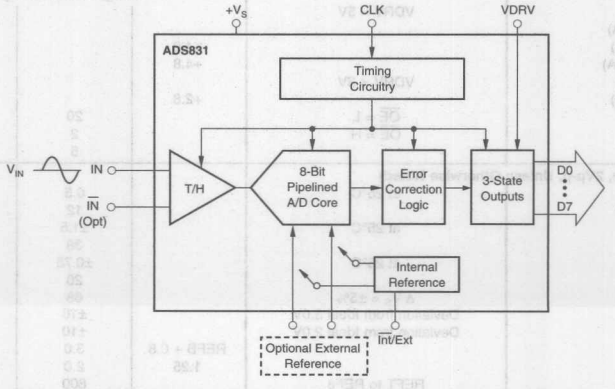
- MEDICAL IMAGING
- VIDEO DIGITIZING
- COMPUTER SCANNERS
- COMMUNICATIONS
- DISK-DRIVE CONTROL

## DESCRIPTION

The ADS831 is a pipeline, CMOS analog-to-digital converter that operates from a single +5V power supply. This converter provides excellent performance with a single-ended input and can be operated with a differential input for added spurious performance. This high performance converter includes an 8-bit quantizer, high bandwidth track/hold, and a high accuracy internal reference. It also allows for the user to disable the internal reference and utilize external references. This external reference option provides excellent gain and offset matching when used in multi-channel applications or in applications where DC full scale range adjustment is required.

The ADS831 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for medical imaging, communications, video, and test instrumentation. The ADS831 offers power dissipation of 265mW and also provides a power-down mode, thus reducing power dissipation to only 20mW.

The ADS831 is specified at a maximum sampling frequency of 80MHz and a single-ended input range of 1.5V to 3.5V. The ADS831 is available in a 20-pin SSOP package and is pin-for-pin compatible with the 8-bit, 60MHz ADS830.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

## SPECIFICATIONS—PRELIMINARY

At $T_A$ = full specified temperature range, single-ended input range = 1.5V to 3.5V, sampling rate = 80MHz, external reference, unless otherwise noted.

| PARAMETER | CONDITIONS | ADS831E MIN | ADS831E TYP | ADS831E MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | 8 Guaranteed | | Bits |
| **SPECIFIED TEMPERATURE RANGE** | Ambient Air | | –40 to +85 | | °C |
| **ANALOG INPUT** | | | | | |
| Standard Single-Ended Input Range | 2Vp-p | 1.5 | | 3.5 | V |
| Optional Single-Ended Input Range | 1Vp-p | 2 | | 3 | V |
| Common-Mode Voltage | | | 2.5 | | V |
| Optional Differential Input Range | 2Vp-p | 2 | | 3 | V |
| Analog Input Bias Current | | | 1 | | µA |
| Input Impedance | | | 1.25 ll 10 | | MΩ ll pF |
| Track-Mode Input Bandwidth | –3dBFS | | 300 | | MHz |
| **CONVERSION CHARACTERISTICS** | | | | | |
| Sample Rate | | 10k | | 80M | Samples/s |
| Data Latency | | | 4 | | Clk Cyc |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Differential Linearity Error (largest code error) | | | | | |
| f = 1MHz | | | ±0.5 | ±1.0 | LSB |
| f = 10MHz | | | ±0.5 | ±1.0 | LSB |
| No Missing Codes | | | Guaranteed | | |
| Integral Nonlinearity Error, f = 1MHz | | | ±0.5 | ±2.0 | LSBs |
| Spurious Free Dynamic Range[1] | | | | | |
| f = 1MHz (–1dB input) | | | 68 | | dBFS[2] |
| f = 10MHz (–1dB input) | | | 65 | | dBFS |
| Two-Tone Intermodulation Distortion[3] | | | | | |
| f = 4.5MHz and 5.5MHz (–7dB each tone) | | | 60 | | dBc |
| Signal-to-Noise Ratio (SNR) | Referred to Full Scale | | | | |
| f = 1MHz | | | 49 | | dB |
| f = 10MHz | | | 48.5 | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | Referred to Full Scale | | | | |
| f = 1MHz | | | 48 | | dB |
| f = 3.58MHz | | | 48 | | dB |
| f = 10MHz | | | 48 | | dB |
| Effective Number of Bits[4], f = 1MHz | | | 7.7 | | Bits |
| Differential Gain Error | NTSC, PAL | | 0.2 | | % |
| Differential Phase Error | NTSC, PAL | | 0.2 | | degrees |
| Output Noise | Input Tied to Common-Mode | | 0.2 | | LSBs rms |
| Aperture Delay Time | | | 3 | | ns |
| Aperture Jitter | | | 1.2 | | ps rms |
| Overvoltage Recovery Time | | | 2 | | ns |
| Full-Scale Step Acquisition Time | | | TBD | | ns |
| **DIGITAL INPUTS** | | | | | |
| Logic Family | | | CMOS | | |
| Convert Command | Start Conversion | | Rising Edge of Convert Clock | | |
| High Level Input Current[5] ($V_{IN}$ = 5V) | | | | 100 | µA |
| Low Level Input Current ($V_{IN}$ = 0V) | | | | 10 | µA |
| High Level Input Voltage | | +3.5 | | | V |
| Low Level Input Voltage | | | | +1.0 | V |
| Input Capacitance | | | 5 | | pF |
| **DIGITAL OUTPUTS** | | | | | |
| Logic Family | | | CMOS | | |
| Logic Coding | | | Straight Offset Binary | | |
| Low Output Voltage ($I_{OL}$ = 50µA) | VDRV = 5V | | | +0.1 | V |
| Low Output Voltage, ($I_{OL}$ = 1.6mA) | | | | +0.2 | V |
| High Output Voltage, ($I_{OH}$ = 50µA) | | +4.9 | | | V |
| High Output Voltage, ($I_{OH}$ = 0.5mA) | | +4.8 | | | V |
| Low Output Voltage, ($I_{OL}$ = 50µA) | VDRV = 3V | | | +0.1 | V |
| High Output Voltage, ($I_{OH}$ = 50µA) | | +2.8 | | | V |
| 3-State Enable Time | $\overline{OE}$ = L | | 20 | 40 | ns |
| 3-State Disable Time | $\overline{OE}$ = H | | 2 | 10 | ns |
| Output Capacitance | | | 5 | | pF |
| **ACCURACY (Internal Reference, 2Vp-p, Unless Otherwise Noted)** | | | | | |
| Zero Error (Referred to –FS) | at 25°C | | 0.5 | 1 | %FS |
| Zero Error Drift (Referred to –FS) | | | 12 | | ppm/°C |
| Gain Error[6] | at 25°C | | ±1.5 | ±2.5 | %FS |
| Gain Error Drift[6] | | | 38 | | ppm/°C |
| Gain Error[7] | at 25°C | | ±0.75 | ±1.5 | %FS |
| Gain Error Drift[7] | | | 20 | | ppm/°C |
| Power Supply Rejection of Gain | $\Delta V_S$ = ±5% | | 68 | | dB |
| REFT Tolerance | Deviation from Ideal 3.0V | | ±10 | ±25 | mV |
| REFB Tolerance | Deviation from Ideal 2.0V | | ±10 | ±25 | mV |
| External REFT Voltage Range | | REFB + 0.8 | 3.0 | $V_S$ – 1.25 | V |
| External REFB Voltage Range | | 1.25 | 2.0 | REFT – 0.8 | V |
| Reference Input Resistance | REFT to REF3 | | 800 | | Ω |

## SPECIFICATIONS—PRELIMINARY

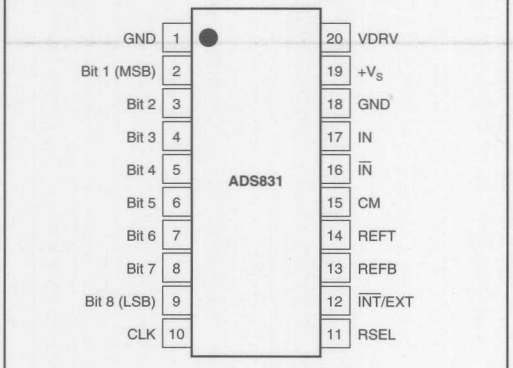
At $T_A$ = full specified temperature range, single-ended input range = 1.5V to 3.5V, sampling rate = 60MHz external reference, unless otherwise noted.

| PARAMETER | CONDITIONS | ADS831E | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Supply Voltage: $+V_S$ | Operating | +4.75 | +5.0 | +5.25 | V |
| Supply Current: $+I_S$ | Operating | | | | mA |
| Power Dissipation: VDRV = 5V | External Reference | | 275 | | mW |
| VDRV = 3V | External Reference | | 265 | | mW |
| VDRV = 5V | Internal Reference | | 295 | | mW |
| VDRV = 3V | Internal Reference | | 285 | | mW |
| Power Down | Operating | | 20 | | mW |
| Thermal Resistance, $\theta_{JA}$ 20-Pin SSOP | | | | | °C/W |

NOTES: (1) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to Full Scale. (3) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (4) Effective number of bits (ENOB) is defined by (SINAD – 1.76)/6.02. (5) A 50kΩ pull-down resistor is inserted internally. (6) Includes internal reference. (7) Excludes internal reference.

### PIN CONFIGURATION

Top View SSOP




### PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | GND | Ground |
| 2 | Bit 1 | Data Bit 1 (D7) (MSB) |
| 3 | Bit 2 | Data Bit 2 (D6) |
| 4 | Bit 3 | Data Bit 3 (D5) |
| 5 | Bit 4 | Data Bit 4 (D4) |
| 6 | Bit 5 | Data Bit 5 (D3) |
| 7 | Bit 6 | Data Bit 6 (D2) |
| 8 | Bit 7 | Data Bit 7 (D1) |
| 9 | Bit 8 | Data Bit 8 (D0) (LSB) |
| 10 | CLK | Convert Clock |
| 11 | RSEL | Input Range Select: HI = 2V; LO = 1V |
| 12 | INT/EXT | Reference Select: HI = External; LO = Internal |
| 13 | REFB | Bottom Reference |
| 14 | REFT | Top Reference |
| 15 | CM | Common-Mode Voltage Output |
| 16 | IN | Complementary Input |
| 17 | IN | Analog Input |
| 18 | GND | Ground |
| 19 | $+V_S$ | +5V Supply |
| 20 | VDRV | Output Logic Driver Supply Voltage |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Analog Input | –0.3V to ($+V_S$ + 0.3V) |
| Logic Input | –0.3V to ($+V_S$ + 0.3V) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +150°C |

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS831E | 20-Pin SSOP | 349 | –40°C to +85°C |

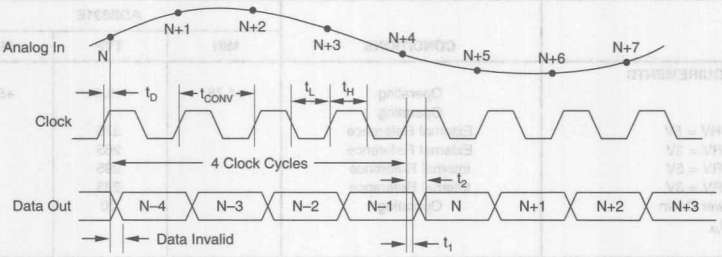
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 12.5 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 5.8 | 6.25 | | ns |
| $t_H$ | Clock Pulse High | 5.8 | 6.25 | | ns |
| $t_D$ | Aperture Delay | | 3 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12 | ns |

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# ADS900

www.burr-brown.com/databook/ADS900.html

## SpeedPLUS™ 10-Bit, 20MHz, +3V Supply ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- +2.7V TO +3.7V SUPPLY OPERATION
- INTERNAL REFERENCE
- LOW POWER: 52mW at +3V
- SINGLE-ENDED INPUT RANGE: 1V to 2V
- WIDEBAND TRACK/HOLD: 350MHz
- 28-LEAD SSOP PACKAGE

## APPLICATIONS

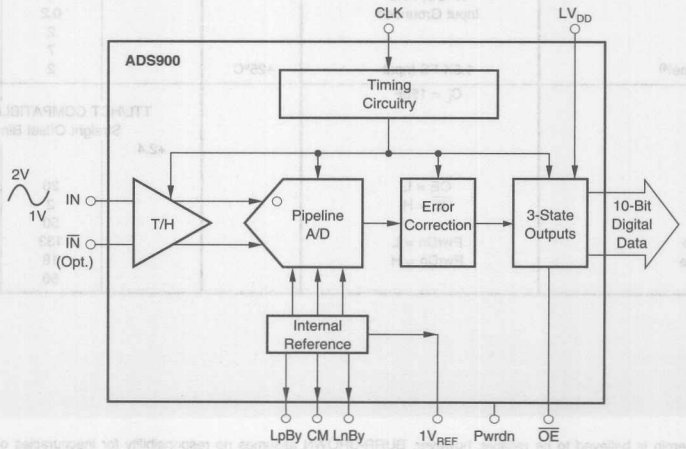
- PORTABLE INSTRUMENTATION
- IF AND BASEBAND COMMUNICATIONS
- CABLE MODEMS
- SET-TOP BOXES
- PORTABLE TEST EQUIPMENT
- COMPUTER SCANNERS

## DESCRIPTION

The ADS900 is a high speed pipelined analog-to-digital converter. This complete converter includes a high bandwidth track/hold, a 10-bit quantizer and an internal reference.

The ADS900 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for telecommunications, video and test instrumentation applications.

This high performance A/D converter is specified for performance at a 20MHz sampling rate. The ADS900 is available in a 28-lead SSOP package.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = $LV_{DD}$ = +3V, Single-Ended Input, Sampling Rate = 20MHz, unless otherwise specified.

| PARAMETER | CONDITIONS | TEMP | ADS900E MIN | ADS900E TYP | ADS900E MAX | UNITS |
|---|---|---|---|---|---|---|
| Resolution | | | | 10 | | Bits |
| Specified Temperature Range | Ambient Air | | –40 | | +85 | °C |
| **ANALOG INPUT** | | | | | | |
| Single-Ended Full Scale Input Range | (1Vp-p) | | | 1.0 to 2.0 | | V |
| Differential Full Scale Input Range | (0.5Vp-pX 2) | | | 1.25 to 1.75 | | V |
| Common-Mode Voltage | | | | 1.5 | | V |
| Analog Input Bias Current | | | | 1 | | µA |
| Input Impedance | | | | 1.25 ll 5 | | MΩ ll pF |
| Analog Input Bandwidth | | | | | | |
| Small Signal | –20dBFS Input | +25°C | | 350 | | MHz |
| Full Power | 0dBFS Input | +25°C | | 100 | | MHz |
| **DIGITAL INPUTS** | | Full | | | | |
| Logic Family | | | | TTL/HCT COMPATIBLE CMOS | | |
| High Input Voltage, $V_{IH}$ | | | 2.0 | | $V_{DD}$ | V |
| Low Input Voltage, $V_{IL}$ | | | | | 0.8 | V |
| High Input Current, $I_{IH}$ | | | | ±10 | | µA |
| Low Input Current, $I_{IL}$ | | | | ±10 | | µA |
| Input Capacitance | | | | 5 | | pF |
| **CONVERSION CHARACTERISTICS** | | | | | | |
| Start Conversion | | | | RISING EDGE OF CONVERT CLOCK | | |
| Sample Rate | | Full | 10k | | 20M | Samples/s |
| Data Latency | | | | 5 | | Clk Cyc |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Differential Linearity Error | | | | | | |
| f = 500kHz (Largest Code Error) | | Full | | ±0.7 | ±1.0 | LSBs |
| f = 10MHz (Largest Code Error) | | Full | | ±0.7 | ±1.0 | LSBs |
| No Missing Codes | | Full | | Guaranteed | | |
| Integral Nonlinearity Error, f = 500kHz | | Full | | ±3.5 | | LSBs |
| Spurious Free Dynamic Range[1] | | | | | | |
| f = 500kHz (–1dBFS[2] input) | | Full | 47 | 53 | | dBFS[2] |
| f = 10MHz (–1dBFS[2] input) | | Full | 47 | 53 | | dBFS |
| Two-Tone Intermodulation Distortion[3] | | | | | | |
| f = 4.5MHz and 5.0MHz (–7dBFS each tone) | | +25°C | | 50 | | dBc |
| Signal-to-Noise Ratio (SNR) | | | | | | |
| f = 500kHz (–1dBFS input) | | Full | 45 | 49 | | dB |
| f = 10MHz (–1dBFS input) | | Full | 45 | 49 | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | | | | | | |
| f = 500kHz (–1dBFS input) | | Full | 44 | 48 | | dB |
| f = 3.58MHz (–1dBFS input) | | Full | 44 | 48 | | dB |
| f = 10MHz (–1dBFS input) | | Full | 44 | 48 | | dB |
| Differential Gain Error | NTSC, PAL | | | 2.3 | | % |
| Differential Phase Error | NTSC, PAL | | | 1 | | degrees |
| Output Noise | Input Grounded | | | 0.2 | | LSBs rms |
| Aperture Delay Time | | | | 2 | | ns |
| Aperture Jitter | | | | 7 | | ps rms |
| Overvoltage Recovery Time[4] | 1.5X FS Input | +25°C | | 2 | | ns |
| **DIGITAL OUTPUTS** | $C_L$ = 15pF | | | | | |
| Logic Family | | | | TTL/HCT COMPATIBLE CMOS | | |
| Logic Coding | | | | Straight Offset Binary | | |
| High Output Voltage, $V_{OH}$ | | | +2.4 | | $LV_{DD}$ | V |
| Low Output Voltage, $V_{OL}$ | | | | | +0.4 | V |
| 3-State Enable Time | $\overline{OE}$ = L | | | 20 | 40 | ns |
| 3-State Disable Time | $\overline{OE}$ = H | | | 2 | 10 | ns |
| Internal Pull-Down | | | | 50 | | kΩ |
| Power-Down Enable Time | PwrDn = L | | | 133 | | ns |
| Power-Down Disable Time | PwrDn = H | | | 18 | | ns |
| Internal Pull-Down | | | | 50 | | kΩ |

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## SPECIFICATIONS (CONT)

At $T_A$ = +25°C, $V_S$ = +3V, Single-Ended Input, Sampling Rate = 20MHz, unless otherwise specified.

| PARAMETER | CONDITIONS | TEMP | ADS900E MIN | ADS900E TYP | ADS900E MAX | UNITS |
|---|---|---|---|---|---|---|
| **ACCURACY** | | | | | | |
| Gain Error | | +25°C | | 8 | ±10 | %FS |
| Input Offset | Referred to Ideal Midscale | Full | | 15 | ±60 | mV |
| Power Supply Rejection (Gain) | Δ $V_S$ = +10% | Full | 42 | 55 | | dB |
| Power Supply Rejection (Offset) | | Full | 42 | 62 | | dB |
| Internal Positive Reference Voltage | | Full | | +1.75 | | V |
| Internal Negative Reference Voltage | | Full | | +1.25 | | V |
| **POWER SUPPLY REQUIREMENTS** | | | | | | |
| Supply Voltage: +$V_S$ | Operating | Full | +2.7 | +3 | +3.7 | V |
| Supply Current: +$I_S$ | Operating | Full | | 18 | 22 | mA |
| Power Dissipation | Operating, +3V | Full | | 54 | 66 | mW |
| | | 25°C | | 52 | | mW |
| Power Dissipation (Power Down) | +3V | Full | | 10 | | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | | |
| 28-Lead SSOP | | | | 50 | | °C/W |

NOTES: (1) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to full scale. (3) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (4) No rollover of bits.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| +$V_S$ | +6V |
| Analog Input | +$V_S$ +0.3V |
| Logic Input | +$V_S$ +0.3V |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +150°C |

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS900E | 28-Lead SSOP | 324 | –40°C to +85°C |

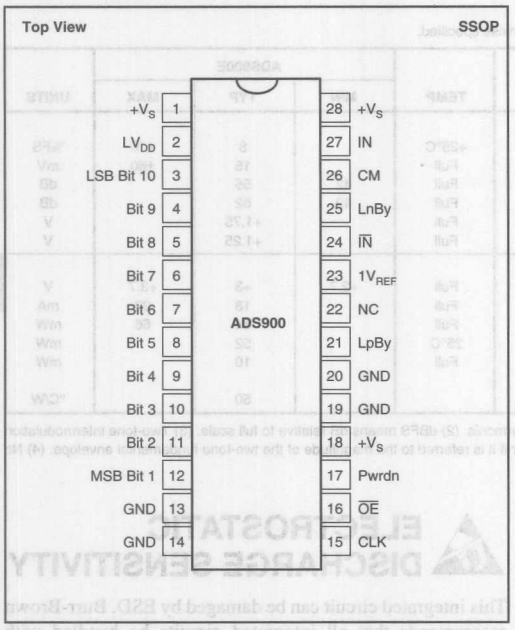
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

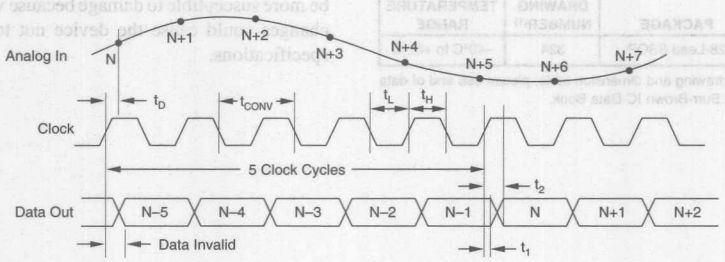
## PIN CONFIGURATION




## PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | $+V_S$ | Analog Supply |
| 2 | $LV_{DD}$ | Output Logic Driver Supply Voltage |
| 3 | Bit 10 | Data Bit 10 (D0) (LSB) |
| 4 | Bit 9 | Data Bit 9 (D1) |
| 5 | Bit 8 | Data Bit 8 (D2) |
| 6 | Bit 7 | Data Bit 7 (D3) |
| 7 | Bit 6 | Data Bit 6 (D4) |
| 8 | Bit 5 | Data Bit 5 (D5) |
| 9 | Bit 4 | Data Bit 4 (D6) |
| 10 | Bit 3 | Data Bit 3 (D7) |
| 11 | Bit 2 | Data Bit 2 (D8) |
| 12 | Bit 1 | Data Bit 1 (D9) (MSB) |
| 13 | GND | Analog Ground |
| 14 | GND | Analog Ground |
| 15 | CLK | Convert Clock Input |
| 16 | $\overline{OE}$ | Output Enable, Active Low |
| 17 | Pwrdn | Power Down Pin |
| 18 | $+V_S$ | Analog Supply |
| 19 | GND | Analog Ground |
| 20 | GND | Analog Ground |
| 21 | LpBy | Positive Ladder Bypass |
| 22 | NC | No Connection |
| 23 | $1V_{REF}$ | 1V Reference Output |
| 24 | $\overline{IN}$ | Complementary Input |
| 25 | LnBy | Negative Ladder Bypass |
| 26 | CM | Common-Mode Voltage Output |
| 27 | IN | Analog Input |
| 28 | $+V_S$ | Analog Supply |

## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 50 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 24 | 25 | | ns |
| $t_H$ | Clock Pulse High | 24 | 25 | | ns |
| $t_D$ | Aperture Delay | | 2 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12 | ns |

BURR-BROWN®




# ADS901

www.burr-brown.com/databook/ADS901.html

## SpeedPLUS™ 10-Bit, 20MHz, +3V Supply ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- LOW POWER: 48mW at +3V
- SUPPLY RANGE: +2.7V to +3.7V
- ADJUSTABLE FULL SCALE RANGE WITH EXTERNAL REFERENCES
- NO MISSING CODES
- WIDEBAND TRACK/HOLD: 350MHz
- POWER DOWN: 15mW
- 28-LEAD SSOP PACKAGE

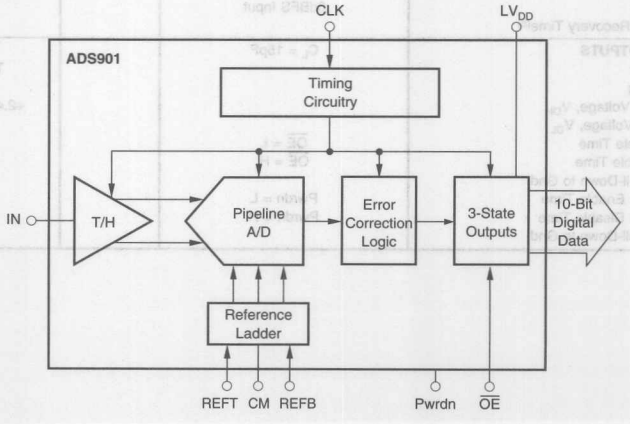
## APPLICATIONS

- BATTERY POWERED EQUIPMENT
- CAMCORDERS
- DIGITAL CAMERAS
- COMPUTER SCANNERS
- COMMUNICATIONS

## DESCRIPTION

The ADS901 is a high-speed pipelined analog-to-digital converter that operates from a +3V power supply. This complete converter includes a wide bandwidth track/hold and a 10-bit quantizer. The full scale input range is set by external references.

The ADS901 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for telecommunications, video and test instrumentation applications. The ADS901 is available in a 28-lead SSOP package.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = $LV_{DD}$ = +3V, REFB = 1V, REFT = 2V, Specified Input Range = 1V to 2V, Sampling Rate = 20MHz, unless otherwise specified.

| PARAMETER | CONDITIONS | TEMP | ADS901E MIN | ADS901E TYP | ADS901E MAX | UNITS |
|---|---|---|---|---|---|---|
| Resolution | | | | 10 | | Bits |
| Specified Temperature Range | Ambient Air | | –40 | | +85 | °C |
| **ANALOG INPUT** | | | | | | |
| Specified Full Scale Input Range[1] | | | | 1Vp-p | | V |
| Common-Mode Voltage (Midscale) | | | | 1.5 | | V |
| Analog Input Bias Current | | | | 1 | | µA |
| Input Impedance | | | | 1.25 ll 5 | | MΩ ll pF |
| **DIGITAL INPUT** | | | | | | |
| Logic Family | | | | TTL/HCT Compatible CMOS | | |
| Convert Command (Start Conversion) | Start Conversion | | | Rising Edge of Convert Clock | | |
| **CONVERSION CHARACTERISTICS** | | | | | | |
| Sample Rate | | Full | 10k | | 20M | Samples/s |
| Data Latency | | | | 5 | | Clk Cyc |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Differential Linearity Error (Largest Code Error) | | | | | | |
| f = 500kHz | | Full | | ±0.8 | ±1.0 | LSB |
| f = 9MHz | | Full | | ±0.9 | ±1.0 | LSB |
| No Missing Codes | | Full | | Guaranteed | | |
| Integral Nonlinearity Error, f = 500kHz | | Full | | ±3.5 | | LSB |
| Spurious Free Dynamic Range[2] | | | | | | |
| f = 500kHz (–1dBFS[3] input) | | Full | 45 | 50 | | dBFS[3] |
| f = 9MHz (–1dBFS input) | | Full | 45 | 49 | | dBFS |
| Two-Tone Intermodulation Distortion[4] | | | | | | |
| f = 4.5MHz and 5.5MHz (–7dBFS each tone) | | | | | | dBc |
| Signal-to-Noise Ratio (SNR) | Referred to Sinewave Input Signal | | | | | |
| f = 500kHz (–1dBFS input) | | Full | 48 | 53 | | dB |
| f = 9MHz (–1dBFS input) | | Full | 48 | 53 | | dB |
| Maximum SNR | Referred to DC Full Scale Input Signal | | | | | |
| f = 9MHz (–1dBFS input) | | | | 62 | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | | | | | | |
| f = 500kHz (–1dBFS input) | | Full | 46 | 50 | | dB |
| f = 3.58MHz (–1dBFS input) | | Full | | 50 | | dB |
| f = 9MHz (–1dBFS input) | | Full | 45 | 49 | | dB |
| Effective Number of Bits[5] | $f_{IN}$ = 3.58MHz | | | 8.0 | | Bits |
| Differential Gain Error | NTSC, PAL | | | 2.3 | | % |
| Differential Phase Error | NTSC, PAL | | | 1.0 | | degrees |
| Output Noise | Input Grounded | | | 0.2 | | LSB rms |
| Aperture Delay Time | | | | 3 | | ns |
| Aperture Jitter | | | | 7 | | ps rms |
| Analog Input Bandwidth | | | | | | |
| Small Signal | –20dBFS Input | | | 350 | | MHz |
| Full Power | 0dBFS Input | | | 100 | | MHz |
| Overvoltage Recovery Time[6] | | | | 2 | | ns |
| **DIGITAL OUTPUTS** | $C_L$ = 15pF | | | | | |
| Logic Family | | | | TTL/HCT Compatible CMOS | | |
| Logic Coding | | | | Straight Offset Binary | | |
| High Output Voltage, $V_{OH}$ | | | +2.4 | | $LV_{DD}$ | V |
| Low Output Voltage, $V_{OL}$ | | | | | +0.4 | V |
| 3-State Enable Time | $\overline{OE}$ = L | | | 20 | 40 | ns |
| 3-State Disable Time | $\overline{OE}$ = H | | | 18 | 10 | ns |
| Internal Pull-Down to Gnd | | | | 50 | | kΩ |
| Power-Down Enable Time | Pwrdn = L | | | 133 | | ns |
| Power-Down Disable Time | Pwrdn = H | | | 18 | | ns |
| Internal Pull-Down to Gnd | | | | 50 | | kΩ |

## SPECIFICATIONS (CONT)

At $T_A$ = +25°C, $V_S$ = $LV_{DD}$ = +3V, REFB = 1V, REFT = 2V, Specified Input Range = 1V to 2V, Sampling Rate = 20MHz, unless otherwise specified.

| PARAMETER | CONDITIONS | TEMP | ADS901E MIN | ADS901E TYP | ADS901E MAX | UNITS |
|---|---|---|---|---|---|---|
| **ACCURACY** | | | | | | |
| Gain Error | | Full | | 2.5 | | %FS |
| Input Offset[7] | | Full | | 0.4 | | %FS |
| Power Supply Rejection (Gain) | $\Delta V_S$ = +10% | Full | 42 | 56 | | dB |
| Power Supply Rejection (Offset) | | Full | 42 | 68 | | dB |
| External REFT Voltage Range | | Full | REFB +0.5 | 2 | $V_S$–0.8 | V |
| External REFB Voltage Range | | Full | 0.8 | 1 | REFT –0.5 | V |
| Reference Input Resistance | | | | 4 | | kΩ |
| **POWER SUPPLY REQUIREMENTS** | | | | | | |
| Supply Voltage: $+V_S$ | Operating | Full | +2.7 | +3.0 | +3.7 | V |
| Supply Current: $+I_S$ | Operating | Full | | 16 | | mA |
| Power Dissipation | Operating | Full | | 49 | 60 | mW |
| Power Dissipation (Power Down) | Operating | Full | | 15 | | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | | |
| 28-Lead SSOP | | | | 50 | | °C/W |

NOTES: (1) The single-ended input range is set by REFB and REFT values. (2) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (3) dBFS is dB relative to full scale. (4) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (5) Based on (SINAD - 1.76)/6.02. (6) No "Rollover" of bits. (7) Offset Deviation from Ideal Negative Full Scale.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Logic $V_{DD}$ | +6V |
| Analog Input | $+V_S$ +0.3V |
| Logic Input | $+V_S$ +0.3V |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +125°C |

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| ADS901E | 28-Lead SSOP | 324 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

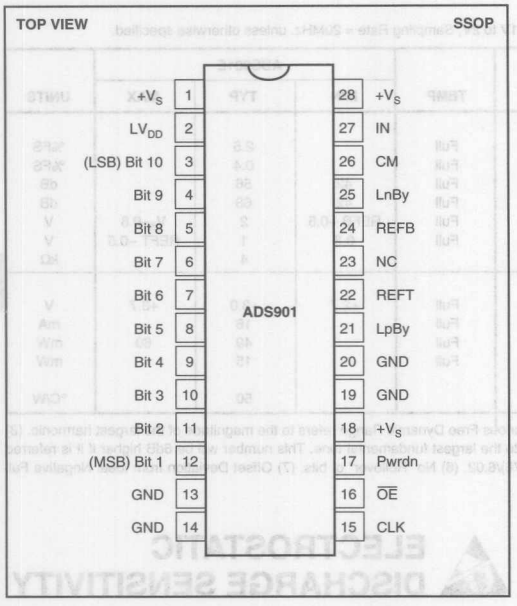
### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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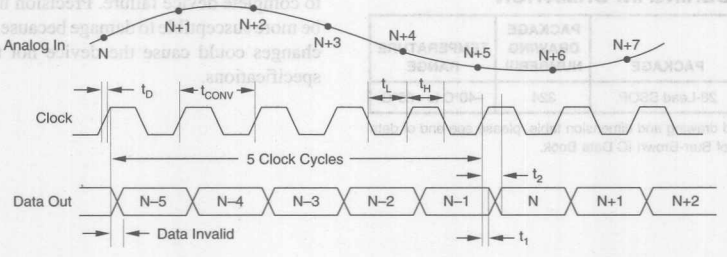
## PIN CONFIGURATION




## PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | $+V_S$ | Analog Supply |
| 2 | $LV_{DD}$ | Output Logic Driver Supply Voltage |
| 3 | Bit 10 | Data Bit 10 (D0) (LSB) |
| 4 | Bit 9 | Data Bit 9 (D1) |
| 5 | Bit 8 | Data Bit 8 (D2) |
| 6 | Bit 7 | Data Bit 7 (D3) |
| 7 | Bit 6 | Data Bit 6 (D4) |
| 8 | Bit 5 | Data Bit 5 (D5) |
| 9 | Bit 4 | Data Bit 4 (D6) |
| 10 | Bit 3 | Data Bit 3 (D7) |
| 11 | Bit 2 | Data Bit 2 (D8) |
| 12 | Bit 1 | Data Bit 1 (D9) (MSB) |
| 13 | GND | Analog Ground |
| 14 | GND | Analog Ground |
| 15 | CLK | Convert Clock Input |
| 16 | $\overline{OE}$ | Output Enable, Active Low |
| 17 | Pwrdn | Power Down Pin |
| 18 | $+V_S$ | Analog Supply |
| 19 | GND | Analog Ground |
| 20 | GND | Analog Ground |
| 21 | LpBy | Positive Ladder Bypass |
| 22 | REFT | Top Reference Input |
| 23 | NC | No Connection |
| 24 | REFB | Bottom Reference Input |
| 25 | LnBy | Negative Ladder Bypass |
| 26 | CM | Common-Mode Voltage Output |
| 27 | IN | Analog Input |
| 28 | $+V_S$ | Analog Supply |

## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 50 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 24 | 25 | | ns |
| $t_H$ | Clock Pulse High | 24 | 25 | | ns |
| $t_D$ | Aperture Delay | | 3 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12 | ns |

BURR - BROWN®




# ADS902

www.burr-brown.com/databook/ADS902.html

## SpeedPLUS™ 10-Bit, 30MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- HIGH SNR: 57dB
- EXTERNAL REFERENCE
- LOW POWER: 140mW
- ADJUSTABLE FULL SCALE RANGE
- POWER DOWN
- 28-PIN SSOP PACKAGE

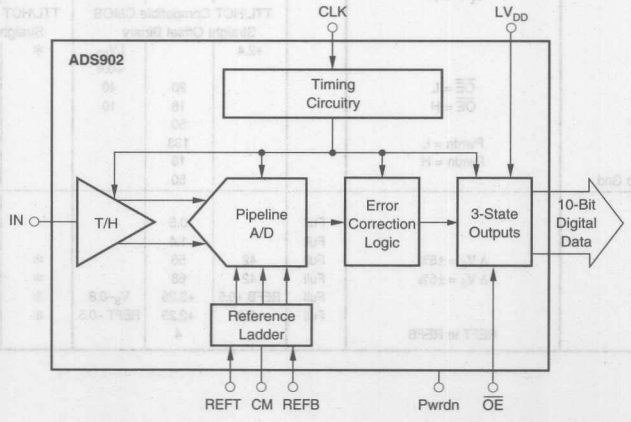
## APPLICATIONS

- BATTERY POWERED EQUIPMENT
- CAMCORDERS
- PORTABLE TEST EQUIPMENT
- COMPUTER SCANNERS
- COMMUNICATIONS

## DESCRIPTION

The ADS902 is a high speed pipelined analog-to-digital converter that is specified to operate from a single +5V supply. This converter includes a wide bandwidth track/hold and a 10-bit quantizer. The performance is specified with a single-ended input range of 2.25V to 3.25V, or 2V to 4V. The input range is set by the external reference values.

The ADS902 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for telecommunications, video and test instrumentation applications. This high performance A/D converter is specified to operate at a 30MHz sampling rate. The ADS902 is available in a 28-pin SSOP package.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = $LV_{DD}$ = +5V, REFB = +2.25V, REFT = +3.25V, Sampling Rate = 30MHz, unless otherwise specified.

| PARAMETER | CONDITIONS | TEMP | ADS902E 1Vp-p MIN | 1Vp-p TYP | 1Vp-p MAX | ADS902E 2Vp-p MIN | 2Vp-p TYP | 2Vp-p MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Resolution | | | | 10 | | | 10 | | Bits |
| Specified Temperature Range | Ambient Air | | –40 | | +85 | –40 | | +85 | °C |
| **ANALOG INPUT** | | | | | | | | | |
| Specified Full Scale Input Range[1] | | | | 1 | | | 2 | | Vp-p |
| Common-Mode Voltage (Midscale) | | | | +2.75 | | | 3 | | V |
| Track-Mode Input Bandwidth | | | | 350 | | | * | | MHz |
| Analog Input Bias Current | | | | 1 | | | * | | µA |
| Input Impedance | | | | 1.25 ll 5 | | | * | | MΩ ll pF |
| **DIGITAL INPUTS** | | | | | | | | | |
| Logic Family | | | | TTL/HCT Compatible CMOS | | | TTL/HCT Compatible CMOS | | |
| High Input Voltage, $V_{IH}$ | | | +2.0 | | $+V_S$ | * | | * | V |
| Low Input Voltage, $V_{IL}$ | | | | | +0.8 | | | * | V |
| High Input Current, $I_{IH}$ | | | | ±10 | | | * | | µA |
| Low Input Current, $I_{IL}$ | | | | ±10 | | | * | | µA |
| Input Capacitance | | | | 5 | | | * | | pF |
| **CONVERSION CHARACTERISTICS** | | | | | | | | | |
| Sample Rate | | Full | 10k | | 30M | * | | * | Samples/s |
| Data Latency | | | | 5 | | | * | | Clk Cyc |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | | |
| Differential Linearity Error (Largest Code Error) | | | | | | | | | |
| f = 500kHz | | Full | | ±0.3 | ±1.0 | | * | * | LSB |
| f = 12.5MHz | | Full | | ±0.3 | ±1.0 | | * | * | LSB |
| No Missing Codes | | Full | | Guaranteed | | | Guaranteed | | |
| Spurious-Free Dynamic Range | | | | | | | | | |
| f = 12.5MHz (–1dBFS[2] input) | | Full | | 53 | | 50 | 58 | | dB |
| Integral Nonlinearity Error, f = 500kHz | | Full | | ±2.0 | ±4.5 | | * | * | LSB |
| Signal-to-Noise Ratio (SNR) | Referred to Sinewave Input Signal | | | | | | | | |
| f = 500kHz (–1dBFS input) | | Full | 48 | 53 | | | | | dB |
| f = 12.5MHz (–1dBFS input) | | Full | 48 | 53 | | 52 | 57 | | dB |
| Maximum SNR | Referred to DC FS Input Signal | | | | | | | | |
| f = 9MHz (–1dBFS input) | | | | 62 | | | 66 | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | | | | | | | | | |
| f = 500kHz (–1dBFS input) | | Full | 46 | 50 | | | | | dB |
| f = 3.58MHz (–1dBFS input) | | Full | 45 | 50 | | | | | dB |
| f = 12.5MHz (–1dBFS) input) | | Full | 45 | 49 | | 47 | 53 | | dB |
| Effective Number of Bits[3], f =12.5MHz | | | | 7.8 | | | | | Bits |
| Output Noise | Input Grounded | | | 0.2 | | | * | | LSB rms |
| Aperture Delay Time | | | | 4 | | | * | | ns |
| Aperture Jitter | | | | 7 | | | * | | ps rms |
| **DIGITAL OUTPUTS** | $C_L$ = 15pF | | | | | | | | |
| Logic Family | | | | TTL/HCT Compatible CMOS | | | TTL/HCT Compatible CMOS | | |
| Logic Coding | | | | Straight Offset Binary | | | Straight Offset Binary | | |
| High Output Voltage, $V_{OH}$ | | | +2.4 | | $LV_{DD}$ | * | | * | V |
| Low Output Voltage, $V_{OL}$ | | | | | +0.4 | | | * | V |
| 3-State Enable Time | $\overline{OE}$ = L | | | 20 | 40 | | * | * | ns |
| 3-State Disable Time | $\overline{OE}$ = H | | | 18 | 10 | | * | * | ns |
| OE Internal Pull-Down to Gnd | | | | 50 | | | * | | kΩ |
| Power-Down Enable Time | Pwrdn = L | | | 133 | | | * | | ns |
| Power-Down Disable Time | Pwrdn = H | | | 18 | | | * | | ns |
| Power-Down Internal Pull-Down to Gnd | | | | 50 | | | * | | kΩ |
| **ACCURACY** | | | | | | | | | |
| Gain Error | | Full | | 0.5 | | | 1 | | %FS |
| Input Offset Error[4] | | Full | | 1.4 | | | * | | %FS |
| Power Supply Rejection (Gain) | $\Delta V_S$ = ±5% | Full | 42 | 56 | | * | * | | dB |
| Power Supply Rejection (Offset) | $\Delta V_S$ = ±5% | Full | 42 | 68 | | * | * | | dB |
| External REFT Voltage Range | | Full | REFB +0.5 | +3.25 | $V_S$–0.8 | * | +4 | * | V |
| External REFB Voltage Range | | Full | +0.8 | +2.25 | REFT –0.5 | * | +2 | * | V |
| Reference Input Resistance | REFT to REFB | | | 4 | | | * | | kΩ |

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## SPECIFICATIONS (CONT)

At $T_A$ = +25°C, $V_S$ = $LV_{DD}$ = +5V, REFB = +2.25V, REFT = +3.25V, Sampling Rate = 30MHz, unless otherwise specified.

| PARAMETER | CONDITIONS | TEMP | ADS902E | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1Vp-p | | | 2Vp-p | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | | |
| Supply Voltage: $+V_S$ | | Full | +4.25 | +5.0 | +5.25 | * | * | * | V |
| Supply Current: $+I_S$ | | Full | | 28 | | | * | | mA |
| Power Dissipation | | Full | | 140 | 160 | | * | * | mW |
| Power Dissipation (Power Down) | | Full | | 15 | | | * | | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | | |
| 28-Pin SSOP | | | | 50 | | | * | | °C/W |

* Specification same as 1Vp-p.

NOTES: (1) The single-ended input range is set by REFB and REFT values. (2) dBFS means dB relative to Full Scale. (3) Effective number of bits (ENOB) is defined by (SINAD – 1.76)/6.02. (4) Offset deviation from ideal negative full scale.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$, $LV_{DD}$ | +6V |
| Analog Input | $+V_S$ +0.3V |
| Logic Input | $+V_S$ +0.3V |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +150°C |

### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

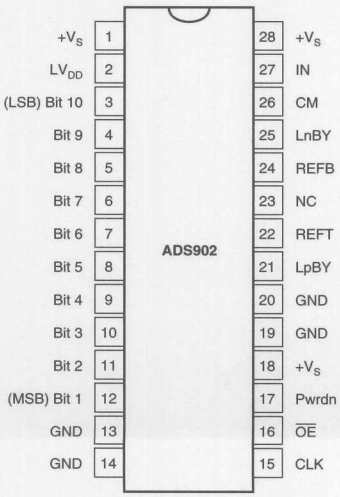
### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS902E | 28-Pin SSOP | 324 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### PIN CONFIGURATION

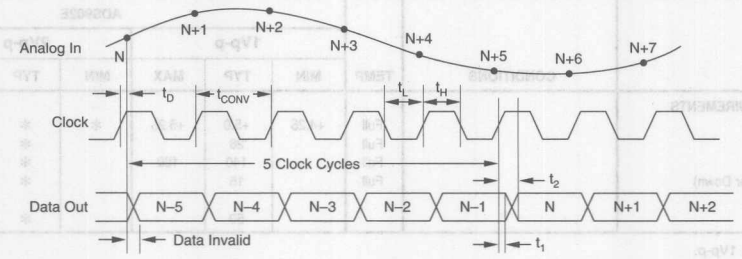
Top View SSOP




### PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | $+V_S$ | Analog Supply |
| 2 | $LV_{DD}$ | Output Logic Driver Supply Voltage |
| 3 | Bit 10 | Data Bit 10 (D0, LSB) |
| 4 | Bit 9 | Data Bit 9 (D1) |
| 5 | Bit 8 | Data Bit 8 (D2) |
| 6 | Bit 7 | Data Bit 7 (D3) |
| 7 | Bit 6 | Data Bit 6 (D4) |
| 8 | Bit 5 | Data Bit 5 (D5) |
| 9 | Bit 4 | Data Bit 4 (D6) |
| 10 | Bit 3 | Data Bit 3 (D7) |
| 11 | Bit 2 | Data Bit 2 (D8) |
| 12 | Bit 1 | Data Bit 1 (D9, MSB) |
| 13 | GND | Analog Ground |
| 14 | GND | Analog Ground |
| 15 | CLK | Convert Clock Input |
| 16 | $\overline{OE}$ | Output Enable, Active Low |
| 17 | Pwrdn | Power Down Pin |
| 18 | $+V_S$ | Analog Supply |
| 19 | GND | Analog Ground |
| 20 | GND | Analog Ground |
| 21 | LpBy | Positive Ladder Bypass |
| 22 | REFT | Top Reference |
| 23 | NC | No Connection |
| 24 | REFB | Bottom Reference |
| 25 | LnBy | Negative Ladder Bypass |
| 26 | CM | Common-Mode Voltage Output |
| 27 | IN | Analog Input |
| 28 | $+V_S$ | Analog Supply |

## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 33 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 15.5 | 16.5 | | ns |
| $t_H$ | Clock Pulse High | 15.5 | 16.5 | | ns |
| $t_D$ | Aperture Delay | | 2 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 4 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12 | ns |

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# ADS930

www.burr-brown.com/databook/ADS930.html

## SpeedPLUS™ 8-Bit, 30MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- +3V TO +5V SUPPLY OPERATION
- INTERNAL REFERENCE
- SINGLE-ENDED INPUT RANGE: 1V to 2V
- LOW POWER: 66mW at +3V
- HIGH SNR: 46dB
- LOW DNL: 0.4LSB
- 28-LEAD SSOP PACKAGE

## APPLICATIONS

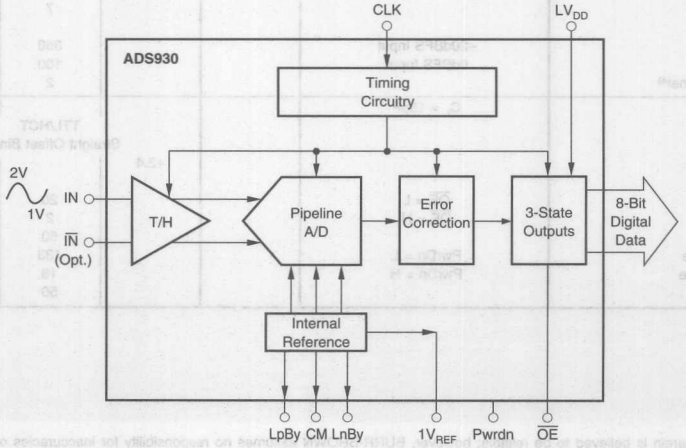
- BATTERY POWERED EQUIPMENT
- CAMCORDERS
- PORTABLE TEST EQUIPMENT
- COMPUTER SCANNERS
- COMMUNICATIONS

## DESCRIPTION

The ADS930 is a high speed pipelined analog-to-digital converter specified to operate from nominal +3V or +5V power supplies with tolerances of up to 10%. This complete converter includes a high bandwidth track/hold, a 8-bit quantizer and an internal reference.

The ADS930 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for telecommunications, video and test instrumentation applications.

This high performance A/D converter is specified for performance at a 30MHz sampling rate. The ADS930 is available in a 28-lead SSOP package.




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# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = +3V, Single-ended Input and Sampling Rate = 30MHz, unless otherwise specified.

| PARAMETER | CONDITIONS | TEMP | ADS930E MIN | ADS930E TYP | ADS930E MAX | UNITS |
|---|---|---|---|---|---|---|
| **RESOLUTION** | | | | 8 | | Bits |
| Specified Temperature Range | Ambient Air | | –40 | | +85 | °C |
| **ANALOG INPUT** | | | | | | |
| Differential Full Scale Input Range | 0.5Vp-p | | 1.25 | | 1.75 | V |
| Single-Ended Full Scale Input Range | 1Vp-p | | 1.0 | | 2.0 | V |
| Common-mode Voltage | | | | 1.5 | | V |
| Analog Input Bias Current | | | | 1 | | µA |
| Input Impedance | | | | 1.25 ll 5 | | MΩ ll pF |
| **DIGITAL INPUTS** | | Full | | | | |
| Logic Family | | | | TTL/HCT Compatible CMOS | | |
| High Input Voltage, $V_{IH}$ | | | 2.0 | | $V_{DD}$ | V |
| Low Input Voltage, $V_{IL}$ | | | | | 0.8 | V |
| High Input Current, $I_{IH}$ | | | | ±10 | | µA |
| Low Input Current, $I_{IL}$ | | | | ±10 | | µA |
| Input Capacitance | | | | 5 | | pF |
| **CONVERSION CHARACTERISTICS** | | | | | | |
| Start Conversion | | | | Rising Edge of Convert Clock | | |
| Sample Rate | | Full | 10k | | 20M | Samples/s |
| Data Latency | | | | 5 | | Clk Cyc |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Differential Linearity Error | | | | | | |
| f = 500kHz | Largest Code Error | Full | | ±0.4 | ±1 | LSB |
| f = 12MHz | Largest Code Error | Full | | ±0.4 | ±1 | LSB |
| No Missing Codes | | Full | | Guaranteed | | |
| Integral Nonlinearity Error, f = 500kHz | | Full | | ±1.0 | ±2.5 | LSB |
| Spurious Free Dynamic Range[1] | | | | | | |
| f = 500kHz (–1dBFS input) | | Full | 46 | 51 | | dBFS[2] |
| f = 12MHz (–1dB input) | | Full | 46 | 50 | | dBFS |
| Two-Tone Intermodulation Distortion[3] | | | | | | |
| f = 3.4MHz and 3.5MHz (–7dBFS each tone) | | | | 54 | | dBc |
| Signal-to-Noise Ratio (SNR) | | | | | | |
| f = 500kHz (–1dBFS input) | | Full | 44 | 46 | | dB |
| f = 12MHz (–1dBFS input) | | Full | 44 | 46 | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | | | | | | |
| f = 500kHz (–1dBFS input) | | Full | 43 | 45 | | dB |
| f = 3.58MHz (–1dBFS input) | | Full | 42 | 45 | | dB |
| f = 12MHz (–1dBFS input) | | Full | 42 | 45 | | dB |
| Differential Gain Error | NTSC, PAL | | | 2.3 | | % |
| Differential Phase Error | NTSC, PAL | | | 1 | | degrees |
| Output Noise | Input Grounded | | | 0.2 | | LSBs rms |
| Aperture Delay Time | | | | 2 | | ns |
| Aperture Jitter | | | | 7 | | ps rms |
| Analog Input Bandwidth | | | | | | |
| Small Signal | –20dBFS Input | | | 350 | | MHz |
| Full Power | 0dBFS Input | | | 100 | | MHz |
| Overvoltage Recovery Time[4] | | | | 2 | | ns |
| **DIGITAL OUTPUTS** | $C_L$ = 15pF | | | | | |
| Logic Family | | | | TTL/HCT | | |
| Logic Coding | | | | Straight Offset Binary | | |
| High Output Voltage, $V_{OH}$ | | | +2.4 | | $LV_{DD}$ | V |
| Low Output Voltage, $V_{OL}$ | | | | | 0.4 | V |
| 3-State Enable Time | $\overline{OE}$ = L | | | 20 | 40 | ns |
| 3-State Disable Time | $\overline{OE}$ = H | | | 2 | 10 | ns |
| Internal Pull-Down | | | | 50 | | kΩ |
| Power-Down Enable Time | PwrDn = L | | | 133 | | ns |
| Power-Down Disable Time | PwrDn = H | | | 18 | | ns |
| Internal Pull-Down | | | | 50 | | kΩ |

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## SPECIFICATIONS (CONT)

At $T_A$ = +25°C, $V_S$ = +3V, Single-ended Input and Sampling Rate = 30MHz, unless otherwise specified.

| PARAMETER | CONDITIONS | TEMP | ADS930E MIN | ADS930E TYP | ADS930E MAX | UNITS |
|---|---|---|---|---|---|---|
| **ACCURACY** | | | | | | |
| Gain Error | | Full | | 5.9 | 10 | %FS |
| Input Offset | Referred to Ideal Midscale | Full | | ±10 | ±60 | mV |
| Power Supply Rejection (Gain) | $\Delta V_S$ = +10% | Full | 42 | 56 | | dB |
| Power Supply Rejection (Offset) | | Full | 42 | 56 | | dB |
| Internal Positive Reference Voltage | | Full | | +1.75 | | V |
| Internal Negative Reference Voltage | | Full | | +1.25 | | V |
| **POWER SUPPLY REQUIREMENTS** | | | | | | |
| Supply Voltage: $+V_S$ | Operating | Full | +2.7 | +3.0 | +5.25 | V |
| Supply Current: $+I_S$ | Operating, +3V | Full | | 22 | | mA |
| Power Dissipation | Operating, +3V | Full | | 66 | 84 | mW |
| | Operating, +5V | Full | | 168 | | mW |
| Power Dissipation (Power Down) | Operating, +3V | Full | | 10 | | mW |
| | Operating, +5V | Full | | 15 | | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | | |
| 28-Lead SSOP | | | | 50 | | °C/W |

NOTES: (1) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to full scale. (3) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (4) No "Rollover" of bits.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Analog Input | $+V_S$ +0.3V |
| Logic Input | $+V_S$ +0.3V |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +150°C |

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS930E | 28-Lead SSOP | 324 | –40°C to +85°C |

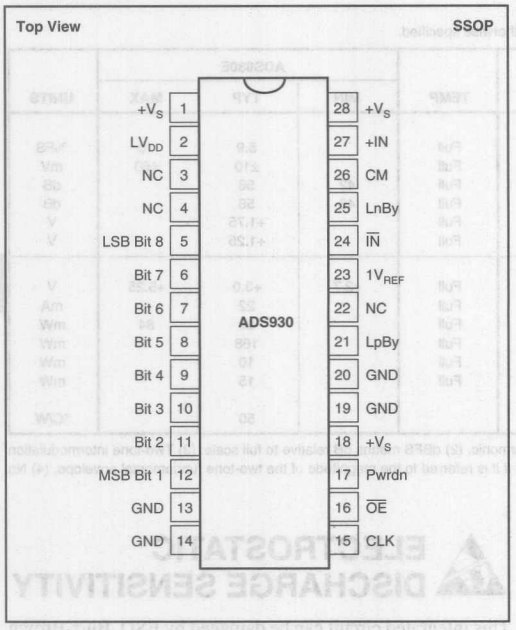
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

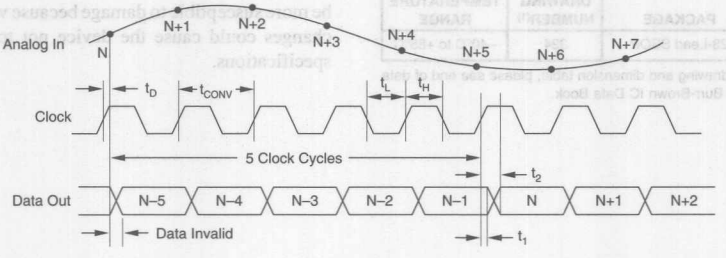
## PIN CONFIGURATION




## PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | $+V_S$ | Analog Supply |
| 2 | $LV_{DD}$ | Output Logic Driver Supply Voltage |
| 3 | NC | No Connection |
| 4 | NC | No Connection |
| 5 | Bit 8 (LSB) | Data Bit 8 (D7) |
| 6 | Bit 7 | Data Bit 7 (D6) |
| 7 | Bit 6 | Data Bit 6 (D5) |
| 8 | Bit 5 | Data Bit 5 (D4) |
| 9 | Bit 4 | Data Bit 4 (D3) |
| 10 | Bit 3 | Data Bit 3 (D2) |
| 11 | Bit 2 | Data Bit 2 (D1) |
| 12 | Bit 1(MSB) | Data Bit 1 (D0) |
| 13 | GND | Analog Ground |
| 14 | GND | Analog Ground |
| 15 | CLK | Convert Clock Input |
| 16 | $\overline{OE}$ | Output Enable, Active Low |
| 17 | Pwrdn | Power Down Pin |
| 18 | $+V_S$ | Analog Supply |
| 19 | GND | Analog Ground |
| 20 | GND | Analog Ground |
| 21 | LpBy | Positive Ladder Bypass |
| 22 | NC | No Connection |
| 23 | $1V_{REF}$ | 1V Reference Output |
| 24 | $\overline{IN}$ | Complementary Input |
| 25 | LnBy | Negative Ladder Bypass |
| 26 | CM | Common-Mode Voltage Output |
| 27 | +IN | Analog Input |
| 28 | $+V_S$ | Analog Supply |

## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 33 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 15.5 | 16.5 | | ns |
| $t_H$ | Clock Pulse High | 15.5 | 16.5 | | ns |
| $t_D$ | Aperture Delay | | 2 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12 | ns |

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# ADS931

www.burr-brown.com/databook/ADS931.html



## SpeedPLUS™ 8-Bit, 30MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- +2.7V TO +5.5V SUPPLY OPERATION
- LOW POWER: 69mW at +3V
- ADJUSTABLE FULL SCALE RANGE WITH EXTERNAL REFERENCE
- NO MISSING CODES
- POWER DOWN
- 28-LEAD SSOP PACKAGE

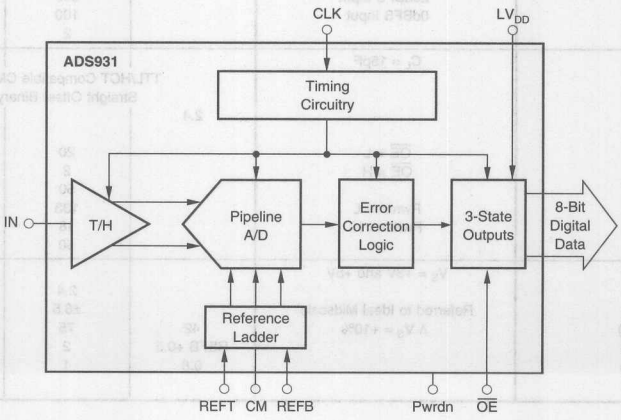
## APPLICATIONS

- BATTERY POWERED EQUIPMENT
- CAMCORDERS
- PORTABLE TEST EQUIPMENT
- DIGITAL CAMERAS
- COMMUNICATIONS

## DESCRIPTION

The ADS931 is a high speed pipelined analog-to-digital converter that is specified to operate from standard +5V or +3V power supplies. This converter includes a high bandwidth track/hold and an 8-bit quantizer. The performance is specified with a single-ended input range of 1V to 2V when operating off of a +3V supply. This device also allows for standard input ranges such as 2V to 4V or 2V to 3V, when operating on +5V supplies. The full scale input range is set by an external reference.

The ADS931 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for telecommunications, video and test instrumentation applications. This high performance A/D converter is specified for performance at a 30MHz sampling rate. The ADS931 is available in a 28-Lead SSOP package.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

At $T_A$ = full specified temperature range unless otherwise noted. $+V_S = LV_{DD} = +3V$, specified single-ended input (1V to 2V) and sampling rate = 30MHz, unless otherwise specified. The input range is 2.25V to 3.25V when specified for +5V operation.

| PARAMETER | CONDITIONS | ADS931E MIN | ADS931E TYP | ADS931E MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | 8 | | Bits |
| **SPECIFIED TEMPERATURE RANGE** | Ambient Air | | –40 to +85 | | °C |
| **ANALOG INPUT** | | | | | |
| Specified Full Scale Input Range[1] | 1Vp-p | +1.0 | | +2.0 | V |
| Common-mode Voltage | | | +1.5 | | V |
| Analog Input Bias Current | | | 1 | | µA |
| Input Impedance | | | 1.25 ll 5 | | MΩ ll pF |
| **DIGITAL INPUTS** | | | | | |
| Logic Family | | | TTL/HCT Compatible CMOS | | |
| High Input Voltage, $V_{IH}$ | | +2.0 | | $LV_{DD}$ | V |
| Low Input Voltage, $V_{IL}$ | | | | +0.8 | V |
| High Input Current, $I_{IH}$ | | | ±10 | | µA |
| Low Input Current, $I_{IL}$ | | | ±10 | | µA |
| Input Capacitance | | | 5 | | pF |
| **CONVERSION CHARACTERISTICS** | | | | | |
| Start Conversion | | | Rising Edge of Convert Clock | | |
| Sample Rate | | 10k | | 30M | Samples/s |
| Data Latency | | | 5 | | Clk Cycles |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Differential Linearity Error | $V_S$ = +3V and +5V | | | | |
| f = 500MHz | | | ±0.7 | ±1.0 | LSB |
| f = 12.5MHz | | | ±0.7 | | LSB |
| No Missing Codes | $V_S$ = +3V and +5V | | Guaranteed | | |
| Integral Nonlinearity Error, f = 500kHz | $V_S$ = +3V and +5V | | ±1.0 | ±2.5 | LSB |
| Spurious Free Dynamic Range[2] | $V_S$ = +3V and +5V | | | | |
| f = 500kHz (–1dBFS input) | | | 49 | | dBFS[3] |
| f = 12.5MHz (–1dBFS input) | | 43 | 49 | | dBFS |
| Two-Tone Intermodulation Distortion[4] | | | | | |
| f = 3.6MHz and 3.5MHz (–7dBFS each tone) | | | 54 | | dBFS |
| Signal-to-Noise Ratio (SNR) | $V_S$ = +3V and +5V | | | | |
| f = 500kHz (–1dBFS input) | | | 48 | | dB |
| f = 12.5MHz (–1dBFS input) | | 44 | 48 | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | $V_S$ = +3V and +5V | | | | |
| f = 500kHz (–1dBFS input) | | | 45 | | dB |
| f = 12.5MHz (–1dBFS input) | | 40 | 45 | | dB |
| Effective Number of Bits | f = 12MHz[5] | | 7.2 | | Bits |
| Differential Gain Error | NTSC, PAL | | 2.3 | | % |
| Differential Phase Error | NTSC, PAL | | 1 | | degrees |
| Output Noise | Input AC-Grounded | | 0.2 | | LSBs rms |
| Aperture Delay Time | | | 2 | | ns |
| Aperture Jitter | | | 7 | | ps rms |
| Analog Input Bandwidth | | | | | |
| Small Signal | –20dBFS Input | | 350 | | MHz |
| Full Power | 0dBFS Input | | 100 | | MHz |
| Overvoltage Recovery Time[6] | | | 2 | | ns |
| **DIGITAL OUTPUTS** | $C_L$ = 15pF | | | | |
| Logic Family | | | TTL/HCT Compatible CMOS | | |
| Logic Coding | | | Straight Offset Binary | | |
| High Output Voltage, $V_{OH}$ | | 2.4 | | $V_{DD}$ | V |
| Low Output Voltage, $V_{OL}$ | | | | 0.4 | V |
| 3-State Enable Time | $\overline{OE}$ = L | | 20 | 40 | ns |
| 3-State Disable Time | $\overline{OE}$ = H | | 2 | 10 | ns |
| Internal Pull-Down | | | 50 | | kΩ |
| Power-Down Enable Time | Pwrdn = L | | 133 | | ns |
| Power-Down Disable Time | Pwrdn = H | | 18 | | ns |
| Internal Pull-Down | | | 50 | | kΩ |
| **ACCURACY** | $V_S$ = +3V and +5V | | | | |
| Gain Error | | | 2.4 | 3.5 | %FS |
| Input Offset[7] | Referred to Ideal Midscale | | ±6.5 | ±25 | mV |
| Power Supply Rejection (Gain) | Δ $V_S$ = +10% | 42 | 75 | | dB |
| External REFT Voltage Range | | REFB +0.5 | 2 | $V_S$–0.8 | V |
| External REFB Voltage Range | | 0.8 | 1 | REFT –0.5 | V |
| Reference Input Resistance | | | | 4 | kΩ |

## SPECIFICATIONS (CONT)

At $T_A$ = full specified temperature range unless otherwise noted. $+V_S = LV_{DD} = +3V$, specified single-ended input (1V to 2V) and sampling rate = 30MHz, unless otherwise specified. The input range is 2.25V to 3.25V when specified for +5V operation.

| PARAMETER | CONDITIONS | ADS931E MIN | ADS931E TYP | ADS931E MAX | UNITS |
|---|---|---|---|---|---|
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Supply Voltage: $+V_S$ | Operating | +2.7 | +3.0 | +5.5 | V |
| Supply Current: $+I_S$ | $V_S$ = +3V | | 23 | 29 | mA |
| Power Dissipation | $V_S$ = +3V | | 69 | 87 | mW |
| | $V_S$ = +5V | | 154 | | mW |
| Power Dissipation (Power Down) | $V_S$ = +3V | | 10 | | mW |
| | $V_S$ = +5V | | 15 | | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| 28-Lead SSOP | | | 50 | | °C/W |

NOTES: (1) The single-ended input range is set by REFB and REFT values. (2) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (3) dBFS is dB relative to full scale. (4) Two-tone intermodulation distortion is referred to as the largest fundamental tone. (5) Based on (SINAD –1.76)/6.02. (6) No "Rollover" of bits. (7) Offset deviation from ideal negative full scale.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Analog Input | (–0.3V) to ($+V_S$ +0.3V) |
| Logic Input | (–0.3V) to ($+V_S$ +0.3V) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +150°C |

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS931E | 28-Lead SSOP | 324 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

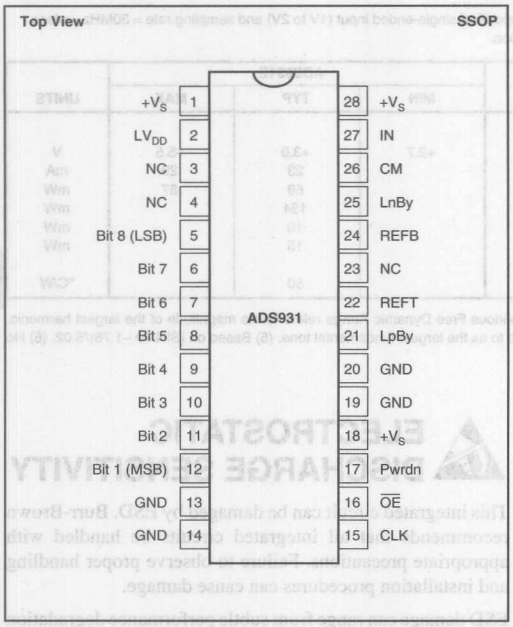
### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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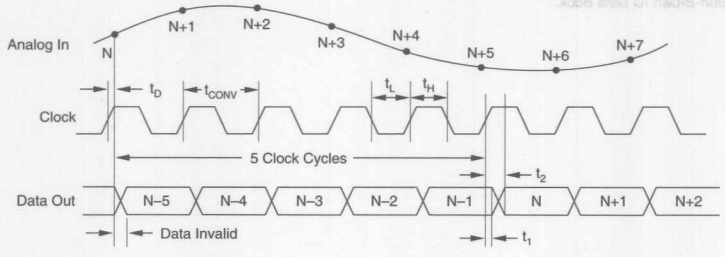
## PIN CONFIGURATION




## PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | $+V_S$ | Analog Supply |
| 2 | $LV_{DD}$ | Output Logic Driver Supply Voltage |
| 3 | NC | No Connection |
| 4 | NC | No Connection |
| 5 | Bit 8 (LSB) | Data Bit 8 (D7) LSB |
| 6 | Bit 7 | Data Bit 7 (D6) |
| 7 | Bit 6 | Data Bit 6 (D5) |
| 8 | Bit 5 | Data Bit 5 (D4) |
| 9 | Bit 4 | Data Bit 4 (D3) |
| 10 | Bit 3 | Data Bit 3 (D2) |
| 11 | Bit 2 | Data Bit 2 (D1) |
| 12 | Bit 1 (MSB) | Data Bit 1 (D0) MSB |
| 13 | GND | Analog Ground |
| 14 | GND | Analog Ground |
| 15 | CLK | Convert Clock Input |
| 16 | $\overline{OE}$ | Output Enable, Active Low |
| 17 | Pwrdn | Power Down Pin |
| 18 | $+V_S$ | Analog Supply |
| 19 | GND | Analog Ground |
| 20 | GND | Analog Ground |
| 21 | LpBy | Positive Ladder Bypass |
| 22 | REFT | Reference Voltage Top |
| 23 | NC | No Connection |
| 24 | REFB | Reference Voltage Bottom |
| 25 | LnBy | Negative Ladder Bypass |
| 26 | CM | Common-Mode Pin |
| 27 | IN | Analog Input |
| 28 | $+V_S$ | Analog Supply |

## TIMING DIAGRAM




| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 33 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 15.5 | 16.5 | | ns |
| $t_H$ | Clock Pulse High | 15.5 | 16.5 | | ns |
| $t_D$ | Aperture Delay | | 2 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12 | ns |

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# ADS1201

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

www.burr-brown.com/databook/ADS1201.html



# High Dynamic Range DELTA-SIGMA MODULATOR

## FEATURES

- 130dB DYNAMIC RANGE
- FULLY DIFFERENTIAL INPUT
- TWO-WIRE INTERFACE
- INTERNAL/EXTERNAL REFERENCE
- ON CHIP SELF-CALIBRATION

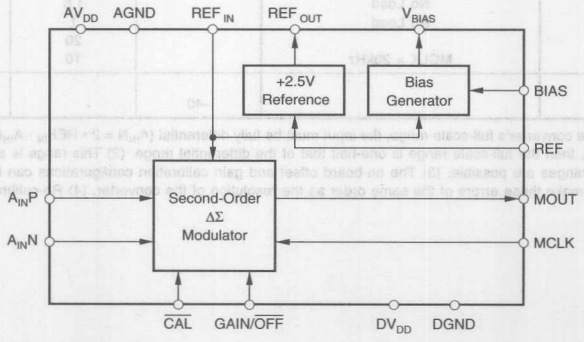
## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- INSTRUMENTATION
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTS
- WEIGH SCALES
- PRESSURE TRANSDUCERS

## DESCRIPTION

The ADS1201 is a precision, 130dB dynamic range, delta-sigma (ΔΣ) modulator operating from a single +5V supply. The differential inputs are ideal for direct connection to transducers or low level signals. With the appropriate digital filter and modulator rate, the device can be used to achieve 24-bit analog-to-digital (A/D) conversion with no missing codes. Effective resolution of 20-bits can be maintained up to a sample rate of 1kHz with a modulator rate of 320kHz.

The ADS1201 is designed for use in high resolution measurement applications including smart transmitters, industrial process control, weigh scales, chromatography, and portable instrumentation. It is available in a 16-lead SOIC package.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = +25°C, $AV_{DD}$ = $DV_{DD}$ = +5V, MCLK = 320kHz, $REF_{OUT}$ disabled, $V_{BIAS}$ disabled, and external +2.5V reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS1201U MIN | ADS1201U TYP | ADS1201U MAX | UNITS |
|---|---|---|---|---|---|
| **ANALOG INPUT** | | | | | |
| Input Voltage Range[1] | | 0 | | +5 | V |
| | With $V_{BIAS}$[2] | –10 | | +10 | V |
| Input Impedance | | | 4 | | MΩ |
| Input Capacitance | | | 8 | | pF |
| Input Leakage Current | | | 5 | 50 | pA |
| **SYSTEM PERFORMANCE** | | | | | |
| Dynamic Range | 10Hz Bandwidth | | 134 | | dB |
| | 60Hz Bandwidth | TBD | 130 | | dB |
| | 1kHz Bandwidth | | 120 | | dB |
| Integral Linearity Error | 60Hz Bandwidth | | | ±0.0015 | %FSR |
| | 1kHz Bandwidth | | | ±0.0015 | %FSR |
| Unipolar Offset Error[3] | | | TBD | | |
| Unipolar Offset Drift[4] | | | 1 | | µV/°C |
| Gain Error[3] | | | TBD | | |
| Gain Error Drift[4] | | | 1 | | µV/°C |
| Common-Mode Rejection | At DC | 80 | 100 | | dB |
| Power Supply Rejection | | | 60 | | dB |
| **REFERENCE** | | | | | |
| Internal Reference ($REF_{OUT}$) | | 2.4 | 2.5 | 2.6 | V |
| Drift | | | 25 | | ppm/°C |
| Noise | | | 50 | | µVp-p |
| Load Current | Source or Sink | | | 1 | mA |
| Output Impedance | | | 2 | | Ω |
| External Reference ($REF_{IN}$) | | 2.0 | | 3.0 | V |
| Load Current | | | | 2.5 | µA |
| $V_{BIAS}$ Output | Using Internal Reference | 3.15 | 3.3 | 3.45 | V |
| Drift | | | 50 | | ppm/°C |
| Load Current | | | | 10 | mA |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic Family | | | TTL Compatible CMOS | | |
| Logic Levels: | | | | | |
| $V_{IH}$ | $I_{IH}$ = +5µA | 2.0 | | $DV_{DD}$ +0.3 | V |
| $V_{IL}$ | $I_{IL}$ = +5µA | –0.3 | | 0.8 | V |
| $V_{OH}$ | $I_{OH}$ = 2 TTL Loads | 2.4 | | | V |
| $V_{OL}$ | $I_{OL}$ = 2 TTL Loads | | | 0.4 | V |
| MCLK Frequency | | TBD | | 10 | MHz |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Power Supply Voltage | Specified Performance | 4.75 | | 5.25 | V |
| Supply Current | | | | | |
| Analog Current | | | 4 | | mA |
| Digital Current | | | 0.1 | | mA |
| Additional Analog Current with | | | | | |
| $REF_{OUT}$ Enabled | No Load | | 1.6 | | mA |
| $V_{BIAS}$ Enabled | No Load | | 1 | | mA |
| Power Dissipation | | | 20 | TBD | mW |
| | MCLK = 20kHz | | 10 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified Performance | | –40 | | +85 | °C |

NOTES: (1) In order to achieve the converter's full-scale range, the input must be fully differential ($A_{IN}N = 2 \bullet REF_{IN} - A_{IN}P$). If the input is single-ended ($A_{IN}N$ or $A_{IN}P$ is held at a fixed voltage), then the full-scale range is one-half that of the differential range. (2) This range is set with external resistors and $V_{BIAS}$ (as described in the text). Other ranges are possible. (3) The on-board offset and gain calibration configurations can be used along with the appropriate software calibration algorithms to make these errors of the same order as the resolution of the converter. (4) Re-calibration can remove these errors.

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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Input: Current | ±100mA, Momentary |
| | ±10mA, Continuous |
| Voltage | AGND –0.3V to $AV_{DD}$ +0.3V |
| $AV_{DD}$ to $DV_{DD}$ | –0.3V to 6V |
| $AV_{DD}$ to AGND | –0.3V to 6V |
| $DV_{DD}$ to DGND | –0.3V to 6V |
| AGND to DGND | ±0.3V |
| $REF_{IN}$ Voltage to AGND | –0.3V to $AV_{DD}$ +0.3V |
| Digital Input Voltage to DGND | –0.3V to $DV_{DD}$ +0.3V |
| Digital Output Voltage to DGND | –0.3V to $DV_{DD}$ +0.3V |
| Lead Temperature (soldering, 10s) | +300°C |
| Internal Power Dissipation | 500mW |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

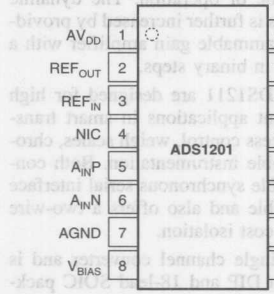
## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| ADS1201U | 16-Lead SOIC | 211 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN CONFIGURATION

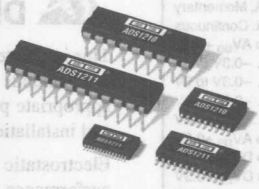
Top View SOIC




## PIN DESCRIPTIONS

| PIN NO | NAME | DESCRIPTION |
|---|---|---|
| 1 | $AV_{DD}$ | Analog Supply, +5V nominal. |
| 2 | $REF_{OUT}$ | Internal Reference Voltage Output: +2.5V nominal. |
| 3 | $REF_{IN}$ | Reference Voltage Input. |
| 4 | NIC | Not Internally Connected. |
| 5 | $A_{IN}P$ | Noninverting Input. |
| 6 | $A_{IN}N$ | Inverting Input. |
| 7 | AGND | Analog Ground. |
| 8 | $V_{BIAS}$ | Bias Voltage Output, nominally +3.3V (with +2.5V reference). |
| 9 | BIAS | Bias Voltage Enable Input (HIGH = enabled, LOW = disabled). |
| 10 | GAIN/$\overline{OFF}$ | Gain/Offset Calibration Select Input (with CAL LOW; HIGH = gain configuration, LOW = offset configuration). |
| 11 | $\overline{CAL}$ | Calibration Control Input (HIGH = normal operation, LOW = gain or offset calibration configuration). |
| 12 | DGND | Digital Ground. |
| 13 | $DV_{DD}$ | Digital Supply, +5V nominal. |
| 14 | MCLK | Modulator Clock Input. |
| 15 | MOUT | Modulator Output. |
| 16 | REF | Internal Reference Voltage Enable Input (HIGH = enabled, LOW = disabled). |

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# ADS1210
# ADS1211

www.burr-brown.com/databook/ADS1210.html

# 24-Bit ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- DELTA-SIGMA A/D CONVERTER
- 24 BITS NO MISSING CODES
- 23 BITS EFFECTIVE RESOLUTION AT 10Hz AND 20 BITS AT 1000Hz
- DIFFERENTIAL INPUTS
- PROGRAMMABLE GAIN AMPLIFIER
- FLEXIBLE SPI COMPATIBLE SSI INTERFACE WITH 2-WIRE MODE
- PROGRAMMABLE CUT-OFF FREQUENCY UP TO 15.6kHz
- INTERNAL/EXTERNAL REFERENCE
- ON CHIP SELF-CALIBRATION
- ADS1211 INCLUDES 4 CHANNEL MUX

## APPLICATIONS

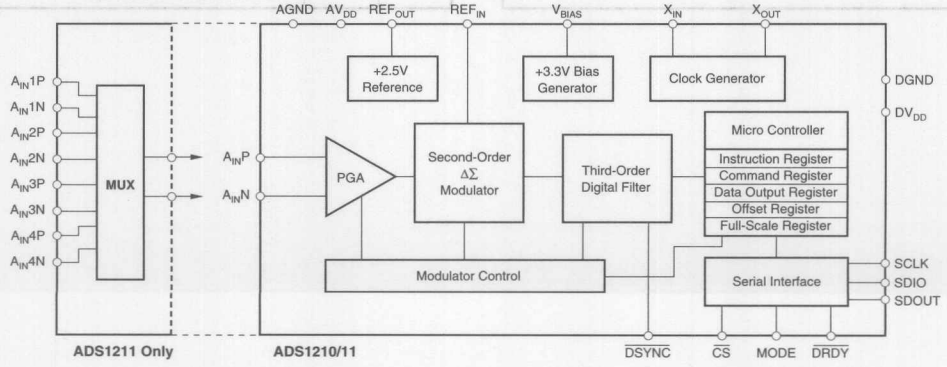
- INDUSTRIAL PROCESS CONTROL
- INSTRUMENTATION
- BLOOD ANALYSIS
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTS
- WEIGH SCALES
- PRESSURE TRANSDUCERS

## DESCRIPTION

The ADS1210 and ADS1211 are precision, wide dynamic range, delta-sigma analog-to-digital converters with 24-bit resolution operating from a single +5V supply. The differential inputs are ideal for direct connection to transducers or low level voltage signals. The delta-sigma architecture is used for wide dynamic range and to guarantee 24 bits of no missing code performance. An effective resolution of 23 bits is achieved through the use of a very low-noise input amplifier at conversion rates up to 10Hz. Effective resolutions of 20 bits can be maintained up to a sample rate of 1kHz through the use of the unique Turbo modulator mode of operation. The dynamic range of the converters is further increased by providing a low-noise programmable gain amplifier with a gain range of 1 to 16 in binary steps.

The ADS1210 and ADS1211 are designed for high resolution measurement applications in smart transmitters, industrial process control, weigh scales, chromatography and portable instrumentation. Both converters include a flexible synchronous serial interface which is SPI compatible and also offers a two-wire control mode for low cost isolation.

The ADS1210 is a single channel converter and is offered in both 18-pin DIP and 18-lead SOIC packages. The ADS1211 includes a 4 channel input multiplexer and is available in 24-pin DIP, 24-lead SOIC, and 28-lead SSOP packages.




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PDS-1284C

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# SPECIFICATIONS

All specifications $T_{MIN}$ to $T_{MAX}$, $AV_{DD} = DV_{DD} = +5V$, $f_{XIN} = 10MHz$, programmable gain amplifier setting of 1, Turbo Mode Rate of 1, $REF_{OUT}$ disabled, $V_{BIAS}$ disabled, and external 2.5V reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS1210U, P/ADS1211U, P, E MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **ANALOG INPUT** | | | | | |
| Input Voltage Range[1] | | 0 | | +5 | V |
| | With $V_{BIAS}$[2] | –10 | | +10 | V |
| Input Impedance | G = Gain, TMR = Turbo Mode Rate | | 4/(G • TMR)[3] | | MΩ |
| Programmable Gain Amplifier | User Programmable: 1, 2, 4, 8, or 16 | 1 | | 16 | |
| Input Capacitance | | | 8 | | pF |
| Input Leakage Current | At +25°C | | 5 | 50 | pA |
| | At $T_{MIN}$ to $T_{MAX}$ | | | 1 | nA |
| **SYSTEMS PERFORMANCE** | | | | | |
| Resolution | | | 24 | | Bits |
| No Missing Codes | $f_{DATA}$ = 60Hz | 24 | | | Bits |
| | $f_{DATA}$ = 100Hz, TMR of 4 | 24 | | | Bits |
| | $f_{DATA}$ = 250Hz, TMR of 8 | 23 | | | Bits |
| | $f_{DATA}$ = 500Hz, TMR of 16 | 24 | | | Bits |
| | $f_{DATA}$ = 1000Hz, TMR of 16 | 23 | | | Bits |
| Integral Linearity | $f_{DATA}$ = 60Hz | | | ±0.0015 | %FSR |
| | $f_{DATA}$ = 1000Hz, TMR of 16 | | | ±0.0015 | %FSR |
| Unipolar Offset Error[4] | | | See Note 5 | | |
| Unipolar Offset Drift[6] | | | 1 | | µV/°C |
| Gain Error[4] | | | See Note 5 | | |
| Gain Error Drift[6] | | | 1 | | µV/°C |
| Common-Mode Rejection | At DC, +25°C | 100 | 115 | | dB |
| | At DC, $T_{MIN}$ to $T_{MAX}$ | 90 | 115 | | dB |
| | 50Hz, $f_{DATA}$ = 50Hz[7] | 160 | | | dB |
| | 60Hz, $f_{DATA}$ = 60Hz[7] | 160 | | | dB |
| Normal-Mode Rejection | 50Hz, $f_{DATA}$ = 50Hz[7] | 100 | | | dB |
| | 60Hz, $f_{DATA}$ = 60Hz[7] | 100 | | | dB |
| Output Noise | | | See Typical Performance Curves | | |
| Power Supply Rejection | DC, 50Hz, and 60Hz | 65 | | | dB |
| **VOLTAGE REFERENCE** | | | | | |
| Internal Reference ($REF_{OUT}$) | | 2.4 | 2.5 | 2.6 | V |
| Drift | | | 25 | | ppm/°C |
| Noise | | | 50 | | µVp-p |
| Load Current | Source or Sink | | | 1 | mA |
| Output Impedance | | | 2 | | Ω |
| External Reference ($REF_{IN}$) | | 2.0 | | 3.0 | V |
| Load Current | | | | 2.5 | µA |
| $V_{BIAS}$ Output | Using Internal Reference | 3.15 | 3.3 | 3.45 | V |
| Drift | | | 50 | | ppm/°C |
| Load Current | Source or Sink | | | 10mA | |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic Family | | | TTL Compatible CMOS | | |
| Logic Level: (all except $X_{IN}$) | | | | | |
| $V_{IH}$ | $I_{IH}$ = +5µA | 2.0 | | $DV_{DD}$ +0.3 | V |
| $V_{IL}$ | $I_{IL}$ = +5µA | –0.3 | | 0.8 | V |
| $V_{OH}$ | $I_{OH}$ = 2 TTL Loads | 2.4 | | | V |
| $V_{OL}$ | $I_{OL}$ = 2 TTL Loads | | | 0.4 | V |
| $X_{IN}$ Input Levels: $V_{IH}$ | | 3.5 | | $DV_{DD}$ +0.3 | V |
| $V_{IL}$ | | –0.3 | | 0.8 | V |
| $X_{IN}$ Frequency Range ($f_{XIN}$) | | 0.5 | | 10 | MHz |
| Output Data Rate ($f_{DATA}$) | User Programmable | 2.4 | | 15,625 | Hz |
| | $f_{XIN}$ = 500kHz | 0.12 | | 781 | Hz |
| Data Format | User Programmable | | Two's Complement or Offset Binary | | |
| **SYSTEM CALIBRATION** | | | | | |
| Offset and Full-Scale Limits | $V_{FS}$ = Full-Scale Differential Voltage[8] | 0.7 • (2 • $REF_{IN}$)/G | | | |
| $V_{FS} - \lvert V_{OS} \rvert$ | $V_{OS}$ = Offset Differential Voltage[8] | | | 1.3 • (2 • $REF_{IN}$)/G | |

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## SPECIFICATIONS (CONT)

All specifications $T_{MIN}$ to $T_{MAX}$, $AV_{DD} = DV_{DD} = +5V$, $f_{XIN} = 10MHz$, programmable gain amplifier setting of 1, Turbo Mode Rate of 1, $REF_{OUT}$ disabled, $V_{BIAS}$ disabled, and external 2.5V reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS1210U, P/ADS1211U, P, E MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Power Supply Voltage | | 4.75 | | 5.25 | V |
| Power Supply Current: | | | | | |
| Analog Current | | | 2 | | mA |
| Digital Current | | | 3.5 | | mA |
| Additional Analog Current with | | | | | |
| $REF_{OUT}$ Enabled | | | 1.6 | | mA |
| $V_{BIAS}$ Enabled | No Load | | 1 | | mA |
| Power Dissipation | | | 26 | 40 | mW |
| | TMR of 16 | | 37 | 60 | mW |
| | $f_{XIN}$ = 2.5MHz | | 17 | | mW |
| | $f_{XIN}$ = 2.5MHz, TMR of 16 | | 27 | | mW |
| | Sleep Mode | | 11 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified | | –40 | | +85 | °C |
| Storage | | –60 | | +125 | °C |

NOTES: (1) In order to achieve the converter's full-scale range, the input must be fully differential ($A_{IN}N = 2 \bullet REF_{IN} - A_{IN}P$). If the input is single-ended ($A_{IN}N$ or $A_{IN}P$ is fixed), then the full scale range is one-half that of the differential range. (2) This range is set with external resistors and $V_{BIAS}$ (as described in the text). Other ranges are possible. (3) Input impedance is higher with lower $f_{XIN}$. (4) Applies after calibration. (5) After system calibration, these errors will be of the order of the effective resolution of the converter. Refer to the Typical Performance Curves which apply to the desired mode of operation. (6) Recalibration can remove these errors. (7) The specification also applies at $f_{DATA}/i$, where i is 2, 3, 4, etc. (8) Voltages at the analog inputs must remain within AGND to $AV_{DD}$.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Input: Current | ±100mA, Momentary |
| | ±10mA, Continuous |
| Voltage | AGND –0.3V to $AV_{DD}$ +0.3V |
| $AV_{DD}$ to $DV_{DD}$ | –0.3V to 6V |
| $AV_{DD}$ to AGND | –0.3V to 6V |
| $DV_{DD}$ to DGND | –0.3V to 6V |
| AGND to DGND | ±0.3V |
| $REF_{IN}$ Voltage to AGND | –0.3V to $AV_{DD}$ +0.3V |
| Digital Input Voltage to DGND | –0.3V to $DV_{DD}$ +0.3V |
| Digital Output Voltage to DGND | –0.3V to $DV_{DD}$ +0.3V |
| Lead Temperature (soldering, 10s) | +300°C |
| Power Dissipation (Any package) | 500mW |

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS1210P | 18-Pin Plastic DIP | 218 | –40°C to +85°C |
| ADS1210U | 18-Lead SOIC | 219 | –40°C to +85°C |
| ADS1211P | 24-Pin Plastic DIP | 243 | –40°C to +85°C |
| ADS1211U | 24-Lead SOIC | 239 | –40°C to +85°C |
| ADS1211E | 28-Lead SSOP | 324 | –40°C to +85°C |

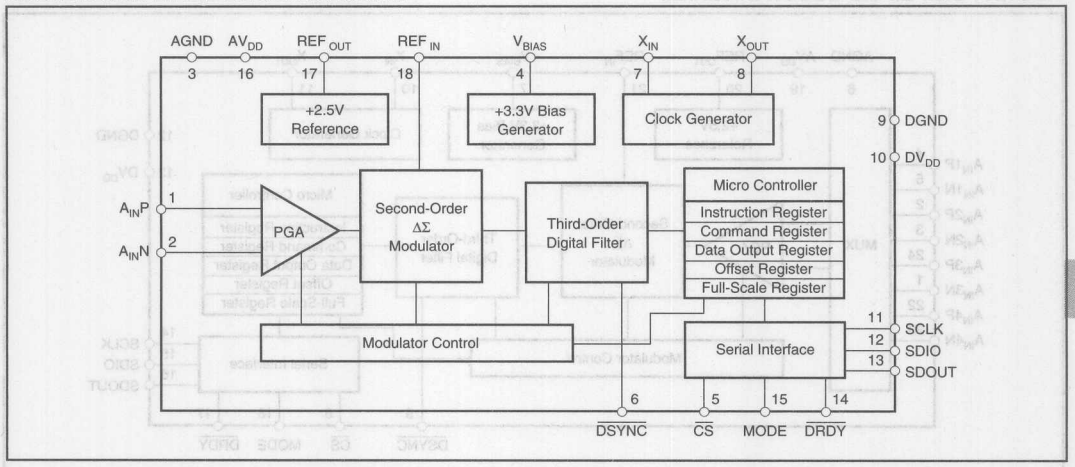
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

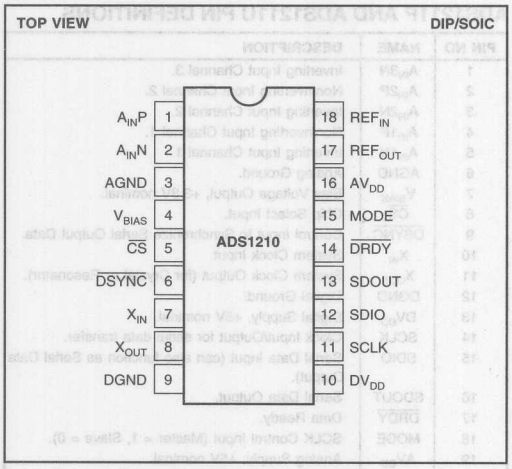
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

## ADS1210 SIMPLIFIED BLOCK DIAGRAM



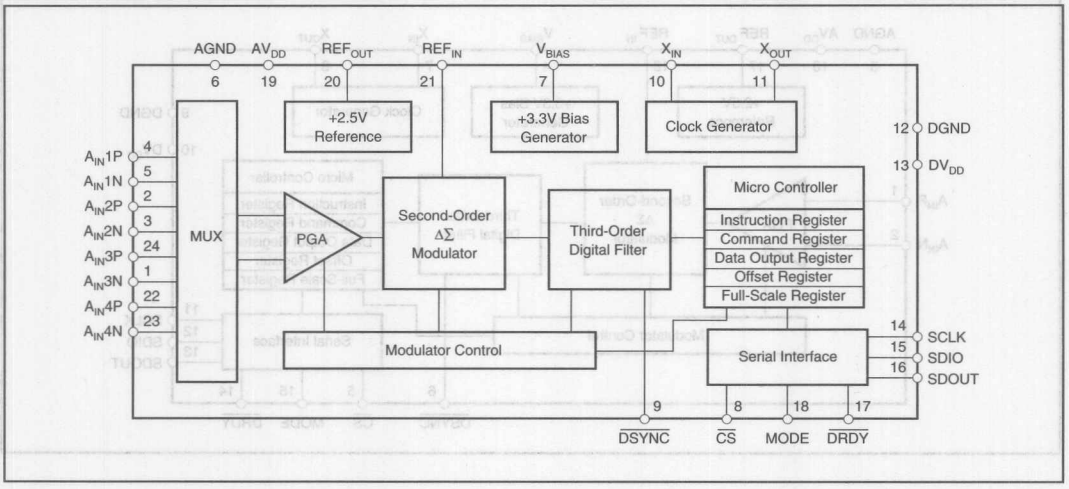

## ADS1210 PIN CONFIGURATION



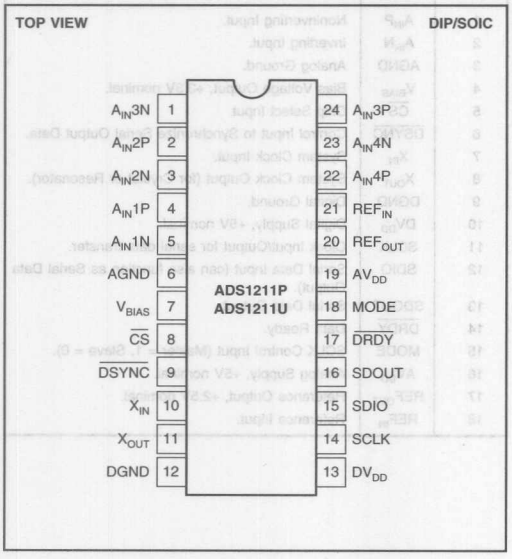

## ADS1210 PIN DEFINITIONS

| PIN NO | NAME | DESCRIPTION |
|---|---|---|
| 1 | $A_{IN}P$ | Noninverting Input. |
| 2 | $A_{IN}N$ | Inverting Input. |
| 3 | AGND | Analog Ground. |
| 4 | $V_{BIAS}$ | Bias Voltage Output, +3.3V nominal. |
| 5 | $\overline{CS}$ | Chip Select Input. |
| 6 | $\overline{DSYNC}$ | Control Input to Synchronize Serial Output Data. |
| 7 | $X_{IN}$ | System Clock Input. |
| 8 | $X_{OUT}$ | System Clock Output (for Crystal or Resonator). |
| 9 | DGND | Digital Ground. |
| 10 | $DV_{DD}$ | Digital Supply, +5V nominal. |
| 11 | SCLK | Clock Input/Output for serial data transfer. |
| 12 | SDIO | Serial Data Input (can also function as Serial Data Output). |
| 13 | SDOUT | Serial Data Output. |
| 14 | $\overline{DRDY}$ | Data Ready. |
| 15 | MODE | SCLK Control Input (Master = 1, Slave = 0). |
| 16 | $AV_{DD}$ | Analog Supply, +5V nominal. |
| 17 | $REF_{OUT}$ | Reference Output, +2.5V nominal. |
| 18 | $REF_{IN}$ | Reference Input. |

## ADS1211 SIMPLIFIED BLOCK DIAGRAM



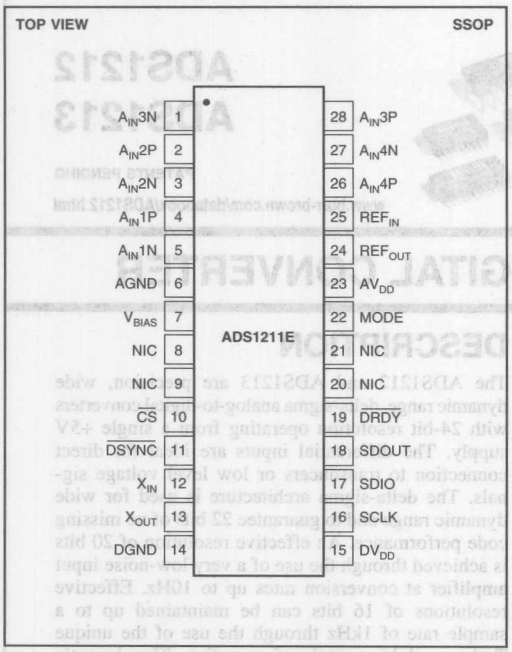

## ADS1211P AND ADS1211U PIN CONFIGURATION




## ADS1211P AND ADS1211U PIN DEFINITIONS

| PIN NO | NAME | DESCRIPTION |
|---|---|---|
| 1 | $A_{IN}3N$ | Inverting Input Channel 3. |
| 2 | $A_{IN}2P$ | Noninverting Input Channel 2. |
| 3 | $A_{IN}2N$ | Inverting Input Channel 2. |
| 4 | $A_{IN}1P$ | Noninverting Input Channel 1. |
| 5 | $A_{IN}1N$ | Inverting Input Channel 1. |
| 6 | AGND | Analog Ground. |
| 7 | $V_{BIAS}$ | Bias Voltage Output, +3.3V nominal. |
| 8 | $\overline{CS}$ | Chip Select Input. |
| 9 | $\overline{DSYNC}$ | Control Input to Synchronize Serial Output Data. |
| 10 | $X_{IN}$ | System Clock Input. |
| 11 | $X_{OUT}$ | System Clock Output (for Crystal or Resonator). |
| 12 | DGND | Digital Ground. |
| 13 | $DV_{DD}$ | Digital Supply, +5V nominal. |
| 14 | SCLK | Clock Input/Output for serial data transfer. |
| 15 | SDIO | Serial Data Input (can also function as Serial Data Output). |
| 16 | SDOUT | Serial Data Output. |
| 17 | $\overline{DRDY}$ | Data Ready. |
| 18 | MODE | SCLK Control Input (Master = 1, Slave = 0). |
| 19 | $AV_{DD}$ | Analog Supply, +5V nominal. |
| 20 | $REF_{OUT}$ | Reference Output: +2.5V nominal. |
| 21 | $REF_{IN}$ | Reference Input. |
| 22 | $A_{IN}4P$ | Noninverting Input Channel 4. |
| 23 | $A_{IN}4N$ | Inverting Input Channel 4. |
| 24 | $A_{IN}3P$ | Noninverting Input Channel 3. |

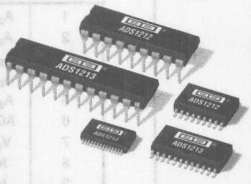
## ADS1211E PIN CONFIGURATION




## ADS1211E PIN DEFINITIONS

| PIN NO | NAME | DESCRIPTION |
|---|---|---|
| 1 | $A_{IN}3N$ | Inverting Input Channel 3. |
| 2 | $A_{IN}2P$ | Noninverting Input Channel 2. |
| 3 | $A_{IN}2N$ | Inverting Input Channel 2. |
| 4 | $A_{IN}1P$ | Noninverting Input Channel 1. |
| 5 | $A_{IN}1N$ | Inverting Input Channel 1. |
| 6 | AGND | Analog Ground. |
| 7 | $V_{BIAS}$ | Bias Voltage Output, +3.3V nominal. |
| 8 | NIC | Not Internally Connected. |
| 9 | NIC | Not Internally Connected. |
| 10 | $\overline{CS}$ | Chip Select Input. |
| 11 | $\overline{DSYNC}$ | Control Input to Synchronize Serial Output Data. |
| 12 | $X_{IN}$ | System Clock Input. |
| 13 | $X_{OUT}$ | System Clock Output (for Crystal or Resonator). |
| 14 | DGND | Digital Ground. |
| 15 | $DV_{DD}$ | Digital Supply, +5V nominal. |
| 16 | SCLK | Clock Input/Output for serial data transfer. |
| 17 | SDIO | Serial Data Input (can also function as Serial Data Output). |
| 18 | SDOUT | Serial Data Output. |
| 19 | $\overline{DRDY}$ | Data Ready. |
| 20 | NIC | Not Internally Connected. |
| 21 | NIC | Not Internally Connected. |
| 22 | MODE | SCLK Control Input (Master = 1, Slave = 0). |
| 23 | $AV_{DD}$ | Analog Supply, +5V nominal. |
| 24 | $REF_{OUT}$ | Reference Output: +2.5V nominal. |
| 25 | $REF_{IN}$ | Reference Input. |
| 26 | $A_{IN}4P$ | Noninverting Input Channel 4. |
| 27 | $A_{IN}4N$ | Inverting Input Channel 4. |
| 28 | $A_{IN}3P$ | Noninverting Input Channel 3. |

BURR-BROWN®



# ADS1212
# ADS1213

PATENTS PENDING

www.burr-brown.com/databook/ADS1212.html

# 22-Bit ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- DELTA-SIGMA A/D CONVERTER
- 22 BITS NO MISSING CODES
- 20 BITS EFFECTIVE RESOLUTION AT 10Hz AND 16 BITS AT 1000Hz
- LOW POWER: 1.4mW
- DIFFERENTIAL INPUTS
- PROGRAMMABLE GAIN AMPLIFIER
- SPI COMPATIBLE SSI INTERFACE
- PROGRAMMABLE CUT-OFF FREQUENCY UP TO 6.25kHz
- INTERNAL/EXTERNAL REFERENCE
- ON CHIP SELF-CALIBRATION
- ADS1213 INCLUDES 4 CHANNEL MUX

## APPLICATIONS

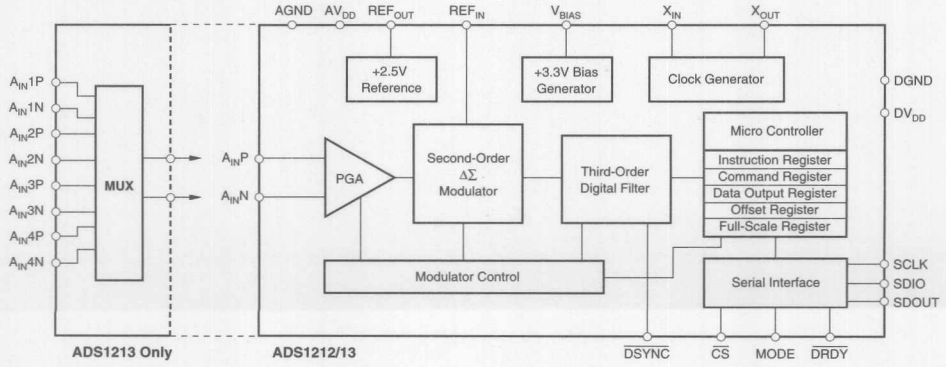
- INDUSTRIAL PROCESS CONTROL
- INSTRUMENTATION
- BLOOD ANALYSIS
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTS
- WEIGH SCALES
- PRESSURE TRANSDUCERS

## DESCRIPTION

The ADS1212 and ADS1213 are precision, wide dynamic range, delta-sigma analog-to-digital converters with 24-bit resolution operating from a single +5V supply. The differential inputs are ideal for direct connection to transducers or low level voltage signals. The delta-sigma architecture is used for wide dynamic range and to guarantee 22 bits of no missing code performance. An effective resolution of 20 bits is achieved through the use of a very low-noise input amplifier at conversion rates up to 10Hz. Effective resolutions of 16 bits can be maintained up to a sample rate of 1kHz through the use of the unique Turbo modulator mode of operation. The dynamic range of the converters is further increased by providing a low-noise programmable gain amplifier with a gain range of 1 to 16 in binary steps.

The ADS1212 and ADS1213 are designed for high resolution measurement applications in smart transmitters, industrial process control, weigh scales, chromatography and portable instrumentation. Both converters include a flexible synchronous serial interface which is SPI compatible and also offers a two-wire control mode for low cost isolation.

The ADS1212 is a single channel converter and is offered in both 18-pin DIP and 18-lead SOIC packages. The ADS1213 includes a 4 channel input multiplexer and is available in 24-pin DIP, 24-lead SOIC, and 28-lead SSOP packages.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

All specifications $T_{MIN}$ to $T_{MAX}$, $AV_{DD} = DV_{DD} = +5V$, $f_{XIN} = 1MHz$, programmable gain amplifier setting of 1, Turbo Mode Rate of 1, $REF_{OUT}$ disabled, $V_{BIAS}$ disabled, and external 2.5V reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS1212U, P/ADS1213U, P, E MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **ANALOG INPUT** | | | | | |
| Input Voltage Range[1] | | 0 | | +5 | V |
| | With $V_{BIAS}$[2] | –10 | | +10 | V |
| Input Impedance | G = Gain, TMR = Turbo Mode Rate | | 20/(G • TMR)[3] | | MΩ |
| Programmable Gain Amplifier | User Programmable: 1, 2, 4, 8, or 16 | 1 | | 16 | |
| Input Capacitance | | | 5 | | pF |
| Input Leakage Current | At +25°C | | 5 | 50 | pA |
| | $T_{MIN}$ to $T_{MAX}$ | | | 1 | nA |
| **SYSTEMS PERFORMANCE** | | | | | |
| No Missing Codes | $f_{DATA}$ = 10Hz | 22 | | | Bits |
| | $f_{DATA}$ = 60Hz | 19 | | | Bits |
| | $f_{DATA}$ = 100Hz, TMR of 4 | 21 | | | Bits |
| | $f_{DATA}$ = 250Hz, TMR of 8 | 20 | | | Bits |
| | $f_{DATA}$ = 500Hz, TMR of 16 | 20 | | | Bits |
| | $f_{DATA}$ = 1000Hz, TMR of 16 | 18 | | | Bits |
| Integral Linearity | $f_{DATA}$ = 60Hz | | | ±0.0015 | %FSR |
| | $f_{DATA}$ = 1000Hz, TMR of 16 | | | ±0.0015 | %FSR |
| Unipolar Offset Error[4] | | | See Note 5 | | |
| Unipolar Offset Drift[6] | | | 1 | | ppm/°C |
| Gain Error[4] | | | See Note 5 | | |
| Gain Error Drift[6] | | | 4 | | ppm/°C |
| Common-Mode Rejection | At DC, $T_{MIN}$ to $T_{MAX}$ | 90 | 100 | | dB |
| | 50Hz, $f_{DATA}$ = 50Hz[7] | 160 | | | dB |
| | 60Hz, $f_{DATA}$ = 60Hz[7] | 160 | | | dB |
| Normal-Mode Rejection | 50Hz, $f_{DATA}$ = 50Hz[7] | 100 | | | dB |
| | 60Hz, $f_{DATA}$ = 60Hz[7] | 100 | | | dB |
| Output Noise | | See Typical Performance Curves | | | |
| Power Supply Rejection | DC, 50Hz, and 60Hz | 60 | | | dB |
| **VOLTAGE REFERENCE** | | | | | |
| Internal Reference ($REF_{OUT}$) | | 2.4 | 2.5 | 2.6 | V |
| Drift | | | 25 | | ppm/°C |
| Noise | | | 50 | | µVp-p |
| Load Current | Source or Sink | | | 1 | mA |
| Output Impedance | | | 2 | | Ω |
| External Reference ($REF_{IN}$) | | 2.0 | | 3.0 | V |
| Load Current | | | | 2.5 | µA |
| $V_{BIAS}$ Output | Using Internal Reference | 3.15 | 3.3 | 3.45 | V |
| Drift | | | 50 | | ppm/°C |
| Load Current | Source or Sink | | | 10mA | |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic Family | | | TTL Compatible CMOS | | |
| Logic Level: (all except $X_{IN}$) | | | | | |
| $V_{IH}$ | $I_{IH}$ = +5µA | 2.0 | | $DV_{DD}$ +0.3 | V |
| $V_{IL}$ | $I_{IL}$ = +5µA | –0.3 | | 0.8 | V |
| $V_{OH}$ | $I_{OH}$ = 2 TTL Loads | 2.4 | | | V |
| $V_{OL}$ | $I_{OL}$ = 2 TTL Loads | | | 0.4 | V |
| $X_{IN}$ Input Levels: $V_{IH}$ | | 3.5 | | $DV_{DD}$ +0.3 | V |
| $V_{IL}$ | | –0.3 | | 0.8 | V |
| $X_{IN}$ Frequency Range ($f_{XIN}$) | | 0.5 | | 2.5 | MHz |
| Output Data Rate ($f_{DATA}$) | User Programmable and TMR = 1 to 16 | 0.96 | | 6,250 | Hz |
| | $f_{XIN}$ = 500kHz | 0.48 | | 3,125 | Hz |
| | $f_{XIN}$ = 2.5MHz | 2.4 | | 15,625 | Hz |
| Data Format | User Programmable | | Two's Complement or Offset Binary | | |
| **SYSTEM CALIBRATION** | | | | | |
| Offset and Full-Scale Limits | $V_{FS}$ = Full-Scale Differential Voltage[8] | 0.7 • (2 • $REF_{IN}$)/G | | | |
| $V_{FS} - \lvert V_{OS} \rvert$ | $V_{OS}$ = Offset Differential Voltage[8] | | | 1.3 • (2 • $REF_{IN}$)/G | |

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## SPECIFICATIONS (CONT)

All specifications $T_{MIN}$ to $T_{MAX}$, $AV_{DD} = DV_{DD} = +5V$, $f_{XIN}$ = 1MHz, programmable gain amplifier setting of 1, Turbo Mode Rate of 1, $REF_{OUT}$ disabled, $V_{BIAS}$ disabled, and external 2.5V reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS1212U, P/ADS1213U, P, E MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Power Supply Voltage | | 4.75 | | 5.25 | V |
| Power Supply Current: | | | | | |
| Analog Current | | | 95 | | µA |
| Digital Current | | | 185 | | µA |
| Additional Analog Current with | | | | | |
| $REF_{OUT}$ Enabled | | | 1.8 | | mA |
| $V_{BIAS}$ Enabled | No Load | | 1 | | mA |
| Power Dissipation | At +25°C | | 1.4 | | mW |
| | $T_{MIN}$ to $T_{MAX}$ | | | 1.8 | mW |
| | TMR of 16 | | 6 | 8.5 | mW |
| | $f_{XIN}$ = 2.5MHz | | 2.2 | | mW |
| | $f_{XIN}$ = 2.5MHz, TMR of 16 | | 7.5 | | mW |
| | Sleep Mode | | 0.45 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified | | –40 | | +85 | °C |
| Storage | | –60 | | +125 | °C |

NOTES: (1) In order to achieve the converter's full-scale range, the input must be fully differential ($A_{IN}N = 2 \bullet REF_{IN} - A_{IN}P$). If the input is single-ended ($A_{IN}N$ or $A_{IN}P$ is fixed), then the full scale range is one-half that of the differential range. (2) This range is set with external resistors and $V_{BIAS}$ (as described in the text). Other ranges are possible. (3) Input impedance is higher with lower $f_{XIN}$. (4) Applies after calibration. (5) After system calibration, these errors will be of the order of the effective resolution of the converter. Refer to the Typical Performance Curves which apply to the desired mode of operation. (6) Recalibration can remove these errors. (7) The specification also applies at $f_{DATA}/i$, where i is 2, 3, 4, etc. (8) Voltages at the analog inputs must remain within AGND to $AV_{DD}$.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Input: Current | ±100mA, Momentary |
| | ±10mA, Continuous |
| Voltage | AGND –0.3V to $AV_{DD}$ +0.3V |
| $AV_{DD}$ to $DV_{DD}$ | –0.3V to 6V |
| $AV_{DD}$ to AGND | –0.3V to 6V |
| $DV_{DD}$ to DGND | –0.3V to 6V |
| AGND to DGND | ±0.3V |
| $REF_{IN}$ Voltage to AGND | –0.3V to $AV_{DD}$ +0.3V |
| Digital Input Voltage to DGND | –0.3V to $DV_{DD}$ +0.3V |
| Digital Output Voltage to DGND | –0.3V to $DV_{DD}$ +0.3V |
| Lead Temperature (soldering, 10s) | +300°C |
| Power Dissipation (Any package) | 500mW |

### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS1212P | 18-Pin Plastic DIP | 218 | –40°C to +85°C |
| ADS1212U | 18-Lead SOIC | 219 | –40°C to +85°C |
| ADS1213P | 24-Pin Plastic DIP | 243 | –40°C to +85°C |
| ADS1213U | 24-Lead SOIC | 239 | –40°C to +85°C |
| ADS1213E | 28-Lead SSOP | 324 | –40°C to +85°C |

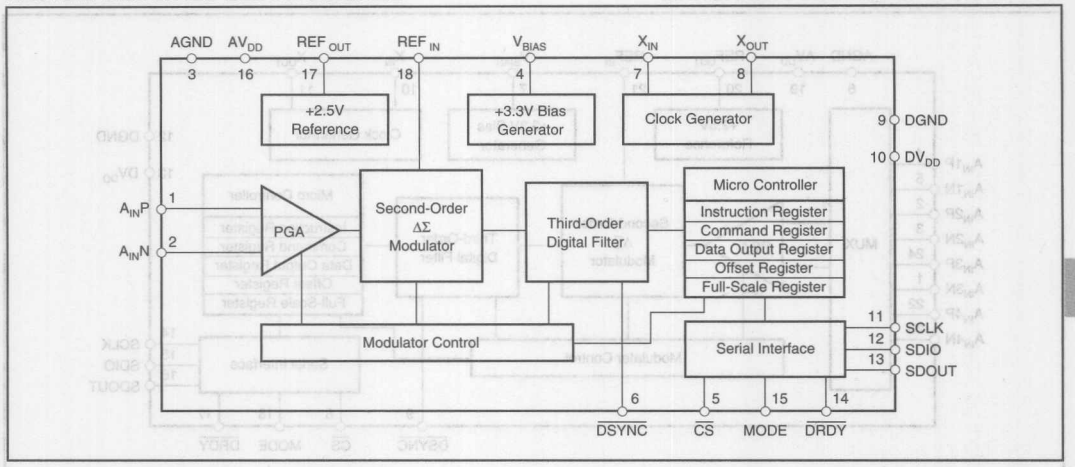
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

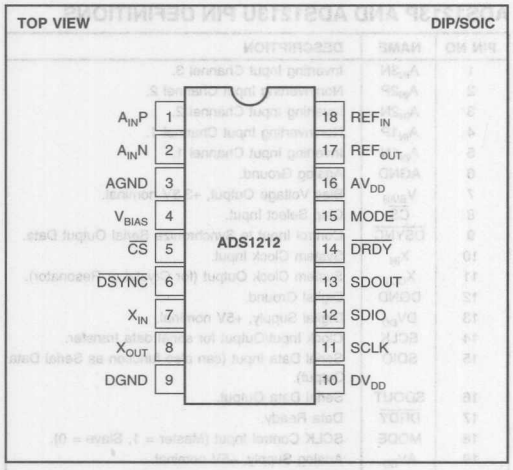
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

## ADS1212 SIMPLIFIED BLOCK DIAGRAM

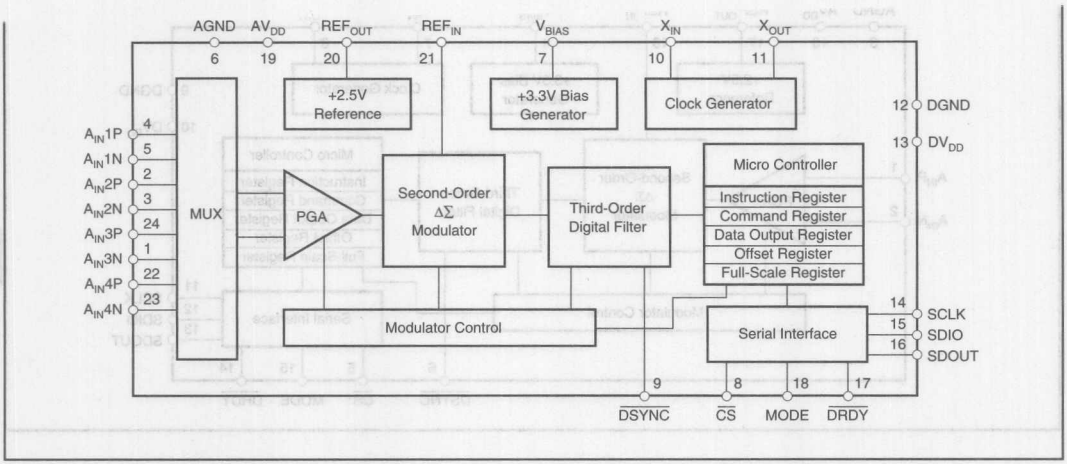



## ADS1212 PIN CONFIGURATION

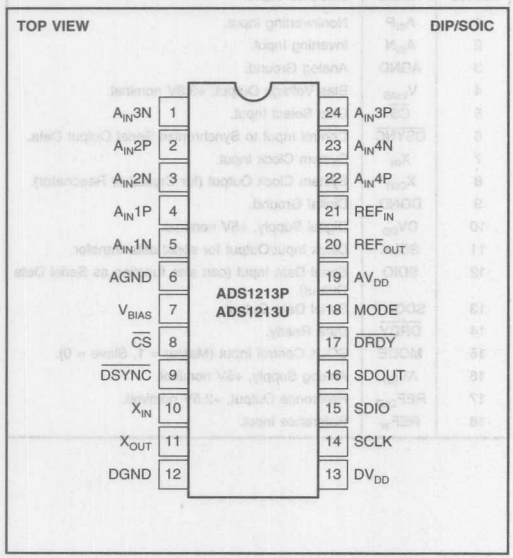



## ADS1212 PIN DEFINITIONS

| PIN NO | NAME | DESCRIPTION |
|---|---|---|
| 1 | $A_{IN}P$ | Noninverting Input. |
| 2 | $A_{IN}N$ | Inverting Input. |
| 3 | AGND | Analog Ground. |
| 4 | $V_{BIAS}$ | Bias Voltage Output, +3.3V nominal. |
| 5 | $\overline{CS}$ | Chip Select Input. |
| 6 | $\overline{DSYNC}$ | Control Input to Synchronize Serial Output Data. |
| 7 | $X_{IN}$ | System Clock Input. |
| 8 | $X_{OUT}$ | System Clock Output (for Crystal or Resonator). |
| 9 | DGND | Digital Ground. |
| 10 | $DV_{DD}$ | Digital Supply, +5V nominal. |
| 11 | SCLK | Clock Input/Output for serial data transfer. |
| 12 | SDIO | Serial Data Input (can also function as Serial Data Output). |
| 13 | SDOUT | Serial Data Output. |
| 14 | $\overline{DRDY}$ | Data Ready. |
| 15 | MODE | SCLK Control Input (Master = 1, Slave = 0). |
| 16 | $AV_{DD}$ | Analog Supply, +5V nominal. |
| 17 | $REF_{OUT}$ | Reference Output, +2.5V nominal. |
| 18 | $REF_{IN}$ | Reference Input. |



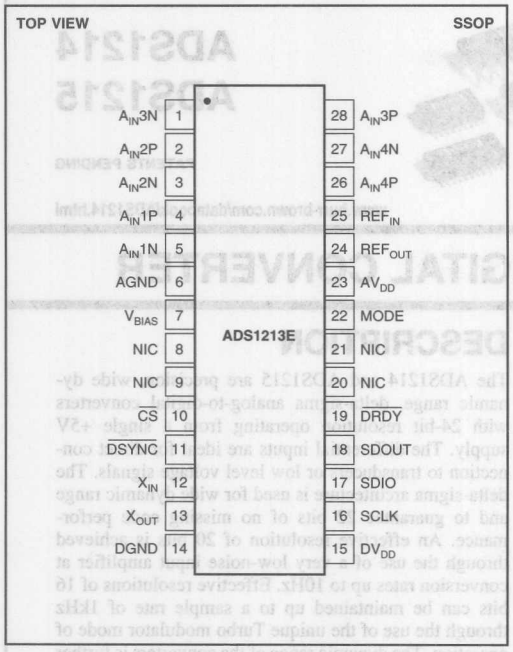

## ADS1213P AND ADS1213U PIN CONFIGURATION




## ADS1213P AND ADS1213U PIN DEFINITIONS

| PIN NO | NAME | DESCRIPTION |
|---|---|---|
| 1 | $A_{IN}3N$ | Inverting Input Channel 3. |
| 2 | $A_{IN}2P$ | Noninverting Input Channel 2. |
| 3 | $A_{IN}2N$ | Inverting Input Channel 2. |
| 4 | $A_{IN}1P$ | Noninverting Input Channel 1. |
| 5 | $A_{IN}1N$ | Inverting Input Channel 1. |
| 6 | AGND | Analog Ground. |
| 7 | $V_{BIAS}$ | Bias Voltage Output, +3.3V nominal. |
| 8 | $\overline{CS}$ | Chip Select Input. |
| 9 | $\overline{DSYNC}$ | Control Input to Synchronize Serial Output Data. |
| 10 | $X_{IN}$ | System Clock Input. |
| 11 | $X_{OUT}$ | System Clock Output (for Crystal or Resonator). |
| 12 | DGND | Digital Ground. |
| 13 | $DV_{DD}$ | Digital Supply, +5V nominal. |
| 14 | SCLK | Clock Input/Output for serial data transfer. |
| 15 | SDIO | Serial Data Input (can also function as Serial Data Output). |
| 16 | SDOUT | Serial Data Output. |
| 17 | $\overline{DRDY}$ | Data Ready. |
| 18 | MODE | SCLK Control Input (Master = 1, Slave = 0). |
| 19 | $AV_{DD}$ | Analog Supply, +5V nominal. |
| 20 | $REF_{OUT}$ | Reference Output: +2.5V nominal. |
| 21 | $REF_{IN}$ | Reference Input. |
| 22 | $A_{IN}4P$ | Noninverting Input Channel 4. |
| 23 | $A_{IN}4N$ | Inverting Input Channel 4. |
| 24 | $A_{IN}3P$ | Noninverting Input Channel 3. |

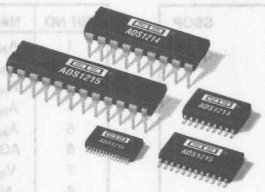
## ADS1213E PIN CONFIGURATION




## ADS1213E PIN DEFINITIONS

| PIN NO | NAME | DESCRIPTION |
|---|---|---|
| 1 | $A_{IN}3N$ | Inverting Input Channel 3. |
| 2 | $A_{IN}2P$ | Noninverting Input Channel 2. |
| 3 | $A_{IN}2N$ | Inverting Input Channel 2. |
| 4 | $A_{IN}1P$ | Noninverting Input Channel 1. |
| 5 | $A_{IN}1N$ | Inverting Input Channel 1. |
| 6 | AGND | Analog Ground. |
| 7 | $V_{BIAS}$ | Bias Voltage Output, +3.3V nominal. |
| 8 | NIC | Not Internally Connected. |
| 9 | NIC | Not Internally Connected. |
| 10 | $\overline{CS}$ | Chip Select Input. |
| 11 | $\overline{DSYNC}$ | Control Input to Synchronize Serial Output Data. |
| 12 | $X_{IN}$ | System Clock Input. |
| 13 | $X_{OUT}$ | System Clock Output (for Crystal or Resonator). |
| 14 | DGND | Digital Ground. |
| 15 | $DV_{DD}$ | Digital Supply, +5V nominal. |
| 16 | SCLK | Clock Input/Output for serial data transfer. |
| 17 | SDIO | Serial Data Input (can also function as Serial Data Output). |
| 18 | SDOUT | Serial Data Output. |
| 19 | $\overline{DRDY}$ | Data Ready. |
| 20 | NIC | Not Internally Connected. |
| 21 | NIC | Not Internally Connected. |
| 22 | MODE | SCLK Control Input (Master = 1, Slave = 0). |
| 23 | $AV_{DD}$ | Analog Supply, +5V nominal. |
| 24 | $REF_{OUT}$ | Reference Output: +2.5V nominal. |
| 25 | $REF_{IN}$ | Reference Input. |
| 26 | $A_{IN}4P$ | Noninverting Input Channel 4. |
| 27 | $A_{IN}4N$ | Inverting Input Channel 4. |
| 28 | $A_{IN}3P$ | Noninverting Input Channel 3. |

BURR-BROWN®



# ADS1214
# ADS1215

PATENTS PENDING

www.burr-brown.com/databook/ADS1214.html

# 22-Bit ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- DELTA-SIGMA A/D CONVERTER
- 22 BITS NO MISSING CODES
- 20 BITS EFFECTIVE RESOLUTION AT 10Hz AND 16 BITS AT 1000Hz
- INPUT RANGES: 20mV to 320mV
- TWO 200μA CURRENT SOURCES
- LOW POWER: 3mW
- DIFFERENTIAL INPUTS
- PROGRAMMABLE GAIN AMPLIFIER
- ON CHIP SELF-CALIBRATION
- ADS1215 INCLUDES 4 CHANNEL MUX

## APPLICATIONS

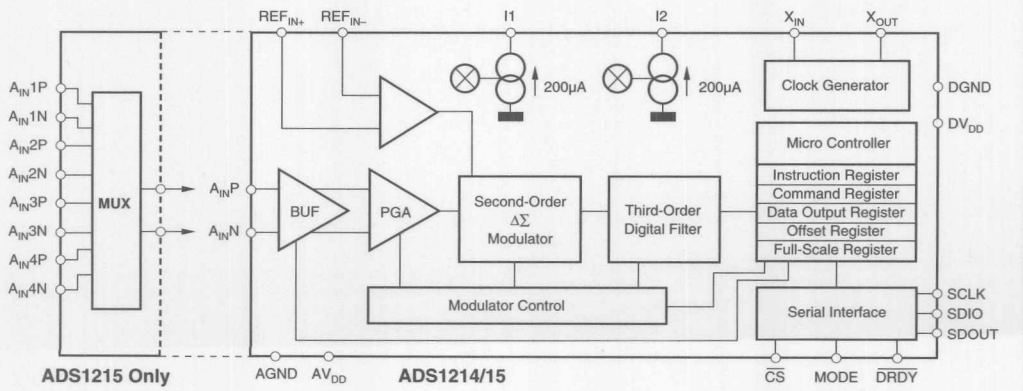
- INDUSTRIAL PROCESS CONTROL
- INSTRUMENTATION
- BLOOD ANALYSIS
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTS
- WEIGH SCALES
- PRESSURE TRANSDUCERS

## DESCRIPTION

The ADS1214 and ADS1215 are precision, wide dynamic range, delta-sigma analog-to-digital converters with 24-bit resolution operating from a single +5V supply. The differential inputs are ideal for direct connection to transducers or low level voltage signals. The delta-sigma architecture is used for wide dynamic range and to guarantee 22 bits of no missing code performance. An effective resolution of 20 bits is achieved through the use of a very low-noise input amplifier at conversion rates up to 10Hz. Effective resolutions of 16 bits can be maintained up to a sample rate of 1kHz through the use of the unique Turbo modulator mode of operation. The dynamic range of the converters is further increased by providing a low-noise programmable gain amplifier with a gain range of 1 to 16 in binary steps.

The ADS1214 and ADS1215 are designed for high resolution measurement applications in smart transmitters, industrial process control, weigh scales, chromatography and portable instrumentation. Both converters include a flexible synchronous serial interface which is SPI compatible and also offers a two-wire control mode for low cost isolation.

The ADS1214 is a single channel converter and is offered in both 18-pin DIP and 18-lead SOIC packages. The ADS1215 includes a 4 channel input multiplexer and is available in 24-pin DIP, 24-lead SOIC, and 28-lead SSOP packages.




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# SPECIFICATIONS

All specifications $T_{MIN}$ to $T_{MAX}$, $AV_{DD} = DV_{DD} = +5V$, $f_{XIN} = 2.5MHz$, Programmable Gain Amplifier setting of 1, Turbo Mode Rate of 1, $REF_{IN+} = 2.5V$, $REF_{IN-} = 0V$, Reference Range 0 (2.5V), Buffer enabled, and internal current sources off, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS1214U, P/ADS1215U, P, E MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **ANALOG INPUT** | | | | | |
| Input Voltage Range[1] | | 0 | | 320 | mV |
| Input Impedance[2] | G = Gain, TMR = Turbo Mode Rate | | TBD | | MΩ |
| Programmable Gain Amplifier | User Programmable: 1, 2, 4, 8, or 16 | 1 | | 16 | |
| Input Capacitance | | | TBD | | pF |
| Input Leakage Current | At +25°C | | 5 | 50 | pA |
| | $T_{MIN}$ to $T_{MAX}$ | | | 1 | nA |
| **SYSTEMS PERFORMANCE** | | | | | |
| No Missing Codes | $f_{DATA}$ = 10Hz | 22 | | | Bits |
| | $f_{DATA}$ = 60Hz | 19 | | | Bits |
| | $f_{DATA}$ = 100Hz, TMR of 4 | 21 | | | Bits |
| | $f_{DATA}$ = 250Hz, TMR of 8 | 20 | | | Bits |
| | $f_{DATA}$ = 500Hz, TMR of 16 | 19 | | | Bits |
| | $f_{DATA}$ = 1000Hz, TMR of 16 | 18 | | | Bits |
| Integral Linearity | $f_{DATA}$ = 60Hz | | | ±0.0015 | %FSR |
| | $f_{DATA}$ = 1000Hz, TMR of 16 | | | ±0.0015 | %FSR |
| Unipolar Offset Error[3] | | | See Note 4 | | |
| Unipolar Offset Drift[5] | | | 1 | | ppm/°C |
| Gain Error[3] | | | See Note 4 | | |
| Gain Error Drift[5] | | | 4 | | ppm/°C |
| Common-Mode Rejection | At DC, $T_{MIN}$ to $T_{MAX}$ | 90 | 100 | | dB |
| | 50Hz, $f_{DATA}$ = 50Hz[6] | 160 | | | dB |
| | 60Hz, $f_{DATA}$ = 60Hz[6] | 160 | | | dB |
| Normal-Mode Rejection | 50Hz, $f_{DATA}$ = 50Hz[6] | 100 | | | dB |
| | 60Hz, $f_{DATA}$ = 60Hz[6] | 100 | | | dB |
| Output Noise | | | See Typical Performance Curves | | |
| Power Supply Rejection | DC, 50Hz, and 60Hz | TBD | | | dB |
| **VOLTAGE REFERENCE** | | | | | |
| External Reference | $REF_{IN+} - REF_{IN-}$ | 1.0 | 2.5 | 5.0 | V |
| Common-Mode Range | | 0.5 | 2.5 | 4.5 | V |
| Common-Mode Rejection | At DC | 100 | | | dB |
| | 60Hz, $f_{DATA}$ = 60Hz[7] | 100 | | | dB |
| Load Current | | | | 100 | nA |
| Current Source | | | | | |
| Output Current | | | 200 | | µA |
| Output Current Accuracy | | | | TBD | % |
| Output Current Drift | | | TBD | TBD | ppm/°C |
| Output Current Match | | | TBD | 1 | % |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic Family | | | TTL Compatible CMOS | | |
| Logic Level: (all except $X_{IN}$) | | | | | |
| $V_{IH}$ | $I_{IH}$ = +5µA | 2.0 | | $DV_{DD}$ +0.3 | V |
| $V_{IL}$ | $I_{IL}$ = +5µA | –0.3 | | 0.8 | V |
| $V_{OH}$ | $I_{OH}$ = 2 TTL Loads | 2.4 | | | V |
| $V_{OL}$ | $I_{OL}$ = 2 TTL Loads | | | 0.4 | V |
| $X_{IN}$ Input Levels: $V_{IH}$ | | 3.5 | | $DV_{DD}$ +0.3 | V |
| $V_{IL}$ | | –0.3 | | 0.8 | V |
| $X_{IN}$ Frequency Range ($f_{XIN}$) | | 0.5 | | 2.5 | MHz |
| Output Data Rate ($f_{DATA}$) | User Programmable and TMR = 1 to 16 | 2.4 | | 15,625 | Hz |
| | $f_{XIN}$ = 500kHz | 0.48 | | 3,125 | Hz |
| | $f_{XIN}$ = 1MHz | 0.96 | | 6250 | Hz |
| Data Format | User Programmable | | Two's Complement or Offset Binary | | |
| **SYSTEM CALIBRATION** | | | | | |
| Offset and Full-Scale Limits | $V_{FS}$ = Full-Scale Differential Voltage[7] | TBD | | | |
| $V_{FS} - \lvert V_{OS} \rvert$ | $V_{OS}$ = Offset Differential Voltage[7] | | | TBD | |

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## SPECIFICATIONS (CONT)

All specifications $T_{MIN}$ to $T_{MAX}$, $AV_{DD} = DV_{DD} = +5V$, $f_{XIN} = 2.5MHz$, Programmable Gain Amplifier setting of 1, Turbo Mode Rate of 1, $REF_{IN+} = 2.5V$, $REF_{IN-} = 0V$, Reference Range 0 (2.5V), Buffer enabled, and internal current sources off, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS1214U, P/ADS1215U, P, E MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Power Supply Voltage | | 4.75 | | 5.25 | V |
| Power Supply Current: | | | | | |
| Analog Current | | | 125 | | µA |
| Digital Current | | | 462 | | µA |
| Additional Analog Current with | | | | | |
| Buffer Enabled | | | 500 | | µA |
| Current Sources Enabled | No Load | | 1 | | mA |
| Power Dissipation | At +25°C | | 3 | | mW |
| | $T_{MIN}$ to $T_{MAX}$ | | | TBD | mW |
| | TMR of 16 | | TBD | TBD | mW |
| | $f_{XIN}$ = 1MHz | | TBD | | mW |
| | $f_{XIN}$ = 1MHz, TMR of 16 | | TBD | | mW |
| | Sleep Mode | | 0.45 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified | | –40 | | +85 | °C |
| Storage | | –60 | | +125 | °C |

NOTES: (1) In order to achieve the converter's full-scale range, the input must be fully differential. If the input is single-ended ($A_{IN}N$ or $A_{IN}P$ is fixed), then the full scale range is one-half that of the differential range. (2) Input impedance is higher with lower $f_{XIN}$. (3) Applies after calibration. (4) These errors will be of the order of the effective resolution of the converter. Refer to the Typical Performance Curves which apply to the desired mode of operation. (5) Recalibration can remove these errors. (6) The specification also applies at $f_{DATA}/i$, where i is 2, 3, 4, etc. (7) Voltages at the analog inputs must remain within AGND to $AV_{DD}$.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Input: Current | ±100mA, Momentary |
| | ±10mA, Continuous |
| Voltage | AGND – 0.3V to $AV_{DD}$ + 0.3V |
| $AV_{DD}$ to $DV_{DD}$ | –0.3V to 6V |
| $AV_{DD}$ to AGND | –0.3V to 6V |
| $DV_{DD}$ to DGND | –0.3V to 6V |
| AGND to DGND | ±0.3V |
| $REF_{IN}$ Voltage to AGND | –0.3V to $AV_{DD}$ + 0.3V |
| Digital Input Voltage to DGND | –0.3V to $DV_{DD}$ + 0.3V |
| Digital Output Voltage to DGND | –0.3V to $DV_{DD}$ + 0.3V |
| Lead Temperature (soldering, 10s) | +300°C |
| Power Dissipation (Any package) | 500mW |

### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

### PACKAGE INFORMATION

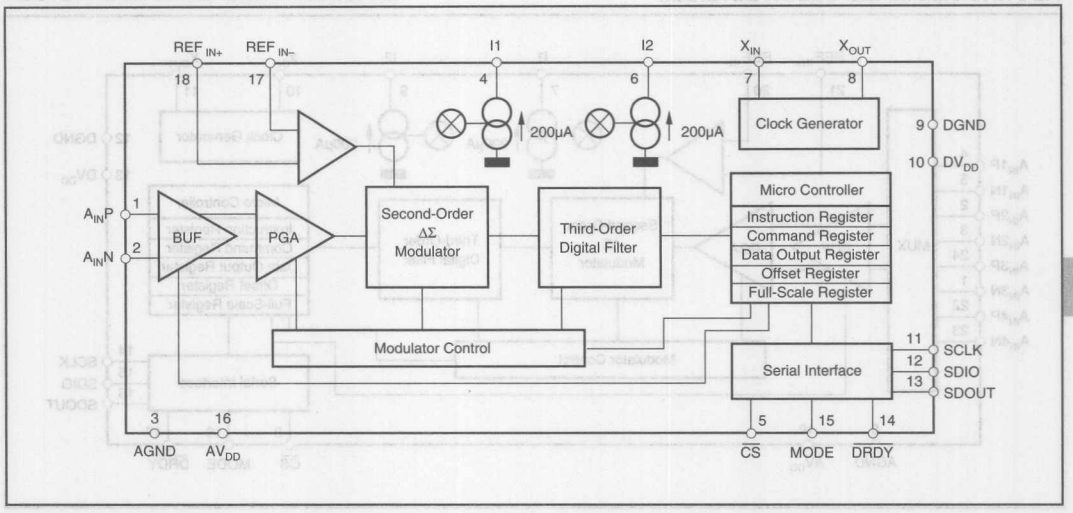
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ADS1214P | 18-Pin Plastic DIP | 218 |
| ADS1214U | 18-Lead SOIC | 219 |
| ADS1215P | 24-Pin Plastic DIP | 243 |
| ADS1215U | 24-Lead SOIC | 239 |
| ADS1215E | 28-Lead SSOP | 324 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### ORDERING INFORMATION

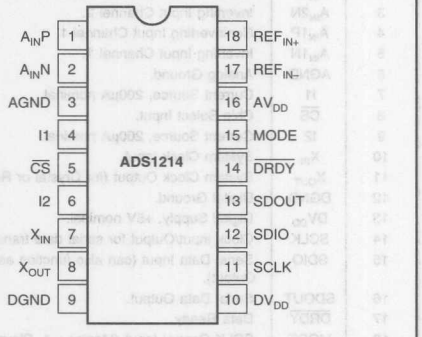
| PRODUCT | PACKAGE | TEMPERATURE RANGE |
|---|---|---|
| ADS1214P | 18-Pin Plastic DIP | –40°C to +85°C |
| ADS1214U | 18-Lead SOIC | –40°C to +85°C |
| ADS1215P | 24-Pin Plastic DIP | –40°C to +85°C |
| ADS1215U | 24-Lead SOIC | –40°C to +85°C |
| ADS1215E | 28-Lead SSOP | –40°C to +85°C |

## ADS1214 SIMPLIFIED BLOCK DIAGRAM




## ADS1214 PIN CONFIGURATION

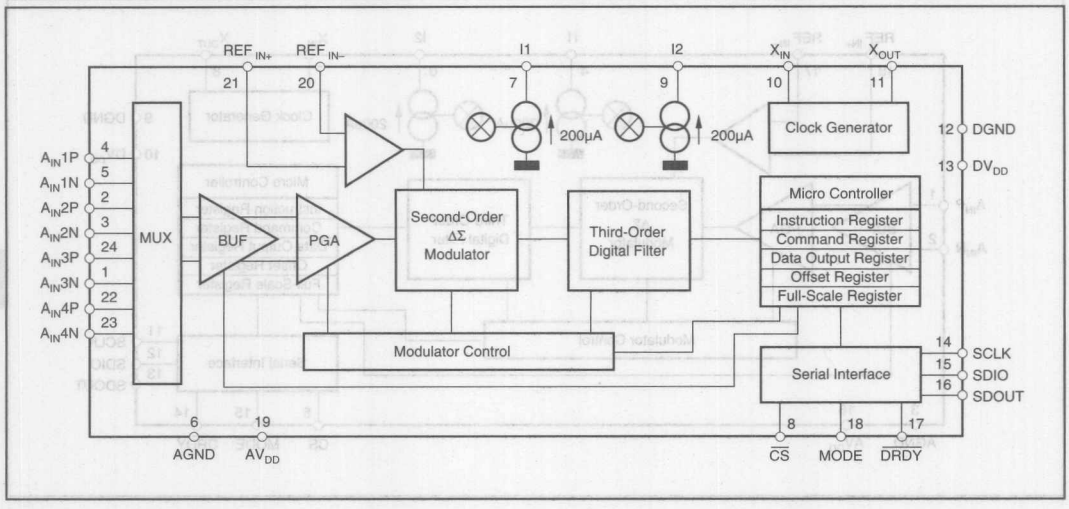
Top View DIP/SOIC



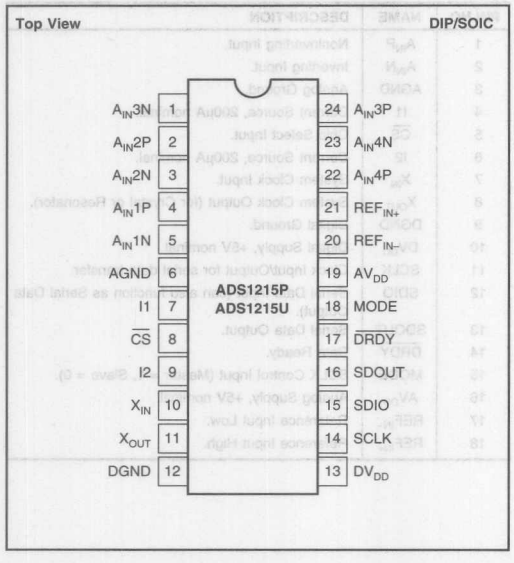

## ADS1214 PIN DEFINITIONS

| PIN NO | NAME | DESCRIPTION |
|---|---|---|
| 1 | $A_{IN}P$ | Noninverting Input. |
| 2 | $A_{IN}N$ | Inverting Input. |
| 3 | AGND | Analog Ground. |
| 4 | I1 | Current Source, 200µA nominal. |
| 5 | $\overline{CS}$ | Chip Select Input. |
| 6 | I2 | Current Source, 200µA nominal. |
| 7 | $X_{IN}$ | System Clock Input. |
| 8 | $X_{OUT}$ | System Clock Output (for Crystal or Resonator). |
| 9 | DGND | Digital Ground. |
| 10 | $DV_{DD}$ | Digital Supply, +5V nominal. |
| 11 | SCLK | Clock Input/Output for serial data transfer. |
| 12 | SDIO | Serial Data Input (can also function as Serial Data Output). |
| 13 | SDOUT | Serial Data Output. |
| 14 | $\overline{DRDY}$ | Data Ready. |
| 15 | MODE | SCLK Control Input (Master = 1, Slave = 0). |
| 16 | $AV_{DD}$ | Analog Supply, +5V nominal. |
| 17 | $REF_{IN-}$ | Reference Input Low. |
| 18 | $REF_{IN+}$ | Reference Input High. |

## ADS1215 SIMPLIFIED BLOCK DIAGRAM



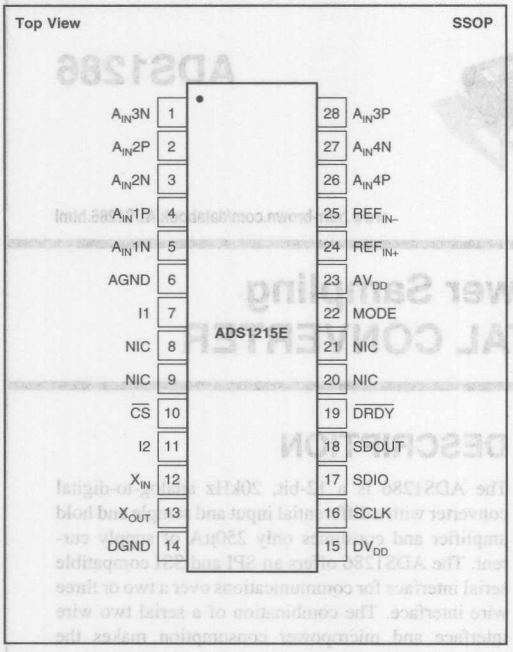

## ADS1215P AND ADS1215U PIN CONFIGURATION




## ADS1215P AND ADS1215U PIN DEFINITIONS

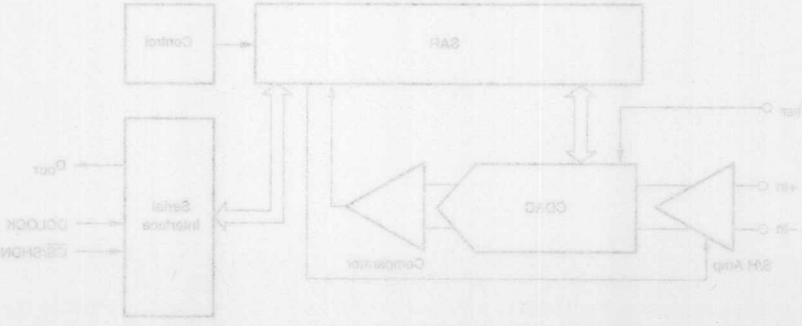
| PIN NO | NAME | DESCRIPTION |
|---|---|---|
| 1 | $A_{IN}3N$ | Inverting Input Channel 3. |
| 2 | $A_{IN}2P$ | Noninverting Input Channel 2. |
| 3 | $A_{IN}2N$ | Inverting Input Channel 2. |
| 4 | $A_{IN}1P$ | Noninverting Input Channel 1. |
| 5 | $A_{IN}1N$ | Inverting Input Channel 1. |
| 6 | AGND | Analog Ground. |
| 7 | I1 | Current Source, 200µA nominal. |
| 8 | $\overline{CS}$ | Chip Select Input. |
| 9 | I2 | Current Source, 200µA nominal. |
| 10 | $X_{IN}$ | System Clock Input. |
| 11 | $X_{OUT}$ | System Clock Output (for Crystal or Resonator). |
| 12 | DGND | Digital Ground. |
| 13 | $DV_{DD}$ | Digital Supply, +5V nominal. |
| 14 | SCLK | Clock Input/Output for serial data transfer. |
| 15 | SDIO | Serial Data Input (can also function as Serial Data Output). |
| 16 | SDOUT | Serial Data Output. |
| 17 | $\overline{DRDY}$ | Data Ready. |
| 18 | MODE | SCLK Control Input (Master = 1, Slave = 0). |
| 19 | $AV_{DD}$ | Analog Supply, +5V nominal. |
| 20 | $REF_{IN-}$ | Reference Input Low. |
| 21 | $REF_{IN+}$ | Reference Input High. |
| 22 | $A_{IN}4P$ | Noninverting Input Channel 4. |
| 23 | $A_{IN}4N$ | Inverting Input Channel 4. |
| 24 | $A_{IN}3P$ | Noninverting Input Channel 3. |

## ADS1215E PIN CONFIGURATION

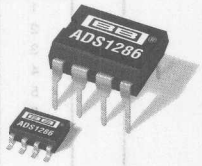



## ADS1215E PIN DEFINITIONS

| PIN NO | NAME | DESCRIPTION |
|---|---|---|
| 1 | $A_{IN}3N$ | Inverting Input Channel 3. |
| 2 | $A_{IN}2P$ | Noninverting Input Channel 2. |
| 3 | $A_{IN}2N$ | Inverting Input Channel 2. |
| 4 | $A_{IN}1P$ | Noninverting Input Channel 1. |
| 5 | $A_{IN}1N$ | Inverting Input Channel 1. |
| 6 | AGND | Analog Ground. |
| 7 | I1 | Current Source, 200µA nominal. |
| 8 | NIC | Not Internally Connected. |
| 9 | NIC | Not Internally Connected. |
| 10 | $\overline{CS}$ | Chip Select Input. |
| 11 | I2 | Current Source, 200µA nominal. |
| 12 | $X_{IN}$ | System Clock Input. |
| 13 | $X_{OUT}$ | System Clock Output (for Crystal or Resonator). |
| 14 | DGND | Digital Ground. |
| 15 | $DV_{DD}$ | Digital Supply, +5V nominal. |
| 16 | SCLK | Clock Input/Output for serial data transfer. |
| 17 | SDIO | Serial Data Input (can also function as Serial Data Output). |
| 18 | SDOUT | Serial Data Output. |
| 19 | $\overline{DRDY}$ | Data Ready. |
| 20 | NIC | Not Internally Connected. |
| 21 | NIC | Not Internally Connected. |
| 22 | MODE | SCLK Control Input (Master = 1, Slave = 0). |
| 23 | $AV_{DD}$ | Analog Supply, +5V nominal. |
| 24 | $REF_{IN-}$ | Reference Input Low. |
| 25 | $REF_{IN+}$ | Reference Input High. |
| 26 | $A_{IN}4P$ | Noninverting Input Channel 4. |
| 27 | $A_{IN}4N$ | Inverting Input Channel 4. |
| 28 | $A_{IN}3P$ | Noninverting Input Channel 3. |



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# ADS1286

www.burr-brown.com/databook/ADS1286.html

# 12-Bit Micro Power Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- SERIAL INTERFACE
- GUARANTEED NO MISSING CODES
- 20kHz SAMPLING RATE
- LOW SUPPLY CURRENT: 250µA
- ALTERNATE SOURCE TO LTC1286

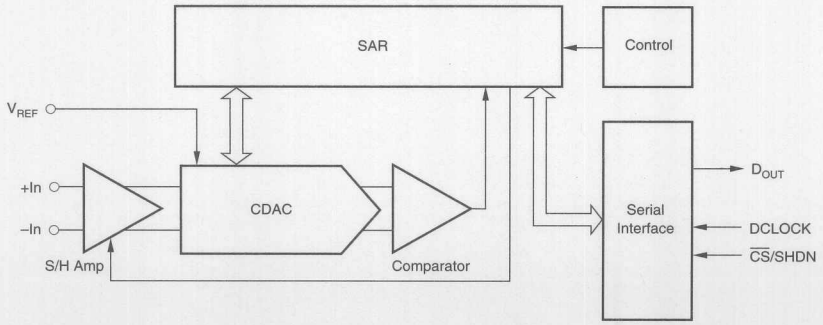
## APPLICATIONS

- REMOTE DATA ACQUISITION
- ISOLATED DATA ACQUISITION
- TRANSDUCER INTERFACE
- BATTERY OPERATED SYSTEMS

## DESCRIPTION

The ADS1286 is a 12-bit, 20kHz analog-to-digital converter with a differential input and sample and hold amplifier and consumes only 250µA of supply current. The ADS1286 offers an SPI and SSI compatible serial interface for communications over a two or three wire interface. The combination of a serial two wire interface and micropower consumption makes the ADS1286 ideal for remote applications and for those requiring isolation.

The ADS1286 is available in a 8-pin plastic mini DIP and a 8-lead SOIC.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A = T_{MIN}$ to $T_{MAX}$, $+V_{CC} = +5V$, $V_{REF} = +5V$, $f_{SAMPLE} = 12.5kHz$, , $f_{CLK} = 16 \bullet f_{SAMPLE}$, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS1286, ADS1286A | | | ADS1286K, ADS1286B | | | ADS1286C, ADS1286L | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ANALOG INPUT** | | | | | | | | | | | |
| Input Voltage Range (Unipolar) | | –0.05V | | $V_{CC}$+0.05V | * | | * | * | | * | V |
| Input Capacitance | | | 25 | | | * | | | * | | pF |
| Input Leakage Current | | | ±1 | | | * | | | * | | µA |
| **SYSTEM PERFORMANCE** | | | | | | | | | | | |
| Resolution | | | 12 | | | * | | | * | | Bits |
| No Missing Codes | | 12 | | | * | | | * | | | Bits |
| Integral Linearity | | | ±1 | ±2 | | * | * | | ±0.5 | ±1 | LSB |
| Differential Linearity | | | ±0.5 | ±1.0 | | * | ±0.75 | | ±0.25 | ±0.75 | LSB |
| Offset Error | | | 0.75 | ±3 | | * | * | | * | * | LSB |
| Gain Error | | | ±2 | ±8 | | * | * | | * | * | LSB |
| Noise | | | 50 | | | * | | | * | | µVrms |
| Power Supply Rejection | | | 82 | | | * | | | * | | dB |
| **SAMPLING DYNAMICS** | | | | | | | | | | | |
| Conversion Time | | | | 12 | | | * | | | * | Clk Cycles |
| Acquisition Time | | 1.5 | | | * | | | * | | | Clk Cycles |
| Small Signal Bandwidth | | | 500 | | | * | | | * | | kHz |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | | | | |
| Total Harmonic Distortion | $V_{IN}$ = 5.0Vp-p at 1kHz | | –85 | | | * | | | * | | dB |
| | $V_{IN}$ = 5.0Vp-p at 5kHz | | –83 | | | * | | | * | | dB |
| SINAD | $V_{IN}$ = 5.0Vp-p at 1kHz | | 72 | | | * | | | * | | dB |
| Spurious Free Dynamic Range | $V_{IN}$ = 5.0Vp-p at 1kHz | | 90 | | | * | | | * | | dB |
| **REFERENCE INPUT** | | | | | | | | | | | |
| REF Input Range | | 1.25 | 2.5 | $V_{CC}$+0.05V | * | * | * | * | * | * | V |
| Input Resistance | $\overline{CS} = V_{CC}$ | | 5000 | | | * | | | * | | MΩ |
| | $\overline{CS}$ = GND, $f_{CLK}$ = 0Hz | | 5000 | | | * | | | * | | MΩ |
| Current Drain | $\overline{CS} = V_{CC}$ | | 0.01 | 2.5 | | * | * | | * | * | µA |
| | $t_{CYC} \geq 640µs$, $f_{CLK} \leq 25kHz$ | | 2.4 | 20 | | * | * | | * | * | µA |
| | $t_{CYC}$ = 80µs, $f_{CLK}$ = 200kHz | | 2.4 | 20 | | * | * | | * | * | µA |
| **DIGITAL INPUT/OUTPUT** | | | | | | | | | | | |
| Logic Family | | | CMOS | | | * | | | * | | |
| Logic Levels: | | | | | | | | | | | |
| $V_{IH}$ | $I_{IH} = +5µA$ | 3 | | $+V_{CC}$ | * | | * | * | | * | V |
| $V_{IL}$ | $I_{IL} = +5µA$ | 0.0 | | 0.8 | * | | * | * | | * | V |
| $V_{OH}$ | $I_{OH} = 250µA$ | 3 | | $+V_{CC}$ | * | | * | * | | * | V |
| $V_{OL}$ | $I_{OL} = 250µA$ | 0.0 | | 0.4 | * | | * | * | | * | V |
| Data Format | | | Straight Binary | | | * | | | * | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | | | | |
| Power Supply Voltage $V_{CC}$ | | +4.50 | 5 | 5.25 | * | * | * | * | * | * | V |
| Quiescent Current, $V_{ANA}$ | $t_{CYC} \geq 640µS$, $f_{CLK} \leq 25kHz$ | | 200 | 400 | | * | * | | * | * | µA |
| | $t_{CYC}$ = 90µS, $f_{CLK}$ = 200kHz | | 250 | 500 | | * | * | | * | * | µA |
| Power Down | $\overline{CS} = V_{CC}$ | | | 3 | | | * | | | * | µA |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specified Performance | ADS1286, K, L | 0 | | +70 | * | | * | * | | * | °C |
| | ADS1286A, B, C | –40 | | +85 | * | | * | * | | * | °C |

* Specifications same as grade to the left.

# TIMING CHARACTERISTICS

$f_{CLK}$ = 200kHz, $T_A = T_{MIN}$ to $T_{MAX}$.

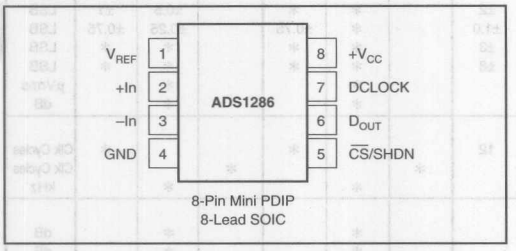
| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $t_{SMPL}$ | Analog Input Sample Time | See Operating Sequence | 1.5 | | 2.0 | Clk Cycles |
| $t_{SMPL\ (MAX)}$ | Maximum Sampling Frequency | ADS1286 | | | 20 | kHz |
| $t_{CONV}$ | Conversion Time | See Operating Sequence | | 12 | | Clk Cycles |
| $t_{dDO}$ | Delay TIme, DCLOCK↓ to $D_{OUT}$ Data Valid | See Test Circuits | | 85 | 150 | ns |
| $t_{dis}$ | Delay TIme, $\overline{CS}$↑ to $D_{OUT}$ Hi-Z | See Test Circuits | | 25 | 50 | ns |
| $t_{en}$ | Delay TIme, DCLOCK↓ to $D_{OUT}$ Enable | See Test Circuits | | 50 | 100 | ns |
| $t_{hDO}$ | Output Data Remains Valid After DCLOCK↓ | $C_{LOAD}$ = 100pF | 15 | 30 | | ns |
| $t_f$ | $D_{OUT}$ Fall Time | See Test Circuits | | 70 | 100 | ns |
| $t_r$ | $D_{OUT}$ Rise Time | See Test Circuits | | 60 | 100 | ns |
| $t_{CSD}$ | Delay Time, $\overline{CS}$↓ to DCLOCK↓ | See Operating Sequence | | | 0 | ns |
| $t_{SUCS}$ | Delay Time, $\overline{CS}$↓ to DCLOCK↑ | See Operating Sequence | 30 | | | ns |

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| $+V_{CC}$ | +6V |
| Analog Input | −0.3V to ($+V_{CC}$ + 300mV) |
| Logic Input | −0.3V to ($+V_{CC}$ + 300mV) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +125°C |
| External Reference Voltage | +5.5V |

NOTE: (1) Stresses above these ratings may permanently damage the device.

## PIN CONFIGURATION




8-Pin Mini PDIP
8-Lead SOIC

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN ASSIGNMENTS

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_{REF}$ | Reference Input. |
| 2 | +In | Non Inverting Input. |
| 3 | −In | Inverting Input. Connect to ground or remote ground sense point. |
| 4 | GND | Ground. |
| 5 | $\overline{CS}$/SHDN | Chip Select when low, Shutdown Mode when high. |
| 6 | $D_{OUT}$ | The serial output data word is comprised of 12 bits of data. In operation the data is valid on the falling edge of DCLOCK. The second clock pulse after the falling edge of $\overline{CS}$ enables the serial output. After one null bit the data is valid for the next 12 edges. |
| 7 | DCLOCK | Data Clock synchronizes the serial data transfer and determines conversion speed. |
| 8 | $+V_{CC}$ | Power Supply. |

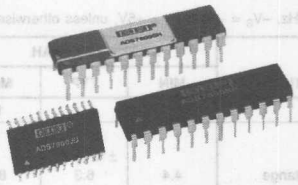
## PACKAGE/ORDERING INFORMATION

| PRODUCT | INTEGRAL LINEARITY | TEMPERATURE RANGE | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|---|---|
| ADS1286P | ±2 | 0°C to +70°C | Plastic DIP | 006 |
| ADS1286PK | ±2 | 0°C to +70°C | Plastic DIP | 006 |
| ADS1286PL | ±1 | 0°C to +70°C | Plastic DIP | 006 |
| ADS1286U | ±2 | 0°C to +70°C | SOIC | 182 |
| ADS1286UK | ±2 | 0°C to +70°C | SOIC | 182 |
| ADS1286UL | ±1 | 0°C to +70°C | SOIC | 182 |
| ADS1286PA | ±2 | −40°C to +85°C | Plastic DIP | 006 |
| ADS1286PB | ±2 | −40°C to +85°C | Plastic DIP | 006 |
| ADS1286PC | ±1 | −40°C to +85°C | Plastic DIP | 006 |
| ADS1286UA | ±2 | −40°C to +85°C | SOIC | 182 |
| ADS1286UB | ±2 | −40°C to +85°C | SOIC | 182 |
| ADS1286UC | ±1 | −40°C to +85°C | SOIC | 182 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# ADS7800

www.burr-brown.com/databook/ADS7800.html

# 12-Bit 3µs Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- 333k SAMPLES PER SECOND
- STANDARD ±10V AND ±5V INPUT RANGES
- DC PERFORMANCE OVER TEMP:
  No Missing Codes
  1/2LSB Integral Linearity Error
  3/4LSB Differential Linearity Error
- AC PERFORMANCE OVER TEMP:
  72dB Signal-to-Noise Ratio
  80dB Spurious-free Dynamic Range
  –80dB Total Harmonic Distortion
- INTERNAL SAMPLE/HOLD, REFERENCE, CLOCK, AND 3-STATE OUTPUTS
- POWER DISSIPATION: 215mW max
- PACKAGE: 24-Pin Single-wide DIP
  24-Lead SOIC

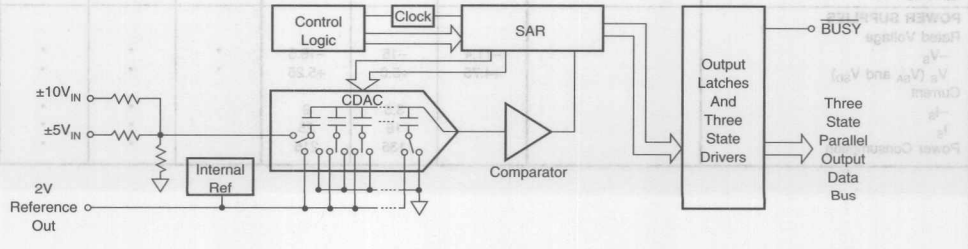
## DESCRIPTION

The ADS7800 is a complete 12-bit sampling analog-to-digital converter using state-of-the-art CMOS structures. It contains a complete 12-bit successive approximation A/D converter with internal sample/hold, reference, clock, digital interface for microprocessor control, and three-state output drivers.

The ADS7800 is specified at a 333kHz sampling rate. Conversion time is factory set for 2.70µs max over temperature, and the high speed sampling input stage insures a total acquisition and conversion time of 3µs max over temperature. Precision, laser-trimmed scaling resistors provide industry-standard input ranges of ±5V or ±10V.

AC and DC performance are completely specified. Two grades based on linearity and dynamic performance are available to provide the optimum price/performance fit in a wide range of applications.

The 24-pin ADS7800 is available in plastic and side-braze hermetic 0.3" wide DIPs, and in an SOIC package. It operates from a +5V supply and either a –12V or –15V supply. The ADS7800 is available in grades specified over 0°C to +70°C and –40°C to +85°C temperature ranges.




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# SPECIFICATIONS

## ELECTRICAL

At $T_A = T_{MIN}$ to $T_{MAX}$, Sampling Frequency, $f_S$, = 333kHz, $-V_S = -15V$, $V_S = +5V$, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7800JP/JU/AH MIN | ADS7800JP/JU/AH TYP | ADS7800JP/JU/AH MAX | ADS7800KP/KU/BH MIN | ADS7800KP/KU/BH TYP | ADS7800KP/KU/BH MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **RESOLUTION** | | | | 12 | | | * | Bits |
| **ANALOG INPUT** | | | | | | | | |
| Voltage Ranges | | | ±10V/±5V | | | * | | V |
| Impedance | ±10V Range | 4.4 | 6.3 | 8.1 | * | * | * | kΩ |
| | ±5V Range | 2.9 | 4.2 | 5.4 | * | * | * | kΩ |
| **THROUGHPUT SPEED** | | | | | | | | |
| Conversion Time | Conversion Alone | | 2.5 | 2.7 | | * | * | µs |
| Complete Cycle | Acquisition + Conversion | | 2.6 | 3.0 | | * | * | µs |
| Throughput Rate | | 333 | 380 | | * | * | | kHz |
| **DC ACCURACY** | | | | | | | | |
| Full Scale Error[1] | | | | ±0.50 | | | ±0.35 | % |
| Full Scale Error Drift | | | 6 | | | * | | ppm/°C |
| Integral Linearity Error | | | | ±1 | | | ±1/2 | LSB[2] |
| Differential Linearity Error | | | | ±1 | | | ±3/4 | LSB |
| No Missing Codes | | | Guaranteed | | | Guaranteed | | |
| Bipolar Zero[1] | | | | ±4 | | | ±2 | LSB |
| Bipolar Zero Drift | | | 1 | | | * | | ppm/°C |
| Power Supply Sensitivity | | | | | | | | |
| | $-16.5V < -V_S < -13.5V$ | | | ±1/2 | | | * | LSB |
| | $-12.6V < -V_S < -11.4V$ | | | ±1/2 | | | * | LSB |
| | $+4.75V < V_S < +5.25V$ | | | ±1 | | | ±1/2 | LSB |
| Transition Noise[3] | | | 0.1 | | | * | | LSB |
| **AC ACCURACY** | | | | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 47kHz | 74 | 77 | | 77 | 80 | | dB[4] |
| Total Harmonic Distortion | $f_{IN}$ = 47kHz | | –77 | –74 | | –80 | –77 | dB |
| Two-tone Intermodulation Distortion | $f_{IN1}$ = 24.4kHz (–6dB) $f_{IN2}$ = 28.5kHz (–6dB) | | –77 | –74 | | –80 | –77 | dB |
| Signal-to-(Noise + Distortion) Ratio | $f_{IN}$ = 47kHz | 67 | 70 | | 69 | 72 | | dB |
| Signal-to-Noise Ratio (SNR) | $f_{IN}$ = 47kHz | 68 | 71 | | 70 | 73 | | dB |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Aperture Delay | | | 13 | | | * | | ns |
| Aperture Jitter | | | 150 | | | * | | ps, rms |
| Transient Response[5] | | | 130 | | | * | | ns |
| Overvoltage Recovery[6] | | | 150 | | | * | | ns |
| **INTERNAL REFERENCE VOLTAGE** | | | | | | | | |
| Voltage | | 1.9 | 2.0 | 2.1 | * | * | * | V |
| Source Current Available for External Loads | | | 10 | | | * | | µA |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Levels | | | | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | * | | * | V |
| $V_{IH}$ | | +2.4 | | +5.3 | * | | * | V |
| $I_{IL}$ | | –5 | | | * | | | µA |
| $I_{IH}$ | | +5 | | | * | | | µA |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Data Format | | | | Parallel, 12-bit or 8-bit/4-bit | | | | |
| Data Coding | | | | Binary Offset Binary | | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | 0.0 | | +0.4 | * | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +2.4 | | +5.0 | * | | * | V |
| $I_{LEAKAGE}$ (High-Z State) | | | ±0.1 | ±5 | | * | * | µA |
| **POWER SUPPLIES** | | | | | | | | |
| Rated Voltage | | | | | | | | |
| $-V_S$ | | –11.4 | –15 | –16.5 | * | * | * | V |
| $V_S$ ($V_{SA}$ and $V_{SD}$) | | +4.75 | +5.0 | +5.25 | * | * | * | V |
| Current | | | | | | | | |
| $-I_S$ | | | 3.5 | 6 | | * | * | mA |
| $I_S$ | | | 18 | 25 | | * | * | mA |
| Power Consumption | | | 135 | 215 | | * | * | mW |

# SPECIFICATIONS (CONT)

## ELECTRICAL

At $T_A = T_{MIN}$ to $T_{MAX}$, Sampling Frequency, $f_S$, = 333kHz, $-V_S = -15V$, $V_S = +5V$, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7800JP/JU/AH | | | ADS7800KP/KU/BH | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | JP/JU/KP/KU | 0 | | +70 | * | | * | °C |
| | AH/BH | –40 | | +85 | * | | * | °C |
| Operating | JP/KP/JU/KU | –40 | | +85 | * | | * | °C |
| Storage | | –65 | | +150 | * | | * | °C |

* Same as specification for ADS7800JP/JU/AH.

NOTES: (1) Adjustable to zero with external potentiometer. (2) LSB means Least Significant Bit. For ADS7800, 1LSB = 2.44mV for the ±5V range, 1LSB = 4.88mV for the ±10V range. (3) Noise was characterized over temperature near full scale, 0V, and negative full scale. 0.1LSB represents a typical rms level of noise at the worst case, which was near full scale input at +125°C. (4) All specifications in dB are referred to a full-scale input, either ±10V or ±5V. (5) For full scale step input, 12-bit accuracy attained in specified time. (6) Recovers to specified performance in specified time after 2 x $F_S$ input overvoltage.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $-V_S$ to ANALOG COMMON | –16.5V |
| $V_S$ to DIGITAL COMMON | +7V |
| Pin 23 ($V_{SD}$) to Pin 24 ($V_{SA}$) | ±0.3V |
| ANALOG COMMON to DIGITAL COMMON | ±1V |
| Control Inputs to DIGITAL COMMON | –0.3 to $V_S$ + 0.3V |
| Analog Input Voltage | ±20V |
| Maximum Junction Temperature | 160°C |
| Internal Power Dissipation | 750mW |
| Lead Temperature (soldering, 10s) | +300°C |
| Thermal Resistance, $\theta_{JA}$: | |
| Plastic DIP | 100°C/W |
| SOIC | 100°C/W |
| Ceramic | 50°C/W |

## ELECTROSTATIC DISCHARGE SENSITIVITY

The ADS7800 is an ESD (electrostatic discharge) sensitive device. The digital control inputs have a special FET structure, which turns on when the input exceeds the supply by 18V, to minimize ESD damage. However, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | INTEGRAL LINEARITY ERROR (LSB) | SIGNAL-TO-(NOISE+DISTORTION) RATIO (dB min) | SPECIFICATION TEMPERATURE RANGE (°C) | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|---|---|---|
| ADS7800JP | ±1 | 67 | 0 to +70 | 24-Pin Plastic DIP | 243 |
| ADS7800KP | ±1/2 | 69 | 0 to +70 | 24-Pin Plastic DIP | 243 |
| ADS7800JU | ±1 | 67 | 0 to +70 | 24-Pin Plastic SOIC | 239 |
| ADS7800KU | ±1/2 | 69 | 0 to +70 | 24-Pin Plastic SOIC | 239 |
| ADS7800AH | ±1 | 67 | –40 to +85 | 24-Pin Ceramic DIP | 245 |
| ADS7800BH | ±1/2 | 69 | –40 to +85 | 24-Pin Ceramic DIP | 245 |

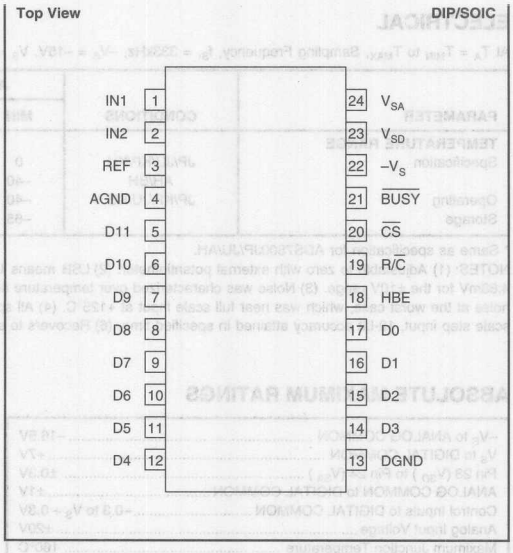
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



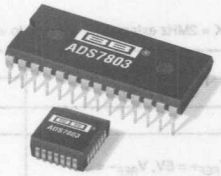
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| PIN # | NAME | DESCRIPTION |
|---|---|---|
| 1 | IN1 | ±10V Analog Input. Connected to GND for ±5V range. |
| 2 | IN2 | ±5V Analog Input. Connected to GND for ±10V range. |
| 3 | REF | +2V Reference Output. Bypass to GND with 22µF to 47µF Tantalum. Buffer for external loads. |
| 4 | AGND | Analog Ground. Connect to pin 13. |
| 5 | D11 | Data Bit 11. Most Significant Bit (MSB). |
| 6 | D10 | Data Bit 10. |
| 7 | D9 | Data Bit 9. |
| 8 | D8 | Data Bit 8. |
| 9 | D7 | Data Bit 7 if HBE is LOW; LOW if HBE is HIGH. |
| 10 | D6 | Data Bit 6 if HBE is LOW; LOW if HBE is HIGH. |
| 11 | D5 | Data Bit 5 if HBE is LOW; LOW if HBE is HIGH. |
| 12 | D4 | Data Bit 4 if HBE is LOW; LOW if HBE is HIGH. |
| 13 | DGND | Digital Ground. Connect to pin 4. |
| 14 | D3 | Data Bit 3 if HBE is LOW; Data Bit 11 if HBE is HIGH. |
| 15 | D2 | Data Bit 2 if HBE is LOW; Data Bit 10 if HBE is HIGH. |
| 16 | D1 | Data Bit 1 if HBE is LOW; Data Bit 9 if HBE is HIGH. |
| 17 | D0 | Data Bit 0 if HBE is LOW. Least Significant Bit (LSB); Data Bit 8 if HBE is HIGH. |
| 18 | HBE | High Byte Enable. When held LOW, data output as 12-bits in parallel. When held HIGH, four MSBs presented on pins 14-17, pins 9-12 output LOWs. Must be LOW to initiate conversion. |
| 19 | R/$\overline{C}$ | Read/Convert. Falling edge initiates conversion when $\overline{CS}$ is LOW, HBE is LOW, and $\overline{BUSY}$ is HIGH. |
| 20 | $\overline{CS}$ | Chip Select. Outputs in Hi-Z state when HIGH. Must be LOW to initiate conversion or read data. |
| 21 | $\overline{BUSY}$ | Busy. Output LOW during conversion. Data valid on rising edge in Convert Mode. |
| 22 | $-V_S$ | Negative Power Supply. –12V or –15V. Bypass to GND. |
| 23 | $V_{SD}$ | Positive Digital Power Supply. +5V. Connect to pin 24, and bypass to GND. |
| 24 | $V_{SA}$ | Positive Analog Power Supply. +5V. Connect to pin 23, and bypass to GND. |

Top View DIP/SOIC



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# ADS7803

www.burr-brown.com/databook/ADS7803.html

# Autocalibrating, 4-Channel, 12-Bit ANALOG-TO-DIGITAL CONVERTER

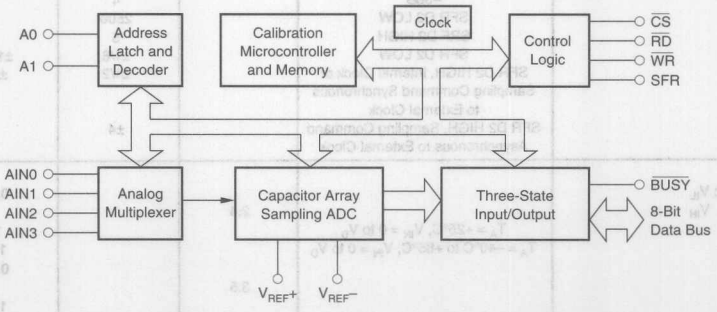
## FEATURES

- LOW POWER: 10mW plus Power Down
- SIGNAL-TO-(NOISE + DISTORTION) RATIO OVER TEMPERATURE:
  69dB min with $f_{IN}$ = 1kHz
  66dB min with $f_{IN}$ = 50kHz
- FAST CONVERSION TIME: 8.5µs Including Acquisition (117kHz Sampling Rate)
- DC PERFORMANCE OVER TEMPERATURE:
  ±3/4 LSB max Total Error
  ±1/4 LSB max Channel Mismatch
- FOUR-CHANNEL INPUT MULTIPLEXER
- SINGLE SUPPLY: +5V
- PIN COMPATIBLE WITH ADC7802

## DESCRIPTION

The ADS7803 is a monolithic CMOS 12-bit analog-to-digital converter with internal sample/hold and four-channel multiplexer. It is designed and tested for full dynamic performance with input signals to 50kHz. An autocalibration cycle guarantees a total unadjusted error within ±3/4LSB over the specified temperature range, eliminating the need for offset or gain adjustment. The 5V single-supply requirements and standard $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ control signals make the part easy to use in microprocessor applications. Conversion results are available in two bytes through an 8-bit three-state output bus.

The ADS7803 is available in a 28-pin plastic DIP and 28-lead PLCC, fully specified for operation over the industrial –40°C to +85°C temperature range.




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# SPECIFICATIONS

## ELECTRICAL

$V_A = V_D = V_{REF}+ = 5V \pm 5\%$; $V_{REF}- = AGND = DGND = 0V$; CLK = 2MHz external, $T_A = -40°C$ to $+85°C$, after calibration at any temperature, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7803BP/ADS7803BN MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | | 12 | Bits |
| **ANALOG INPUT** | | | | | |
| Voltage Input Range | $V_{REF}+ = 5V$, $V_{REF}- = 0V$ | 0 | | 5 | V |
| Input Capacitance | | | 50 | | pF |
| On State Bias Current | | | 100 | | nA |
| Off State Bias Current | $T_A = +25°C$ | | | 10 | nA |
| | $T_A = -40°C$ to $+85°C$ | | | 100 | nA |
| On Resistance Multiplexer | | | 2 | | kΩ |
| Off Resistance Multiplexer | | | 10 | | MΩ |
| Channel Separation | 500Hz | | 92 | | dB |
| **REFERENCE INPUT** | | | | | |
| For Specified Performance: $V_{REF}+$ | $V_{REF}+ \leq V_A$ | | 5 | | V |
| $V_{REF}-$ | | | 0 | | V |
| For Derated Performance[1]: $V_{REF}+$ | | 4.5 | | $V_A$ | V |
| $V_{REF}-$ | | 0 | | 1 | V |
| Input Reference Current | $V_{REF}+ = 5V$, $V_{REF}- = 0V$ | | 10 | 100 | µA |
| **THROUGHPUT TIMING** | | | | | |
| Conversion Time With External Clock (Including | CLK = 2MHz | | | 8.5 | µs |
| Multiplexer Settling Time and Acquisition Time) | CLK = 1MHz | | | 17 | µs |
| | CLK = 500kHz | | | 34 | µs |
| With Internal Clock Using Recommended | $T_A = +25°C$ | | | 10 | µs |
| Clock Components | $T_A = -40°C$ to $+85°C$ | | 10 | | µs |
| Multiplexer Settling Time to 0.01% | | | 460 | | ns |
| Multiplexer Access Time | | | | 20 | ns |
| **DC ACCURACY** | | | | | |
| Total Error, All Channels[2] | | | ±1/2 | ±3/4 | LSB |
| Differential Nonlinearity | | | ±1/4 | ±1/2 | LSB |
| No Missing Codes | | | Guaranteed | | |
| Gain Error | All Channels | | ±1/8 | ±1/4 | LSB |
| Gain Error Drift | Between Calibration Cycles | | ±0.2 | | ppm/°C |
| Offset Error | All Channels | | ±1/8 | ±1/4 | LSB |
| Offset Error Drift | Between Calibration Cycles | | ±0.2 | | ppm/°C |
| Channel-to-Channel Mismatch | | | | ±1/4 | LSB |
| Power Supply Sensitivity | $V_A = V_D = 4.75V$ to $5.25V$ | | ±1/8 | | LSB |
| **AC ACCURACY** | | | | | |
| Signal-to-(Noise + Distortion) Ratio | $f_{IN} = 1kHz$ | 69 | 71 | | dB |
| | $f_{IN} = 50kHz$ | 66 | 69 | | dB |
| Total Harmonic Distortion | $f_{IN} = 50kHz$ | | –75 | | dB |
| Signal-to-Noise Ratio | $f_{IN} = 50kHz$ | | 70 | | dB |
| Spurious Free Dynamic Range | $f_{IN} = 1kHz$ | | 90 | | dB |
| | $f_{IN} = 50kHz$ | | 82 | | dB |
| **SAMPLING DYNAMICS** | | | | | |
| Full Power Bandwidth | –3dB | | 4 | | MHz |
| Aperture Delay | SFR D2 LOW | | 2500 | | ns |
| Offset Error | SRF D2 HIGH | | 5 | | ns |
| | SFR D2 LOW | | ±1/8 | ±1/4 | LSB |
| | SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock | | ±1/2 | ±1 | LSB |
| | SFR D2 HIGH, Sampling Command Asynchronous to External Clock | | ±4 | | LSB |
| **DIGITAL INPUTS** | | | | | |
| All Pins Other Than CLK: $V_{IL}$ | | | | 0.8 | V |
| $V_{IH}$ | | 2.4 | | | V |
| Input Current | $T_A = +25°C$, $V_{IN} = 0$ to $V_D$ | | | 1 | µA |
| | $T_A = -40°C$ to $+85°C$, $V_{IN} = 0$ to $V_D$ | | | 10 | µA |
| CLK Input: $V_{IL}$ | | | | 0.8 | V |
| $V_{IH}$ | | 3.5 | | | V |
| $I_{IL}$ | | | | 10 | µA |
| $I_{IH}$ | | | | 1.5 | mA |
| $I_{IH}$ | Power Down Mode (D3 in SFR HIGH) | | | 100 | nA |

NOTES: (1) For $(V_{REF}+) - (V_{REF}-)$ as low as 4.5V, the total error will typically not exceed ±1LSB. (2) After calibration cycle, without external adjustment. Includes gain (full scale) error, offset error, integral nonlinearity, differential nonlinearity, and drift.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

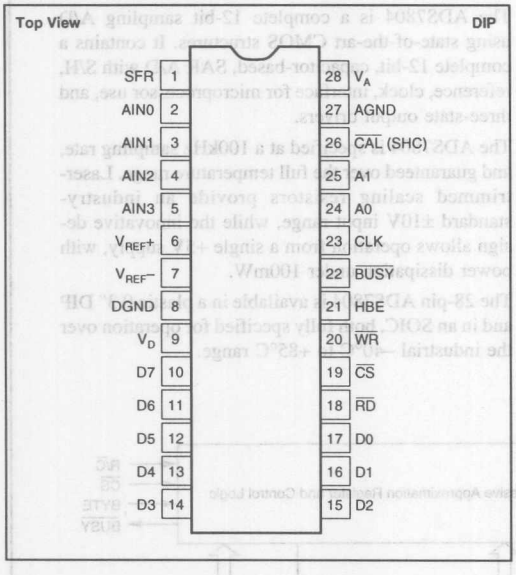
# SPECIFICATIONS (CONT)

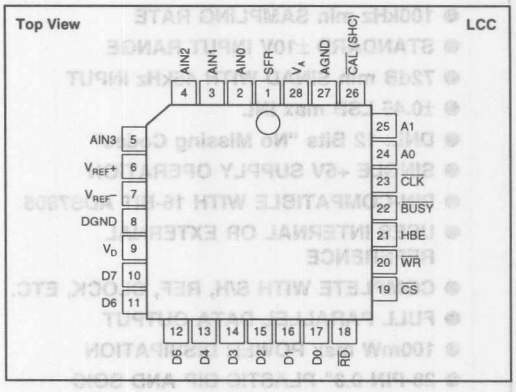
## ELECTRICAL

$V_A = V_D = V_{REF}+ = 5V \pm 5\%$; $V_{REF}-$ = AGND = DGND = 0V; CLK = 2MHz external, $T_A$ = –40°C to +85°C, after calibration at any temperature, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7803BP/ADS7803BN MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **DIGITAL OUTPUTS** | | | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | 0.4 | V |
| $V_{OH}$ | $I_{SOURCE}$ = 200µA | 4 | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_D$ | | | ±1 | µA |
| Output Capacitance | High-Z State | | 4 | 15 | pF |
| **POWER SUPPLIES** | | | | | |
| Supply Voltage for Specified Performance: $V_A$ | | 4.75 | 5 | 5.25 | V |
| $V_D$ | $V_A \geq V_D$ | 4.75 | 5 | 5.25 | V |
| Supply Current: $I_A$ | | | 1 | 2.5 | mA |
| $I_D$ | Logic Input Pins HIGH or LOW | | 1 | 2 | mA |
| Power Dissipation | $\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = HIGH | | 10 | | mW |
| Power Down Mode | See Table III | | 50 | | µW |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –40 | | +85 | °C |
| Storage | | –65 | | +150 | °C |

## PIN CONFIGURATIONS




## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| ADC7803BN | 28-Pin LCC | 251 |
| ADS7803BP | 28-Pin Plastic DIP | 215 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

| PRODUCT | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO, dB | MAXIMUM TOTAL ERROR, LSB | SPECIFICATION TEMPERATURE RANGE |
|---|---|---|---|
| ADS7803BN | 69 | ±3/4 | –40°C to +85°C |
| ADS7803BP | 69 | ±3/4 | –40°C to +85°C |

## ABSOLUTE MAXIMUM RATINGS

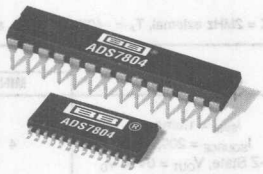
| | |
|---|---|
| $V_A$ to Analog Ground | 6.5V |
| $V_D$ to Digital Ground | 6.5V |
| Pin $V_A$ to Pin $V_D$ | ±0.3V |
| Analog Ground to Digital Ground | ±1V |
| Control Inputs to Digital Ground | –0.3V to $V_D$ + 0.3V |
| Analog Input Voltage to Analog Ground | –0.3V to $V_D$ + 0.3V |
| Maximum Junction Temperature | 150°C |
| Internal Power Dissipation | 875mW |
| Lead Temperature (soldering, 10s) | +300°C |
| Thermal Resistance, $\theta_{JA}$: Plastic DIP | 75°C/W |
| PLCC | 75°C/W |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# ADS7804

**DEMO BOARD AVAILABLE**
**See Appendix A**

www.burr-brown.com/databook/ADS7804.html

# 12-Bit 10µs Sampling CMOS ANALOG-to-DIGITAL CONVERTER

## FEATURES

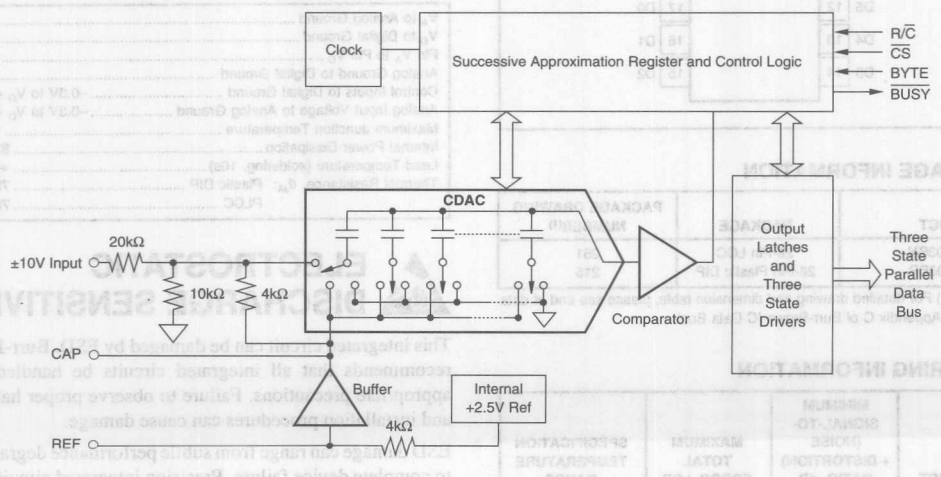
- 100kHz min SAMPLING RATE
- STANDARD ±10V INPUT RANGE
- 72dB min SINAD WITH 45kHz INPUT
- ±0.45 LSB max INL
- DNL: 12 Bits "No Missing Codes"
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 16-BIT ADS7805
- USES INTERNAL OR EXTERNAL REFERENCE
- COMPLETE WITH S/H, REF, CLOCK, ETC.
- FULL PARALLEL DATA OUTPUT
- 100mW max POWER DISSIPATION
- 28-PIN 0.3" PLASTIC DIP AND SOIC

## DESCRIPTION

The ADS7804 is a complete 12-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 12-bit, capacitor-based, SAR A/D with S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7804 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide an industry-standard ±10V input range, while the innovative design allows operation from a single +5V supply, with power dissipation under 100mW.

The 28-pin ADS7804 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132



PDS-1156C

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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 100kHz, and $V_{DIG} = V_{ANA}$ = +5V, using internal reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7804P, U | | | ADS7804PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | | 12 | | | * | Bits |
| **ANALOG INPUT** | | | | | | | | |
| Voltage Ranges | | | ±10V | | | * | | V |
| Impedance | | | 23 | | | * | | kΩ |
| Capacitance | | | 35 | | | * | | pF |
| **THROUGHPUT SPEED** | | | | | | | | |
| Conversion Time | | | 5.7 | 8 | | * | * | µs |
| Complete Cycle | Acquire and Convert | | | 10 | | | * | µs |
| Throughput Rate | | 100 | | | * | | | kHz |
| **DC ACCURACY** | | | | | | | | |
| Integral Linearity Error | | | | ±0.9 | | | ±0.45 | LSB[1] |
| Differential Linearity Error | | | | ±0.9 | | | ±0.45 | LSB |
| No Missing Codes | | | Guaranteed | | | * | | Bits |
| Transition Noise[2] | | | 0.1 | | | * | | LSB |
| Full Scale Error[3,4] | | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | | | ±7 | | | ±5 | | ppm/°C |
| Full Scale Error[3,4] | Ext. 2.5000V Ref | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | Ext. 2.5000V Ref | | ±2 | | | * | | ppm/°C |
| Bipolar Zero Error[3] | | | | ±10 | | | ±10 | mV |
| Bipolar Zero Error Drift | | | ±2 | | | * | | ppm/°C |
| Power Supply Sensitivity ($V_{DIG} = V_{ANA} = V_D$) | +4.75V < $V_D$ < +5.25V | | | ±0.5 | | | * | LSB |
| **AC ACCURACY** | | | | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 45kHz | 80 | | | * | | | dB[5] |
| Total Harmonic Distortion | $f_{IN}$ = 45kHz | | | –80 | | | * | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 45kHz | 70 | | | 72 | | | dB |
| Signal-to-Noise | $f_{IN}$ = 45kHz | 70 | | | 72 | | | dB |
| Full-Power Bandwidth[6] | | | 250 | | | * | | kHz |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Aperture Delay | | | 40 | | | * | | ns |
| Aperture Jitter | | | Sufficient to meet AC specs | | | * | | |
| Transient Response | FS Step | | | 2 | | | * | µs |
| Overvoltage Recovery[7] | | | 150 | | | * | | ns |
| **REFERENCE** | | | | | | | | |
| Internal Reference Voltage | | 2.48 | 2.5 | 2.52 | * | * | * | V |
| Internal Reference Source Current (Must use external buffer.) | | | 1 | | | * | | µA |
| Internal Reference Drift | | | 8 | | | | | ppm/°C |
| External Reference Voltage Range for Specified Linearity | | 2.3 | 2.5 | 2.7 | * | * | * | V |
| External Reference Current Drain | Ext. 2.5000V Ref | | | 100 | | | * | µA |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Levels | | | | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | * | | * | V |
| $V_{IH}$ | | +2.0 | | $V_D$ +0.3V | * | | * | V |
| $I_{IL}$ | | | | ±10 | | | * | µA |
| $I_{IH}$ | | | | ±10 | | | * | µA |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Data Format | | | | Parallel 12 bits | | | | |
| Data Coding | | | | Binary Two's Complement | | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +4 | | | * | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_{DIG}$ | | | ±5 | | | * | µA |
| Output Capacitance | High-Z State | | | 15 | | | 15 | pF |
| **DIGITAL TIMING** | | | | | | | | |
| Bus Access Time | | | | 83 | | | * | ns |
| Bus Relinquish Time | | | | 83 | | | * | ns |

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# SPECIFICATIONS (CONT)

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 100kHz, and $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7804P, U | | | ADS7804PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **POWER SUPPLIES** | | | | | | | | |
| Specified Performance | | | | | | | | |
| $V_{DIG}$ | Must be ≤ $V_{ANA}$ | +4.75 | +5 | +5.25 | * | * | * | V |
| $V_{ANA}$ | | +4.75 | +5 | +5.25 | * | * | * | V |
| $+I_{DIG}$ | | | 0.3 | | | * | | mA |
| $+I_{ANA}$ | | | 16 | | | * | | mA |
| Power Dissipation | $f_S$ = 100kHz | | | 100 | | | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | °C |
| Derated Performance | | –55 | | +125 | * | | * | °C |
| Storage | | –65 | | +150 | * | | * | °C |
| Thermal Resistance ($\theta_{JA}$) | | | | | | | | |
| Plastic DIP | | | 75 | | | * | | °C/W |
| SOIC | | | 75 | | | * | | °C/W |

* Specifications same as ADS7804P, U.

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, ±10V input ADS7804, one LSB is 4.88mV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $V_{IN}$ | ±25V |
| CAP | $+V_{ANA}$ +0.3V to AGND2 –0.3V |
| REF | Indefinite Short to AGND2 |
| | Momentary Short to $V_{ANA}$ |
| Ground Voltage Differences: DGND, AGND1, AGND2 | ±0.3V |
| $V_{ANA}$ | 7V |
| $V_{DIG}$ to $V_{ANA}$ | +0.3V |
| $V_{DIG}$ | 7V |
| Digital Inputs | –0.3V to $+V_{DIG}$ +0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ADS7804P | Plastic DIP | 246 |
| ADS7804PB | Plastic DIP | 246 |
| ADS7804U | SOIC | 217 |
| ADS7804UB | SOIC | 217 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

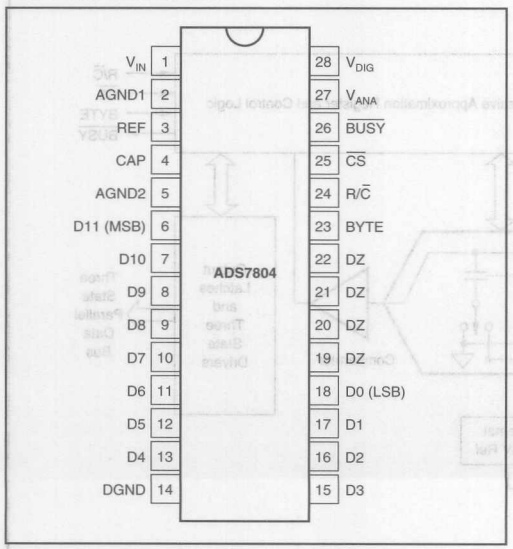
## ORDERING INFORMATION

| PRODUCT | MAXIMUM LINEARITY ERROR (LSB) | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE |
|---|---|---|---|---|
| ADS7804P | ±0.9 | 70 | –40°C to +85°C | Plastic DIP |
| ADS7804PB | ±0.45 | 72 | –40°C to +85°C | Plastic DIP |
| ADS7804U | ±0.9 | 70 | –40°C to +85°C | SOIC |
| ADS7804UB | ±0.45 | 72 | –40°C to +85°C | SOIC |

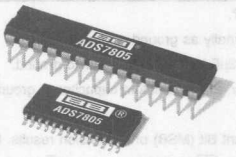
| PIN # | NAME | DIGITAL I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $V_{IN}$ | | Analog Input. See Figure 7. |
| 2 | AGND1 | | Analog Ground. Used internally as ground reference point. |
| 3 | REF | | Reference Input/Output. 2.2µF tantalum capacitor to ground. |
| 4 | CAP | | Reference Buffer Capacitor. 2.2µF tantalum capacitor to ground. |
| 5 | AGND2 | | Analog Ground. |
| 6 | D15 (MSB) | O | Data Bit 11. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 7 | D14 | O | Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 8 | D13 | O | Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 9 | D12 | O | Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 10 | D11 | O | Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 11 | D10 | O | Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 12 | D9 | O | Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 13 | D8 | O | Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 14 | DGND | | Digital Ground. |
| 15 | D7 | O | Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 16 | D6 | O | Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 17 | D5 | O | Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 18 | D4 | O | Data Bit 0. Lease Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 19 | D3 | O | LOW when $\overline{CS}$ LOW, R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 20 | D2 | O | LOW when $\overline{CS}$ LOW, R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 21 | D1 | O | LOW when $\overline{CS}$ LOW, R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 22 | D0 (LSB) | O | LOW when $\overline{CS}$ LOW, R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 23 | BYTE | I | Selects 8 most significant bits (LOW) or 8 least significant bits (HIGH). |
| 24 | R/$\overline{C}$ | I | With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output. |
| 25 | $\overline{CS}$ | I | Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ initiates a new conversion. |
| 26 | $\overline{BUSY}$ | O | At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated. |
| 27 | $V_{ANA}$ | | Analog Supply Input. Nominally +5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors. |
| 28 | $V_{DIG}$ | | Digital Supply Input. Nominally +5V. Connect directly to pin 27. Must be ≤ $V_{ANA}$. |

TABLE I. Pin Assignments.

## PIN CONFIGURATION



BURR-BROWN®



# ADS7805

**DEMO BOARD AVAILABLE**
**See Appendix A**

www.burr-brown.com/databook/ADS7805.html

# 16-Bit 10μs Sampling CMOS ANALOG-to-DIGITAL CONVERTER

## FEATURES

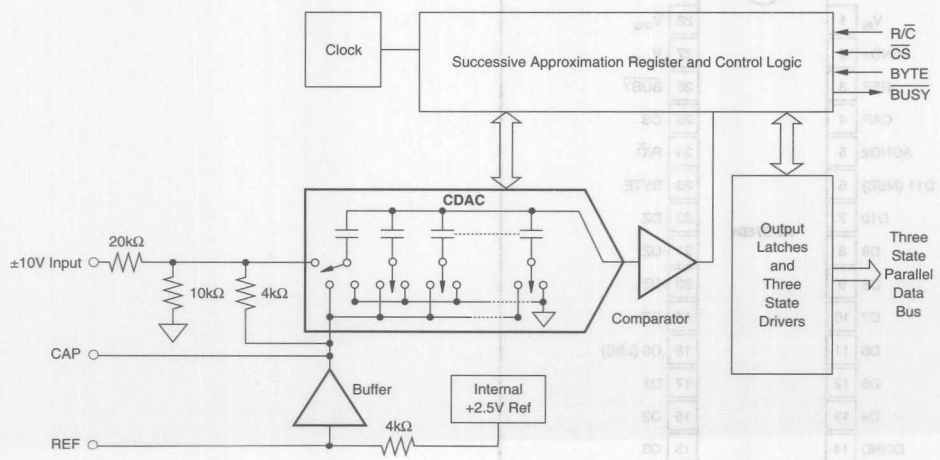
- 100kHz min SAMPLING RATE
- STANDARD ±10V INPUT RANGE
- 86dB min SINAD WITH 20kHz INPUT
- ±3.0 LSB max INL
- DNL: 16-bits "No Missing Codes"
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 12-BIT ADS7804
- USES INTERNAL OR EXTERNAL REFERENCE
- FULL PARALLEL DATA OUTPUT
- 100mW max POWER DISSIPATION
- 28-PIN 0.3" PLASTIC DIP AND SOIC

## DESCRIPTION

The ADS7805 is a complete 16-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, SAR A/D with S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7805 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide an industry-standard ±10V input range, while the innovative design allows operation from a single +5V supply, with power dissipation under 100mW.

The 28-pin ADS7805 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –25°C to +85°C range.




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PDS-1157E

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# SPECIFICATIONS

## ELECTRICAL

$T_A$ = –25°C to +85°C, $f_S$ = 100kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7805P, U | | | ADS7805PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | | 16 | | | * | Bits |
| **ANALOG INPUT** | | | | | | | | |
| Voltage Ranges | | | ±10V | | | * | | V |
| Impedance | | | 23 | | | * | | kΩ |
| Capacitance | | | 35 | | | * | | pF |
| **THROUGHPUT SPEED** | | | | | | | | |
| Conversion Cycle | Acquire and Convert | | | 10 | | | * | µs |
| Throughput Rate | | 100 | | | * | | | kHz |
| **DC ACCURACY** | | | | | | | | |
| Integral Linearity Error | | | | ±4 | | | ±3 | LSB[1] |
| No Missing Codes | | 15 | | | 16 | | | Bits |
| Transition Noise[2] | | | 1.3 | | | * | | LSB |
| Full Scale Error[3,4] | | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | | | ±7 | | | ±5 | | ppm/°C |
| Full Scale Error[3,4] | Ext. 2.5000V Ref | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | Ext. 2.5000V Ref | | ±2 | | | * | | ppm/°C |
| Bipolar Zero Error[3] | | | | ±10 | | | * | mV |
| Bipolar Zero Error Drift | | | ±2 | | | * | | ppm/°C |
| Power Supply Sensitivity | +4.75V < $V_D$ < +5.25V | | | ±8 | | | * | LSB |
| ($V_{DIG}$ = $V_{ANA}$ = $V_D$) | | | | | | | | |
| **AC ACCURACY** | | | | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 20kHz | 90 | | | 94 | | | dB[5] |
| Total Harmonic Distortion | $f_{IN}$ = 20kHz | | | –90 | | | –94 | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 20kHz | 83 | | | 86 | | | dB |
| | –60dB Input | | 30 | | | 32 | | dB |
| Signal-to-Noise | $f_{IN}$ = 20kHz | 83 | | | 86 | | | dB |
| Full-Power Bandwidth[6] | | | 250 | | | * | | kHz |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Aperture Delay | | | 40 | | | * | | ns |
| Transient Response | FS Step | | | 2 | | | * | µs |
| Overvoltage Recovery[7] | | | 150 | | | * | | ns |
| **REFERENCE** | | | | | | | | |
| Internal Reference Voltage | | 2.48 | 2.5 | 2.52 | * | * | * | V |
| Internal Reference Source Current (Must use external buffer.) | | | 1 | | | * | | µA |
| Internal Reference Drift | | | 8 | | | * | | ppm/°C |
| External Reference Voltage Range for Specified Linearity | | 2.3 | 2.5 | 2.7 | * | * | * | V |
| External Reference Current Drain | Ext. 2.5000V Ref | | | 100 | | | * | µA |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Levels | | | | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | * | | * | V |
| $V_{IH}$ | | +2.0 | | $V_D$ +0.3V | * | | * | V |
| $I_{IL}$ | | | | ±10 | | | * | µA |
| $I_{IH}$ | | | | ±10 | | | * | µA |
| **DIGITAL OUTPUTS** | | | Parallel 16-bits | | | | | |
| Data Format | | | Binary Two's Complement | | | | | |
| Data Coding | | | | | | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +4 | | | * | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_{DIG}$ | | | ±5 | | | * | µA |
| Output Capacitance | High-Z State | | | 15 | | | 15 | pF |
| **DIGITAL TIMING** | | | | | | | | |
| Bus Access Time | | | | 83 | | | * | ns |
| Bus Relinquish Time | | | | 83 | | | * | ns |

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# SPECIFICATIONS (CONT)

## ELECTRICAL

$T_A$ = –25°C to +85°C, $f_S$ = 100kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7805P, U | | | ADS7805PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **POWER SUPPLIES** | | | | | | | | |
| Specified Performance | | | | | | | | |
| $V_{DIG}$ | Must be ≤ $V_{ANA}$ | +4.75 | +5 | +5.25 | * | * | * | V |
| $V_{ANA}$ | | +4.75 | +5 | +5.25 | * | * | * | V |
| $I_{DIG}$ | | | 0.3 | | | * | | mA |
| $I_{ANA}$ | | | 16 | | | * | | mA |
| Power Dissipation | $f_S$ = 100kHz | | | 100 | | | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –25 | | +85 | * | | * | °C |
| Derated Performance | | –55 | | +125 | * | | * | °C |
| Storage | | –65 | | +150 | * | | * | °C |
| Thermal Resistance ($\theta_{JA}$) | | | | | | | | |
| Plastic DIP | | | 75 | | | * | | °C/W |
| SOIC | | | 75 | | | * | | °C/W |

* Specifications same as ADS7805P, U.

NOTES: (1) LSB means Least Significant Bit. For the 16-bit, ±10V input ADS7805, one LSB is 305µV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $V_{IN}$ | ±25V |
| CAP | +$V_{ANA}$ +0.3V to AGND2 –0.3V |
| REF | Indefinite Short to AGND2, Momentary Short to $V_{ANA}$ |
| Ground Voltage Differences: DGND, AGND1, AGND2 | ±0.3V |
| $V_{ANA}$ | 7V |
| $V_{DIG}$ to $V_{ANA}$ | +0.3V |
| $V_{DIG}$ | 7V |
| Digital Inputs | –0.3V to +$V_{DIG}$ +0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ADS7805P | Plastic DIP | 246 |
| ADS7805PB | Plastic DIP | 246 |
| ADS7805U | SOIC | 217 |
| ADS7805UB | SOIC | 217 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

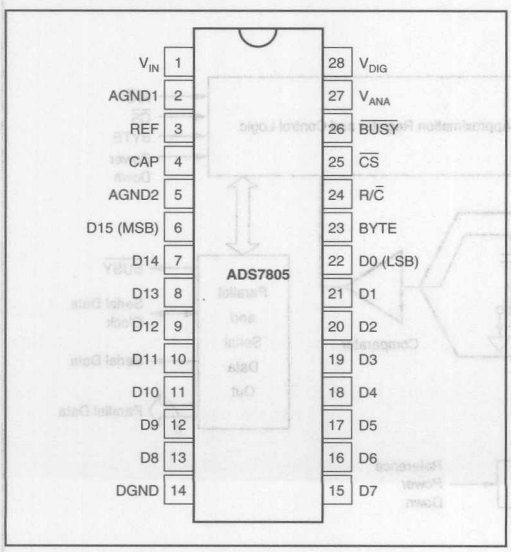
## ORDERING INFORMATION

| PRODUCT | MAXIMUM LINEARITY ERROR (LSB) | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE |
|---|---|---|---|---|
| ADS7805P | ±4 | 83 | –25°C to +85°C | Plastic DIP |
| ADS7805PB | ±3 | 86 | –25°C to +85°C | Plastic DIP |
| ADS7805U | ±4 | 83 | –25°C to +85°C | SOIC |
| ADS7805UB | ±3 | 86 | –25°C to +85°C | SOIC |

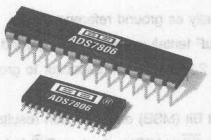
| PIN # | NAME | DIGITAL I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $V_{IN}$ | | Analog Input. See Figure 7. |
| 2 | AGND1 | | Analog Ground. Used internally as ground reference point. |
| 3 | REF | | Reference Input/Output. 2.2µF tantalum capacitor to ground. |
| 4 | CAP | | Reference Buffer Capacitor. 2.2µF tantalum capacitor to ground. |
| 5 | AGND2 | | Analog Ground. |
| 6 | D15 (MSB) | O | Data Bit 15. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 7 | D14 | O | Data Bit 14. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 8 | D13 | O | Data Bit 13. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 9 | D12 | O | Data Bit 12. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 10 | D11 | O | Data Bit 11. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 11 | D10 | O | Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 12 | D9 | O | Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 13 | D8 | O | Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 14 | DGND | | Digital Ground. |
| 15 | D7 | O | Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 16 | D6 | O | Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 17 | D5 | O | Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 18 | D4 | O | Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 19 | D3 | O | Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 20 | D2 | O | Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 21 | D1 | O | Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 22 | D0 (LSB) | O | Data Bit 0. Lease Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 23 | BYTE | I | Selects 8 most significant bits (LOW) or 8 least significant bits (HIGH). |
| 24 | R/$\overline{C}$ | I | With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output. |
| 25 | $\overline{CS}$ | I | Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ initiates a new conversion. |
| 26 | $\overline{BUSY}$ | O | At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated. |
| 27 | $V_{ANA}$ | | Analog Supply Input. Nominally +5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors. |
| 28 | $V_{DIG}$ | | Digital Supply Input. Nominally +5V. Connect directly to pin 27. Must be ≤ $V_{ANA}$. |

TABLE I. Pin Assignments.

## PIN CONFIGURATION



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# ADS7806

www.burr-brown.com/databook/ADS7806.html

# Low-Power 12-Bit Sampling CMOS ANALOG-TO-DIGITAL CONVERTER

## FEATURES

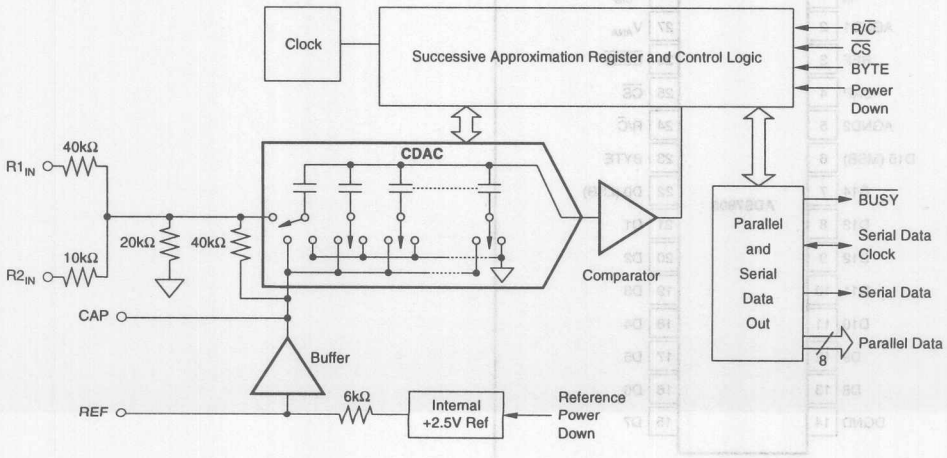
- 35mW max POWER DISSIPATION
- 50µW POWER DOWN MODE
- 25µs max ACQUISITION AND CONVERSION
- ±1/2LSB max INL AND DNL
- 72dB min SINAD WITH 1kHz INPUT
- ±10V, 0V TO +5V, AND 0V TO +4V INPUT RANGES
- SINGLE +5V SUPPLY OPERATION
- PARALLEL AND SERIAL DATA OUTPUT
- PIN-COMPATIBLE WITH 16-BIT ADS7807
- USES INTERNAL OR EXTERNAL REFERENCE
- 28-PIN 0.3" PLASTIC DIP AND SOIC

## DESCRIPTION

The ADS7806 is a low-power 12-bit sampling analog-to-digital using state-of-the-art CMOS structures. It contains a complete 12-bit, capacitor-based, SAR A/D with S/H, clock, reference, and microprocessor interface with parallel and serial output drivers.

The ADS7806 can acquire and convert to full 12-bit accuracy in 25µs max while consuming only 35mW max. Laser-trimmed scaling resistors provide standard industrial input ranges of ±10V and 0V to +5V. In addition, a 0V to +4V range allows development of complete single supply systems.

The 28-pin ADS7806 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C temperature range.




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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 40kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7806P, U MIN | ADS7806P, U TYP | ADS7806P, U MAX | ADS7806PB, UB MIN | ADS7806PB, UB TYP | ADS7806PB, UB MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **RESOLUTION** | | | | 12 | | | * | Bits |
| **ANALOG INPUT** | | | | | | | | |
| Voltage Ranges | | | | ±10, 0 to +5, 0 to +4 | | | | V |
| Impedance | | | | (See Table II) | | | | |
| Capacitance | | | 35 | | | * | | pF |
| **THROUGHPUT SPEED** | | | | | | | | |
| Conversion Time | | | | 20 | | | * | µs |
| Complete Cycle | Acquire and Convert | | | 25 | | | * | µs |
| Throughput Rate | | 40 | | | * | | | kHz |
| **DC ACCURACY** | | | | | | | | |
| Integral Linearity Error | | | ±0.15 | ±0.9 | | * | ±0.45 | LSB[1] |
| Differential Linearity Error | | | ±0.15 | ±0.9 | | * | ±0.45 | LSB |
| No Missing Codes | | | Guaranteed | | | * | | Bits |
| Transition Noise[2] | | | 0.1 | | | * | | LSB |
| Gain Error | | | ±0.2 | | | ±0.1 | | % |
| Full Scale Error[3,4] | | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | | | ±7 | | | ±5 | | ppm/°C |
| Full Scale Error[3,4] | Ext. 2.5000V Ref | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | Ext. 2.5000V Ref | | ±0.5 | | | * | | ppm/°C |
| Bipolar Zero Error[3] | ±10V Range | | | ±10 | | | * | mV |
| Bipolar Zero Error Drift | ±10V Range | | ±0.5 | | | * | | ppm/°C |
| Unipolar Zero Error[3] | 0V to 5V, 0V to 4V Ranges | | | ±3 | | | * | mV |
| Unipolar Zero Error Drift | 0V to 5V, 0V to 4V Ranges | | ±0.5 | | | * | | ppm/°C |
| Recovery Time to Rated Accuracy from Power Down[5] | 2.2µF Capacitor to CAP | | 1 | | | * | | ms |
| Power Supply Sensitivity ($V_{DIG}$ = $V_{ANA}$ = $V_S$) | +4.75V < $V_S$ < +5.25V | | | ±0.5 | | | * | LSB |
| **AC ACCURACY** | | | | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 1kHz, ±10V | 80 | 90 | | * | * | | dB[6] |
| Total Harmonic Distortion | $f_{IN}$ = 1kHz, ±10V | | –90 | –80 | | * | * | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 1kHz, ±10V | 70 | 73 | | 72 | * | | dB |
| Signal-to-Noise | $f_{IN}$ = 1kHz, ±10V | 70 | 73 | | 72 | * | | dB |
| Usable Bandwidth[7] | | | 130 | | | * | | kHz |
| Full Power Bandwidth (-3dB) | | | 600 | | | * | | kHz |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Aperture Delay | | | 40 | | | * | | ns |
| Aperture Jitter | | | 20 | | | * | | ps |
| Transient Response | FS Step | | | 5 | | | * | µs |
| Overvoltage Recovery[8] | | | 750 | | | * | | ns |
| **REFERENCE** | | | | | | | | |
| Internal Reference Voltage | No Load | 2.48 | 2.5 | 2.52 | * | * | * | V |
| Internal Reference Source Current (Must use external buffer.) | | | 1 | | | * | | µA |
| Internal Reference Drift | | | 8 | | | * | | ppm/°C |
| External Reference Voltage Range for Specified Linearity | | 2.3 | 2.5 | 2.7 | * | * | * | V |
| External Reference Current Drain | Ext. 2.5000V Ref | | | 100 | | | * | µA |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Levels | | | | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | * | | * | V |
| $V_{IH}$ | | +2.0 | | $V_D$ +0.3V | * | | * | V |
| $I_{IL}$ | $V_{IL}$ = 0V | | | ±10 | | | * | µA |
| $I_{IH}$ | $V_{IH}$ = 5V | | | ±10 | | | * | µA |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Data Format | | | Parallel 12-bits in 2-bytes; Serial | | | | | |
| Data Coding | | | Binary Two's Complement or Straight Binary | | | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +4 | | | * | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_{DIG}$ | | | ±5 | | | * | µA |
| Output Capacitance | High-Z State | | | 15 | | | * | pF |

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## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 40kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7806P, U | | | ADS7806PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **DIGITAL TIMING** | | | | | | | | |
| Bus Access Time | $R_L$ = 3.3kΩ, $C_L$ = 50pF | | | 83 | | | * | ns |
| Bus Relinquish Time | $R_L$ = 3.3kΩ, $C_L$ = 10pF | | | 83 | | | * | ns |
| **POWER SUPPLIES** | | | | | | | | |
| Specified Performance | | | | | | | | |
| $V_{DIG}$ | Must be ≤ $V_{ANA}$ | +4.75 | +5 | +5.25 | * | * | * | V |
| $V_{ANA}$ | | +4.75 | +5 | +5.25 | * | * | * | V |
| $I_{DIG}$ | | | 0.6 | | | * | | mA |
| $I_{ANA}$ | | | 5.0 | | | * | | mA |
| Power Dissipation | $V_{ANA}$ = $V_{DIG}$ = 5V, $f_S$ = 40kHz | | 28 | 35 | | * | * | mW |
| | REFD HIGH | | 23 | | | * | | mW |
| | PWRD and REFD HIGH | | 50 | | | * | | µW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | °C |
| Derated Performance | | –55 | | +125 | * | | * | °C |
| Storage | | –65 | | +150 | * | | * | °C |
| Thermal Resistance ($\theta_{JA}$) | | | | | | | | |
| Plastic DIP | | | 75 | | | * | | °C/W |
| SOIC | | | 75 | | | * | | °C/W |

* Specifications same as ADS7806P, U.

NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 4.88mV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) This is the time delay after the ADS7806 is brought out of Power Down Mode until all internal settling occurs and the analog input is acquired to rated accuracy. A Convert Command after this delay will yield accurate results. (6) All specifications in dB are referred to a full-scale input. (7) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (8) Recovers to specified performance after 2 x FS input overvoltage.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $R1_{IN}$ | ±25V |
| $R2_{IN}$ | ±25V |
| CAP | $V_{ANA}$ +0.3V to AGND2 –0.3V |
| REF | Indefinite Short to AGND2, Momentary Short to $V_{ANA}$ |
| Ground Voltage Differences: DGND, AGND1, and AGND2 | ±0.3V |
| $V_{ANA}$ | 7V |
| $V_{DIG}$ to $V_{ANA}$ | +0.3V |
| $V_{DIG}$ | 7V |
| Digital Inputs | –0.3V to $V_{DIG}$ +0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ADS7806P | Plastic DIP | 246 |
| ADS7806PB | Plastic DIP | 246 |
| ADS7806U | SOIC | 217 |
| ADS7806UB | SOIC | 217 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

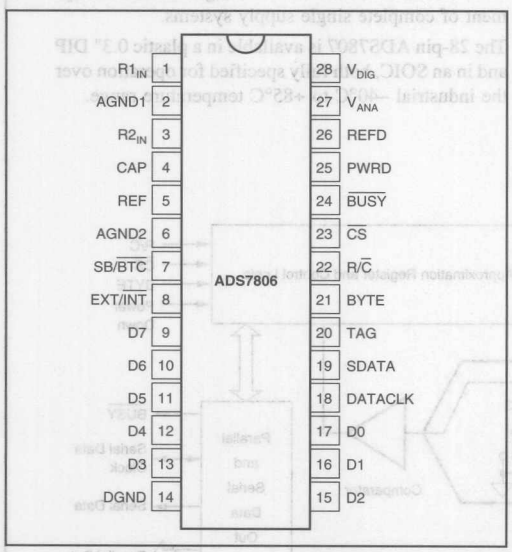
## ORDERING INFORMATION

| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) *RATIO (dB)* | SPECIFICATION TEMPERATURE *RANGE* | PACKAGE |
|---|---|---|---|---|
| ADS7806P | ±0.9 | 70 | –40°C to +85°C | Plastic DIP |
| ADS7806PB | ±0.45 | 72 | –40°C to +85°C | Plastic DIP |
| ADS7806U | ±0.9 | 70 | –40°C to +85°C | SOIC |
| ADS7806UB | ±0.45 | 72 | –40°C to +85°C | SOIC |

| PIN # | NAME | DIGITAL I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $R1_{IN}$ | | Analog Input. See Figure 7. |
| 2 | AGND1 | | Analog Sense Ground. |
| 3 | $R2_{IN}$ | | Analog Input. See Figure 7. |
| 4 | CAP | | Reference Buffer Output. 2.2µF tantalum capacitor to ground. |
| 5 | REF | | Reference Input/Output. 2.2µF tantalum capacitor to ground. |
| 6 | AGND2 | | Analog Ground. |
| 7 | SB/$\overline{BTC}$ | I | Selects Straight Binary or Binary Two's Complement for Output Data Format. |
| 8 | EXT/$\overline{INT}$ | I | External/Internal data clock select. |
| 9 | D7 | O | Data Bit 3 if BYTE is HIGH. Data bit 11 (MSB) if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. Leave unconnected when using serial output. |
| 10 | D6 | O | Data Bit 2 if BYTE is HIGH. Data bit 10 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 11 | D5 | O | Data Bit 1 if BYTE is HIGH. Data bit 9 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 12 | D4 | O | Data Bit 0 (LSB) if BYTE is HIGH. Data bit 8 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 13 | D3 | O | LOW if BYTE is HIGH. Data bit 7 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 14 | DGND | | Digital Ground. |
| 15 | D2 | O | LOW if BYTE is HIGH. Data bit 6 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 16 | D1 | O | LOW if BYTE is HIGH. Data bit 5 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 17 | D0 | O | LOW if BYTE is HIGH. Data bit 4 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 18 | DATACLK | I/O | Data Clock Output when EXT/$\overline{INT}$ is LOW. Data clock input when EXT/$\overline{INT}$ is HIGH. |
| 19 | SDATA | O | Serial Output Synchronized to DATACLK. |
| 20 | TAG | I | Serial Input When Using an External Data Clock. |
| 21 | BYTE | I | Selects 8 most significant bits (LOW) or 4 least significant bits (HIGH) on parallel output pins. |
| 22 | R/$\overline{C}$ | I | With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output. |
| 23 | $\overline{CS}$ | I | Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ is LOW, a falling edge on $\overline{CS}$ initiates a new conversion. If EXT/$\overline{INT}$ is LOW, this same falling edge will start the transmission of serial data results from the previous conversion. |
| 24 | $\overline{BUSY}$ | O | At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated. |
| 25 | PWRD | I | PWRD HIGH shuts down all analog circuitry except the reference. Digital circuitry remains active. |
| 26 | REFD | I | REFD HIGH shuts down the internal reference. External reference will be required for conversions. |
| 27 | $V_{ANA}$ | | Analog Supply. Nominally +5V. Decouple with 0.1µF ceramic and 10µF tantalum capacitors. |
| 28 | $V_{DIG}$ | | Digital Supply. Nominally +5V. Connect directly to pin 27. Must be ≤ $V_{ANA}$. |

TABLE I. Pin Assignments.

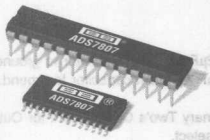
## PIN CONFIGURATION




| ANALOG INPUT RANGE | CONNECT $R1_{IN}$ VIA 200Ω TO | CONNECT $R2_{IN}$ VIA 100Ω TO | IMPEDANCE |
|---|---|---|---|
| ±10V | $V_{IN}$ | CAP | 45.7kΩ |
| 0V to 5V | AGND | $V_{IN}$ | 20.0kΩ |
| 0V to 4V | $V_{IN}$ | $V_{IN}$ | 21.4kΩ |

TABLE II. Input Range Connections.

BURR-BROWN®



# ADS7807

www.burr-brown.com/databook/ADS7807.html

# Low-Power 16-Bit Sampling CMOS ANALOG-to-DIGITAL CONVERTER

## FEATURES

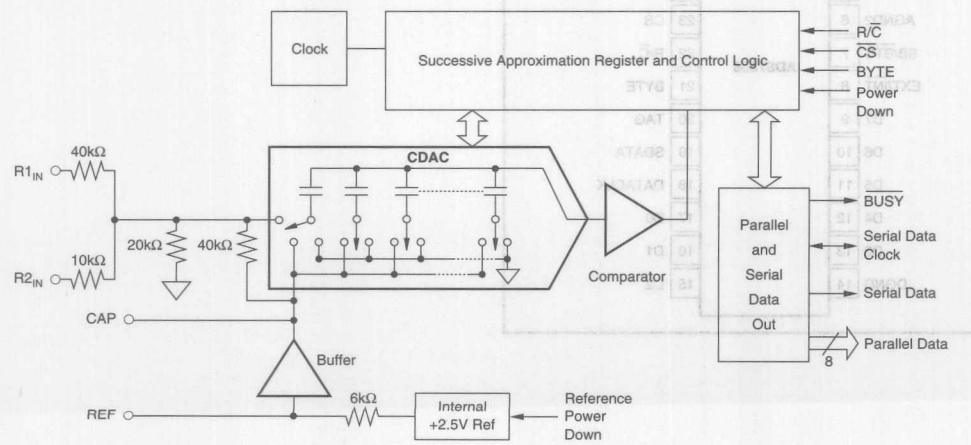
- 35mW max POWER DISSIPATION
- 50µW POWER DOWN MODE
- 25µs max ACQUISITION AND CONVERSION
- ±1.5LSB max INL
- DNL: 16 bits "No Missing Codes"
- 86dB min SINAD WITH 1kHz INPUT
- ±10V, 0V TO +5V, AND 0V TO +4V INPUT RANGES
- SINGLE +5V SUPPLY OPERATION
- PARALLEL AND SERIAL DATA OUTPUT
- PIN-COMPATIBLE WITH 12-BIT ADS7806
- USES INTERNAL OR EXTERNAL REFERENCE
- 28-PIN 0.3" PLASTIC DIP AND SOIC

## DESCRIPTION

The ADS7807 is a low-power, 16-bit, sampling A/D using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, SAR A/D with S/H, clock, reference, and microprocessor interface with parallel and serial output drivers.

The ADS7807 can acquire and convert 16-bits to within ±1.5LSB in 25µs max while consuming only 35mW max. Laser-trimmed scaling resistors provide standard industrial input ranges of ±10V and 0V to +5V. In addition, a 0V to +4V range allows development of complete single supply systems.

The 28-pin ADS7807 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C temperature range.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 40kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7807P, U MIN | ADS7807P, U TYP | ADS7807P, U MAX | ADS7807PB, UB MIN | ADS7807PB, UB TYP | ADS7807PB, UB MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **RESOLUTION** | | | | 16 | | | * | Bits |
| **ANALOG INPUT** | | | | | | | | |
| Voltage Ranges | | | | ±10, 0 to +5, 0 to +4 (See Table II) | | | | V |
| Impedance | | | | | | | | |
| Capacitance | | | 35 | | | * | | pF |
| **THROUGHPUT SPEED** | | | | | | | | |
| Conversion Time | | | | 20 | | | * | µs |
| Complete Cycle | Acquire and Convert | | | 25 | | | * | µs |
| Throughput Rate | | 40 | | | * | | | kHz |
| **DC ACCURACY** | | | | | | | | |
| Integral Linearity Error | | | | ±3 | | | ±1.5 | LSB[1] |
| Differential Linearity Error | | | | +3, –2 | | | +1.5, –1 | LSB |
| No Missing Codes | | 15 | | | 16 | | | Bits |
| Transition Noise[2] | | | 0.8 | | | * | | LSB |
| Gain Error | | | ±0.2 | | | ±0.1 | | % |
| Full Scale Error[3,4] | | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | | | ±7 | | | ±5 | | ppm/°C |
| Full Scale Error[3,4] | Ext. 2.5000V Ref | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | Ext. 2.5000V Ref | | ±0.5 | | | * | | ppm/°C |
| Bipolar Zero Error[3] | ±10V Range | | | ±10 | | | * | mV |
| Bipolar Zero Error Drift | ±10V Range | | ±0.5 | | | * | | ppm/°C |
| Unipolar Zero Error[3] | 0V to 5V, 0V to 4V Ranges | | | ±3 | | | * | mV |
| Unipolar Zero Error Drift | 0V to 5V, 0V to 4V Ranges | | ±0.5 | | | * | | ppm/°C |
| Recovery Time to Rated Accuracy from Power Down[5] | 2.2µF Capacitor to CAP | | 1 | | | * | | ms |
| Power Supply Sensitivity ($V_{DIG}$ = $V_{ANA}$ = $V_S$) | +4.75V < $V_S$ < +5.25V | | | ±8 | | | * | LSB |
| **AC ACCURACY** | | | | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 1kHz, ±10V | 90 | 100 | | 96 | * | | dB[6] |
| Total Harmonic Distortion | $f_{IN}$ = 1kHz, ±10V | | –100 | –90 | | * | –96 | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 1kHz, ±10V | 83 | 88 | | 86 | * | | dB |
| | –60dB Input | | 30 | | | 32 | | dB |
| Signal-to-Noise | $f_{IN}$ = 1kHz, ±10V | 83 | 88 | | 86 | * | | dB |
| Usable Bandwidth[7] | | | 130 | | | * | | kHz |
| Full Power Bandwidth (–3dB) | | | 600 | | | * | | kHz |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Aperture Delay | | | 40 | | | * | | ns |
| Aperture Jitter | | | 20 | | | * | | ps |
| Transient Response | FS Step | | | 5 | | | * | µs |
| Overvoltage Recovery[8] | | | 750 | | | * | | ns |
| **REFERENCE** | | | | | | | | |
| Internal Reference Voltage | No Load | 2.48 | 2.5 | 2.52 | * | * | * | V |
| Internal Reference Source Current (Must use external buffer.) | | | 1 | | | * | | µA |
| Internal Reference Drift | | | 8 | | | * | | ppm/°C |
| External Reference Voltage Range for Specified Linearity | | 2.3 | 2.5 | 2.7 | * | * | * | V |
| External Reference Current Drain | Ext. 2.5000V Ref | | | 100 | | | * | µA |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Levels | | | | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | * | | * | V |
| $V_{IH}$ | | +2.0 | | $V_D$ +0.3V | * | | * | V |
| $I_{IL}$ | $V_{IL}$ = 0V | | | ±10 | | | * | µA |
| $I_{IH}$ | $V_{IH}$ = 5V | | | ±10 | | | * | µA |
| **DIGITAL OUTPUTS** | | Parallel 16 bits in 2-bytes; Serial | | | | | | |
| Data Format | | Binary Two's Complement or Straight Binary | | | | | | |
| Data Coding | | | | | | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +4 | | | * | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_{DIG}$ | | | ±5 | | | * | µA |
| Output Capacitance | High-Z State | | | 15 | | | * | pF |

# SPECIFICATIONS (CONT)

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 40kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7807P, U MIN | ADS7807P, U TYP | ADS7807P, U MAX | ADS7807PB, UB MIN | ADS7807PB, UB TYP | ADS7807PB, UB MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **DIGITAL TIMING** | | | | | | | | |
| Bus Access Time | $R_L$ = 3.3kΩ, $C_L$ = 50pF | | | 83 | | | * | ns |
| Bus Relinquish Time | $R_L$ = 3.3kΩ, $C_L$ = 10pF | | | 83 | | | * | ns |
| **POWER SUPPLIES** | | | | | | | | |
| Specified Performance | | | | | | | | |
| $V_{DIG}$ | Must be ≤ $V_{ANA}$ | +4.75 | +5 | +5.25 | * | * | * | V |
| $V_{ANA}$ | | +4.75 | +5 | +5.25 | * | * | * | V |
| $I_{DIG}$ | | | 0.6 | | | * | | mA |
| $I_{ANA}$ | | | 5.0 | | | * | | mA |
| Power Dissipation | $V_{ANA}$ = $V_{DIG}$ = 5V, $f_S$ = 40kHz | | 28 | 35 | | * | * | mW |
| | REFD HIGH | | 23 | | | * | | mW |
| | PWRD and REFD HIGH | | 50 | | | * | | µW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | °C |
| Derated Performance | | –55 | | +125 | * | | * | °C |
| Storage | | –65 | | +150 | * | | * | °C |
| Thermal Resistance ($\theta_{JA}$) | | | | | | | | |
| Plastic DIP | | | 75 | | | * | | °C/W |
| SOIC | | | 75 | | | * | | °C/W |

* Specifications same as ADS7807P, U.

NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 305µV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) This is the time delay after the ADS7807 is brought out of Power Down Mode until all internal settling occurs and the analog input is acquired to rated accuracy. A Convert Command after this delay will yield accurate results. (6) All specifications in dB are referred to a full-scale input. (7) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (8) Recovers to specified performance after 2 x FS input overvoltage.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $R1_{IN}$ | ±25V |
| $R2_{IN}$ | ±25V |
| CAP | $V_{ANA}$ +0.3V to AGND2 –0.3V |
| REF | Indefinite Short to AGND2, Momentary Short to $V_{ANA}$ |
| Ground Voltage Differences: DGND, AGND1, and AGND2 | ±0.3V |
| $V_{ANA}$ | 7V |
| $V_{DIG}$ to $V_{ANA}$ | +0.3V |
| $V_{DIG}$ | 7V |
| Digital Inputs | –0.3V to $V_{DIG}$ +0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ADS7807P | Plastic DIP | 246 |
| ADS7807PB | Plastic DIP | 246 |
| ADS7807U | SOIC | 217 |
| ADS7807UB | SOIC | 217 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

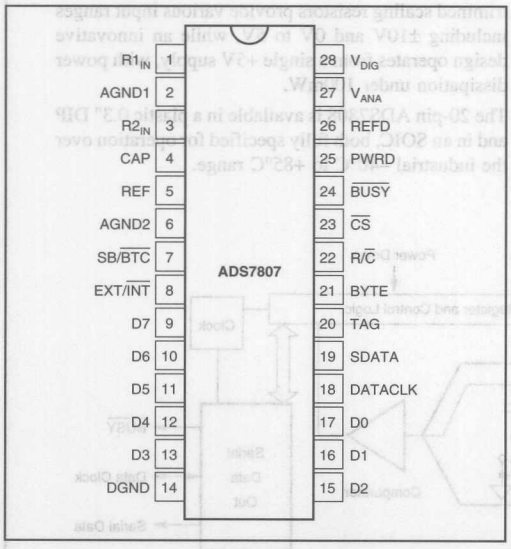
## ORDERING INFORMATION

| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | GUARANTEED NO MISSING CODE LEVEL (LSB) | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE |
|---|---|---|---|---|---|
| ADS7807P | ±3 | 15 | 83 | –40°C to +85°C | Plastic DIP |
| ADS7807PB | ±1.5 | 16 | 86 | –40°C to +85°C | Plastic DIP |
| ADS7807U | ±3 | 15 | 83 | –40°C to +85°C | SOIC |
| ADS7807UB | ±1.5 | 16 | 86 | –40°C to +85°C | SOIC |

| PIN # | NAME | DIGITAL I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $R1_{IN}$ | | Analog Input. See Figure 7. |
| 2 | AGND1 | | Analog Sense Ground. |
| 3 | $R2_{IN}$ | | Analog Input. See Figure 7. |
| 4 | CAP | | Reference Buffer Output. 2.2µF tantalum capacitor to ground. |
| 5 | REF | | Reference Input/Output. 2.2µF tantalum capacitor to ground. |
| 6 | AGND2 | | Analog Ground. |
| 7 | SB/$\overline{BTC}$ | I | Selects Straight Binary or Binary Two's Complement for Output Data Format. |
| 8 | EXT/$\overline{INT}$ | I | External/Internal data clock select. |
| 9 | D7 | O | Data Bit 7 if BYTE is HIGH. Data bit 15 (MSB) if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. Leave unconnected when using serial output. |
| 10 | D6 | O | Data Bit 6 if BYTE is HIGH. Data bit 14 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 11 | D5 | O | Data Bit 5 if BYTE is HIGH. Data bit 13 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 12 | D4 | O | Data Bit 4 if BYTE is HIGH. Data bit 12 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 13 | D3 | O | Data Bit 3 if BYTE is HIGH. Data bit 11 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 14 | DGND | | Digital Ground. |
| 15 | D2 | O | Data Bit 2 if BYTE is HIGH. Data bit 10 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 16 | D1 | O | Data Bit 1 if BYTE is HIGH. Data bit 9 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 17 | D0 | O | Data Bit 0 (LSB) if BYTE is HIGH. Data bit 8 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 18 | DATACLK | I/O | Data Clock Output when EXT/$\overline{INT}$ is LOW. Data clock input when EXT/$\overline{INT}$ is HIGH. |
| 19 | SDATA | O | Serial Output Synchronized to DATACLK. |
| 20 | TAG | I | Serial Input When Using an External Data Clock. |
| 21 | BYTE | I | Selects 8 most significant bits (LOW) or 8 least significant bits (HIGH) on parallel output pins. |
| 22 | R/$\overline{C}$ | I | With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output. |
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| 24 | $\overline{BUSY}$ | O | At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated. |
| 25 | PWRD | I | PWRD HIGH shuts down all analog circuitry except the reference. Digital circuitry remains active. |
| 26 | REFD | I | REFD HIGH shuts down the internal reference. External reference will be required for conversions. |
| 27 | $V_{ANA}$ | | Analog Supply. Nominally +5V. Decouple with 0.1µF ceramic and 10µF tantalum capacitors. |
| 28 | $V_{DIG}$ | | Digital Supply. Nominally +5V. Connect directly to pin 27. Must be ≤ $V_{ANA}$. |

TABLE I. Pin Assignments.

## PIN CONFIGURATION



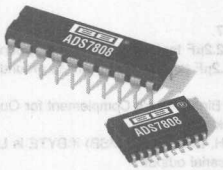

| ANALOG INPUT RANGE | CONNECT $R1_{IN}$ VIA 200Ω TO | CONNECT $R2_{IN}$ VIA 100Ω TO | IMPEDANCE |
|---|---|---|---|
| ±10V | $V_{IN}$ | CAP | 45.7kΩ |
| 0V to 5V | AGND | $V_{IN}$ | 20.0kΩ |
| 0V to 4V | $V_{IN}$ | $V_{IN}$ | 21.4kΩ |

TABLE II. Input Range Connections.



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# ADS7808

www.burr-brown.com/databook/ADS7808.html

# 12-Bit 10μs Serial CMOS Sampling ANALOG-to-DIGITAL CONVERTER

## FEATURES

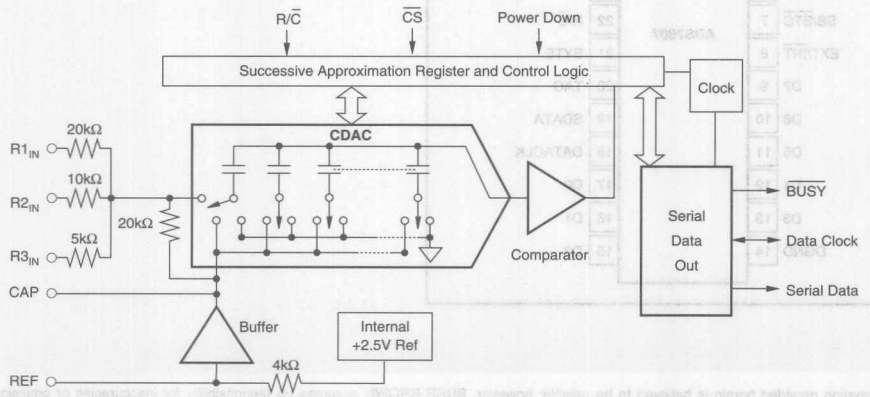
- 100kHz SAMPLING RATE
- 72dB SINAD WITH 45kHz INPUT
- ±1/2 LSB INL AND DNL
- SIX SPECIFIED INPUT RANGES
- SERIAL OUTPUT
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 16-BIT ADS7809
- USES INTERNAL OR EXTERNAL REFERENCE
- 100mW MAX POWER DISSIPATION
- 20-PIN 0.3" PLASTIC DIP AND SOIC
- SIMPLE DSP INTERFACE

## DESCRIPTION

The ADS7808 is a complete 12-bit sampling analog-to-digital using state-of-the-art CMOS structures. It contains a 12-bit capacitor-based SAR A/D with S/H, reference, clock, and a serial data interface. Data can be output using the internal clock, or can be synchronized to an external data clock. The ADS7808 also provides an output synchronization pulse for ease of use with standard DSP processors.

The ADS7808 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide various input ranges including ±10V and 0V to 5V, while an innovative design operates from a single +5V supply, with power dissipation under 100mW.

The 20-pin ADS7808 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 100kHz, $V_{DIG} = V_{ANA}$ = +5V, using internal reference and fixed resistors as shown in Figure 4, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7808P, U | | | ADS7808PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | | 12 | | | * | Bits |
| **ANALOG INPUT** | | | | | | | | |
| Voltage Ranges | | | | ±10V, 0V to 5V, etc. (See Table I) | | | | |
| Impedance | | | | See Table I | | | | |
| Capacitance | | | 35 | | | * | | pF |
| **THROUGHPUT SPEED** | | | | | | | | |
| Conversion Time | | | 5.7 | 8 | | * | * | µs |
| Complete Cycle | Acquire and Convert | | | 10 | | | * | µs |
| Throughput Rate | | 100 | | | * | | | kHz |
| **DC ACCURACY** | | | | | | | | |
| Integral Linearity Error | | | | ±0.9 | | | ±0.45 | LSB[1] |
| Differential Linearity Error | | | | ±0.9 | | | ±0.45 | LSB |
| No Missing Codes | | | Guaranteed | | | * | | |
| Transition Noise[2] | | | 0.1 | | | * | | LSB |
| Full Scale Error[3,4] | | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | | | ±7 | | | ±5 | | ppm/°C |
| Full Scale Error[3,4] | Ext. 2.5000V Ref | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | Ext. 2.5000V Ref | | ±2 | | | * | | ppm/°C |
| Bipolar Zero Error[3] | Bipolar Ranges | | | ±10 | | | * | mV |
| Bipolar Zero Error Drift | Bipolar Ranges | | ±2 | | | ±2 | | ppm/°C |
| Unipolar Zero Error[3] | 0V to 10V Range | | | ±5 | | | * | mV |
| | 0V to 4V Range | | | ±3 | | | * | mV |
| | 0V to 5V Range | | | ±3 | | | * | mV |
| Unipolar Zero Error Drift | Unipolar Ranges | | ±2 | | | * | | ppm/°C |
| Recovery to Rated Accuracy after Power Down | 1µF Capacitor to CAP | | 1 | | | * | | ms |
| Power Supply Sensitivity ($V_{DIG} = V_{ANA} = V_D$) | +4.75V < $V_D$ < +5.25V | | | ±0.5 | | | * | LSB |
| **AC ACCURACY** | | | | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 45kHz | 80 | 90 | | * | * | | dB[5] |
| Total Harmonic Distortion | $f_{IN}$ = 45kHz | | –90 | –80 | | * | * | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 45kHz | 70 | 73 | | 72 | * | | dB |
| Signal-to-Noise | $f_{IN}$ = 45kHz | 70 | 73 | | 72 | * | | dB |
| Full-Power Bandwidth[6] | | | 250 | | | * | | kHz |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Aperture Delay | | | 40 | | | * | | ns |
| Aperture Jitter | | | Sufficient to meet AC specs | | | * | | ns |
| Transient Response | FS Step | | | 2 | | | * | µs |
| Overvoltage Recovery[7] | | | 150 | | | * | | ns |
| **REFERENCE** | | | | | | | | |
| Internal Reference Voltage | No Load | 2.48 | 2.5 | 2.52 | * | * | * | V |
| Internal Reference Source Current (Must use external buffer) | | | 1 | | | * | | µA |
| External Reference Voltage Range for Specified Linearity | | 2.3 | 2.5 | 2.7 | * | * | * | V |
| External Reference Current Drain | Ext. 2.5000V Ref | | | 100 | | | * | µA |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Levels | | | | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | * | | * | V |
| $V_{IH}$ | | +2.0 | | $V_D$ +0.3V | * | | * | V |
| $I_{IL}$ | $V_{IL}$ = 0V | | | ±10 | | | * | µA |
| $I_{IH}$ | $V_{IH}$ = 5V | | | ±10 | | | * | µA |

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# SPECIFICATIONS (CONT)

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 100kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference and fixed resistors shown in Figure 4, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7808P, U MIN | ADS7808P, U TYP | ADS7808P, U MAX | ADS7808PB, UB MIN | ADS7808PB, UB TYP | ADS7808PB, UB MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **DIGITAL OUTPUTS** | | | | | | | | |
| Data Format | | | Serial 12 bits | | | | | |
| Data Coding | | | Binary Two's Complement or Straight Binary | | | | | |
| Pipeline Delay | | | Conversion results only available after completed conversion. | | | | | |
| Data Clock | | | Selectable for internal or external data clock | | | | | |
| Internal | EXT/$\overline{INT}$ LOW | | 2.3 | | | * | | MHz |
| (Output Only When Transmitting Data) | | | | | | | | |
| External (Can Run Continually) | EXT/$\overline{INT}$ HIGH | 0.1 | | 10 | * | | * | MHz |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +4 | | | * | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_{DIG}$ | | | ±5 | | | * | µA |
| Output Capacitance | High-Z State | | | 15 | | | 15 | pF |
| **POWER SUPPLIES** | | | | | | | | |
| Specified Performance | | | | | | | | |
| $V_{DIG}$ | Must be ≤ $V_{ANA}$ | +4.75 | +5 | +5.25 | * | * | * | V |
| $V_{ANA}$ | +4.75 | +5 | +5.25 | * | * | * | V | |
| $I_{DIG}$ | | 0.3 | | | * | | mA | |
| $I_{ANA}$ | | 16 | | | * | | mA | |
| Power Dissipation: PWRD LOW | $V_{DIG}$ = $V_{ANA}$ = 5V, $f_S$ = 100kHz | | | 100 | | | * | mW |
| PWRD HIGH | | | 50 | | | * | | µW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | °C |
| Derated Performance | | –55 | | +125 | * | | * | °C |
| Storage | | –65 | | +150 | * | | * | °C |
| Thermal Resistance ($\theta_{JA}$) | | | | | | | | |
| Plastic DIP | | | 75 | | | * | | °C/W |
| SOIC | | | 75 | | | * | | °CW |

* Specifications same as ADS7808P, U.

NOTES: (1) LSB means Least Significant Bit. For the ±10V input range, one LSB is 4.88mV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors in Figure 4. Adjustable to zero with external potentiometer. (4) For bipolar input ranges, full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to (Noise + Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $R1_{IN}$ | ±25V |
| $R2_{IN}$ | ±25V |
| $R3_{IN}$ | ±25V |
| CAP | $V_{ANA}$+0.3V to AGND2 –0.3V |
| REF | Indefinite Short to AGND2, Momentary Short to $V_{ANA}$ |
| Ground Voltage Differences: DGND, AGND2 | ±0.3V |
| $V_{ANA}$ | 7V |
| $V_{DIG}$ to $V_{ANA}$ | +0.3 |
| $V_{DIG}$ | 7V |
| Digital Inputs | –0.3V to $V_{DIG}$ +0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 700mW |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

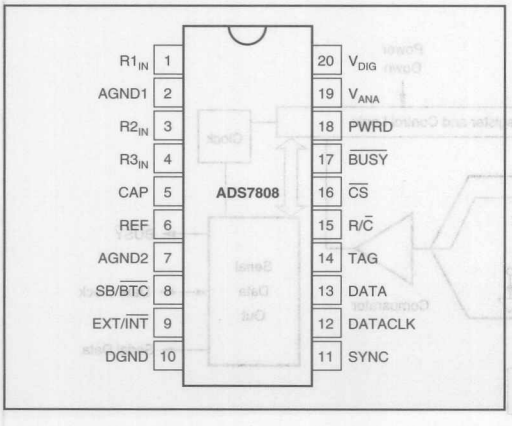
| PRODUCT | MAXIMUM LINEARITY ERROR (LSB) | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO(dB) | SPECIFICATION TEMPERATURE RANGE (°C) | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|---|---|---|
| ADS7808P | ±0.9 | 70 | –40°C to +85°C | 20-Pin Plastic DIP | 222 |
| ADS7808PB | ±0.45 | 72 | –40°C to +85°C | 20-Pin Plastic DIP | 222 |
| ADS7808U | ±0.9 | 70 | –40°C to +85°C | 20-Pin SOIC | 221 |
| ADS7808UB | ±0.45 | 72 | –40°C to +85°C | 20-Pin SOIC | 221 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN ASSIGNMENTS

| PIN # | NAME | DESCRIPTION |
|---|---|---|
| 1 | $R1_{IN}$ | Analog Input. See Table I and Figure 4 for input range connections. |
| 2 | AGND1 | Analog Ground. Used internally as ground reference point. Minimal current flow. |
| 3 | $R2_{IN}$ | Analog Input. See Table I and Figure 4 for input range connections. |
| 4 | $R3_{IN}$ | Analog Input. See Table I and Figure 4 for input range connections. |
| 5 | CAP | Reference Buffer Capacitor. 2.2µF Tantalum to ground. |
| 6 | REF | Reference Input/Output. Outputs internal 2.5V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2µF Tantalum capacitor. |
| 7 | AGND2 | Analog Ground. |
| 8 | SB/$\overline{BTC}$ | Select Straight Binary or Binary Two's Complement data output format. If HIGH, data will be output in a Straight Binary format. If LOW, data will be output in a Binary Two's complement format. |
| 9 | EXT/$\overline{INT}$ | Select External or Internal Clock for transmitting data. If HIGH, data will be output synchronized to the clock input on DATACLK. If LOW, a convert command will initiate the transmission of the data from the previous conversion, along with 12 clock pulses output on DATACLK. |
| 10 | DGND | Digital Ground. |
| 11 | SYNC | Synch Output. If EXT/$\overline{INT}$ is HIGH, either a rising edge on R/$\overline{C}$ with $\overline{CS}$ LOW or a falling edge on $\overline{CS}$ with R/$\overline{C}$ HIGH will output a pulse on SYNC synchronized to the external DATACLK. |
| 12 | DATACLK | Either an input or an output depending on the EXT/$\overline{INT}$ level. Output data will be synchronized to this clock. If EXT/$\overline{INT}$ is LOW, DATACLK will transmit 12 pulses after each conversion, and then remain LOW between conversions. |
| 13 | DATA | Serial Data Output. Data will be synchronized to DATACLK, with the format determined by the level of SB/$\overline{BTC}$. In the external clock mode, after 12-bits of data, the ADS7808 will output the level input on TAG as long as $\overline{CS}$ is LOW and R/$\overline{C}$ is HIGH (see Figure 3.) If EXT/$\overline{INT}$ is LOW, data will be valid on both the rising and falling edges of DATACLK, and between conversions DATA will stay at the level of the TAG input when the conversion was started. |
| 14 | TAG | Tag Input for use in external clock mode. If EXT/$\overline{INT}$ is HIGH, digital data input on TAG will be output on DATA with a delay of 12 DATACLK pulses as long as $\overline{CS}$ is LOW and R/$\overline{C}$ is HIGH. See Figure 3. |
| 15 | R/$\overline{C}$ | Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. When EXT/$\overline{INT}$ is LOW, this also initiates the transmission of the data results from the previous conversion. If EXT/$\overline{INT}$ is HIGH, a rising edge on R/$\overline{C}$ with $\overline{CS}$ LOW, or a falling edge on $\overline{CS}$ with R/$\overline{C}$ HIGH, transmits a pulse on SYNC and initiates the transmission of data from the previous conversion. |
| 16 | $\overline{CS}$ | Chip Select. Internally OR'ed with R/$\overline{C}$. |
| 17 | $\overline{BUSY}$ | Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output shift register. $\overline{CS}$ or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ rises, or another conversion will start without time for signal acquisition. |
| 18 | PWRD | Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register. |
| 19 | $V_{ANA}$ | Analog Supply Input. Nominally +5V. Connect directly to pin 20, and decouple to ground with 0.1µF ceramic and 10µF Tantalum capacitors. |
| 20 | $V_{DIG}$ | Digital Supply Input. Nominally +5V. Connect directly to pin 19. Must be ≤ $V_{ANA}$. |

## PIN CONFIGURATION

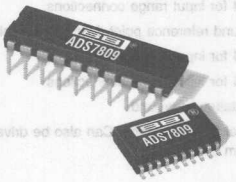



| ANALOG INPUT RANGE | CONNECT $R1_{IN}$ VIA 200Ω TO | CONNECT $R2_{IN}$ VIA 100Ω TO | CONNECT $R3_{IN}$ TO | IMPEDANCE |
|---|---|---|---|---|
| ±10V | $V_{IN}$ | AGND | CAP | 22.9kΩ |
| ±5V | AGND | $V_{IN}$ | CAP | 13.3kΩ |
| ±3.33 | $V_{IN}$ | $V_{IN}$ | CAP | 10.7kΩ |
| 0V to 10V | AGND | $V_{IN}$ | AGND | 13.3kΩ |
| 0V to 5V | AGND | AGND | $V_{IN}$ | 10.0kΩ |
| 0V to 4V | $V_{IN}$ | AGND | $V_{IN}$ | 10.7kΩ |

TABLE I. Input Range Connections.

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# ADS7809




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# 16-Bit 10µs Serial CMOS Sampling ANALOG-to-DIGITAL CONVERTER

## FEATURES

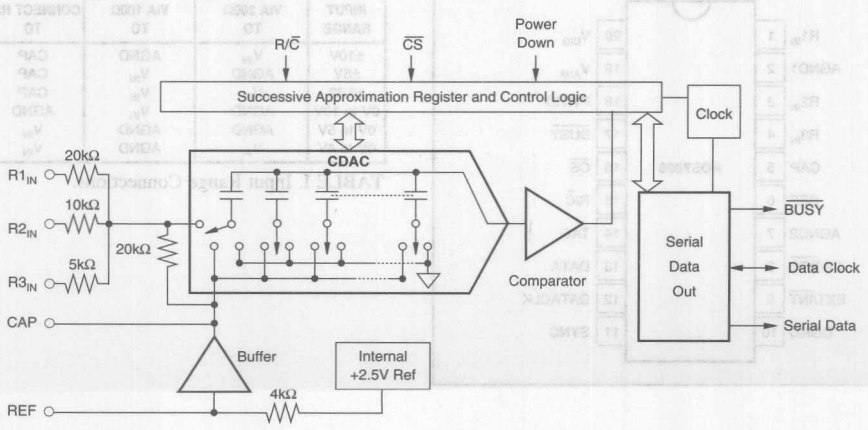
- 100kHz SAMPLING RATE
- 86dB SINAD WITH 20kHz INPUT
- ±2 LSB INL
- DNL: 16 BITS "No Missing Codes"
- SIX SPECIFIED INPUT RANGES
- SERIAL OUTPUT
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 12-BIT ADS7808
- USES INTERNAL OR EXTERNAL REFERENCE
- 100mW MAX POWER DISSIPATION
- 20-PIN 0.3" PLASTIC DIP AND SOIC
- SIMPLE DSP INTERFACE

## DESCRIPTION

The ADS7809 is a complete 16-bit sampling analog-to-digital using state-of-the-art CMOS structures. It contains a 16-bit capacitor-based SAR A/D with S/H, reference, clock, and a serial data interface. Data can be output using the internal clock, or can be synchronized to an external data clock. The ADS7809 also provides an output synchronization pulse for ease of use with standard DSP processors.

The ADS7809 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide various input ranges including ±10V and 0V to 5V, while an innovative design operates from a single +5V supply, with power dissipation under 100mW.

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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 100kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference and fixed resistors as shown in Figure 4, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7809P, U | | | ADS7809PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | | 16 | | | * | Bits |
| **ANALOG INPUT** | | | | | | | | |
| Voltage Ranges | | | ±10, 0V to 5V, etc. (See Table I) | | | | | |
| Impedance | | | See Table I | | | | | |
| Capacitance | | | 35 | | | * | | pF |
| **THROUGHPUT SPEED** | | | | | | | | |
| Complete Cycle | Acquire and Convert | | | 10 | | | * | µs |
| Throughput Rate | | 100 | | | * | | | kHz |
| **DC ACCURACY** | | | | | | | | |
| Integral Linearity Error | | | | ±3 | | | ±2 | LSB[1] |
| Differential Linearity Error | | | | +3, –2 | | | ±1 | LSB |
| No Missing Codes | | 15 | | | 16 | | | Bits |
| Transition Noise[2] | | | 1.3 | | | * | | LSB |
| Full Scale Error[3,4] | | | | ±0.5 | | | * | % |
| Full Scale Error Drift | | | ±7 | | | * | | ppm/°C |
| Full Scale Error[3,4] | Ext. 2.5000V Ref | | | ±0.5 | | | * | % |
| Full Scale Error Drift | Ext. 2.5000V Ref | | ±2 | | | * | | ppm/°C |
| Bipolar Zero Error[3] | Bipolar Ranges | | | ±10 | | | * | mV |
| Bipolar Zero Error Drift | Bipolar Ranges | | ±2 | | | * | | ppm/°C |
| Unipolar Zero Error[3] | 0V tp 10V Ranges | | | ±5 | | | * | mV |
| Unipolar Zero Error[3] | 0V to 4V, 0V to 5V Ranges | | | ±3 | | | * | mV |
| Unipolar Zero Error Drift | Unipolar Ranges | | ±2 | | | * | | ppm/°C |
| Recovery to Rated Accuracy after Power Down | 1µF Capacitor to CAP | | 1 | | | * | | ms |
| Power Supply Sensitivity ($V_{DIG}$ = $V_{ANA}$ = $V_D$) | +4.75V < $V_D$ < +5.25V | | | ±8 | | | * | LSB |
| **AC ACCURACY** | | | | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 20kHz | 90 | 100 | | 96 | * | | dB[5] |
| Total Harmonic Distortion | $f_{IN}$ = 20kHz | | –100 | –90 | | * | –94 | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 20kHz | 83 | 88 | | 86 | * | | dB |
| | –60dB Input | | 30 | | | 32 | | dB |
| Signal-to-Noise | $f_{IN}$ = 20kHz | 83 | 88 | | 86 | * | | dB |
| Full-Power Bandwidth[6] | | | 250 | | | * | | kHz |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Aperture Delay | | | 40 | | | * | | ns |
| Transient Response | FS Step | | | 2 | | | * | µs |
| Overvoltage Recovery[7] | | | 150 | | | * | | ns |
| **REFERENCE** | | | | | | | | |
| Internal Reference Voltage | No Load | 2.48 | 2.5 | 2.52 | * | * | * | V |
| Internal Reference Source Current (Must use external buffer) | | | 1 | | | * | | µA |
| External Reference Voltage Range For Specified Linearity | | 2.3 | 2.5 | 2.7 | * | * | * | V |
| External Reference Current Drain | Ext. 2.5000V Ref | | | 100 | | | * | µA |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Levels | | | | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | * | | * | V |
| $V_{IH}$ | | +2.0 | | $V_D$ +0.3V | * | | * | V |
| $I_{IL}$ | $V_{IL}$ = 0V | | | ±10 | | | * | µA |
| $I_{IH}$ | $V_{IH}$ = 5V | | | ±10 | | | * | µA |

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## SPECIFICATIONS (CONT)

### ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 100kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference and fixed resistors as shown in Figure 4, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7809P, U MIN | ADS7809P, U TYP | ADS7809P, U MAX | ADS7809PB, UB MIN | ADS7809PB, UB TYP | ADS7809PB, UB MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **DIGITAL OUTPUTS** | | | | | | | | |
| Data Format | | | Serial 16 bits | | | | | |
| Data Co | | | Binary Two's Complement or Straight Binary | | | | | |
| Pipeline Delay | | | Conversion results only available after completed conversion. | | | | | |
| Data Clock | | | Selectable for internal or external data clock | | | | | |
| Internal | EXT/$\overline{INT}$ LOW | | 2.3 | | | * | | MHz |
| (Output Only When Transmitting Data) | | | | | | | | |
| External | EXT/$\overline{INT}$ HIGH | 0.1 | | 10 | * | | * | MHz |
| (Can Run Continually) | | | | | | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +4 | | | * | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_{DIG}$ | | | ±5 | | | * | µA |
| Output Capacitance | High-Z State | | | 15 | | | * | pF |
| **POWER SUPPLIES** | | | | | | | | |
| Specified Performance | | | | | | | | |
| $V_{DIG}$ | Must be ≤ $V_{ANA}$ | +4.75 | +5 | +5.25 | * | * | * | V |
| $V_{ANA}$ | | +4.75 | +5 | +5.25 | * | * | * | V |
| $I_{DIG}$ | | | 0.3 | | | * | | mA |
| $I_{ANA}$ | | | 16 | | | * | | mA |
| Power Dissipation: PWRD LOW | $V_{ANA}$ = $V_{DIG}$ = 5V, $f_S$ = 100kHz | | | 100 | | | * | mW |
| PWRD HIGH | | | 50 | | | * | | µW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | °C |
| Derated Performance | | –55 | | +125 | * | | * | °C |
| Storage | | –65 | | +150 | * | | * | °C |
| Thermal Resistance ($\theta_{JA}$) | | | | | | | | |
| Plastic DIP | | | 75 | | | * | | °C/W |
| SOIC | | | 75 | | | * | | °C/W |

*Same as specification for ADS7809P, U.

NOTES: (1) LSB means Least Significant Bit. For the ±10V input range, one LSB is 305µV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer. (4) For bipolar input ranges, full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $R1_{IN}$ | ±25V |
| $R2_{IN}$ | ±25V |
| $R3_{IN}$ | ±25V |
| CAP | $V_{ANA}$+0.3V to AGND2 –0.3V |
| REF | Indefinite Short to AGND2, Momentary Short to $V_{ANA}$ |
| Ground Voltage Differences: DGND, AGND2 | ±0.3V |
| $V_{ANA}$ | 7V |
| $V_{DIG}$ to $V_{ANA}$ | +0.3 |
| $V_{DIG}$ | 7V |
| Digital Inputs | –0.3V to $V_{DIG}$ +0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 700mW |
| Lead Temperature (soldering, 10s) | +300°C |

### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGE/ORDERING INFORMATION

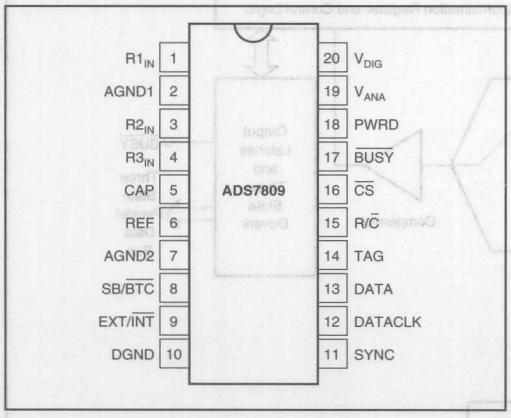
| PRODUCT | MAXIMUM LINEARITY ERROR (LSB) | GUARANTEED NO MISSING CODE LEVEL (LSB) | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB) | SPECIFICATION TEMPERATURE RANGE (°C) | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|---|---|---|---|
| ADS7809P | ±3 | 15 | 83 | –40 to +85 | 20-Pin Plastic DIP | 222 |
| ADS7809PB | ±2 | 16 | 86 | –40 to +85 | 20-Pin Plastic DIP | 222 |
| ADS7809U | ±3 | 15 | 83 | –40 to +85 | 20-Lead SOIC | 221 |
| ADS7809UB | ±2 | 16 | 86 | –40 to +85 | 20-Lead SOIC | 221 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN ASSIGNMENTS

| PIN # | NAME | DESCRIPTION |
|---|---|---|
| 1 | $R1_{IN}$ | Analog Input. See Table I and Figure 4 for input range connections. |
| 2 | AGND1 | Analog Ground. Used internally as ground reference point. Minimal current flow. |
| 3 | $R2_{IN}$ | Analog Input. See Table I and Figure 4 for input range connections. |
| 4 | $R3_{IN}$ | Analog Input. See Table I and Figure 4 for input range connections. |
| 5 | CAP | Reference Buffer Capacitor. 2.2µF Tantalum to ground. |
| 6 | REF | Reference Input/Output. Outputs internal 2.5V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2µF Tantalum capacitor. |
| 7 | AGND2 | Analog Ground. |
| 8 | SB/$\overline{BTC}$ | Select Straight Binary or Binary Two's Complement data output format. If HIGH, data will be output in a Straight Binary format. If LOW, data will be output in a Binary Two's Complement format. |
| 9 | EXT/$\overline{INT}$ | Select External or Internal Clock for transmitting data. If HIGH, data will be output synchronized to the clock input on DATACLK. If LOW, a convert command will initiate the transmission of the data from the previous conversion, along with 16 clock pulses output on DATACLK. |
| 10 | DGND | Digital Ground. |
| 11 | SYNC | Synch Output. If EXT/$\overline{INT}$ is HIGH, either a rising edge on R/$\overline{C}$ with $\overline{CS}$ LOW or a falling edge on $\overline{CS}$ with R/$\overline{C}$ HIGH will output a pulse on SYNC synchronized to the external DATACLK. |
| 12 | DATACLK | Either an input or an output depending on the EXT/$\overline{INT}$ level. Output data will be synchronized to this clock. If EXT/$\overline{INT}$ is LOW, DATACLK will transmit 16 pulses after each conversion, and then remain LOW between conversions. |
| 13 | DATA | Serial Data Output. Data will be synchronized to DATACLK, with the format determined by the level of SB/$\overline{BTC}$. In the external clock mode, after 16 bits of data, the ADS7809 will output the level input on TAG as long as $\overline{CS}$ is LOW and R/$\overline{C}$ is HIGH (see Figure 3.) If EXT/$\overline{INT}$ is LOW, data will be valid on both the rising and falling edges of DATACLK, and between conversions DATA will stay at the level of the TAG input when the conversion was started. |
| 14 | TAG | Tag Input for use in external clock mode. If EXT/$\overline{INT}$ is HIGH, digital data input on TAG will be output on DATA with a delay of 16 DATACLK pulses as long as $\overline{CS}$ is LOW and R/$\overline{C}$ is HIGH. See Figure 3. |
| 15 | R/$\overline{C}$ | Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. When EXT/$\overline{INT}$ is LOW, this also initiates the transmission of the data results from the previous conversion. If EXT/$\overline{INT}$ is HIGH, a rising edge on R/$\overline{C}$ with $\overline{CS}$ LOW, or a falling edge on $\overline{CS}$ with R/$\overline{C}$ HIGH, transmits a pulse on SYNC and initiates the transmission of data from the previous conversion. |
| 16 | $\overline{CS}$ | Chip Select. Internally OR'ed with R/$\overline{C}$. |
| 17 | $\overline{BUSY}$ | Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output shift register. $\overline{CS}$ or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ rises, or another conversion will start without time for signal acquisition. |
| 18 | PWRD | Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register. |
| 19 | $V_{ANA}$ | Analog Supply Input. Nominally +5V. Connect directly to pin 20, and decouple to ground with 0.1µF ceramic and 10µF Tantalum capacitors. |
| 20 | $V_{DIG}$ | Digital Supply Input. Nominally +5V. Connect directly to pin 19. Must be ≤ $V_{ANA}$. |

## PIN CONFIGURATION




| ANALOG INPUT RANGE | CONNECT $R1_{IN}$ VIA 200Ω TO | CONNECT $R2_{IN}$ VIA 100Ω TO | CONNECT $R3_{IN}$ TO | IMPEDANCE |
|---|---|---|---|---|
| ±10V | $V_{IN}$ | AGND | CAP | 22.9kΩ |
| ±5V | AGND | $V_{IN}$ | CAP | 13.3kΩ |
| ±3.33V | $V_{IN}$ | $V_{IN}$ | CAP | 10.7kΩ |
| 0V to 10V | AGND | $V_{IN}$ | AGND | 13.3kΩ |
| 0V to 5V | AGND | AGND | $V_{IN}$ | 10.0kΩ |
| 0V to 4V | $V_{IN}$ | AGND | $V_{IN}$ | 10.7kΩ |

TABLE I. Input Range Connections. See Figure 4 for complete information.

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# ADS7810

www.burr-brown.com/databook/ADS7810.html

# 12-Bit 800kHz Sampling CMOS ANALOG-to-DIGITAL CONVERTER

## FEATURES

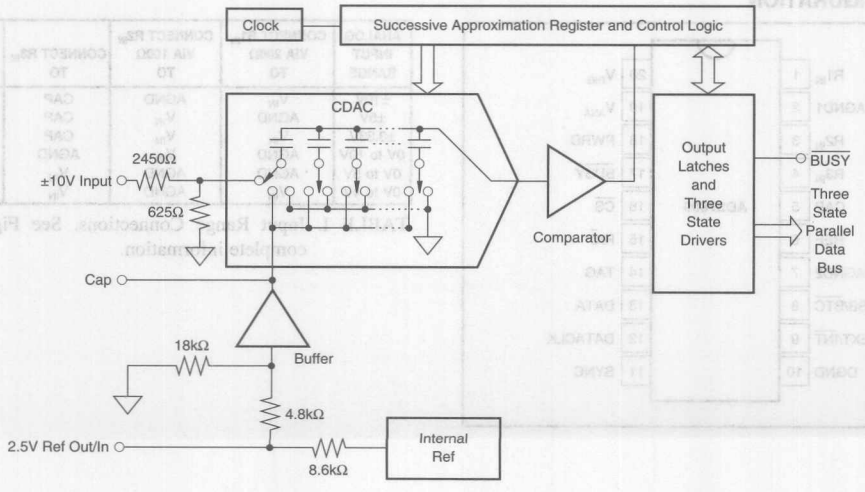
- 1.25µs THROUGHPUT TIME
- STANDARD ±10V INPUT RANGE
- 69dB min SINAD WITH 250kHz INPUT
- ±3/4 LSB max INL AND ±1 LSB max DNL
- INTERNAL REFERENCE
- COMPLETE WITH S/H, REF, CLOCK, ETC.
- PARALLEL DATA w/LATCHES
- 28-PIN SOIC

## DESCRIPTION

The ADS7810 is a complete 12-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 12-bit capacitor-based SAR A/D with inherent S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7810 is specified at an 800kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide the industry-standard ±10V input range, while an innovative design allows operation from ±5V supplies.

The 28-pin ADS7810 is available in a plastic SOIC fully specified for operation over the industrial –40°C to +85°C range.




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PDS-1138E

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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 800kHz, $+V_{DIG} = +V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference and the 50Ω input resistor shown in Figure 4b, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7810U MIN | ADS7810U TYP | ADS7810U MAX | ADS7810UB MIN | ADS7810UB TYP | ADS7810UB MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **RESOLUTION** | | | | 12 | | | * | Bits |
| **ANALOG INPUT** | | | | | | | | |
| Voltage Range | | | ±10 | | | * | | V |
| Impedance | | | 3.1 | | | * | | kΩ |
| Capacitance | | | 5 | | | * | | pF |
| **THROUGHPUT SPEED** | | | | | | | | |
| Conversion Cycle | $t_3 + t_4$ | | 1020 | | | * | | ns |
| Complete Cycle | Acquire & Convert | | | 1250 | | | * | ns |
| Throughput Rate | | 800 | | | * | | | kHz |
| **DC ACCURACY** | | | | | | | | |
| Integral Linearity Error | | | | ±1 | | | ±0.75 | LSB[1] |
| Differential Linearity Error | | | | ±1 | | | * | LSB |
| No Missing Codes | | | Guaranteed | | | * | | |
| Transition Noise[2] | | | 0.1 | | | * | | LSB |
| Full Scale Error[3, 4] | | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | | | ±12 | | | * | | ppm/°C |
| Full Scale Error[3, 4] | Ext. 2.5000V Ref | | | ±0.5 | | | * | % |
| Full Scale Error Drift | Ext. 2.5000V Ref | | ±12 | | | * | | ppm/°C |
| Bipolar Zero Error[3] | | | | ±8 | | | ±4 | LSB |
| Bipolar Zero Error Drift | | | ±2 | | | * | | ppm/°C |
| Power Supply Sensitivity ($+V_{DIG} = +V_{ANA} = V_D$) | +4.75V < $V_D$ < +5.25V | | | ±5 | | | * | LSB |
| | –5.25V < $-V_{ANA}$ < –4.75V | | | ±0.5 | | | * | LSB |
| **AC ACCURACY** | | | | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 250kHz | 74 | 82 | | 77 | 84 | | dB[5] |
| Total Harmonic Distortion | $f_{IN}$ = 250kHz | | –80 | –74 | | –82 | –77 | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 250kHz | 67 | 71 | | 69 | * | | dB |
| Signal-to-Noise | $f_{IN}$ = 250kHz | 68 | 71 | | 70 | * | | dB |
| Usable Bandwidth[6] | | | 1.5 | | | * | | MHz |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Aperture Delay | | | 20 | | | * | | ns |
| Aperture Jitter | | | 10 | | | * | | ps |
| Transient Response | FS Step | | 200 | | | * | | ns |
| Overvoltage Recovery[7] | | | 250 | | | * | | ns |
| **REFERENCE** | | | | | | | | |
| Internal Reference Voltage | | 2.48 | 2.5 | 2.52 | * | * | * | V |
| Internal Reference DC Source Current (External load should be static) | | | 100 | | | * | | µA |
| Internal Reference Drift | | | 8 | | | | | ppm/°C |
| External Reference Voltage Range For Specified Linearity | | 2.3 | 2.5 | 2.7 | * | * | * | V |
| External Reference Current Drain | Ext. 2.5000V Ref | | | 100 | | | * | µA |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Levels | | | | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | * | | * | V |
| $V_{IH}$ | | +2.4 | | $V_D$ + 0.3 | * | | * | V |
| $I_{IL}$ | $V_{IL}$ = 0V | | | ±10 | | | * | µA |
| $I_{IH}$ | $V_{IH}$ = 5V | | | ±10 | | | * | µA |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Data Format | | | | Parallel 12 Bits | | | | |
| Data Coding | | | | Binary Two's Complement | | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +2.8 | | | * | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_{DIG}$ | | | ±5 | | | * | µA |
| Output Capacitance | High-Z State | | | 15 | | | 15 | pF |
| **DIGITAL TIMING** | | | | | | | | |
| Bus Access Time | | | | 62 | | | * | ns |
| Bus Relinquish Time | | | | 83 | | | * | ns |

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

# SPECIFICATIONS (CONT)

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 800kHz, $+V_{DIG} = +V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference and the 50Ω input resistor shown in Figure 4b, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7810U MIN | ADS7810U TYP | ADS7810U MAX | ADS7810UB MIN | ADS7810UB TYP | ADS7810UB MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | | | | |
| Specified Performance | | | | | | | | |
| $+V_{DIG} = +V_{ANA}$ | | +4.75 | +5 | +5.25 | * | * | * | V |
| $-V_{ANA}$ | | –5.25 | –5 | –4.75 | * | * | * | V |
| $+I_{DIG}$ | | | +16 | | | * | | mA |
| $+I_{ANA}$ | | | +16 | | | * | | mA |
| $-I_{ANA}$ | | | –13 | | | * | | mA |
| Derated Performance | | | | | | | | |
| $+V_{DIG} = +V_{ANA}$ | | +4.5 | +5 | +5.5 | * | * | * | V |
| $-V_{ANA}$ | | –5.5 | –5 | –4.5 | * | * | * | V |
| Power Dissipation | $f_S$ = 800kHz | | 225 | 275 | | | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | °C |
| Derated Performance | | –55 | | +125 | | | | °C |
| Storage | | –65 | | +150 | * | | * | °C |
| Thermal Resistance ($\theta_{JA}$) | | | | | | | | |
| Plastic DIP | | | 75 | | | * | | °C/W |
| SOIC | | | 75 | | | * | | °C/W |

* Specification same as ADS7810U.

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, ±10V input ADS7810, one LSB is 4.88mV. (2) Typical rms noise at worst case transitions and temperatures. (3) Measured with 50Ω in series with analog input. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input over voltage.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $V_{IN}$ | ±25V |
| REF | $+V_{ANA}$ +0.3V to AGND2 –0.3V |
| CAP | Indefinite Short to AGND2 |
| | Momentary Short to $+V_{ANA}$ |
| Ground Voltage Differences: DGND, AGND1, AGND2 | ±0.3V |
| $+V_{ANA}$ | +7V |
| $+V_{DIG}$ to $+V_{ANA}$ | +0.3V |
| $+V_{DIG}$ | 7V |
| $-V_{ANA}$ | –7V |
| Digital Inputs | –0.3V to $+V_{DIG}$ +0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING/PACKAGE INFORMATION

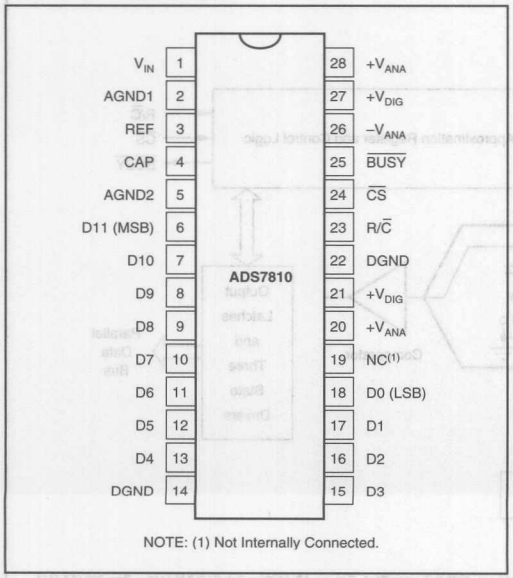
| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|---|---|---|
| ADS7810U | ±1 | 67 | –40°C to +85°C | 28-Pin SOIC | 217 |
| ADS7810UB | ±0.75 | 69 | –40°C to +85°C | 28-Pin SOIC | 217 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN ASSIGNMENTS

| PIN # | NAME | DIGITAL I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $V_{IN}$ | | Analog Input. Connect via 50Ω to analog input. Full-scale input range is ±10V. |
| 2 | AGND1 | | Analog Ground. Used internally as ground reference point. Minimal current flow. |
| 3 | REF | | Reference Input/Output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, decouple to ground with a 0.1µF ceramic capacitor. |
| 4 | CAP | | Reference Buffer Output. 10µF tantalum capacitor to ground. Nominally +2V. |
| 5 | AGND2 | | Analog Ground. |
| 6 | D11 (MSB) | O | Data Bit 11. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 7 | D10 | O | Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 8 | D9 | O | Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 9 | D8 | O | Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 10 | D7 | O | Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 11 | D6 | O | Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 12 | D5 | O | Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 13 | D4 | O | Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 14 | DGND | | Digital Ground. |
| 15 | D3 | O | Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 16 | D2 | O | Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 17 | D1 | O | Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 18 | D0 (LSB) | O | Data Bit 0. Least Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 19 | | | Not internally connected. |
| 20 | $+V_{ANA}$ | | Analog Positive Supply Input. Nominally +5V. Connect directly to pins 21, 27 and 28. |
| 21 | $+V_{DIG}$ | | Digital Supply Input. Nominally +5V. Connect directly to pins 20, 27 and 28. |
| 22 | DGND | | Digital ground. |
| 23 | R/$\overline{C}$ | I | Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW and no conversion in progress, a rising edge on R/$\overline{C}$ enables the output data bits. |
| 24 | $\overline{CS}$ | I | Chip Select. With R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH and no conversion in progress, a falling edge on $\overline{CS}$ will enable the output data bits. |
| 25 | $\overline{BUSY}$ | O | Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output register. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data. |
| 26 | $-V_{ANA}$ | | Analog Negative Supply Input. Nominally –5V. Decouple to ground with 0.1µF ceramic and 10µF tantulum capacitors. |
| 27 | $+V_{DIG}$ | | Digital Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 28. |
| 28 | $+V_{ANA}$ | | Analog Positive Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 27, and decouple to ground with 0.1µF ceramic and 10µF tantulum capacitors. |

## PIN CONFIGURATION




NOTE: (1) Not Internally Connected.

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# ADS7811

www.burr-brown.com/databook/ADS7811.html

# 16-Bit 250kHz Sampling CMOS ANALOG-to-DIGITAL CONVERTER

## FEATURES

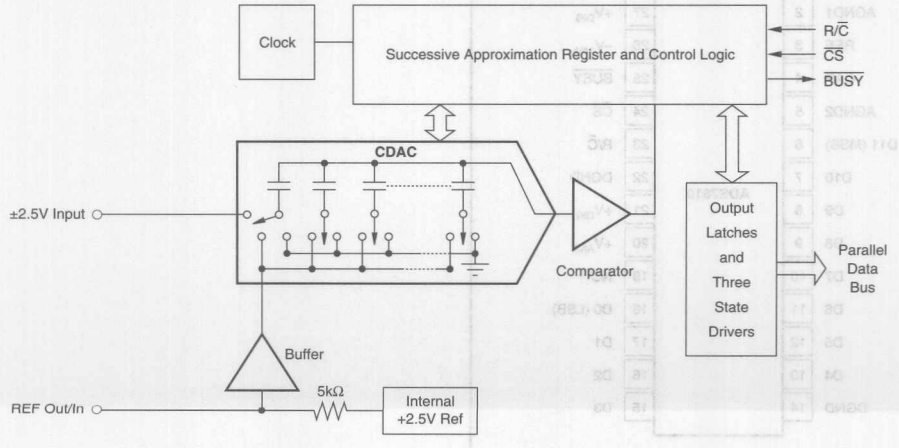
- 250kHz SAMPLING RATE
- COMPLETE WITH S/H, REF, CLOCK, ETC.
- 96dB min SFDR WITH 100kHz INPUT
- 84dB min SINAD
- ±2.5V INPUT RANGE
- 28-LEAD SOIC

## APPLICATIONS

- WIRELESS BASE STATIONS
- SPECTRUM ANALYSIS
- IMAGING SYSTEMS
- DATA ACQUISITION

## DESCRIPTION

The ADS7811 is a complete 16-bit sampling analog-to-digital (A/D) converter featuring excellent AC performance and a 250kHz throughput rate. The design includes a 16-bit capacitor-based SAR A/D converter with an inherent sample and hold (S/H), a precision reference, and an internal clock. Spurious-free dynamic range with a 100kHz full-scale sinewave input is typically greater than 100dB. The ±2.5V input range allows development of precision systems using only ±5V supplies. The converter is available in a 28-lead SOIC package specified for operation over the industrial –25°C to +85°C temperature range.




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# SPECIFICATIONS

At $T_A$ = –25°C to +85°C, $f_S$ = 250kHz, $+V_S$ = +5V, and $-V_S$ = –5V, using internal reference, unless otherwise specified.

| | | ADS7811U | | | |
|---|---|---|---|---|---|
| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
| **RESOLUTION** | | | | 16 | Bits |
| **ANALOG INPUT** | | | | | |
| Voltage Range | | | ±2.5V | | V |
| Impedance | After Input Capacitor is Charged | | 100 | | MΩ |
| Capacitance | | | 30 | | pF |
| **THROUGHPUT SPEED** | | | | | |
| Conversion Cycle | Acquire and Convert | | | 4.0 | µs |
| Throughput Rate | | 250 | | | kHz |
| **DC ACCURACY** | | | | | |
| Integral Linearity Error | | | | ±4 | LSB[1] |
| No Missing Codes | | 15 | | | Bits |
| Transition Noise[2] | | | 0.8 | | LSB |
| Full Scale Error[3] | | | | ±0.5 | % |
| Full Scale Error Drift | | | ±7 | | ppm/°C |
| Full Scale Error[3] | External 2.5000V Reference | | ±0.2 | | % |
| Full Scale Error Drift | External 2.5000V Reference | | 2 | | ppm/°C |
| Bipolar Zero Error | | | | ±10 | mV |
| Bipolar Zero Error Drift | | | ±2 | | ppm/°C |
| Power Supply Sensitivity | $+V_S$ ±5%, $-V_S$ ±5% | | ±6 | ±16 | LSB |
| **AC ACCURACY** | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 100kHz | 96 | 100 | | dB[4] |
| Total Harmonic Distortion | $f_{IN}$ = 100kHz | | –98 | –96 | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 100kHz | 84 | 87 | | dB |
| | –60dB Input | | 28 | | dB |
| Signal-to-Noise | $f_{IN}$ = 100kHz | 84 | 87 | | dB |
| Usable Bandwidth[5] | | | 1 | | MHz |
| Aperture Delay | | | 40 | | ns |
| **REFERENCE** | | | | | |
| Internal Reference Voltage | | 2.48 | 2.5 | 2.52 | V |
| Internal Reference Source Current | | | 1 | | µA |
| Internal Reference Drift | | | 15 | | ppm/°C |
| External Reference Voltage Range | | | 2.5 | | V |
| External Reference Current Drain | $V_{REF}$ = +2.5V | | | 100 | µA |
| **DIGITAL INPUTS** | | | | | |
| Logic Levels | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | V |
| $V_{IH}$ | | +2.8 | | $+V_S$ +0.3V | V |
| $I_{IL}$ | | | | ±10 | µA |
| $I_{IH}$ | | | | ±10 | µA |
| **DIGITAL OUTPUTS** | | | | | |
| Data Format | | | Parallel 16 bits | | |
| Data Coding | | | Binary Two's Complement | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | V |
| $V_{OH}$ | $I_{SOURCE}$ = 200µA | +4 | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_{DIG}$ | | | ±5 | µA |
| Output Capacitance | High-Z State | | | 15 | pF |
| **DIGITAL TIMING** | | | | | |
| Bus Access Time | | | | 83 | ns |
| Bus Relinquish Time | | | | 83 | ns |
| **POWER SUPPLIES** | | | | | |
| $+V_S$ | | +4.75 | +5 | +5.25 | V |
| $-V_S$ | | –5.25 | –5 | –4.75 | V |
| $+I_S$ | | | +30 | | mA |
| $-I_S$ | | | –10 | | mA |
| Power Dissipation | | | 200 | 250 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified Performance | | –25 | | +85 | °C |
| Storage | | –55 | | +125 | °C |

NOTES: (1) LSB means Least Significant Bit. For the 16-bit, ±2.5V input ADS7811, one LSB is 76µV. (2) Typical rms noise at worst case transitions and temperatures. (3) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (4) All specifications in dB are referred to a full-scale ±2.5V input. (5) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $V_{IN}$ | $-V_S - 0.3V$ to $+V_S + 0.3V$ |
| REF | $-0.3V$ to $+V_S + 0.3V$ |
| CAP | Indefinite Short to GND<br>Momentary Short to $+V_S$ |
| $+V_S$ | 7V |
| $-V_S$ | –7V |
| Digital Inputs | $-0.3V$ to $+V_S + 0.3V$ |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS7811U | 28-Pin SOIC | 217 | –25°C to +85°C |

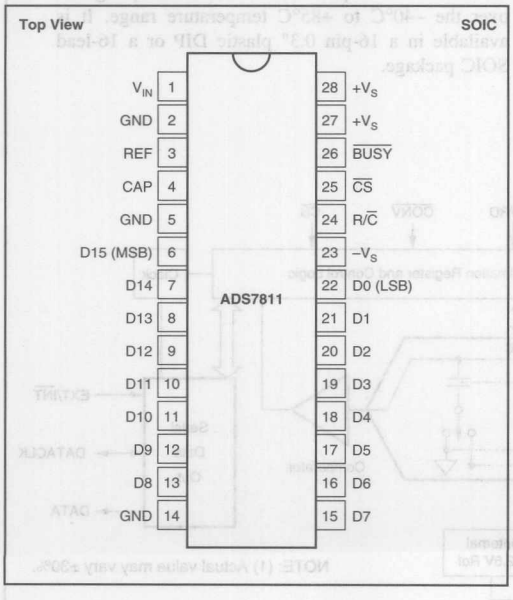
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

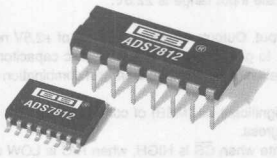
| PIN # | NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_{IN}$ | Analog Input. Full-scale input range is ±2.5V. |
| 2 | GND | Ground. |
| 3 | REF | Reference Input/Output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, connect to ground with a 0.1µF ceramic capacitor in parallel with 2.2µF tantalum capacitor. |
| 4 | CAP | Reference compensation capacitor. Use a parallel combination of a 0.1µF ceramic capacitor and a 2.2µF tantalum capacitor. |
| 5 | GND | Ground. |
| 6 | D15 (MSB) | Data Bit 15. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 7 | D14 | Data Bit 14. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 8 | D13 | Data Bit 13. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 9 | D12 | Data Bit 12. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 10 | D11 | Data Bit 11. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 11 | D10 | Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 12 | D9 | Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 13 | D8 | Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 14 | GND | Ground. |
| 15 | D7 | Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 16 | D6 | Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 17 | D5 | Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 18 | D4 | Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 19 | D3 | Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 20 | D2 | Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 21 | D1 | Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 22 | D0 (LSB) | Data Bit 0. Least Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 23 | $-V_S$ | Negative supply input. Nominally –5V. Decouple to analog ground with 0.1µF ceramic and 10µF tantalum capacitors. |
| 24 | R/$\overline{C}$ | Read/convert input. With R/$\overline{C}$ HIGH, $\overline{CS}$ going LOW will enable the output data bits if a conversion is not in progress. With R/$\overline{C}$ LOW, $\overline{CS}$ going LOW will start a conversion if one is not already in progress. |
| 25 | $\overline{CS}$ | Chip select. With R/$\overline{C}$ LOW, $\overline{CS}$ going LOW will initiate a conversion if one is not already in progress. With R/$\overline{C}$ HIGH, $\overline{CS}$ going LOW will enable the output data bits if a conversion is not in progress. |
| 26 | $\overline{BUSY}$ | Busy output. Falls when a conversion is started, and remains LOW until the conversion is completed. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data. $\overline{CS}$ or R/$\overline{C}$ must be HIGH within 250ns after $\overline{BUSY}$ rises or another conversion will start without time for signal acquisition. |
| 27 | $+V_S$ | Positive supply input. Nominally +5V. Connect directly to pin 28. |
| 28 | $+V_S$ | Positive supply input. Nominally +5V. Connect directly to pin 27. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors. |

TABLE I. Pin Assignments.

## PIN CONFIGURATION



BURR-BROWN®



# ADS7812

DEMO BOARD AVAILABLE
See Appendix A

www.burr-brown.com/databook/ADS7812.html

# Low-Power, Serial 12-Bit Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- 20µs max CONVERSION TIME
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 16-BIT ADS7813
- EASY-TO-USE SERIAL INTERFACE
- 16-PIN 0.3" PLASTIC DIP AND SOIC
- ±0.5LSB max INL AND DNL
- 72dB min SINAD
- USES INTERNAL OR EXTERNAL REFERENCE
- MULTIPLE INPUT RANGES
- 35mW max POWER DISSIPATION
- NO MISSING CODES
- 50µW POWER DOWN MODE

## APPLICATIONS

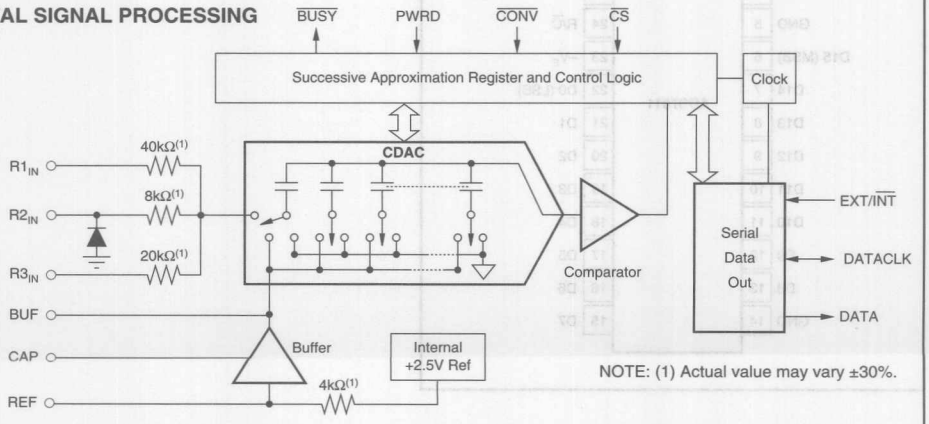
- DATA ACQUISITION SYSTEMS
- INDUSTRIAL CONTROL
- TEST EQUIPMENT
- DIGITAL SIGNAL PROCESSING

## DESCRIPTION

The ADS7812 is a low-power, single +5V supply, 12-bit sampling analog-to-digital converter. It contains a complete 12-bit capacitor-based SAR A/D with a sample/hold, clock, reference, and serial data interface.

The converter can be configured for a variety of input ranges including ±10V, ±5V, 0V to 10V, and 0.5V to 4.5V. A high impedance 0.3V to 2.8V input range is also available (input impedance > 10MΩ). For most input ranges, the input voltage can swing to +16.5V or –16.5V without damage to the converter.

A flexible SPI compatible serial interface allows data to be synchronized to an internal or external clock. The ADS7812 is specified at a 40kHz sampling rate over the –40°C to +85°C temperature range. It is available in a 16-pin 0.3" plastic DIP or a 16-lead SOIC package.




NOTE: (1) Actual value may vary ±30%.

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# SPECIFICATIONS

At $T_A$ = –40°C to +85°C, $f_S$ = 40kHz, $V_S$ = +5V ±5%, using internal reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7812P, U | | | ADS7812PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | | 12 | | | * | Bits |
| **ANALOG INPUT** | | | | | | | | |
| Voltage Range | | | See Table I | | | * | | |
| Impedance | | | See Table I | | | * | | |
| Capacitance | | | 35 | | | * | | pF |
| **THROUGHPUT SPEED** | | | | | | | | |
| Conversion Time | | | | 20 | | | * | µs |
| Complete Cycle | Acquire and Convert | | | 25 | | | * | µs |
| Throughput Rate | | 40 | | | * | | | kHz |
| **DC ACCURACY** | | | | | | | | |
| Integral Linearity Error | | | 0.1 | ±1 | | * | ±0.5 | LSB[1] |
| Differential Linearity Error | | | 0.1 | ±1 | | * | ±0.5 | LSB |
| No Missing Codes | | | Guaranteed | | | * | | |
| Transition Noise[2] | | | 0.05 | | | * | | LSB |
| Full Scale Error[3] | | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | | | ±14 | | | * | | ppm/°C |
| Full Scale Error[3] | Ext. 2.5000V Ref | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | Ext. 2.5000V Ref | | ±5 | | | * | | ppm/°C |
| Bipolar Zero Error | Bipolar Ranges | | | ±10 | | | * | mV |
| Bipolar Zero Error Drift | Bipolar Ranges | | ±3 | | | * | | ppm/°C |
| Unipolar Zero Error | Unipolar Ranges | | | ±6 | | | * | mV |
| Unipolar Zero Error Drift | Unipolar Ranges | | ±3 | | | * | | ppm/°C |
| Recovery Time to Rated Accuracy from Power Down[4] | 1.0µF Capacitor to CAP | | 300 | | | * | | µs |
| Power Supply Sensitivity | +4.75V < ($V_S$ = +5V) < +5.25 | | | ±0.75 | | | * | LSB |
| **AC ACCURACY** | | | | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 1kHz | 80 | 98 | | * | * | | dB[5] |
| Total Harmonic Distortion | $f_{IN}$ = 1kHz | | –96 | –80 | | * | * | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 1kHz | 70 | 74 | | 72 | * | | dB |
| Signal-to-Noise | $f_{IN}$ = 1kHz | 70 | 74 | | 72 | * | | dB |
| Useable Bandwidth[6] | | | 130 | | | * | | kHz |
| Full Power –3dB Bandwidth | | | 600 | | | * | | kHz |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Aperture Delay | | | 40 | | | * | | ns |
| Aperture Jitter | | | 20 | | | * | | ps |
| Transient Response | FS Step | | 5 | | | * | | µs |
| Overvoltage Recovery[7] | | | 750 | | | * | | ns |
| **REFERENCE** | | | | | | | | |
| Internal Reference Voltage | | 2.48 | 2.5 | 2.52 | * | * | * | V |
| Internal Reference Source Current | | | 100 | | | * | | µA |
| Internal Reference Drift | | | 8 | | | * | | ppm/°C |
| External Reference Voltage Range | | 2.3 | 2.5 | 2.7 | * | * | * | V |
| External Reference Current Drain | $V_{REF}$ = +2.5V | | | 100 | | | * | µA |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Levels | | | | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | * | | * | V |
| $V_{IH}$ | | +2.0 | | $V_S$ +0.3V | * | | * | V |
| $I_{IL}$ | | | | ±10 | | | * | µA |
| $I_{IH}$ | | | | ±10 | | | * | µA |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Data Format | | | | Serial | | | | |
| Data Coding | | | | Binary Two's Complement | | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +4 | | | * | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_S$ | | | ±1 | | | * | µA |
| Output Capacitance | High-Z State | | | 15 | | | 15 | pF |

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At $T_A$ = –40°C to +85°C, $f_S$ = 40kHz, $V_S$ = +5V ±5%, using internal reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7812P, U | | | ADS7812PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **POWER SUPPLY** | | | | | | | | |
| $V_S$ | | +4.75 | +5 | +5.25 | * | * | * | V |
| Power Dissipation | $f_S$ = 40kHz | | | 35 | | | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | °C |
| Derated Performance | | –55 | | +125 | * | | * | °C |

* Same specification as ADS7812P, U.

NOTES: (1) LSB means Least Significant Bit. For the ±10V input range, one LSB is 4.88mV. (2) Typical rms noise at worst case transitions and temperatures. (3) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (4) After the ADS7812 is initially powered on and fully settles, this is the time delay after it is brought out of Power Down Mode until all internal settling occurs and the analog input is acquired to rated accuracy, and normal conversions can begin again. (5) All specifications in dB are referred to a full-scale input. (6) Useable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $R1_{IN}$ | ±16.5V |
| $R2_{IN}$ | GND – 0.3V to +16.5V |
| $R3_{IN}$ | ±16.5V |
| REF | GND – 0.3V to $V_S$ + 0.3V |
| CAP | Indefinite Short to GND<br>Momentary Short to $V_S$ |
| $V_S$ | 7V |
| Digital Inputs | GND – 0.3V to $V_S$ + 0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

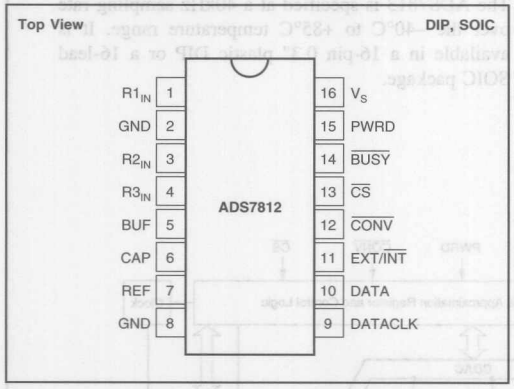
## PACKAGE/ORDERING INFORMATION

| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | GUARANTEED NO MISSING CODE LEVEL (LSB) | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|---|---|---|---|
| ADS7812P | ±1 | 12 | 70 | –40°C to +85°C | Plastic DIP | 180 |
| ADS7812PB | ±0.5 | 12 | 72 | –40°C to +85°C | Plastic DIP | 180 |
| ADS7812U | ±1 | 12 | 70 | –40°C to +85°C | SOIC | 211 |
| ADS7812UB | ±0.5 | 12 | 72 | –40°C to +85°C | SOIC | 211 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

| PIN # | NAME | DESCRIPTION |
|---|---|---|
| 1 | $R1_{IN}$ | Analog Input. See Tables I and IV. |
| 2 | GND | Ground |
| 3 | $R2_{IN}$ | Analog Input. See Tables I and IV. |
| 4 | $R3_{IN}$ | Analog Input. See Tables I and IV. |
| 5 | BUF | Reference Buffer Output. Connect to $R1_{IN}$, $R2_{IN}$, or $R3_{IN}$, as needed. |
| 6 | CAP | Reference Buffer Compensation Node. Decouple to ground with a 1µF tantalum capacitor in parallel with a 0.01µF ceramic capacitor. |
| 7 | REF | Reference Input/Output. Outputs internal +2.5V reference via a series 4kΩ resistor. Decouple this voltage with a 1µF to 2.2µF tantalum capacitor to ground. If an external reference voltage is applied to this pin, it will override the internal reference. |
| 8 | GND | Ground |
| 9 | DATACLK | Data Clock Pin. With EXT/$\overline{INT}$ LOW, this pin is an output and provides the synchronous clock for the serial data. The output is tri-stated when $\overline{CS}$ is HIGH. With EXT/$\overline{INT}$ HIGH, this pin is an input and the serial data clock must be provided externally. |
| 10 | DATA | Serial Data Output. The serial data is always the result of the last completed conversion and is synchronized to DATACLK. If DATACLK is from the internal clock (EXT/$\overline{INT}$ LOW), the serial data is valid on both the rising and falling edges of DATACLK. DATA is tri-stated when $\overline{CS}$ is HIGH. |
| 11 | EXT/$\overline{INT}$ | External or Internal DATACLK Pin. Selects the source of the synchronous clock for serial data. If HIGH, the clock must be provided externally. If LOW, the clock is derived from the internal conversion clock. Note that the clock used to time the conversion is always internal regardless of the status of EXT/$\overline{INT}$. |
| 12 | $\overline{CONV}$ | Convert Input. A falling edge on this input puts the internal sample/hold into the hold state and starts a conversion regardless of the state of $\overline{CS}$. If a conversion is already in progress, the falling edge is ignored. If EXT/$\overline{INT}$ is LOW, data from the previous conversion will be serially transmitted during the current conversion. |
| 13 | $\overline{CS}$ | Chip Select. This input tri-states all outputs when HIGH and enables all outputs when LOW. This includes DATA, $\overline{BUSY}$, and DATACLK (when EXT/$\overline{INT}$ is LOW). Note that a falling edge on $\overline{CONV}$ will initiate a conversion even when $\overline{CS}$ is HIGH. |
| 14 | $\overline{BUSY}$ | Busy Output. When a conversion is started, $\overline{BUSY}$ goes LOW and remains LOW throughout the conversion. If EXT/$\overline{INT}$ is LOW, data is serially transmitted while $\overline{BUSY}$ is LOW. $\overline{BUSY}$ is tri-stated when $\overline{CS}$ is HIGH. |
| 15 | PWRD | Power Down Input. When HIGH, the majority of the ADS7812 is placed in a low power mode and power consumption is significantly reduced. $\overline{CONV}$ must be taken LOW prior to PWRD going LOW in order to achieve the lowest power consumption. The time required for the ADS7812 to return to normal operation after power down depends on a number of factors. Consult the Power Down section for more information. |
| 16 | $V_S$ | +5V Supply Input. For best performance, decouple to ground with a 0.1µF ceramic capacitor in parallel with a 10µF tantalum capacitor. |

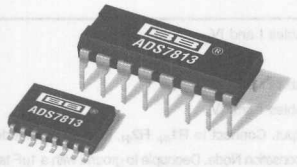
## PIN CONFIGURATION




| ANALOG INPUT RANGE (V) | CONNECT $R1_{IN}$ TO | CONNECT $R2_{IN}$ TO | CONNECT $R3_{IN}$ TO | INPUT IMPEDANCE (kΩ) |
|---|---|---|---|---|
| ±10V | $V_{IN}$ | BUF | GND | 45.7 |
| 0.3125V to 2.8125V | $V_{IN}$ | $V_{IN}$ | $V_{IN}$ | > 10,000 |
| ±5V | GND | BUF | $V_{IN}$ | 26.7 |
| 0V to 10V | BUF | GND | $V_{IN}$ | 26.7 |
| 0V to 4V | BUF | $V_{IN}$ | GND | 21.3 |
| ±3.33V | $V_{IN}$ | BUF | $V_{IN}$ | 21.3 |
| 0.5V to 4.5V | GND | $V_{IN}$ | GND | 21.3 |

TABLE I. ADS7812 Input Ranges.

BURR-BROWN®




# ADS7813

**DEMO BOARD AVAILABLE**
**See Appendix A**

www.burr-brown.com/databook/ADS7813.html

# Low-Power, Serial 16-Bit Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- 20µs max CONVERSION TIME
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 12-BIT ADS7812
- EASY-TO-USE SERIAL INTERFACE
- 16-PIN 0.3" PLASTIC DIP AND SOIC
- ±2.0LSB max INL
- 87dB min SINAD
- USES INTERNAL OR EXTERNAL REFERENCE
- MULTIPLE INPUT RANGES
- 35mW max POWER DISSIPATION
- NO MISSING CODES
- 50µW POWER DOWN MODE

## APPLICATIONS

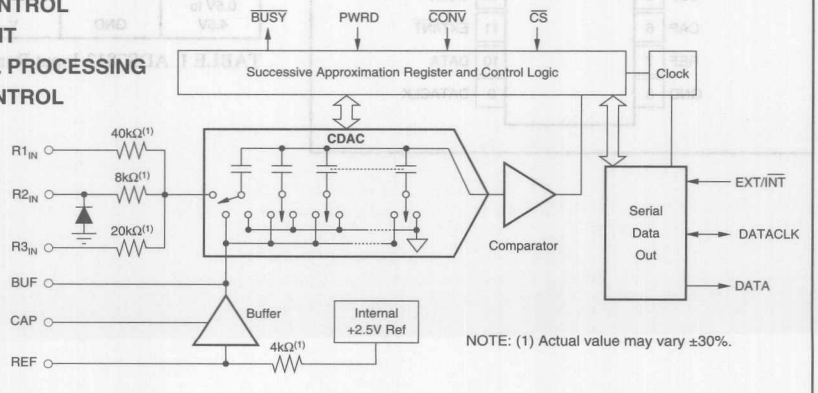
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION SYSTEMS
- ROBOTICS
- INDUSTRIAL CONTROL
- TEST EQUIPMENT
- DIGITAL SIGNAL PROCESSING
- DSP SERVO CONTROL

## DESCRIPTION

The ADS7813 is a low-power, single +5V supply, 16-bit sampling analog-to-digital converter. It contains a complete 16-bit capacitor-based SAR A/D with a sample/hold, clock, reference, and serial data interface.

The converter can be configured for a variety of input ranges including ±10V, ±5V, 0V to 10V, and 0.5V to 4.5V. A high impedance 0.3V to 2.8V input range is also available (input impedance > 10MΩ). For most input ranges, the input voltage can swing to +16.5V or –16.5V without damage to the converter.

A flexible SPI compatible serial interface allows data to be synchronized to an internal or external clock. The ADS7813 is specified at a 40kHz sampling rate over the –40°C to +85°C temperature range. It is available in a 16-pin 0.3" plastic DIP or a 16-lead SOIC package.




NOTE: (1) Actual value may vary ±30%.

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = –40°C to +85°C, $f_S$ = 40kHz, $V_S$ = +5V ±5%, using internal reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7813P, U | | | ADS7813PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | | 16 | | | * | Bits |
| **ANALOG INPUT** | | | | | | | | |
| Voltage Range | | | See Table I | | | * | | |
| Impedance | | | See Table I | | | * | | |
| Capacitance | | | 35 | | | * | | pF |
| **THROUGHPUT SPEED** | | | | | | | | |
| Conversion Time | | | | 20 | | | * | µs |
| Complete Cycle | Acquire and Convert | | | 25 | | | * | µs |
| Throughput Rate | | 40 | | | * | | | kHz |
| **DC ACCURACY** | | | | | | | | |
| Integral Linearity Error | | | | ±3 | | * | ±2 | LSB[1] |
| Differential Linearity Error | | | | +3, –2 | | * | +2, –1 | LSB |
| No Missing Codes | | 15 | | | 16 | | | Bits |
| Transition Noise[2] | | | 0.6 | | | * | | LSB |
| Full Scale Error[3] | | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | | | ±14 | | | * | | ppm/°C |
| Full Scale Error[3] | Ext. 2.5000V Ref | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | Ext. 2.5000V Ref | | ±5 | | | * | | ppm/°C |
| Bipolar Zero Error | Bipolar Ranges | | | ±10 | | | * | mV |
| Bipolar Zero Error Drift | Bipolar Ranges | | ±3 | | | * | | ppm/°C |
| Unipolar Zero Error | Unipolar Ranges | | | ±6 | | | * | mV |
| Unipolar Zero Error Drift | Unipolar Ranges | | ±3 | | | * | | ppm/°C |
| Recovery Time to Rated Accuracy from Power Down[4] | 1.0µF Capacitor to CAP | | 300 | | | * | | µs |
| Power Supply Sensitivity | +4.75V < ($V_S$ = +5V) < +5.25 | | | ±12 | | | * | LSB |
| **AC ACCURACY** | | | | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 1kHz | 90 | 100 | | 96 | 102 | | dB[5] |
| Total Harmonic Distortion | $f_{IN}$ = 1kHz | | –98 | –90 | | –100 | –96 | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 1kHz | 85 | 89 | | 87 | * | | dB |
| Signal-to-Noise | $f_{IN}$ = 1kHz | 85 | 89 | | 87 | * | | dB |
| Useable Bandwidth[6] | | | 130 | | | * | | kHz |
| Full Power –3dB Bandwidth | | | 600 | | | * | | kHz |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Aperture Delay | | | 40 | | | * | | ns |
| Aperture Jitter | | | 20 | | | * | | ps |
| Transient Response | FS Step | | 5 | | | * | | µs |
| Overvoltage Recovery[7] | | | 750 | | | * | | ns |
| **REFERENCE** | | | | | | | | |
| Internal Reference Voltage | | 2.48 | 2.5 | 2.52 | * | * | * | V |
| Internal Reference Source Current | | | 100 | | | * | | µA |
| Internal Reference Drift | | | 8 | | | * | | ppm/°C |
| External Reference Voltage Range | | 2.3 | 2.5 | 2.7 | * | * | * | V |
| External Reference Current Drain | $V_{REF}$ = +2.5V | | | 100 | | | * | µA |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Levels | | | | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | * | | * | V |
| $V_{IH}$ | | +2.0 | | $V_S$ +0.3V | * | | * | V |
| $I_{IL}$ | | | | ±10 | | | * | µA |
| $I_{IH}$ | | | | ±10 | | | * | µA |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Data Format | | | | Serial | | | | |
| Data Coding | | | | Binary Two's Complement | | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +4 | | | * | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_S$ | | | ±1 | | | * | µA |
| Output Capacitance | High-Z State | | | 15 | | | 15 | pF |

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

At $T_A$ = –40°C to +85°C, $f_S$ = 40kHz, $V_S$ = +5V ±5%, using internal reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7813P, U | | | ADS7813PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **POWER SUPPLY** | | | | | | | | |
| $V_S$ | | +4.75 | +5 | +5.25 | * | * | * | V |
| Power Dissipation | $f_S$ = 40kHz | | | 35 | | | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | °C |
| Derated Performance | | –55 | | +125 | * | | * | °C |

* Same specification as ADS7813P, U.

NOTES: (1) LSB means Least Significant Bit. For the ±10V input range, one LSB is 305µV. (2) Typical rms noise at worst case transitions and temperatures. (3) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (4) After the ADS7813 is initially powered on and fully settles, this is the time delay after it is brought out of Power Down Mode until all internal settling occurs and the analog input is acquired to rated accuracy, and normal conversions can begin again. (5) All specifications in dB are referred to a full-scale input. (6) Useable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $R1_{IN}$ | ±16.5V |
| $R2_{IN}$ | GND – 0.3V to +16.5V |
| $R3_{IN}$ | ±16.5V |
| REF | GND – 0.3V to $V_S$ + 0.3V |
| CAP | Indefinite Short to GND<br>Momentary Short to $V_S$ |
| $V_S$ | 7V |
| Digital Inputs | GND – 0.3V to $V_S$ + 0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | GUARANTEED NO MISSING CODE LEVEL (LSB) | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|---|---|---|---|
| ADS7813P | ±3 | 15 | 85 | –40°C to +85°C | Plastic DIP | 180 |
| ADS7813PB | ±2 | 16 | 87 | –40°C to +85°C | Plastic DIP | 180 |
| ADS7813U | ±3 | 15 | 85 | –40°C to +85°C | SOIC | 211 |
| ADS7813UB | ±2 | 16 | 87 | –40°C to +85°C | SOIC | 211 |

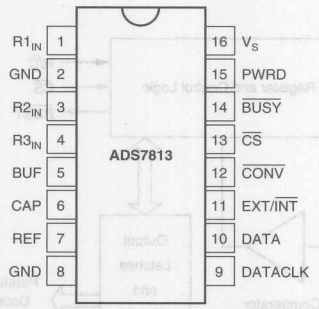
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN CONFIGURATION

| PIN # | NAME | DESCRIPTION |
|---|---|---|
| 1 | $R1_{IN}$ | Analog Input. See Tables I and IV. |
| 2 | GND | Ground |
| 3 | $R2_{IN}$ | Analog Input. See Tables I and IV. |
| 4 | $R3_{IN}$ | Analog Input. See Tables I and IV. |
| 5 | BUF | Reference Buffer Output. Connect to $R1_{IN}$, $R2_{IN}$, or $R3_{IN}$, as needed. |
| 6 | CAP | Reference Buffer Compensation Node. Decouple to ground with a 1µF tantalum capacitor in parallel with a 0.01µF ceramic capacitor. |
| 7 | REF | Reference Input/Output. Outputs internal +2.5V reference via a series 4kΩ resistor. Decouple this voltage with a 1µF to 2.2µF tantalum capacitor to ground. If an external reference voltage is applied to this pin, it will override the internal reference. |
| 8 | GND | Ground |
| 9 | DATACLK | Data Clock Pin. With EXT/$\overline{INT}$ LOW, this pin is an output and provides the synchronous clock for the serial data. The output is tri-stated when $\overline{CS}$ is HIGH. With EXT/$\overline{INT}$ HIGH, this pin is an input and the serial data clock must be provided externally. |
| 10 | DATA | Serial Data Output. The serial data is always the result of the last completed conversion and is synchronized to DATACLK. If DATACLK is from the internal clock (EXT/$\overline{INT}$ LOW), the serial data is valid on both the rising and falling edges of DATACLK. DATA is tri-stated when $\overline{CS}$ is HIGH. |
| 11 | EXT/$\overline{INT}$ | External or Internal DATACLK Pin. Selects the source of the synchronous clock for serial data. If HIGH, the clock must be provided externally. If LOW, the clock is derived from the internal conversion clock. Note that the clock used to time the conversion is always internal regardless of the status of EXT/$\overline{INT}$. |
| 12 | $\overline{CONV}$ | Convert Input. A falling edge on this input puts the internal sample/hold into the hold state and starts a conversion regardless of the state of $\overline{CS}$. If a conversion is already in progress, the falling edge is ignored. If EXT/$\overline{INT}$ is LOW, data from the previous conversion will be serially transmitted during the current conversion. |
| 13 | $\overline{CS}$ | Chip Select. This input tri-states all outputs when HIGH and enables all outputs when LOW. This includes DATA, $\overline{BUSY}$, and DATACLK (when EXT/$\overline{INT}$ is LOW). Note that a falling edge on $\overline{CONV}$ will initiate a conversion even when $\overline{CS}$ is HIGH. |
| 14 | $\overline{BUSY}$ | Busy Output. When a conversion is started, $\overline{BUSY}$ goes LOW and remains LOW throughout the conversion. If EXT/$\overline{INT}$ is LOW, data is serially transmitted while $\overline{BUSY}$ is LOW. $\overline{BUSY}$ is tri-stated when $\overline{CS}$ is HIGH. |
| 15 | PWRD | Power Down Input. When HIGH, the majority of the ADS7813 is placed in a low power mode and power consumption is significantly reduced. $\overline{CONV}$ must be taken LOW prior to PWRD going LOW in order to achieve the lowest power consumption. The time required for the ADS7813 to return to normal operation after power down depends on a number of factors. Consult the Power Down section for more information. |
| 16 | $V_S$ | +5V Supply Input. For best performance, decouple to ground with a 0.1µF ceramic capacitor in parallel with a 10µF tantalum capacitor. |

## PIN CONFIGURATION

Top View DIP, SOIC




| ANALOG INPUT RANGE (V) | CONNECT $R1_{IN}$ TO | CONNECT $R2_{IN}$ TO | CONNECT $R3_{IN}$ TO | INPUT IMPEDANCE (kΩ) |
|---|---|---|---|---|
| ±10V | $V_{IN}$ | BUF | GND | 45.7 |
| 0.3125V to 2.8125V | $V_{IN}$ | $V_{IN}$ | $V_{IN}$ | > 10,000 |
| ±5V | GND | BUF | $V_{IN}$ | 26.7 |
| 0V to 10V | BUF | GND | $V_{IN}$ | 26.7 |
| 0V to 4V | BUF | $V_{IN}$ | GND | 21.3 |
| ±3.33V | $V_{IN}$ | BUF | $V_{IN}$ | 21.3 |
| 0.5V to 4.5V | GND | $V_{IN}$ | GND | 21.3 |

TABLE I. ADS7813 Input Ranges.

BURR-BROWN®




# ADS7815

**DEMO BOARD AVAILABLE**
**See Appendix A**

www.burr-brown.com/databook/ADS7815.html

# 16-Bit 250kHz Sampling CMOS ANALOG-to-DIGITAL CONVERTER

## FEATURES

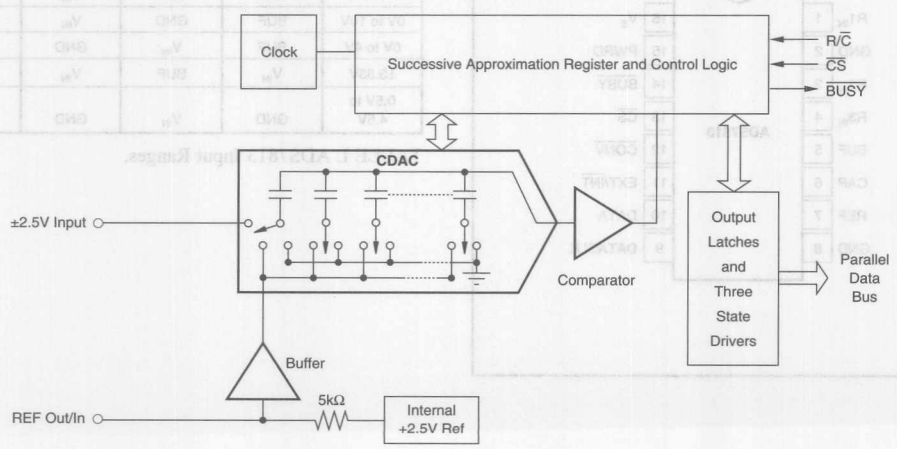
- 250kHz SAMPLING RATE
- COMPLETE WITH S/H, REF, CLOCK, ETC.
- 96dB min SFDR WITH 100kHz INPUT
- 84dB min SINAD
- ±2.5V INPUT RANGE
- 28-LEAD SOIC

## APPLICATIONS

- WIRELESS BASE STATIONS
- SPECTRUM ANALYSIS
- IMAGING SYSTEMS
- DATA ACQUISITION

## DESCRIPTION

The ADS7815 is a complete 16-bit sampling analog-to-digital (A/D) converter featuring excellent AC performance and a 250kHz throughput rate. The design includes a 16-bit capacitor-based SAR A/D converter with an inherent sample and hold (S/H), a precision reference, and an internal clock. Spurious-free dynamic range with a 100kHz full-scale sinewave input is typically greater than 100dB. The ±2.5V input range allows development of precision systems using only ±5V supplies. The converter is available in a 28-lead SOIC package specified for operation over the industrial –25°C to +85°C temperature range.




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# SPECIFICATIONS

At $T_A$ = –25°C to +85°C, $f_S$ = 250kHz, $+V_S$ = +5V, and $-V_S$ = –5V, using internal reference, unless otherwise specified.

| | | ADS7815U | | | |
|---|---|---|---|---|---|
| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
| **RESOLUTION** | | | | 16 | Bits |
| **ANALOG INPUT** | | | | | |
| Voltage Range | | | ±2.5V | | V |
| Impedance | | | 100 | | MΩ |
| Capacitance | | | 30 | | pF |
| **THROUGHPUT SPEED** | | | | | |
| Conversion Cycle | Acquire and Convert | | | 4.0 | µs |
| Throughput Rate | | 250 | | | kHz |
| **DC ACCURACY** | | | | | |
| Integral Linearity Error | | | ±4 | | LSB[1] |
| No Missing Codes | | | 15 | | Bits |
| Transition Noise[2] | | | 0.8 | | LSB |
| Full Scale Error[3] | | | ±0.1 | | % |
| Full Scale Error Drift | | | ±7 | | ppm/°C |
| Bipolar Zero Error | | | ±2 | | mV |
| Bipolar Zero Error Drift | | | ±2 | | ppm/°C |
| Power Supply Sensitivity | $+V_S$ ±5%, $-V_S$ ±5% | | ±6 | | LSB |
| **AC ACCURACY** | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 100kHz | 96 | 100 | | dB[4] |
| Total Harmonic Distortion | $f_{IN}$ = 100kHz | | –98 | –96 | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 100kHz | 84 | | | dB |
| | –60dB Input | | 28 | | dB |
| Signal-to-Noise | $f_{IN}$ = 100kHz | 84 | | | dB |
| Usable Bandwidth[5] | | | 1 | | MHz |
| Aperture Delay | | | 40 | | ns |
| **REFERENCE** | | | | | |
| Internal Reference Voltage | | 2.45 | 2.5 | 2.55 | V |
| Internal Reference Source Current | | | 1 | | µA |
| External Reference Voltage Range | | 2.3 | 2.5 | 2.7 | V |
| External Reference Current Drain | $V_{REF}$ = +2.5V | | | 100 | µA |
| **DIGITAL INPUTS** | | | | | |
| Logic Levels | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | V |
| $V_{IH}$ | | +2.8 | | $+V_S$ +0.3V | V |
| $I_{IL}$ | | | | ±10 | µA |
| $I_{IH}$ | | | | ±10 | µA |
| **DIGITAL OUTPUTS** | | | | | |
| Data Format | | | Parallel 16 bits | | |
| Data Coding | | | Binary Two's Complement | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | V |
| $V_{OH}$ | $I_{SOURCE}$ = 200µA | +4 | | | V |
| Leakage Current | High-Z State, | | | ±5 | µA |
| | $V_{OUT}$ = 0V to $V_{DIG}$ | | | | |
| Output Capacitance | High-Z State | | | 15 | pF |
| **DIGITAL TIMING** | | | | | |
| Bus Access Time | | | | 83 | ns |
| Bus Relinquish Time | | | | 83 | ns |
| **POWER SUPPLIES** | | | | | |
| $+V_S$ | | +4.75 | +5 | +5.25 | V |
| $-V_S$ | | –5.25 | –5 | –4.75 | V |
| $+I_S$ | | | +30 | | mA |
| $-I_S$ | | | –10 | | mA |
| Power Dissipation | | | 200 | 250 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified Performance | | –25 | | +85 | °C |
| Storage | | –55 | | +125 | °C |

NOTES: (1) LSB means Least Significant Bit. For the 16-bit, ±2.5V input ADS7815, one LSB is 76µV. (2) Typical rms noise at worst case transitions and temperatures. (3) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (4) All specifications in dB are referred to a full-scale ±2.5V input. (5) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $V_{IN}$ | $\pm V_S$ |
| REF | GND –0.3V to $+V_S$ +0.3V |
| CAP | Indefinite Short to GND |
| | Momentary Short to $+V_S$ |
| $+V_S$ | 7V |
| $-V_S$ | –7V |
| Digital Inputs | GND –0.3V to $+V_S$ +0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS7815U | 28-Pin SOIC | 217 | –25°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

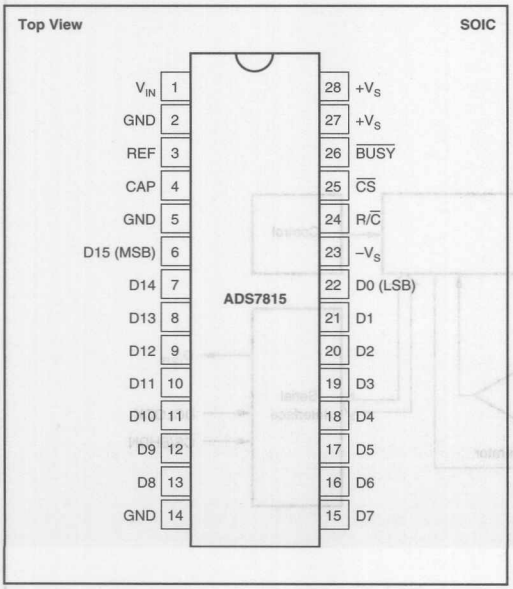
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

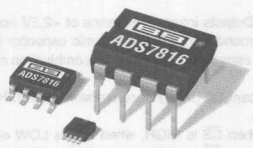
| | | |
|---|---|---|
| 1 | $V_{IN}$ | Analog Input. Full-scale input range is ±2.5V. |
| 2 | GND | Ground. |
| 3 | REF | Reference Input/Output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, connect to ground with a 0.1µF ceramic capacitor in parallel with 2.2µF tantalum capacitor. |
| 4 | CAP | Reference compensation capacitor. Use a parallel combination of a 0.1µF ceramic capacitor and a 2.2µF tantalum capacitor. |
| 5 | GND | Ground. |
| 6 | D15 (MSB) | Data Bit 15. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 7 | D14 | Data Bit 14. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 8 | D13 | Data Bit 13. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 9 | D12 | Data Bit 12. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 10 | D11 | Data Bit 11. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 11 | D10 | Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 12 | D9 | Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 13 | D8 | Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 14 | GND | Ground. |
| 15 | D7 | Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 16 | D6 | Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 17 | D5 | Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 18 | D4 | Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 19 | D3 | Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 20 | D2 | Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 21 | D1 | Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 22 | D0 (LSB) | Data Bit 0. Least Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 23 | $-V_S$ | Negative supply input. Nominally –5V. Decouple to analog ground with 0.1µF ceramic and 10µF tantalum capacitors. |
| 24 | R/$\overline{C}$ | Read/convert input. With R/$\overline{C}$ HIGH, $\overline{CS}$ going LOW will enable the output data bits if a conversion is not in progress. With R/$\overline{C}$ LOW, $\overline{CS}$ going LOW will start a conversion if one is not already in progress. |
| 25 | $\overline{CS}$ | Chip select. With R/$\overline{C}$ LOW, $\overline{CS}$ going LOW will initiate a conversion if one is not already in progress. With R/$\overline{C}$ HIGH, $\overline{CS}$ going LOW will enable the output data bits if a conversion is not in progress. |
| 26 | $\overline{BUSY}$ | Busy output. Falls when a conversion is started, and remains LOW until the conversion is completed. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data. $\overline{CS}$ or R/$\overline{C}$ must be HIGH within 250ns after $\overline{BUSY}$ rises or another conversion will start without time for signal acquisition. |
| 27 | $+V_S$ | Positive supply input. Nominally +5V. Connect directly to pin 28. |
| 28 | $+V_S$ | Positive supply input. Nominally +5V. Connect directly to pin 27. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors. |

TABLE I. Pin Assignments.

## PIN CONFIGURATION



BURR-BROWN®




# ADS7816

www.burr-brown.com/databook/ADS7816.html

# 12-Bit High Speed Micro Power Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- 200kHz SAMPLING RATE
- MICRO POWER:
  1.9mW at 200kHz
  150µW at 12.5kHz
- POWER DOWN: 3µA Max
- 8-PIN MINI-DIP, SOIC, AND MSOP
- DIFFERENTIAL INPUT
- SERIAL INTERFACE

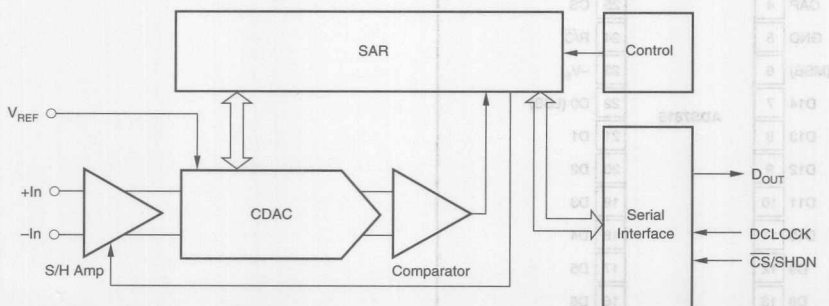
## APPLICATIONS

- BATTERY OPERATED SYSTEMS
- REMOTE DATA ACQUISITION
- ISOLATED DATA ACQUISITION

## DESCRIPTION

The ADS7816 is a 12-bit, 200kHz sampling analog-to-digital converter. It features low power operation with automatic power down, a synchronous serial interface, and a differential input. The reference voltage can be varied from 100mV to 5V, with a corresponding resolution from 24µV to 1.22mV.

Low power, automatic power down, and small size make the ADS7816 ideal for battery operated systems or for systems where a large number of signals must be acquired simultaneously. It is also ideal for remote and/or isolated data acquisition. The ADS7816 is available in an 8-pin plastic mini-DIP, an 8-lead SOIC, or an 8-lead MSOP package.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At –40°C to +85°C, $+V_{CC}$ = +5V, $V_{REF}$ = +5V, $f_{SAMPLE}$ = 200kHz, $f_{CLK}$ = 16 • $f_{SAMPLE}$, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7816 MIN | ADS7816 TYP | ADS7816 MAX | ADS7816B MIN | ADS7816B TYP | ADS7816B MAX | ADS7816C MIN | ADS7816C TYP | ADS7816C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **ANALOG INPUT** | | | | | | | | | | | |
| Full-Scale Input Span | +In – (–In) | 0 | | $V_{REF}$ | * | | * | * | | * | V |
| Absolute Input Voltage | +In | –0.2 | | $V_{CC}$ +0.2 | * | | * | * | | * | V |
| | –In | –0.2 | | +0.2 | * | | * | * | | * | V |
| Capacitance | | | 25 | | | * | | | * | | pF |
| Leakage Current | | | ±1 | | | * | | | * | | µA |
| **SYSTEM PERFORMANCE** | | | | | | | | | | | |
| Resolution | | | 12 | | | * | | | * | | Bits |
| No Missing Codes | | 11 | | | 12 | | | * | | | Bits |
| Integral Linearity Error | | | ±0.5 | ±2 | | ±0.5 | ±2 | | ±0.5 | ±1 | LSB[1] |
| Differential Linearity Error | | | ±0.5 | ±2 | | ±0.5 | ±1 | | ±0.25 | ±0.75 | LSB |
| Offset Error | | | | ±4 | | | * | | | * | LSB |
| Gain Error | | | | ±4 | | | * | | | * | LSB |
| Noise | | | 33 | | | * | | | * | | µVrms |
| Power Supply Rejection | | | 82 | | | * | | | * | | dB |
| **SAMPLING DYNAMICS** | | | | | | | | | | | |
| Conversion Time | | | | 12 | | | * | | | * | Clk Cycles |
| Acquisition Time | | 1.5 | | | * | | | * | | | Clk Cycles |
| Throughput Rate | | | | 200 | | | * | | | * | kHz |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | | | | |
| Total Harmonic Distortion | $V_{IN}$ = 5.0Vp-p at 1kHz | | –84 | | | * | | | * | | dB |
| | $V_{IN}$ = 5.0Vp-p at 5kHz | | –82 | | | * | | | * | | dB |
| SINAD | $V_{IN}$ = 5.0Vp-p at 1kHz | | 72 | | | * | | | * | | dB |
| Spurious Free Dynamic Range | $V_{IN}$ = 5.0Vp-p at 1kHz | | 86 | | | * | | | * | | dB |
| **REFERENCE INPUT** | | | | | | | | | | | |
| Voltage Range | | 0.1 | | 5 | * | | * | * | | * | V |
| Resistance | $\overline{CS}$ = GND, $f_{SAMPLE}$ = 0Hz | | 5 | | | * | | | * | | GΩ |
| | $\overline{CS}$ = $V_{CC}$ | | 5 | | | * | | | * | | GΩ |
| Current Drain | At Code 710h | | 38 | 100 | | * | * | | * | * | µA |
| | $f_{SAMPLE}$ = 12.5kHz | | 2.4 | 20 | | * | * | | * | * | µA |
| | $\overline{CS}$ = $V_{CC}$ | | 0.001 | 3 | | * | * | | * | * | µA |
| **DIGITAL INPUT/OUTPUT** | | | | | | | | | | | |
| Logic Family | | | CMOS | | | * | | | * | | |
| Logic Levels: | | | | | | | | | | | |
| $V_{IH}$ | $I_{IH}$ = +5µA | 3 | | $+V_{CC}$ +0.3 | * | | * | * | | * | V |
| $V_{IL}$ | $I_{IL}$ = +5µA | –0.3 | | 0.8 | * | | * | * | | * | V |
| $V_{OH}$ | $I_{OH}$ = –250µA | 3.5 | | | * | | | * | | | V |
| $V_{OL}$ | $I_{OL}$ = 250µA | | | 0.4 | | | * | | | * | V |
| Data Format | | | Straight Binary | | | * | | | * | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | | | | |
| $V_{CC}$ | Specified Performance | 4.50 | | 5.25 | * | | * | * | | * | V |
| Quiescent Current | | | 380 | 700 | | * | * | | * | * | µA |
| | $f_{SAMPLE}$ = 12.5kHz[2, 3] | | 30 | | | * | | | * | | µA |
| | $f_{SAMPLE}$ = 12.5kHz[3] | | 280 | 400 | | * | | | * | | µA |
| Power Down | $\overline{CS}$ = $V_{CC}$, $f_{SAMPLE}$ = 0Hz | | | 3 | | | * | | | * | µA |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | * | | * | °C |

* Specifications same as ADS7816.

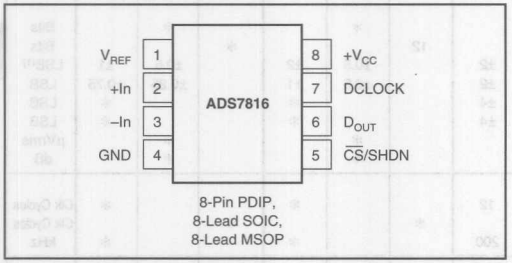
NOTE: (1) LSB means Least Significant Bit, with $V_{REF}$ equal to +5V, one LSB is 1.22mV. (2) $f_{CLK}$ = 3.2MHz, $\overline{CS}$ = $V_{CC}$ for 241 clock cycles out of every 256. (3) See the Power Dissipation section for more information regarding lower sample rates.

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| | |
|---|---|
| $+V_{CC}$ | +6V |
| Analog Input | –0.3V to ($+V_{CC}$ + 0.3V) |
| Logic Input | –0.3V to ($+V_{CC}$ + 0.3V) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +125°C |
| External Reference Voltage | +5.5V |

NOTE: (1) Stresses above these ratings may permanently damage the device.

## PIN CONFIGURATION




8-Pin PDIP,
8-Lead SOIC,
8-Lead MSOP

## DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN ASSIGNMENTS

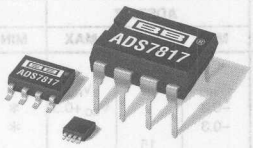
| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_{REF}$ | Reference Input. |
| 2 | +In | Non Inverting Input. |
| 3 | –In | Inverting Input. Connect to ground or to remote ground sense point. |
| 4 | GND | Ground. |
| 5 | $\overline{CS}$/SHDN | Chip Select when LOW, Shutdown Mode when HIGH. |
| 6 | $D_{OUT}$ | The serial output data word is comprised of 12 bits of data. In operation the data is valid on the falling edge of DCLOCK. The second clock pulse after the falling edge of $\overline{CS}$ enables the serial output. After one null bit the data is valid for the next 12 edges. |
| 7 | DCLOCK | Data Clock synchronizes the serial data transfer and determines conversion speed. |
| 8 | $+V_{CC}$ | Power Supply. |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | MAXIMUM DIFFERENTIAL LINEARITY ERROR (LSB) | TEMPERATURE RANGE | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|---|---|---|
| ADS7816P | ±2 | ±2 | –40°C to +85°C | Plastic DIP | 006 |
| ADS7816U | ±2 | ±2 | –40°C to +85°C | SOIC | 182 |
| ADS7816E | ±2 | ±2 | –40°C to +85°C | MSOP | 337 |
| ADS7816PB | ±2 | ±1 | –40°C to +85°C | Plastic DIP | 006 |
| ADS7816UB | ±2 | ±1 | –40°C to +85°C | SOIC | 182 |
| ADS7816EB | ±2 | ±1 | –40°C to +85°C | MSOP | 337 |
| ADS7816PC | ±1 | ±0.75 | –40°C to +85°C | Plastic DIP | 006 |
| ADS7816UC | ±1 | ±0.75 | –40°C to +85°C | SOIC | 182 |
| ADS7816EC | ±1 | ±0.75 | –40°C to +85°C | MSOP | 337 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR-BROWN®




# ADS7817

www.burr-brown.com/databook/ADS7817.html

# 12-Bit Differential Input Micro Power Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- BIPOLAR INPUT RANGE
- TRUE DIFFERENTIAL INPUT
- 200kHz SAMPLING RATE
- MICRO POWER: 2.3mW at 200kHz
- POWER DOWN: 3μA Max
- AVAILABLE IN 8-LEAD MSOP PACKAGE
- SERIAL INTERFACE
- AC COMMON-MODE REJECTION

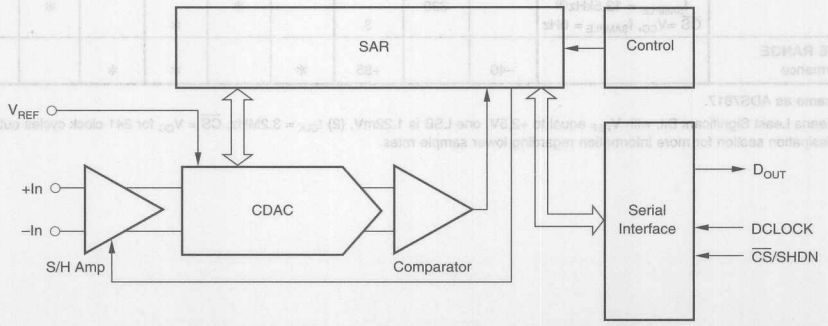
## APPLICATIONS

- TRANSDUCER INTERFACE
- BATTERY OPERATED SYSTEMS
- REMOTE DATA ACQUISITION
- ISOLATED DATA ACQUISITION
- AC MOTOR CONTROL

## DESCRIPTION

The ADS7817 is a 12-bit, 200kHz sampling analog-to-digital converter that features a high impedance fully differential analog input. The reference voltage can be varied from 100mV to 2.5V, with a corresponding input-referred resolution between 49μV and 1.22mV.

The differential input, low power, automatic power down, and small size make the ADS7817 ideal for direct connection to transducers in battery operated systems, remote data acquisition, or multi-channel applications. The ADS7817 is available in an 8-pin plastic mini-DIP, an 8-lead SOIC, or an 8-lead MSOP package.




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# SPECIFICATIONS

At –40°C to +85°C, $+V_{CC}$ = +5V, $V_{REF}$ = +2.5V, $f_{SAMPLE}$ = 200kHz, $f_{CLK}$ = 16 • $f_{SAMPLE}$, –In = +2.5V, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7817 MIN | ADS7817 TYP | ADS7817 MAX | ADS7817B MIN | ADS7817B TYP | ADS7817B MAX | ADS7817C MIN | ADS7817C TYP | ADS7817C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **ANALOG INPUT** | | | | | | | | | | | |
| Full-Scale Input Span | +In – (–In) | $-V_{REF}$ | | $+V_{REF}$ | * | | * | * | | * | V |
| Absolute Input Voltage | +In | –0.3 | | $V_{CC}$ +0.3 | * | | * | * | | * | V |
| | –In | –0.3 | | 4 | * | | * | * | | * | V |
| Capacitance | | | 15 | | | * | | | * | | pF |
| Leakage Current | | | ±1 | | | * | | | * | | µA |
| **SYSTEM PERFORMANCE** | | | | | | | | | | | |
| Resolution | | | 12 | | | * | | | * | | Bits |
| No Missing Codes | | 11 | | | 12 | | | * | | | Bits |
| Integral Linearity Error | | | ±1 | ±2 | | ±0.8 | ±2 | | ±0.5 | ±1 | LSB[1] |
| Differential Linearity Error | | | ±1 | ±2 | | ±0.7 | ±1 | | ±0.4 | ±1 | LSB |
| Offset Error | | | ±1 | ±6 | | * | * | | * | * | LSB |
| Gain Error | | | ±0.5 | ±4 | | * | * | | * | * | LSB |
| Noise | | | 63 | | | * | | | * | | µVrms |
| Common-Mode Rejection | | | 80 | | | * | | | * | | dB |
| Power Supply Rejection | | | 82 | | | * | | | * | | dB |
| **SAMPLING DYNAMICS** | | | | | | | | | | | |
| Conversion Time | | | | 12 | | | * | | | * | Clk Cycles |
| Acquisition Time | | 1.5 | | | * | | | * | | | Clk Cycles |
| Throughput Rate | | | | 200 | | | * | | | * | kHz |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | | | | |
| Total Harmonic Distortion | $V_{IN}$ = 5.0Vp-p at 1kHz | | –83 | | | * | | | * | | dB |
| | $V_{IN}$ = 5.0Vp-p at 5kHz | | –81 | | | * | | | * | | dB |
| SINAD | $V_{IN}$ = 5.0Vp-p at 1kHz | | 71 | | | * | | | * | | dB |
| Spurious Free Dynamic Range | $V_{IN}$ = 5.0Vp-p at 1kHz | | 86 | | | * | | | * | | dB |
| **REFERENCE INPUT** | | | | | | | | | | | |
| Voltage Range | | 0.1 | | 2.5 | * | | * | * | | * | V |
| Resistance | $\overline{CS}$ = $V_{CC}$ | | 5 | | | * | | | * | | GΩ |
| | $\overline{CS}$ = GND, $f_{SAMPLE}$ = 0Hz | | 5 | | | * | | | * | | GΩ |
| Current Drain | At Code FF8h | | 20 | 100 | | * | * | | * | * | µA |
| | $f_{SAMPLE}$ = 12.5kHz | | 1.3 | 20 | | * | * | | * | * | µA |
| | $\overline{CS}$ = $V_{CC}$ | | 0.001 | 3 | | * | * | | * | * | µA |
| **DIGITAL INPUT/OUTPUT** | | | | | | | | | | | |
| Logic Family | | | CMOS | | | * | | | * | | |
| Logic Levels: | | | | | | | | | | | |
| $V_{IH}$ | $I_{IH}$ = +5µA | 3 | | $+V_{CC}$ +0.3 | * | | * | * | | * | V |
| $V_{IL}$ | $I_{IL}$ = +5µA | –0.3 | | 0.8 | * | | * | * | | * | V |
| $V_{OH}$ | $I_{OH}$ = –250µA | 3.5 | | | * | | | * | | | V |
| $V_{OL}$ | $I_{OL}$ = 250µA | | | 0.4 | | | * | | | * | V |
| Data Format | | | Binary Two's Complement | | | | * | | | * | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | | | | |
| $V_{CC}$ | Specified Performance | 4.75 | | 5.25 | * | | * | * | | * | V |
| Quiescent Current | | | 460 | 800 | | * | * | | * | * | µA |
| | $f_{SAMPLE}$ = 12.5kHz[2, 3] | | 40 | | | * | | | * | | µA |
| | $f_{SAMPLE}$ = 12.5kHz[3] | | 330 | | | * | | | * | | µA |
| Power Down | $\overline{CS}$ =$V_{CC}$, $f_{SAMPLE}$ = 0Hz | | | 3 | | | * | | | * | µA |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | * | | * | °C |

* Specifications same as ADS7817.

NOTE: (1) LSB means Least Significant Bit, with $V_{REF}$ equal to +2.5V, one LSB is 1.22mV. (2) $f_{CLK}$ = 3.2MHz, $\overline{CS}$ = $V_{CC}$ for 241 clock cycles out of every 256. (3) See the Power Dissipation section for more information regarding lower sample rates.

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## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| $+V_{CC}$ | +6V |
| Analog Input | –0.3V to ($+V_{CC}$ + 0.3V) |
| Logic Input | –0.3V to ($+V_{CC}$ + 0.3V) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +125°C |
| External Reference Voltage | +5.5V |

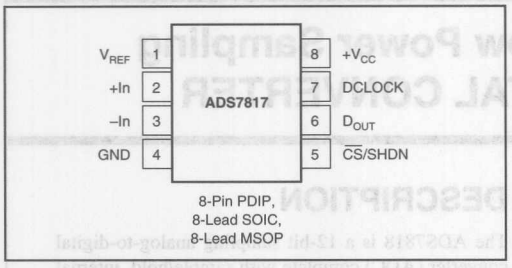
NOTE: (1) Stresses above these ratings may permanently damage the device.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION




8-Pin PDIP,
8-Lead SOIC,
8-Lead MSOP

## PIN ASSIGNMENTS

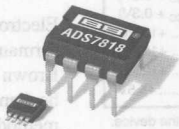
| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_{REF}$ | Reference Input. |
| 2 | +In | Non Inverting Input. |
| 3 | –In | Inverting Input. |
| 4 | GND | Ground. |
| 5 | $\overline{CS}$/SHDN | Chip Select when LOW, Shutdown Mode when HIGH. |
| 6 | $D_{OUT}$ | The serial output data word is comprised of 12 bits of data. In operation the data is valid on the falling edge of DCLOCK. The second clock pulse after the falling edge of $\overline{CS}$ enables the serial output. After one null bit the data is valid for the next 12 edges. |
| 7 | DCLOCK | Data Clock synchronizes the serial data transfer and determines conversion speed. |
| 8 | $+V_{CC}$ | Power Supply. |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | MAXIMUM DIFFERENTIAL LINEARITY ERROR (LSB) | TEMPERATURE RANGE | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|---|---|---|
| ADS7817P | ±2 | ±2 | –40°C to +85°C | Plastic DIP | 006 |
| ADS7817U | ±2 | ±2 | –40°C to +85°C | SOIC | 182 |
| ADS7817E | ±2 | ±2 | –40°C to +85°C | MSOP | 337 |
| ADS7817PB | ±2 | ±1 | –40°C to +85°C | Plastic DIP | 006 |
| ADS7817UB | ±2 | ±1 | –40°C to +85°C | SOIC | 182 |
| ADS7817EB | ±2 | ±1 | –40°C to +85°C | MSOP | 337 |
| ADS7817PC | ±1 | ±1 | –40°C to +85°C | Plastic DIP | 006 |
| ADS7817UC | ±1 | ±1 | –40°C to +85°C | SOIC | 182 |
| ADS7817EC | ±1 | ±1 | –40°C to +85°C | MSOP | 337 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# ADS7818

www.burr-brown.com/databook/ADS7818.html

# 12-Bit High Speed Low Power Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- 500kHz THROUGHPUT RATE
- 2.5V INTERNAL REFERENCE
- LOW POWER: 11mW
- SINGLE SUPPLY +5V OPERATION
- DIFFERENTIAL INPUT
- SERIAL INTERFACE
- GUARANTEED NO MISSING CODES
- 8-PIN MINI-DIP AND MSOP
- UNIPOLAR INPUT RANGE

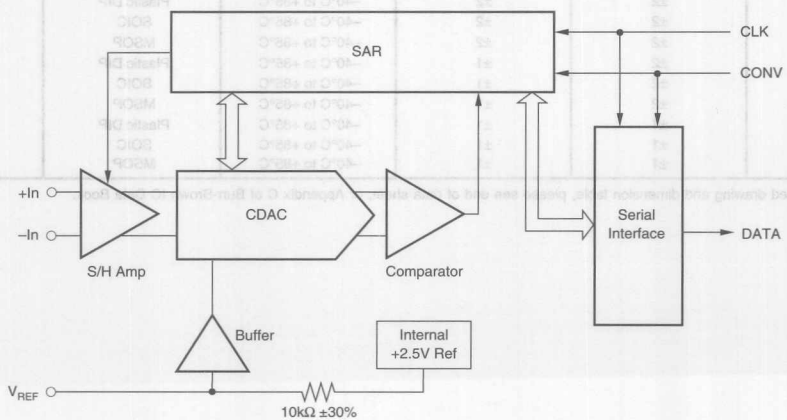
## APPLICATIONS

- BATTERY OPERATED SYSTEMS
- DIGITAL SIGNAL PROCESSING
- HIGH SPEED DATA ACQUISITION
- WIRELESS COMMUNICATION SYSTEMS

## DESCRIPTION

The ADS7818 is a 12-bit sampling analog-to-digital converter (ADC) complete with sample/hold, internal 2.5V reference, and synchronous serial interface. Typical power dissipation is 11mW at a 500kHz throughput rate. The device can be placed into a power down mode which reduces dissipation to just 2.5mW. The input range is zero to two times the reference voltage, and the internal reference can be overdriven by an external voltage.

Low power, small size, and high-speed make the ADS7818 ideal for battery operated systems such as wireless communication devices, portable multi-channel data loggers, and spectrum analyzers. The serial interface also provides low-cost isolation for remote data acquisition. The ADS7818 is available in an 8-pin plastic mini-DIP or an 8-lead MSOP package and is guaranteed over the –40°C to +85°C temperature range.




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# SPECIFICATIONS

At $T_A$ = –40°C to +85°C, $+V_{CC}$ = +5V, $f_{SAMPLE}$ = 500kHz, $f_{CLK}$ = 16 • $f_{SAMPLE}$, internal reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7818P, E MIN | ADS7818P, E TYP | ADS7818P, E MAX | ADS7818PB, EB MIN | ADS7818PB, EB TYP | ADS7818PB, EB MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **ANALOG INPUT** | | | | | | | | |
| Full-Scale Input Span[1] | +In – (–In) | 0 | | 5 | * | | * | V |
| Absolute Input Range | +In | –0.2 | | $V_{CC}$ +0.2 | * | | * | V |
| | –In | –0.2 | | +0.2 | * | | * | V |
| Capacitance | | | 15 | | | * | | pF |
| Leakage Current | | | 1 | | | * | | µA |
| **SYSTEM PERFORMANCE** | | | | | | | | |
| Resolution | | | 12 | | | * | | Bits |
| No Missing Codes | | 12 | | | * | | | Bits |
| Integral Linearity Error | | | ±1 | ±2 | | ±0.5 | ±1 | LSB[2] |
| Differential Linearity Error | | | ±0.8 | | | ±0.5 | ±1 | LSB |
| Offset Error | | | ±2 | ±5 | | ±1 | * | LSB |
| Gain Error[3] | 25°C | | ±12 | ±30 | | ±7 | ±15 | LSB |
| | –40°C to +85°C | | | ±50 | | | ±35 | LSB |
| Common-Mode Rejection | DC, 0.2Vp-p | | 70 | | | * | | dB |
| | 1MHz, 0.2Vp-p | | 50 | | | * | | dB |
| Noise | | | 150 | | | * | | µVrms |
| Power Supply Rejection | Worst Case Δ, $+V_{CC}$ = 5V ±5% | | 1.2 | | | * | | LSB |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Conversion Time | | 1.625 | | | * | | | µs |
| Acquisition Time | | 0.350 | | | * | | | µs |
| Throughput Rate | | | | 500 | | | * | kHz |
| Aperture Delay | | | 5 | | | * | | ns |
| Aperture Jitter | | | 30 | | | * | | ps |
| Step Response | | | 350 | | | * | | ns |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | |
| Signal-to-Noise Ratio | $V_{IN}$ = 5Vp-p at 100kHz | | 72 | | | * | | dB |
| Total Harmonic Distortion[4] | $V_{IN}$ = 5Vp-p at 100kHz | | –78 | –72 | | –82 | –75 | dB |
| Signal-to-(Noise+Distortion) | $V_{IN}$ = 5Vp-p at 100kHz | 68 | 70 | | 70 | 72 | | dB |
| Spurious Free Dynamic Range | $V_{IN}$ = 5Vp-p at 100kHz | 72 | 78 | | 75 | 82 | | dB |
| Usable Bandwidth | SINAD > 68dB | | 350 | | | * | | kHz |
| **REFERENCE OUTPUT** | | | | | | | | |
| Voltage | $I_{OUT}$ = 0 | 2.475 | 2.50 | 2.525 | 2.48 | * | 2.52 | V |
| Source Current[5] | Static Load | | | 50 | | | * | µA |
| Drift | $I_{OUT}$ = 0 | | 20 | | | * | | ppm/°C |
| Line Regulation | 4.75V ≤ $V_{CC}$ ≤ 5.25V | | 0.6 | | | * | | mV |
| **REFERENCE INPUT** | | | | | | | | |
| Range | | 2.0 | | 2.55 | * | | * | V |
| Resistance[6] | to Internal Reference Voltage | | 10 | | * | | * | kΩ |
| **DIGITAL INPUT/OUTPUT** | | | | | | | | |
| Logic Family | | | CMOS | | | * | | |
| Logic Levels: | | | | | | | | |
| $V_{IH}$ | $\lvert I_{IH}\rvert \le +5\mu A$ | 3.0 | | $V_{CC}$ +0.3 | * | | * | V |
| $V_{IL}$ | $\lvert I_{IL}\rvert \le +5\mu A$ | –0.3 | | 0.8 | * | | * | V |
| $V_{OH}$ | $I_{OH}$ = –500µA | 3.5 | | | * | | * | V |
| $V_{OL}$ | $I_{OL}$ = 500µA | | | 0.4 | * | | * | V |
| Data Format | | | Straight Binary | | | * | | |
| **POWER SUPPLY REQUIREMENT** | | | | | | | | |
| $+V_{CC}$ | Specified Performance | 4.75 | | 5.25 | * | | * | V |
| Quiescent Current | $f_{SAMPLE}$ = 500kHz | | 2.2 | | | * | | mA |
| | Power Down | | 0.5 | | | * | | mA |
| Power Dissipation | $f_{SAMPLE}$ = 500kHz | | 11 | 20 | | * | * | mW |
| | Power Down | | 2.5 | | | * | | mW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | °C |

NOTES: (1) Ideal input span, does not include gain or offset error. (2) LSB means Least Significant Bit, with $V_{REF}$ equal to +2.5V, one LSB is 1.22mV. (3) Measured relative to an ideal, full-scale input (+In – (–In)) of 4.999V. Thus, gain error includes the error of the internal voltage reference. (4) Calculated on the first nine harmonics of the input frequency. (5) If the internal reference is required to source current to an external load, the reference voltage will change due to the internal 10kΩ resistor. (6) Can vary ±30%.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| $+V_{CC}$ to GND | –0.3V to 6V |
| Analog Inputs to GND | –0.3V to ($V_{CC}$ + 0.3V) |
| Digital Inputs to GND | –0.3V to ($V_{CC}$ + 0.3V) |
| Power Dissipation | 325mW |
| Maximum Junction Temperature | +150°C |
| Operating Temperature Range | –40°C to +85°C |
| Storage Temperature Range | –65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

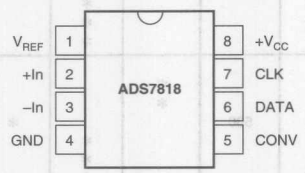
## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

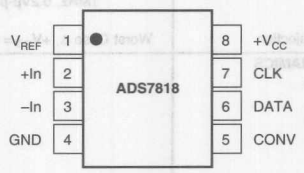
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION

Top View




8-Pin Plastic Mini-DIP




8-Lead MSOP

## PIN ASSIGNMENTS

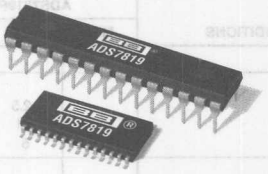
| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_{REF}$ | Reference Output. Decouple to ground with a 0.1µF ceramic capacitor and a 2.2µF tantalum capacitor. |
| 2 | +In | Non-Inverting Input. |
| 3 | –In | Inverting Input. Connect to ground or to remote ground sense point. |
| 4 | GND | Ground. |
| 5 | CONV | Convert Input. Controls the sample/hold mode, start of conversion, start of serial data transfer, type of serial transfer, and power down mode. See the Digital Interface section for more information. |
| 6 | DATA | Serial Data Output. The 12-bit conversion result is serially transmitted most significant bit first with each bit valid on the rising edge of CLK. By properly controlling the CONV input, it is possibly to have the data transmitted least significant bit first. See the Digital Interface section for more information. |
| 7 | CLK | Clock Input. Synchronizes the serial data transfer and determines conversion speed. |
| 8 | $+V_{CC}$ | Power Supply. Decouple to ground with a 0.1µF ceramic capacitor and a 10µF tantalum capacitor. |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | MAXIMUM DIFFERENTIAL LINEARITY ERROR (LSB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|---|---|---|
| ADS7818P | ±2 | N/S[2] | –40°C to +85°C | 8-Pin Mini-DIP | 006 |
| ADS7818E | ±2 | N/S[2] | –40°C to +85°C | 8-Lead MSOP | 337 |
| ADS7818PB | ±1 | ±1 | –40°C to +85°C | 8-Pin Mini-DIP | 006 |
| ADS7818EB | ±1 | ±1 | –40°C to +85°C | 8-Lead MSOP | 337 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) N/S = Not specified, typical only. However, 12 bits no missing codes is guranteed over temperature.

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# ADS7819

www.burr-brown.com/databook/ADS7819.html

# 12-Bit 800kHz Sampling CMOS ANALOG-to-DIGITAL CONVERTER

## FEATURES

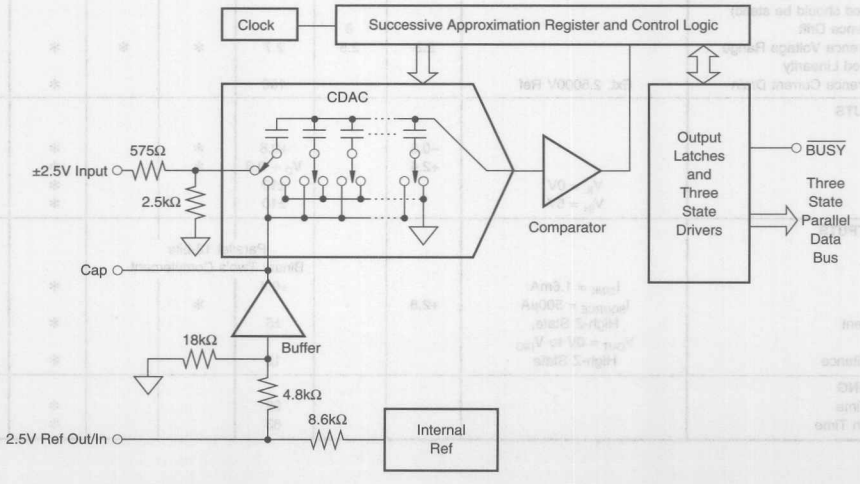
- 1.25µs THROUGHPUT TIME
- STANDARD ±2.5V INPUT RANGE
- 70dB min SINAD WITH 250kHz INPUT
- ±3/4 LSB max INL AND ±1 LSB max DNL
- INTERNAL REFERENCE
- COMPLETE WITH S/H, REF, CLOCK, ETC.
- PARALLEL DATA w/ LATCHES
- 28-PIN 0.3" PDIP AND SOIC

## DESCRIPTION

The ADS7819 is a complete 12-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 12-bit capacitor-based SAR A/D with inherent S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7819 is specified at an 800kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide a ±2.5V input range and inherent overvoltage protection up to ±25V.

The 28-pin ADS7819 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.




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At $T_A$ = –40°C to +85°C, $f_S$ = 800kHz, $+V_{DIG} = +V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference and the 50Ω input resistor shown in Figure 4b, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7819P, U | | | ADS7819PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | | 12 | | | * | Bits |
| **ANALOG INPUT** | | | | | | | | |
| Voltage Range | | | ±2.5 | | | * | | V |
| Impedance | | | 3.1 | | | * | | kΩ |
| Capacitance | | | 5 | | | * | | pF |
| **THROUGHPUT SPEED** | | | | | | | | |
| Conversion Time | | | 940 | | | * | | ns |
| Complete Cycle | Acquire & Convert | | | 1250 | | | * | ns |
| Throughput Rate | | 800 | | | * | | | kHz |
| **DC ACCURACY** | | | | | | | | |
| Integral Linearity Error | | | | ±1 | | | ±0.75 | LSB[1] |
| Differential Linearity Error | | | | ±1 | | | * | LSB |
| No Missing Codes | | | Guaranteed | | | * | | |
| Transition Noise[2] | | | 0.1 | | | * | | LSB |
| Full Scale Error[3, 4] | | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | | | ±12 | | | * | | ppm/°C |
| Full Scale Error[3, 4] | Ext. 2.5000V Ref | | | ±0.5 | | | * | % |
| Full Scale Error Drift | Ext. 2.5000V Ref | | ±12 | | | * | | ppm/°C |
| Bipolar Zero Error[3] | | | | ±8 | | | ±4 | LSB |
| Bipolar Zero Error Drift | | | ±2 | | | * | | ppm/°C |
| Power Supply Sensitivity | | | | | | | | |
| $(+V_{DIG} = +V_{ANA} = V_D)$ | +4.75V < $V_D$ < +5.25V | | | ±5 | | | * | LSB |
| | –5.25V < $-V_{ANA}$ < –4.75V | | | ±0.5 | | | * | LSB |
| **AC ACCURACY** | | | | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 250kHz | 74 | 84 | | 77 | 85 | | dB[5] |
| Total Harmonic Distortion | $f_{IN}$ = 250kHz | | –82 | –74 | | –83 | –77 | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 250kHz | 68 | 71 | | 70 | * | | dB |
| Signal-to-Noise | $f_{IN}$ = 250kHz | 68 | 71 | | 70 | * | | dB |
| Usable Bandwidth[6] | | | 1.5 | | | * | | MHz |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Aperture Delay | | | 20 | | | * | | ns |
| Aperture Jitter | | | 10 | | | * | | ps |
| Transient Response | FS Step | | 180 | | | * | | ns |
| Overvoltage Recovery[7] | | | 250 | | | * | | ns |
| **REFERENCE** | | | | | | | | |
| Internal Reference Voltage | | 2.48 | 2.5 | 2.52 | * | * | * | V |
| Internal Reference DC Source Current (External load should be static) | | | 100 | | | * | | µA |
| Internal Reference Drift | | | 6 | | | | | ppm/°C |
| External Reference Voltage Range For Specified Linearity | | 2.3 | 2.5 | 2.7 | * | * | * | V |
| External Reference Current Drain | Ext. 2.5000V Ref | | | 100 | | | * | µA |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Levels | | | | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | * | | * | V |
| $V_{IH}$ | | +2.4 | | $V_D$ + 0.3 | * | | * | V |
| $I_{IL}$ | $V_{IL}$ = 0V | | | ±10 | | | * | µA |
| $I_{IH}$ | $V_{IH}$ = 5V | | | ±10 | | | * | µA |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Data Format | | | | Parallel 12-bits | | | | |
| Data Coding | | | | Binary Two's Complement | | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +2.8 | | | * | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_{DIG}$ | | | ±5 | | | * | µA |
| Output Capacitance | High-Z State | | | 15 | | | * | pF |
| **DIGITAL TIMING** | | | | | | | | |
| Bus Access Time | | | | 62 | | | * | ns |
| Bus Relinquish Time | | | | 83 | | | * | ns |

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At $T_A$ = –40°C to +85°C, $f_S$ = 800kHz, $+V_{DIG} = +V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference and the 50Ω input resistor shown in Figure 4b, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7819P, U | | | ADS7819PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **POWER SUPPLIES** | | | | | | | | |
| Specified Performance | | | | | | | | |
| $+V_{DIG} = +V_{ANA}$ | | +4.75 | +5 | +5.25 | * | * | * | V |
| $-V_{ANA}$ | | –5.25 | –5 | –4.75 | * | * | * | V |
| $+I_{DIG}$ | | | +16 | | | * | | mA |
| $+I_{ANA}$ | | | +16 | | | * | | mA |
| $-I_{ANA}$ | | | –13 | | | * | | mA |
| Derated Performance | | | | | | | | |
| $+V_{DIG} = +V_{ANA}$ | | +4.5 | +5 | +5.5 | * | * | * | V |
| $-V_{ANA}$ | | –5.5 | –5 | –4.5 | * | * | * | V |
| Power Dissipation | $f_S$ = 800kHz | | 225 | 275 | | | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | °C |
| Derated Performance | | –55 | | +125 | * | | * | °C |
| Storage | | –65 | | +150 | * | | * | °C |
| Thermal Resistance ($\theta_{JA}$) | | | | | | | | |
| Plastic DIP | | | 75 | | | * | | °C/W |
| SOIC | | | 75 | | | * | | °C/W |

* Specifications same as ADS7819P, U.

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, ±2.5V input ADS7819, one LSB is 1.22mV. (2) Typical rms noise at worst case transitions and temperatures. (3) Measured with 50Ω in series with analog input. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±2.5V input. (6) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input over voltage.

## ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $V_{IN}$ ..... ±25V
REF ..... $+V_{ANA}$ +0.3V to AGND2 –0.3V
CAP ..... Indefinite Short to AGND2
Momentary Short to $+V_{ANA}$
Ground Voltage Differences: DGND, AGND1, AGND2 ..... ±0.3V
$+V_{ANA}$ ..... +7V
$+V_{DIG}$ to $+V_{ANA}$ ..... +0.3V
$+V_{DIG}$ ..... 7V
$-V_{ANA}$ ..... –7V
Digital Inputs ..... –0.3V to $+V_{DIG}$ +0.3V
Maximum Junction Temperature ..... +165°C
Internal Power Dissipation ..... 825mW
Lead Temperature (soldering, 10s) ..... +300°C

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

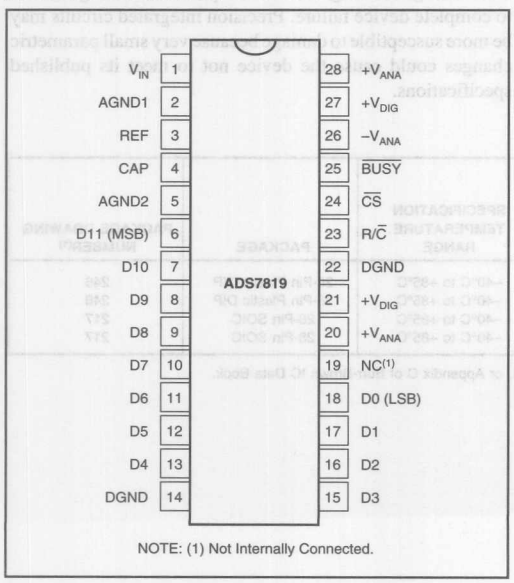
| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|---|---|---|
| ADS7819P | ±1 | 68 | –40°C to +85°C | 28-Pin Plastic DIP | 246 |
| ADS7819PB | ±0.75 | 70 | –40°C to +85°C | 28-Pin Plastic DIP | 246 |
| ADS7819U | ±1 | 68 | –40°C to +85°C | 28-Pin SOIC | 217 |
| ADS7819UB | ±0.75 | 70 | –40°C to +85°C | 28-Pin SOIC | 217 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN ASSIGNMENTS

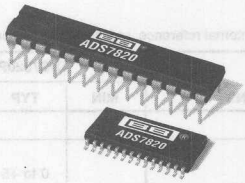
| PIN # | NAME | DIGITAL I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $V_{IN}$ | | Analog Input. Connect via 50Ω to analog input. Full-scale input range is ±2.5V. |
| 2 | AGND1 | | Analog Ground. Used internally as ground reference point. Minimal current flow. |
| 3 | REF | | Reference Input/Output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, decouple to ground with a 0.1µF ceramic capacitor. |
| 4 | CAP | | Reference Buffer Output. 10µF tantalum capacitor to ground. Nominally +2V. |
| 5 | AGND2 | | Analog Ground. |
| 6 | D11 (MSB) | O | Data Bit 11. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 7 | D10 | O | Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 8 | D9 | O | Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 9 | D8 | O | Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 10 | D7 | O | Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 11 | D6 | O | Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 12 | D5 | O | Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 13 | D4 | O | Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 14 | DGND | | Digital Ground. |
| 15 | D3 | O | Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 16 | D2 | O | Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 17 | D1 | O | Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 18 | D0 (LSB) | O | Data Bit 0. Least Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 19 | | | Not internally connected. |
| 20 | $+V_{ANA}$ | | Analog Positive Supply Input. Nominally +5V. Connect directly to pins 21, 27 and 28. |
| 21 | $+V_{DIG}$ | | Digital Supply Input. Nominally +5V. Connect directly to pins 20, 27 and 28. |
| 22 | DGND | | Digital ground. |
| 23 | R/$\overline{C}$ | I | Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW and no conversion in progress, a rising edge on R/$\overline{C}$ enables the output data bits. |
| 24 | $\overline{CS}$ | I | Chip Select. With R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH and no conversion in progress, a falling edge on $\overline{CS}$ will enable the output data bits. |
| 25 | $\overline{BUSY}$ | O | Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output register. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, output data will be valid when BUSY rises, so that the rising edge can be used to latch the data. |
| 26 | $-V_{ANA}$ | | Analog Negative Supply Input. Nominally –5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors. |
| 27 | $+V_{DIG}$ | | Digital Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 28. |
| 28 | $+V_{ANA}$ | | Analog Positive Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 27, and decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors. |

## PIN CONFIGURATION




NOTE: (1) Not Internally Connected.

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# ADS7820

www.burr-brown.com/databook/ADS7820.html

# 12-Bit 10μs Sampling CMOS ANALOG-to-DIGITAL CONVERTER

## FEATURES

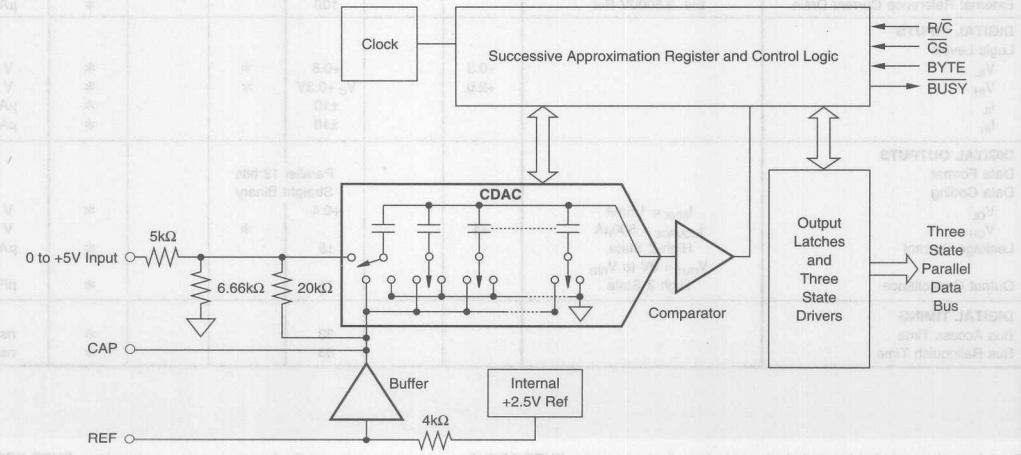
- 100kHz min SAMPLING RATE
- 0 to +5V INPUT RANGE
- 72dB min SINAD WITH 45kHz INPUT
- ±1/2 LSB max INL AND DNL
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 16-BIT ADS7821
- USES INTERNAL OR EXTERNAL REFERENCE
- COMPLETE WITH S/H, REF, CLOCK, ETC.
- FULL PARALLEL DATA OUTPUT
- 100mW max POWER DISSIPATION
- 28-PIN 0.3" PLASTIC DIP AND SOIC

## DESCRIPTION

The ADS7820 is a complete 12-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 12-bit, capacitor-based SAR A/D with S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7820 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide a 0 to +5V input range, with power dissipation under 100mW.

The 28-pin ADS7820 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

$T_A$ = –40°C to +85°C, $f_S$ = 100kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7820P, U | | | ADS7820PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | | 12 | | | * | Bits |
| **ANALOG INPUT** | | | | | | | | |
| Voltage Ranges | | | 0 to +5 | | | * | | V |
| Impedance | | | 10 | | | * | | kΩ |
| Capacitance | | | 35 | | | * | | pF |
| **THROUGHPUT SPEED** | | | | | | | | |
| Conversion Time | | | 5.7 | 8 | | * | * | µs |
| Complete Cycle | Acquire and Convert | | | 10 | | | * | µs |
| Throughput Rate | | 100 | | | * | | | kHz |
| **DC ACCURACY** | | | | | | | | |
| Integral Linearity Error | | | | ±1.0 | | | ±0.5 | LSB[1] |
| Differential Linearity Error | | | | ±1.0 | | | ±0.5 | LSB |
| No Missing Codes | | | Guaranteed | | | * | | Bits |
| Transition Noise[2] | | | 0.1 | | | * | | LSB |
| Full Scale Error[3,4] | | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | | | ±7 | | | ±5 | | ppm/°C |
| Full Scale Error[3,4] | Ext. 2.5000V Ref | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | Ext. 2.5000V Ref | | ±2 | | | * | | ppm/°C |
| Offset Error | | | | ±8 | | | ±4 | mV |
| Offset Error Drift | | | ±2 | | | * | | ppm/°C |
| Power Supply Sensitivity ($V_{DIG}$ = $V_{ANA}$ = $V_D$) | +4.75V < $V_D$ < +5.25V | | | ±0.75 | | | ±0.5 | LSB |
| **AC ACCURACY** | | | | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 45kHz | 80 | | | * | | | dB[5] |
| Total Harmonic Distortion | $f_{IN}$ = 45kHz | | | –80 | | | * | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 45kHz | 70 | | | 72 | | | dB |
| Signal-to-Noise | $f_{IN}$ = 45kHz | 70 | | | 72 | | | dB |
| Full-Power Bandwidth[6] | | | 250 | | | * | | kHz |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Aperture Delay | | | 40 | | | * | | ns |
| Transient Response | FS Step | | | 2 | | | * | µs |
| Overvoltage Recovery[7] | | | 150 | | | * | | ns |
| **REFERENCE** | | | | | | | | |
| Internal Reference Voltage | | 2.48 | 2.5 | 2.52 | * | * | * | V |
| Internal Reference Source Current (Must use external buffer.) | | | 1 | | | * | | µA |
| External Reference Voltage Range for Specified Linearity | | 2.3 | 2.5 | 2.7 | * | * | * | V |
| External Reference Current Drain | Ext. 2.5000V Ref | | | 100 | | | * | µA |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Levels | | | | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | * | | * | V |
| $V_{IH}$ | | +2.0 | | $V_D$ +0.3V | * | | * | V |
| $I_{IL}$ | | | | ±10 | | | * | µA |
| $I_{IH}$ | | | | ±10 | | | * | µA |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Data Format | | | | Parallel 12 bits | | | | |
| Data Coding | | | | Straight Binary | | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +4 | | | * | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_{DIG}$ | | | ±5 | | | * | µA |
| Output Capacitance | High-Z State | | | 15 | | | * | pF |
| **DIGITAL TIMING** | | | | | | | | |
| Bus Access Time | | | | 83 | | | * | ns |
| Bus Relinquish Time | | | | 83 | | | * | ns |

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

# SPECIFICATIONS (CONT)

## ELECTRICAL

$T_A$ = –40°C to +85°C, $f_S$ = 100kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, using internal reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7820P, U | | | ADS7820PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **POWER SUPPLIES** | | | | | | | | |
| Specified Performance | | | | | | | | |
| $V_{DIG}$ | Must be ≤ $V_{ANA}$ | +4.75 | +5 | +5.25 | * | * | * | V |
| $V_{ANA}$ | | +4.75 | +5 | +5.25 | * | * | * | V |
| $+I_{DIG}$ | | | 0.3 | | | * | | mA |
| $+I_{ANA}$ | | | 16 | | | * | | mA |
| Power Dissipation | $f_S$ = 100kHz | | | 100 | | | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | °C |
| Derated Performance | | –55 | | +125 | * | | * | °C |
| Storage | | –65 | | +150 | * | | * | °C |
| Thermal Resistance ($\theta_{JA}$) | | | | | | | | |
| Plastic DIP | | | 75 | | | * | | °C/W |
| SOIC | | | 75 | | | * | | °C/W |

* Specifications same as ADS7820P, U.

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, 0 to +5V input ADS7820, one LSB is 1.22mV. (2) Typical rms noise at worst case transitions and temperatures. (3) Adjustable to zero with external potentiometer as shown in Figure 4b. (4) Full scale error is the worst case of Full Scale untrimmed deviation from ideal last code transition divided by the transition voltage and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $V_{IN}$ | –0.7V to $+V_{ANA}$ +0.3V |
| REF | $+V_{ANA}$ +0.3V to AGND2 –0.3V |
| CAP | Indefinite Short to AGND2 |
| | Momentary Short to $V_{ANA}$ |
| Ground Voltage Differences: DGND, AGND1, AGND2 | ±0.3V |
| $V_{ANA}$ | 7V |
| $V_{DIG}$ to $V_{ANA}$ | +0.3V |
| $V_{DIG}$ | 7V |
| Digital Inputs | –0.3V to $+V_{DIG}$ +0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PACKAGE INFORMATION

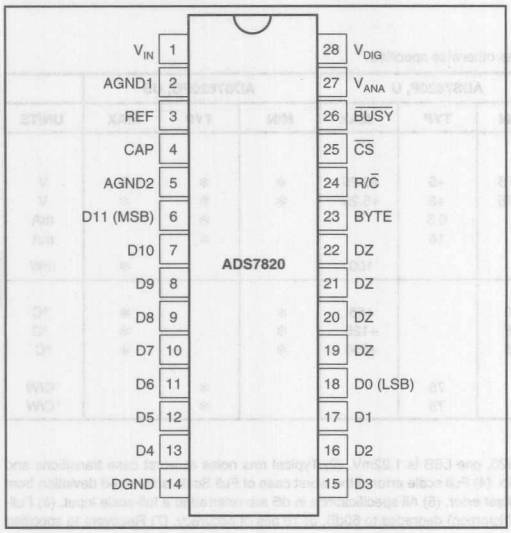
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ADS7820P | Plastic DIP | 246 |
| ADS7820PB | Plastic DIP | 246 |
| ADS7820U | SOIC | 217 |
| ADS7820UB | SOIC | 217 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

## ORDERING INFORMATION

| PRODUCT | MAXIMUM LINEARITY ERROR (LSB) | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE |
|---|---|---|---|---|
| ADS7820P | ±1.0 | 70 | –40°C to +85°C | Plastic DIP |
| ADS7820PB | ±0.5 | 72 | –40°C to +85°C | Plastic DIP |
| ADS7820U | ±1.0 | 70 | –40°C to +85°C | SOIC |
| ADS7820UB | ±0.5 | 72 | –40°C to +85°C | SOIC |

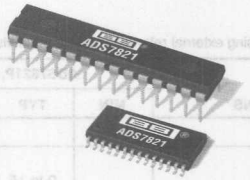
## PIN CONFIGURATION




## PIN ASSIGNMENTS

| PIN # | NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_{IN}$ | Analog Input. Full-scale input range is 0 to +5V. |
| 2 | AGND1 | Analog Ground. Used internally as ground reference point. |
| 3 | REF | Reference Input/Output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, connect to ground with a 2.2µF Tantalum capacitor. |
| 4 | CAP | Reference Buffer Capacitor. 2.2µF Tantalum to ground. |
| 5 | AGND2 | Analog Ground. |
| 6 | D11 (MSB) | Data Bit 11. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 7 | D10 | Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 8 | D9 | Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 9 | D8 | Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 10 | D7 | Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 11 | D6 | Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 12 | D5 | Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 13 | D4 | Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 14 | DGND | Digital Ground. |
| 15 | D3 | Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 16 | D2 | Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 17 | D1 | Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 18 | D0 (LSB) | Data Bit 0. Lease Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 19 | DZ | Data Zero. LOW when $\overline{CS}$ LOW and R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 20 | DZ | Data Zero. LOW when $\overline{CS}$ LOW and R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 21 | DZ | Data Zero. LOW when $\overline{CS}$ LOW and R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 22 | DZ | Data Zero. LOW when $\overline{CS}$ LOW and R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 23 | BYTE | Byte Select. With BYTE LOW, data will be output as indicated above, causing pin 6 (D11) to output the MSB, and pin 18 (D0) to output the LSB. Pins 19 to 22 will output LOWs. With BYTE HIGH, the top and bottom 8 bits of data will be switched, so that pin 6 outputs data bit 3, pin 9 outputs data bit 0 (LSB), pin 10 to 13 output LOWs, pin 15 outputs data bit 11 (MSB) and pin 22 outputs data bit 4. |
| 24 | R/$\overline{C}$ | Read/Convert input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the output data bits. |
| 25 | $\overline{CS}$ | Chip Select. Internally OR'd with R/$\overline{C}$. With R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH, a falling edge on $\overline{CS}$ will enable the output data bits. |
| 26 | $\overline{BUSY}$ | Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output register. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data. $\overline{CS}$ or R/$\overline{C}$ must be high when $\overline{BUSY}$ rises, or another conversion will start, without time for signal acquisition. |
| 27 | $V_{ANA}$ | Analog Supply Input. Nominally +5V. Connect directly to pin 28. Decouple to ground with 0.1µF ceramic and 10µF Tantalum capacitors. |
| 28 | $V_{DIG}$ | Digital Supply Input. Nominally +5V. Connect directly to pin 27. Must be ≤ $V_{ANA}$. |

BURR-BROWN®



# ADS7821

www.burr-brown.com/databook/ADS7821.html



# 16-Bit 10μs Sampling CMOS ANALOG-to-DIGITAL CONVERTER

## FEATURES

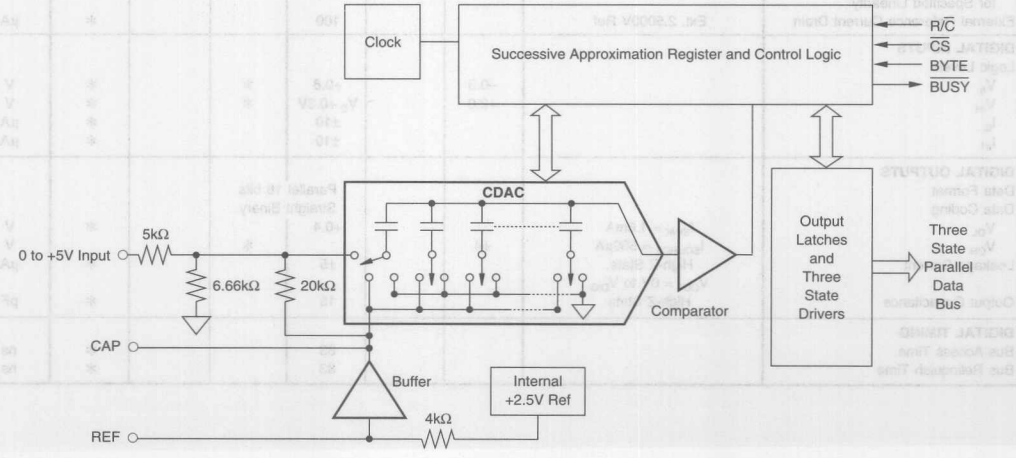
- 100kHz min SAMPLING RATE
- 0 to +5V INPUT RANGE
- 86dB min SINAD WITH 20kHz INPUT
- DNL: 16-bits "No Missing Codes"
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 12-BIT ADS7820
- USES INTERNAL OR EXTERNAL REFERENCE
- FULL PARALLEL DATA OUTPUT
- 100mW max POWER DISSIPATION
- 28-PIN 0.3" PLASTIC DIP AND SOIC

## DESCRIPTION

The ADS7821 is a complete 16-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, SAR A/D with S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7821 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide a 0 to +5V input range, with power dissipation under 100mW.

The 28-pin ADS7821 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the –25°C to +85°C range.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

$T_A$ = –25°C to +85°C, $f_S$ = 100kHz, $V_{DIG}$ = $V_{ANA}$ = $V_D$ = +5V, using external reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7821P, U | | | ADS7821PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | | 16 | | | * | Bits |
| **ANALOG INPUT** | | | | | | | | |
| Voltage Range | | | 0 to +5 | | | * | | V |
| Impedance | | | 10 | | | * | | kΩ |
| Capacitance | | | 35 | | | * | | pF |
| **THROUGHPUT SPEED** | | | | | | | | |
| Conversion Cycle | Acquire and Convert | | | 10 | | | * | µs |
| Throughput Rate | | 100 | | * | | | | kHz |
| **DC ACCURACY** | | | | | | | | |
| Integral Linearity Error | | | | ±4 | | | ±3 | LSB[1] |
| No Missing Codes | | 15 | | | 16 | | | Bits |
| Transition Noise[2] | | | 0.9 | | | * | | LSB |
| Full Scale Error[3,4] | | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | | | ±2 | | | * | | ppm/°C |
| Full Scale Error[3,4] | Internal Reference | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | Internal Reference | | ±7 | | | ±5 | | ppm/°C |
| Offset Error | | | | ±8 | | | ±4 | mV |
| Offset Error Drift | | | ±2 | | | * | | ppm/°C |
| Power Supply Sensitivity ($V_{DIG}$ = $V_{ANA}$ = $V_D$) | +4.75V < $V_D$ < +5.25V | | | ±12 | | | ±8 | LSB |
| **AC ACCURACY** | | | | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 20kHz | 90 | | | 94 | | | dB[5] |
| Total Harmonic Distortion | $f_{IN}$ = 20kHz | | | –90 | | | –94 | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 20kHz | 83 | | | 86 | | | dB |
| | $f_{IN}$ = –60dB Input | | 28 | | | 30 | | dB |
| Signal-to-Noise | $f_{IN}$ = 20kHz | 83 | | | 86 | | | dB |
| Full-Power Bandwidth[6] | | | 250 | | | * | | kHz |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Aperture Delay | | | 40 | | | * | | ns |
| Transient Response | FS Step | | | 2 | | | * | µs |
| Overvoltage Recovery[7] | | | 150 | | | * | | ns |
| **REFERENCE** | | | | | | | | |
| Internal Reference Voltage | | 2.48 | 2.5 | 2.52 | * | * | * | V |
| Internal Reference Source Current (Must use external buffer) | | | 1 | | | * | | µA |
| Internal Reference Drift | | | 8 | | | * | | ppm/°C |
| External Reference Voltage Range for Specified Linearity | | 2.3 | 2.5 | 2.7 | * | * | * | V |
| External Reference Current Drain | Ext. 2.5000V Ref | | | 100 | | | * | µA |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Levels | | | | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | * | | * | V |
| $V_{IH}$ | | +2.0 | | $V_D$ +0.3V | * | | * | V |
| $I_{IL}$ | | | | ±10 | | | * | µA |
| $I_{IH}$ | | | | ±10 | | | * | µA |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Data Format | | | | Parallel 16 bits | | | | |
| Data Coding | | | | Straight Binary | | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +4 | | | * | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_{DIG}$ | | | ±5 | | | * | µA |
| Output Capacitance | High-Z State | | | 15 | | | * | pF |
| **DIGITAL TIMING** | | | | | | | | |
| Bus Access Time | | | | 83 | | | * | ns |
| Bus Relinquish Time | | | | 83 | | | * | ns |

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# SPECIFICATIONS (CONT)

## ELECTRICAL

$T_A$ = –25°C to +85°C, $f_S$ = 100kHz, $V_{DIG} = V_{ANA} = V_D$ = +5V, using external reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7821P, U | | | ADS7821PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **POWER SUPPLIES** | | | | | | | | |
| Specified Performance | | | | | | | | |
| $V_{DIG}$ | Must be ≤ $V_{ANA}$ | +4.75 | +5 | +5.25 | * | * | * | V |
| $V_{ANA}$ | | +4.75 | +5 | +5.25 | * | * | * | V |
| $I_{DIG}$ | | | 0.3 | | | * | | mA |
| $I_{ANA}$ | | | 16 | | | * | | mA |
| Power Dissipation | $f_S$ = 100kHz | | 100 | | | | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –25 | | +85 | * | | * | °C |
| Derated Performance | | –55 | | +125 | * | | * | °C |
| Storage | | –65 | | +150 | * | | * | °C |
| Thermal Resistance ($\theta_{JA}$) | | | | | | | | |
| Plastic DIP | | | 75 | | | * | | °C/W |
| SOIC | | | 75 | | | * | | °C/W |

* Specifications same as ADS7821P, U.

NOTES: (1) LSB means Least Significant Bit. For the 16-bit, 0 to +5V input ADS721, one LSB is 76μV. (2) Typical rms noise at worst case transitions and temperatures. (3) Adjustable to zero with external potentiometer as shown in Figure 6a. (4) Full scale error is the worst case of Full Scale untrimmed deviation from ideal last code transition divided by the transition voltage and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

## ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $V_{IN}$ ..... –0.7V to $V_{ANA}$ +0.3V
REF ..... AGND2 –0.3V to $+V_{ANA}$ +0.3V
CAP ..... Indefinite Short to AGND2, Momentary Short to $V_{ANA}$
Ground Voltage Differences: DGND, AGND1, AGND2 ..... ±0.3V
$V_{ANA}$ ..... 7V
$V_{DIG}$ to $V_{ANA}$ ..... +0.3V
$V_{DIG}$ ..... 7V
Digital Inputs ..... –0.3V to $+V_{DIG}$ +0.3V
Maximum Junction Temperature ..... +165°C
Internal Power Dissipation ..... 825mW
Lead Temperature (soldering, 10s) ..... +300°C

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ADS7821P | Plastic DIP | 246 |
| ADS7821PB | Plastic DIP | 246 |
| ADS7821U | SOIC | 217 |
| ADS7821UB | SOIC | 217 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

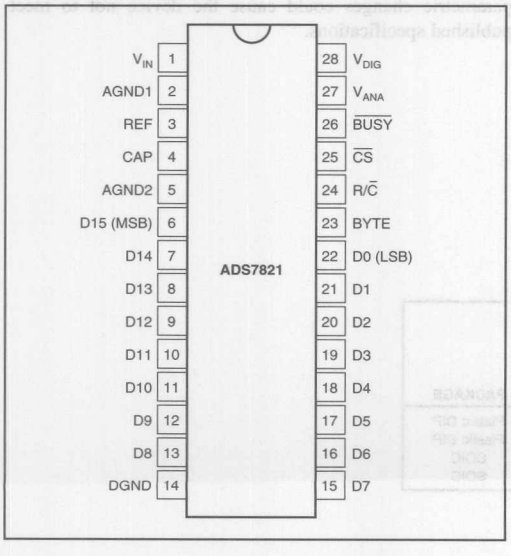
## ORDERING INFORMATION

| PRODUCT | MAXIMUM LINEARITY ERROR (LSB) | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE |
|---|---|---|---|---|
| ADS7821P | ±4 | 83 | –25°C to +85°C | Plastic DIP |
| ADS7821PB | ±3 | 86 | –25°C to +85°C | Plastic DIP |
| ADS7821U | ±4 | 83 | –25°C to +85°C | SOIC |
| ADS7821UB | ±3 | 86 | –25°C to +85°C | SOIC |

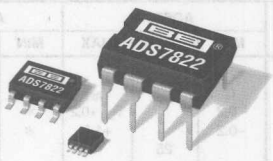
| PIN # | NAME | DIGITAL I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $V_{IN}$ | | Analog Input. |
| 2 | AGND1 | | Analog Ground. Used internally as ground reference point. |
| 3 | REF | | Reference Input/Output. 2.2µF tantalum capacitor to ground. |
| 4 | CAP | | Reference Buffer Capacitor. 2.2µF tantalum capacitor to ground. |
| 5 | AGND2 | | Analog Ground. |
| 6 | D15 (MSB) | O | Data Bit 15. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 7 | D14 | O | Data Bit 14. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 8 | D13 | O | Data Bit 13. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 9 | D12 | O | Data Bit 12. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 10 | D11 | O | Data Bit 11. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 11 | D10 | O | Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 12 | D9 | O | Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 13 | D8 | O | Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 14 | DGND | | Digital Ground. |
| 15 | D7 | O | Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 16 | D6 | O | Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 17 | D5 | O | Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 18 | D4 | O | Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 19 | D3 | O | Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 20 | D2 | O | Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 21 | D1 | O | Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 22 | D0 (LSB) | O | Data Bit 0. Lease Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW. |
| 23 | BYTE | I | Swaps Pins 6 through 13 with Pins 15 through 22 when HIGH. See Figures 2 and 5. |
| 24 | R/$\overline{C}$ | I | With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output. |
| 25 | $\overline{CS}$ | I | Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ initiates a new conversion. |
| 26 | $\overline{BUSY}$ | O | At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated. |
| 27 | $V_{ANA}$ | | Analog Supply Input. Nominally +5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors. |
| 28 | $V_{DIG}$ | | Digital Supply Input. Nominally +5V. Connect directly to pin 27. Must be ≤ $V_{ANA}$. |

TABLE I. Pin Assignments.

## PIN CONFIGURATION



BURR-BROWN®




# ADS7822

www.burr-brown.com/databook/ADS7822.html



# 12-Bit High Speed 2.7V Micro Power Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- 75kHz SAMPLING RATE
- MICRO POWER:
  0.54mW at 75kHz
  0.06mW at 7.5kHz
- POWER DOWN: 3μA max
- 8-PIN MINI-DIP, SOIC, AND MSOP
- DIFFERENTIAL INPUT
- SERIAL INTERFACE

## APPLICATIONS

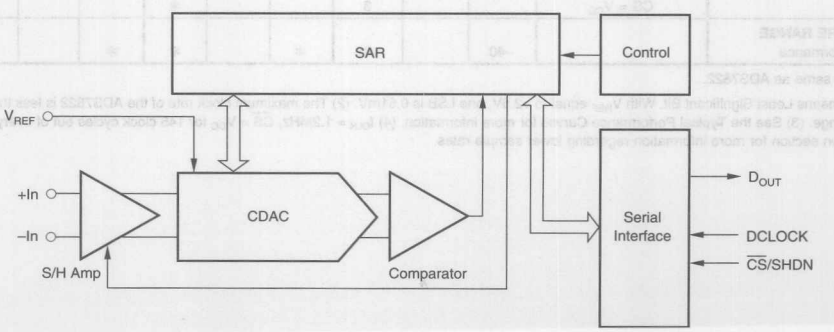
- BATTERY OPERATED SYSTEMS
- REMOTE DATA ACQUISITION
- ISOLATED DATA ACQUISITION
- SIMULTANEOUS SAMPLING, MULTI-CHANNEL SYSTEMS

## DESCRIPTION

The ADS7822 is a 12-bit sampling analog-to-digital converter with guaranteed specifications over a 2.7V to 3.6V supply range. It requires very little power even when operating at the full 75kHz rate. At lower conversion rates, the high speed of the device enables it to spend most of its time in the power down mode—the power dissipation is less than 60μW at 7.5kHz.

The ADS7822 also features operation from 2.0V to 5V, a synchronous serial interface, and a differential input. The reference voltage can be set to any level within the range of 50mV to $V_{CC}$.

Ultra low power and small size make the ADS7822 ideal for battery operated systems. It is also a perfect fit for remote data acquisition modules, simultaneous multi-channel systems, and isolated data acquisition. The ADS7822 is available in an 8-pin plastic mini-DIP, an 8-lead SOIC, or an 8-lead MSOP package.




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At –40°C to +85°C, +$V_{CC}$ = +2.7V, $V_{REF}$ = +2.5V, $f_{SAMPLE}$ = 75kHz, $f_{CLK}$ = 16 • $f_{SAMPLE}$, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7822 | | | ADS7822B | | | ADS7822C | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ANALOG INPUT** | | | | | | | | | | | |
| Full-Scale Input Span | +In – (–In) | 0 | | $V_{REF}$ | * | | * | * | | * | V |
| Absolute Input Range | +In | –0.2 | | $V_{CC}$ +0.2 | * | | * | * | | * | V |
| | –In | –0.2 | | +1.0 | * | | * | * | | * | V |
| Capacitance | | | 25 | | | * | | | * | | pF |
| Leakage Current | | | ±1 | | | * | | | * | | µA |
| **SYSTEM PERFORMANCE** | | | | | | | | | | | |
| Resolution | | | 12 | | | * | | | * | | Bits |
| No Missing Codes | | 11 | | | 12 | | | * | | | Bits |
| Integral Linearity Error | | | ±0.5 | ±2 | | ±0.5 | ±1 | | ±0.25 | ±0.75 | LSB[1] |
| Differential Linearity Error | | | ±0.5 | ±2 | | ±0.5 | ±1 | | ±0.25 | ±0.75 | LSB |
| Offset Error | | | | ±3 | | | * | | | ±1 | LSB |
| Gain Error | | | | ±3 | | | * | | | ±1 | LSB |
| Noise | | | 33 | | | * | | | * | | µVrms |
| Power Supply Rejection | | | 82 | | | * | | | * | | dB |
| **SAMPLING DYNAMICS** | | | | | | | | | | | |
| Conversion Time | | | | 12 | | | * | | | * | Clk Cycles |
| Acquisition Time | | 1.5 | | | * | | | * | | | Clk Cycles |
| Throughput Rate | | | | 75 | | | * | | | * | kHz |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | | | | |
| Total Harmonic Distortion | $V_{IN}$ = 2.5Vp-p at 1kHz | | –82 | | | * | | | * | | dB |
| SINAD | $V_{IN}$ = 2.5Vp-p at 1kHz | | 71 | | | * | | | * | | dB |
| Spurious Free Dynamic Range | $V_{IN}$ = 2.5Vp-p at 1kHz | | 86 | | | * | | | * | | dB |
| **REFERENCE INPUT** | | | | | | | | | | | |
| Voltage Range | | 0.05 | | $V_{CC}$ | * | | * | * | | * | V |
| Resistance | $\overline{CS}$ = GND, $f_{SAMPLE}$ = 0Hz | | 5 | | | * | | | * | | GΩ |
| | $\overline{CS}$ = $V_{CC}$ | | 5 | | | * | | | * | | GΩ |
| Current Drain | At Code 710h | | 8 | 40 | | * | * | | * | * | µA |
| | $f_{SAMPLE}$ = 7.5kHz | | 0.8 | | | * | | | * | | µA |
| | $\overline{CS}$ = $V_{CC}$ | | 0.001 | 3 | | * | * | | * | * | µA |
| **DIGITAL INPUT/OUTPUT** | | | | | | | | | | | |
| Logic Family | | | CMOS | | | * | | | * | | |
| Logic Levels: | | | | | | | | | | | |
| $V_{IH}$ | $I_{IH}$ = +5µA | 2.0 | | 5.5 | * | | * | * | | * | V |
| $V_{IL}$ | $I_{IL}$ = +5µA | –0.3 | | 0.8 | * | | * | * | | * | V |
| $V_{OH}$ | $I_{OH}$ = –250µA | 2.1 | | | * | | | * | | | V |
| $V_{OL}$ | $I_{OL}$ = 250µA | | | 0.4 | | | * | | | * | V |
| Data Format | | | Straight Binary | | | * | | | * | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | | | | |
| $V_{CC}$ | Specified Performance | 2.7 | | 3.6 | * | | * | * | | * | V |
| | See Notes 2 and 3 | 2.0 | | 2.7 | * | | * | * | | * | V |
| | See Note 3 | 3.6 | | 5.25 | * | | * | * | | * | V |
| Quiescent Current | | | 200 | 325 | | * | * | | * | * | µA |
| | $f_{SAMPLE}$ = 7.5kHz[4,5] | | 20 | | | * | | | * | | µA |
| | $f_{SAMPLE}$ = 7.5kHz[5] | | 180 | | | * | | | * | | µA |
| Power Down | $\overline{CS}$ = $V_{CC}$ | | | 3 | | | * | | | * | µA |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | * | | * | °C |

* Specifications same as ADS7822.

Notes: (1) LSB means Least Significant Bit. With $V_{REF}$ equal to +2.5V, one LSB is 0.61mV. (2) The maximum clock rate of the ADS7822 is less than 1.2MHz in this power supply range. (3) See the Typical Performance Curves for more information. (4) $f_{CLK}$ = 1.2MHz, $\overline{CS}$ = $V_{CC}$ for 145 clock cycles out of every 160. (5) See the Power Dissipation section for more information regarding lower sample rates.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| $V_{CC}$ | +6V |
| Analog Input | –0.3V to ($V_{CC}$ + 0.3V) |
| Logic Input | –0.3V to 6V |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +125°C |
| External Reference Voltage | +5.5V |

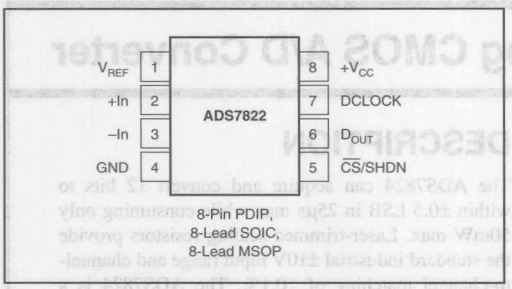
NOTE: (1) Stresses above these ratings may permanently damage the device.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION




8-Pin PDIP,
8-Lead SOIC,
8-Lead MSOP

## PIN ASSIGNMENTS

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_{REF}$ | Reference Input. |
| 2 | +In | Non Inverting Input. |
| 3 | –In | Inverting Input. Connect to ground or to remote ground sense point. |
| 4 | GND | Ground. |
| 5 | $\overline{CS}$/SHDN | Chip Select when LOW, Shutdown Mode when HIGH. |
| 6 | $D_{OUT}$ | The serial output data word is comprised of 12 bits of data. In operation the data is valid on the falling edge of DCLOCK. The second clock pulse after the falling edge of $\overline{CS}$ enables the serial output. After one null bit the data is valid for the next 12 edges. |
| 7 | DCLOCK | Data Clock synchronizes the serial data transfer and determines conversion speed. |
| 8 | +$V_{CC}$ | Power Supply. |

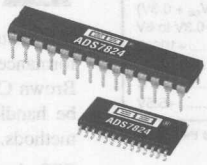
## PACKAGE/ORDERING INFORMATION

| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | MAXIMUM DIFFERENTIAL LINEARITY ERROR (LSB) | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|---|---|
| ADS7822P | ±2 | ±2 | Plastic DIP | 006 |
| ADS7822U | ±2 | ±2 | SOIC | 182 |
| ADS7822E | ±2 | ±2 | MSOP | 337 |
| ADS7822PB | ±1 | ±1 | Plastic DIP | 006 |
| ADS7822UB | ±1 | ±1 | SOIC | 182 |
| ADS7822EB | ±1 | ±1 | MSOP | 337 |
| ADS7822PC | ±0.75 | ±0.75 | Plastic DIP | 006 |
| ADS7822UC | ±0.75 | ±0.75 | SOIC | 182 |
| ADS7822EC | ±0.75 | ±0.75 | MSOP | 337 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# ADS7824

www.burr-brown.com/databook/ADS7824.html

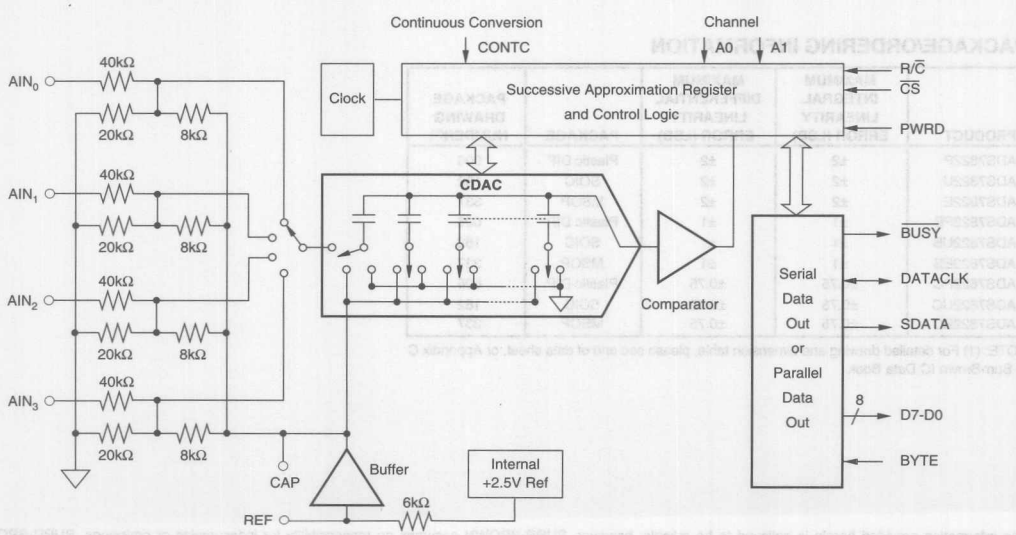
# 4 Channel, 12-Bit Sampling CMOS A/D Converter

## FEATURES

- 25µs max SAMPLING AND CONVERSION
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 16-BIT ADS7825
- PARALLEL AND SERIAL DATA OUTPUT
- 28-PIN 0.3" PLASTIC DIP AND SOIC
- ±0.5 LSB max INL AND DNL
- 50mW max POWER DISSIPATION
- 50µW POWER DOWN MODE
- ±10V INPUT RANGE, FOUR CHANNEL MULTIPLEXER
- CONTINUOUS CONVERSION MODE

## DESCRIPTION

The ADS7824 can acquire and convert 12 bits to within ±0.5 LSB in 25µs max while consuming only 50mW max. Laser-trimmed scaling resistors provide the standard industrial ±10V input range and channel-to-channel matching of ±0.1%. The ADS7824 is a low-power 12-bit sampling A/D with a four channel input multiplexer, S/H, clock, reference, and a parallel/serial microprocessor interface. It can be configured in a continuous conversion mode to sequentially digitize all four channels. The 28-pin ADS7824 is available in a plastic 0.3" DIP and in a SOIC, both fully specified for operation over the industrial –40°C to +85°C range.




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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 40kHz, $V_{S1} = V_{S2} = V_S$ = +5V ±5%, using external reference, CONTC = 0V, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7824P, U | | | ADS7824PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | | 12 | | | *[1] | Bits |
| **ANALOG INPUT** | | | | | | | | |
| Voltage Range | | | ±10V | | | * | | V |
| Impedance | Channel On or Off | | 45.7 | | | * | | kΩ |
| Capacitance | | | 35 | | | * | | pF |
| **THROUGHPUT SPEED** | | | | | | | | |
| Conversion Time | | | 20 | | | * | | µs |
| Acquisition Time | | | 5 | | | * | | µs |
| Multiplexer Settling Time | Includes Acquisition | | 5 | | | * | | µs |
| Complete Cycle (Acquire and Convert) | | | | 25 | | | * | µs |
| Complete Cycle (Acquire and Convert) | CONTC = +5V | | | 40 | | | * | µs |
| Throughput Rate | | 40 | | | * | | | kHz |
| **DC ACCURACY** | | | | | | | | |
| Integral Linearity Error | | | ±0.15 | ±1 | | * | ±0.5 | LSB[2] |
| Differential Linearity Error | | | ±0.15 | ±1 | | * | ±0.5 | LSB |
| No Missing Codes | | | Guaranteed | | | * | | |
| Transition Noise[3] | | | 0.1 | | | * | | LSB |
| Full Scale Error[4] | Internal Reference | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | Internal Reference | | ±7 | | | ±5 | | ppm/°C |
| Full Scale Error[4] | | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | | | ±2 | | | * | | ppm/°C |
| Bipolar Zero Error | | | | ±10 | | | * | mV |
| Bipolar Zero Error Drift | | | ±2 | | | * | | ppm/°C |
| Channel-to-Channel Mismatch | | | | ±0.1 | | | ±0.1 | % |
| Power Supply Sensitivity | +4.75 < $V_S$ < +5.25 | | | ±0.5 | | | * | LSB |
| **AC ACCURACY** | | | | | | | | |
| Spurious-Free Dynamic Range[5] | $f_{IN}$ = 1kHz | 80 | 90 | | * | * | | dB |
| Total Harmonic Distortion | $f_{IN}$ = 1kHz | | –90 | –80 | | * | * | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 1kHz | 70 | 73 | | 72 | * | | dB |
| Signal-to-Noise | $f_{IN}$ = 1kHz | 70 | 73 | | 72 | * | | dB |
| Channel Separation[6] | $f_{IN}$ = 1kHz | 90 | 100 | | * | * | | dB |
| –3dB Bandwidth | | | 2 | | | * | | MHz |
| Useable Bandwidth[7] | | | 90 | | | * | | kHz |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Aperture Delay | | | 40 | | | * | | ns |
| Transient Response[8] | FS Step | | 5 | | | * | | µs |
| Overvoltage Recovery[9] | | | 1 | | | * | | µs |
| **REFERENCE** | | | | | | | | |
| Internal Reference Voltage | | 2.48 | 2.5 | 2.52 | * | * | * | V |
| Internal Reference Source Current (Must use external buffer) | | | 1 | | | * | | µA |
| External Reference Voltage Range for Specified Linearity | | 2.3 | 2.5 | 2.7 | * | * | * | V |
| External Reference Current Drain | $V_{REF}$ = +2.5V | | | 100 | | | * | µA |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Levels | | | | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | * | | * | V |
| $V_{IH}$ | | +2.4 | | $V_S$ +0.3V | * | | * | V |
| $I_{IL}$ | | | | ±10 | | | * | µA |
| $I_{IH}$ | | | | ±10 | | | * | µA |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Data Format | | | Parallel in two bytes; Serial | | | * | | |
| Data Coding | | | Binary Two's Complement | | | * | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +4 | | | * | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_S$ | | | ±5 | | | * | µA |
| Output Capacitance | High-Z State | | | 15 | | | * | pF |

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## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 40kHz, $V_{S1} = V_{S2} = V_S$ = +5V ±5%, using external reference, CONTC = 0V, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7824P, U | | | ADS7824PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **DIGITAL TIMING** | | | | | | | | |
| Bus Access Time | PAR/$\overline{SER}$ = +5V | | | 83 | | | * | ns |
| Bus Relinquish Time | PAR/$\overline{SER}$ = +5V | | | 83 | | | * | ns |
| Data Clock | PAR/$\overline{SER}$ = 0V | | | | | | | |
| Internal Clock (Output only when transmitting data) | EXT/$\overline{INT}$ LOW | 0.5 | | 1.5 | * | | * | MHz |
| External Clock | EXT/$\overline{INT}$ HIGH | 0.1 | | 10 | * | | * | MHz |
| **POWER SUPPLIES** | | | | | | | | |
| $V_{S1} = V_{S2} = V_S$ | | +4.75 | +5 | +5.25 | * | * | * | V |
| Power Dissipation | $f_S$ = 40kHz | | | 50 | | | * | mW |
| | PWRD HIGH | | 50 | | | * | | µW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | °C |
| Storage | | –65 | | +150 | * | | * | °C |
| Thermal Resistance ($\theta_{JA}$) | | | | | | | | |
| Plastic DIP | | | 75 | | | * | | °C/W |
| SOIC | | | 75 | | | * | | °C/W |

NOTES: (1) An asterik (*) specifies same value as grade to the left. (2) LSB means Least Significant Bit. For the 12-bit, ±10V input ADS7824, one LSB is 4.88mV. (3) Typical rms noise at worst case transitions and temperatures. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) A full scale sinewave input on one channel will be attenuated by this amount on the other channels. (7) Useable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (8) The ADS7824 will accurately acquire any input step if given a full acquisition period after the step. (9) Recovers to specified performance after 2 x FS input overvoltage, and normal acquisitions can begin.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB) |
|---|---|---|---|---|---|
| ADS7824P | Plastic Dip | 246 | –40°C to +85°C | ±1 | 70 |
| ADS7824PB | Plastic Dip | 246 | –40°C to +85°C | ±0.5 | 72 |
| ADS7824U | SOIC | 217 | –40°C to +85°C | ±1 | 70 |
| ADS7824UB | SOIC | 217 | –40°C to +85°C | ±0.5 | 72 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $AIN_0$, $AIN_1$, $AIN_2$, $AIN_3$ | ±15V |
| REF | (AGND2 –0.3V) to ($V_S$ + 0.3V) |
| CAP | Indefinite Short to AGND2, Momentary Short to $V_S$ |
| $V_{S1}$ and $V_{S2}$ to AGND2 | 7V |
| $V_{S1}$ to $V_{S2}$ | ±0.3V |
| Difference between AGND1, AGND2 and DGND | ±0.3V |
| Digital Inputs and Outputs | –0.3V to ($V_S$ + 0.3V) |
| Maximum Junction Temperature | 150°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |
| Maximum Input Current to Any Pin | 100mA |

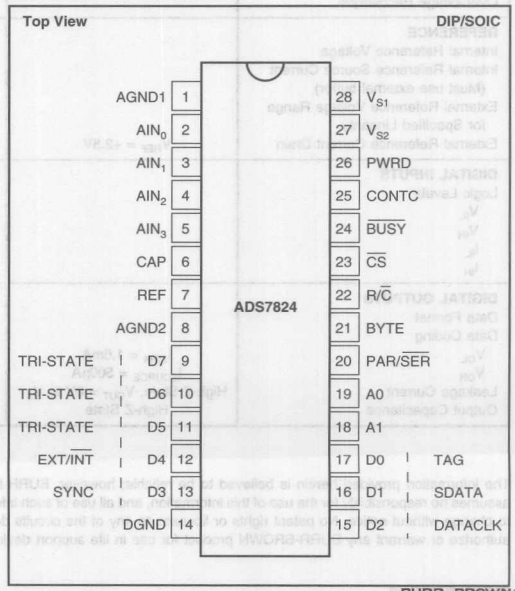
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN CONFIGURATION

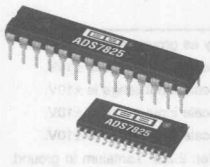
Top View DIP/SOIC



## PIN ASSIGNMENTS

| PIN # | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| 1 | AGND1 | | Analog Ground. Used internally as ground reference point. |
| 2 | $AIN_0$ | | Analog Input Channel 0. Full-scale input range is ±10V. |
| 3 | $AIN_1$ | | Analog Input Channel 1. Full-scale input range is ±10V. |
| 4 | $AIN_2$ | | Analog Input Channel 2. Full-scale input range is ±10V. |
| 5 | $AIN_3$ | | Analog Input Channel 3. Full-scale input range is ±10V. |
| 6 | CAP | | Internal Reference Output Buffer. 2.2µF Tantalum to ground. |
| 7 | REF | | Reference Input/Output. Outputs +2.5V nominal. If used externally, must be buffered to maintain ADS7825 accuracy. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2µF Tantalum capacitor. |
| 8 | AGND2 | | Analog Ground. |
| 9 | D7 | O | Parallel Data Bit 7 if PAR/$\overline{SER}$ HIGH; Tri-state if PAR/$\overline{SER}$ LOW. See Table I. |
| 10 | D6 | O | Parallel Data Bit 6 if PAR/$\overline{SER}$ HIGH; Tri-state if PAR/$\overline{SER}$ LOW. See Table I. |
| 11 | D5 | O | Parallel Data Bit 5 if PAR/$\overline{SER}$ HIGH; Tri-state if PAR/$\overline{SER}$ LOW. See Table I. |
| 12 | D4 | I/O | Parallel Data Bit 4 if PAR/$\overline{SER}$ HIGH; if PAR/$\overline{SER}$ LOW, a LOW level input here will transmit serial data on SDATA from the previous conversion using the internal serial clock; a HIGH input here will transmit serial data using an external serial clock input on DATACLK (D2). See Table I. |
| 13 | D3 | O | Parallel Data Bit 3 if PAR/$\overline{SER}$ HIGH; SYNC output if PAR/$\overline{SER}$ LOW. See Table I. |
| 14 | DGND | | Digital Ground. |
| 15 | D2 | I/O | Parallel Data Bit 2 if PAR/$\overline{SER}$ HIGH; if PAR/$\overline{SER}$ LOW, this will output the internal serial clock if EXT/$\overline{INT}$ (D4) is LOW; will be an input for an external serial clock if EXT/$\overline{INT}$ (D4) is HIGH. See Table I. |
| 16 | D1 | O | Parallel Data Bit 1 if PAR/$\overline{SER}$ HIGH; SDATA serial data output if PAR/$\overline{SER}$ LOW. See Table I. |
| 17 | D0 | I/O | Parallel Data Bit 0 if PAR/$\overline{SER}$ HIGH; TAG data input if PAR/$\overline{SER}$ LOW. See Table I. |
| 18 | A1 | I/O | Channel Address. Input if CONTC LOW, output if CONTC HIGH. See Table I. |
| 19 | A0 | I/O | Channel Address. Input if CONTC LOW, output if CONTC HIGH. See Table I. |
| 20 | PAR/$\overline{SER}$ | I | Select Parallel or Serial Output. If HIGH, parallel data will be output on D0 thru D7. If LOW, serial data will be output on SDATA. See Table I and Figure 1. |
| 21 | BYTE | I | Byte Select. Only used with parallel data, when PAR/$\overline{SER}$ HIGH. Determines which byte is available on D0 thru D7. Changing BYTE with $\overline{CS}$ LOW and R/$\overline{C}$ HIGH will cause the data bus to change accordingly. LOW selects the 8 MSBs; HIGH selects the 4 LSBs, see Figures 2 and 3. |
| 22 | R/$\overline{C}$ | I | Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the output data bits if PAR/$\overline{SER}$ HIGH, or starts transmission of serial data if PAR/$\overline{SER}$ LOW and EXT/$\overline{INT}$ HIGH. |
| 23 | $\overline{CS}$ | I | Chip Select. Internally OR'd with R/$\overline{C}$. With CONTC LOW and R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH, a falling edge on $\overline{CS}$ will enable the output data bits if PAR/$\overline{SER}$ HIGH, or starts transmission of serial data if PAR/$\overline{SER}$ LOW and EXT/$\overline{INT}$ HIGH. |
| 24 | $\overline{BUSY}$ | O | Busy Output. Falls when conversion is started; remains LOW until the conversion is completed and the data is latched into the output register. In parallel output mode, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data. |
| 25 | CONTC | I | Continuous Conversion Input. If LOW, conversions will occur normally when initiated using $\overline{CS}$ and R/$\overline{C}$; if HIGH, acquisition and conversions will take place continually, cycling through all four input channels, as long as $\overline{CS}$, R/$\overline{C}$ and PWRD are LOW. See Table I. For serial mode only. |
| 26 | PWRD | I | Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output register. In the continuous conversion mode, the multiplexer address channel is reset to channel 0 |
| 27 | $V_{S2}$ | | Supply Input. Nominally +5V. Connect directly to pin 28. Decouple to ground with 0.1µF ceramic and 10µF Tantalum capacitors. |
| 28 | $V_{S1}$ | | Supply Input. Nominally +5V. Connect directly to pin 27. |

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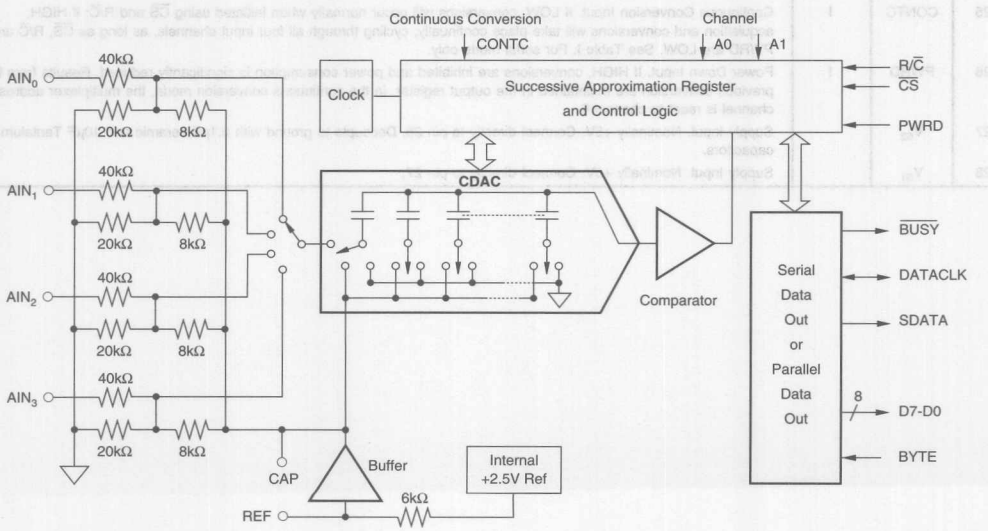
# 4 Channel, 16-Bit Sampling CMOS A/D Converter

## FEATURES

- 25µs max SAMPLING AND CONVERSION
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 12-BIT ADS7824
- PARALLEL AND SERIAL DATA OUTPUT
- 28-PIN 0.3" PLASTIC DIP AND SOIC
- ±2.0 LSB max INL
- 50mW max POWER DISSIPATION
- 50µW POWER DOWN MODE
- ±10V INPUT RANGE, FOUR CHANNEL MULTIPLEXER
- CONTINUOUS CONVERSION MODE

## DESCRIPTION

The ADS7825 can acquire and convert 16 bits to within ±2.0 LSB in 25µs max while consuming only 50mW max. Laser-trimmed scaling resistors provide the standard industrial ±10V input range and channel-to-channel matching of ±0.1%. The ADS7825 is a low-power 16-bit sampling A/D with a four channel input multiplexer, S/H, clock, reference, and a parallel/serial microprocessor interface. It can be configured in a continuous conversion mode to sequentially digitize all four channels. The 28-pin ADS7825 is available in a plastic 0.3" DIP and in a SOIC, both fully specified for operation over the industrial –40°C to +85°C range.




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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = –40°C to +85°C, $f_S$ = 40kHz, $V_{S1} = V_{S2} = V_S$ = +5V ±5%, using external reference, CONTC = 0V, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7825P, U | | | ADS7825PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | | 16 | | | *[1] | Bits |
| **ANALOG INPUT** | | | | | | | | |
| Voltage Range | | | ±10V | | | * | | V |
| Impedance | Channel On or Off | | 45.7 | | | * | | kΩ |
| Capacitance | | | 35 | | | * | | pF |
| **THROUGHPUT SPEED** | | | | | | | | |
| Conversion Time | | | 20 | | | * | | µs |
| Acquisition Time | | | 5 | | | * | | µs |
| Multiplexer Settling Time | Includes Acquisition | | 5 | | | * | | µs |
| Complete Cycle (Acquire and Convert) | | | | 25 | | | * | µs |
| Complete Cycle (Acquire and Convert) | CONTC = +5V | | | 40 | | | * | µs |
| Throughput Rate | | 40 | | | * | | | kHz |
| **DC ACCURACY** | | | | | | | | |
| Integral Linearity Error | | | | ±3 | | | ±2 | LSB[2] |
| No Missing Codes | | 15 | | | 16 | | | |
| Transition Noise[3] | | | 0.8 | | | * | | LSB |
| Full Scale Error[4] | Internal Reference | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | Internal Reference | | ±7 | | | ±5 | | ppm/°C |
| Full Scale Error[4] | | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | | | ±2 | | | * | | ppm/°C |
| Bipolar Zero Error | | | | ±10 | | | * | mV |
| Bipolar Zero Error Drift | | | ±2 | | | * | | ppm/°C |
| Channel-to-Channel Mismatch | | | | ±0.1 | | | ±0.1 | % |
| Power Supply Sensitivity | +4.75 < $V_S$ < +5.25 | | | ±8 | | | * | LSB |
| **AC ACCURACY** | | | | | | | | |
| Spurious-Free Dynamic Range[5] | $f_{IN}$ = 1kHz | 90 | | | * | | | dB |
| Total Harmonic Distortion | $f_{IN}$ = 1kHz | | | –90 | | | * | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 1kHz | 83 | | | 86 | | | dB |
| Signal-to-Noise | $f_{IN}$ = 1kHz | 83 | | | 86 | | | dB |
| Channel Separation[6] | $f_{IN}$ = 1kHz | 100 | 120 | | * | * | | dB |
| –3dB Bandwidth | | | 2 | | | * | | MHz |
| Useable Bandwidth[7] | | | 90 | | | * | | kHz |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Aperture Delay | | | 40 | | | * | | ns |
| Transient Response[8] | FS Step | | 5 | | | * | | µs |
| Overvoltage Recovery[9] | | | 1 | | | * | | µs |
| **REFERENCE** | | | | | | | | |
| Internal Reference Voltage | | 2.48 | 2.5 | 2.52 | * | * | * | V |
| Internal Reference Source Current (Must use external buffer) | | | 1 | | | * | | µA |
| External Reference Voltage Range for Specified Linearity | | 2.3 | 2.5 | 2.7 | * | * | * | V |
| External Reference Current Drain | $V_{REF}$ = +2.5V | | | 100 | | | * | µA |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Levels | | | | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | * | | * | V |
| $V_{IH}$ | | +2.4 | | $V_S$ +0.3V | * | | * | V |
| $I_{IL}$ | | | | ±10 | | | * | µA |
| $I_{IH}$ | | | | ±10 | | | * | µA |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Data Format | | Parallel in two bytes; Serial | | | * | | | |
| Data Coding | | Binary Two's Complement | | | * | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +4 | | | * | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_S$ | | | ±5 | | | * | µA |
| Output Capacitance | High-Z State | | | 15 | | | * | pF |

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| PARAMETER | CONDITIONS | ADS7825P, U | | | ADS7825PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **DIGITAL TIMING** | | | | | | | | |
| Bus Access Time | PAR/$\overline{SER}$ = +5V | | | 83 | | | * | ns |
| Bus Relinquish Time | PAR/$\overline{SER}$ = +5V | | | 83 | | | * | ns |
| Data Clock | PAR/$\overline{SER}$ = 0V | | | | | | | |
| Internal Clock (Output only when transmitting data) | EXT/$\overline{INT}$ LOW | 0.5 | | 1.5 | * | | * | MHz |
| External Clock | EXT/$\overline{INT}$ HIGH | 0.1 | | 10 | * | | * | MHz |
| **POWER SUPPLIES** | | | | | | | | |
| $V_{S1} = V_{S2} = V_S$ | | +4.75 | +5 | +5.25 | * | * | * | V |
| Power Dissipation | $f_S$ = 40kHz | | | 50 | | | * | mW |
| | PWRD HIGH | | 50 | | | * | | µW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | °C |
| Storage | | –65 | | +150 | * | | * | °C |
| Thermal Resistance ($\theta_{JA}$) | | | | | | | | |
| Plastic DIP | | | 75 | | | * | | °C/W |
| SOIC | | | 75 | | | * | | °C/W |

NOTES: (1) An asterik (*) specifies same value as grade to the left. (2) LSB means Least Significant Bit. For the 16-bit, ±10V input ADS7825, one LSB is 305µV. (3) Typical rms noise at worst case transitions and temperatures. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) A full scale sinewave input on one channel will be attenuated by this amount on the other channels. (7) Useable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (8) The ADS7825 will accurately acquire any input step if given a full acquisition period after the step. (9) Recovers to specified performance after 2 x FS input overvoltage, and normal acquisitions can begin.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB) |
|---|---|---|---|---|---|
| ADS7825P | Plastic Dip | 246 | –40°C to +85°C | ±3 | 83 |
| ADS7825PB | Plastic Dip | 246 | –40°C to +85°C | ±2 | 86 |
| ADS7825U | SOIC | 217 | –40°C to +85°C | ±3 | 83 |
| ADS7825UB | SOIC | 217 | –40°C to +85°C | ±2 | 86 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $AIN_0$, $AIN_1$, $AIN_2$, $AIN_3$ | ±15V |
| REF | (AGND2 –0.3V) to ($V_S$ + 0.3V) |
| CAP | Indefinite Short to AGND2, Momentary Short to $V_S$ |
| $V_{S1}$ and $V_{S2}$ to AGND2 | 7V |
| $V_{S1}$ to $V_{S2}$ | ±0.3V |
| Difference between AGND1, AGND2 and DGND | ±0.3V |
| Digital Inputs and Outputs | –0.3V to ($V_S$ + 0.3V) |
| Maximum Junction Temperature | 150°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |
| Maximum Input Current to Any Pin | 100mA |

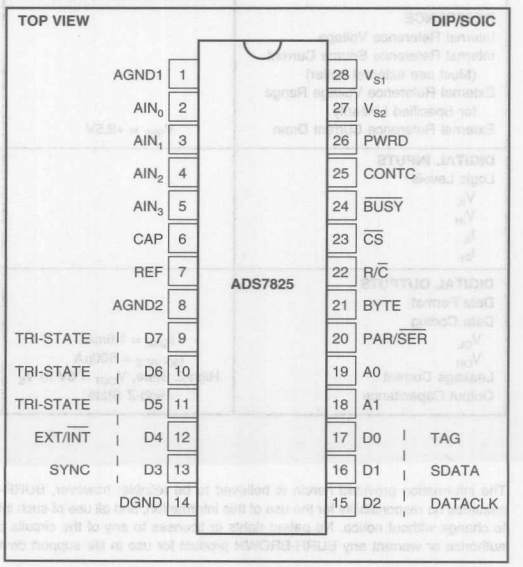
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN CONFIGURATION

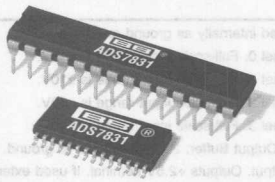
TOP VIEW — DIP/SOIC



## PIN ASSIGNMENTS

| PIN # | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| 1 | AGND1 | | Analog Ground. Used internally as ground reference point. |
| 2 | $AIN_0$ | | Analog Input Channel 0. Full-scale input range is ±10V. |
| 3 | $AIN_1$ | | Analog Input Channel 1. Full-scale input range is ±10V. |
| 4 | $AIN_2$ | | Analog Input Channel 2. Full-scale input range is ±10V. |
| 5 | $AIN_3$ | | Analog Input Channel 3. Full-scale input range is ±10V. |
| 6 | CAP | | Internal Reference Output Buffer. 2.2µF Tantalum to ground. |
| 7 | REF | | Reference Input/Output. Outputs +2.5V nominal. If used externally, must be buffered to maintain ADS7825 accuracy. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2µF Tantalum capacitor. |
| 8 | AGND2 | | Analog Ground. |
| 9 | D7 | O | Parallel Data Bit 7 if PAR/$\overline{SER}$ HIGH; Tri-state if PAR/$\overline{SER}$ LOW. See Table I. |
| 10 | D6 | O | Parallel Data Bit 6 if PAR/$\overline{SER}$ HIGH; Tri-state if PAR/$\overline{SER}$ LOW. See Table I. |
| 11 | D5 | O | Parallel Data Bit 5 if PAR/$\overline{SER}$ HIGH; Tri-state if PAR/$\overline{SER}$ LOW. See Table I. |
| 12 | D4 | I/O | Parallel Data Bit 4 if PAR/$\overline{SER}$ HIGH; if PAR/$\overline{SER}$ LOW, a LOW level input here will transmit serial data on SDATA from the previous conversion using the internal serial clock; a HIGH input here will transmit serial data using an external serial clock input on DATACLK (D2). See Table I. |
| 13 | D3 | O | Parallel Data Bit 3 if PAR/$\overline{SER}$ HIGH; SYNC output if PAR/$\overline{SER}$ LOW. See Table I. |
| 14 | DGND | | Digital Ground. |
| 15 | D2 | I/O | Parallel Data Bit 2 if PAR/$\overline{SER}$ HIGH; if PAR/$\overline{SER}$ LOW, this will output the internal serial clock if EXT/$\overline{INT}$ (D4) is LOW; will be an input for an external serial clock if EXT/$\overline{INT}$ (D4) is HIGH. See Table I. |
| 16 | D1 | O | Parallel Data Bit 1 if PAR/$\overline{SER}$ HIGH; SDATA serial data output if PAR/$\overline{SER}$ LOW. See Table I. |
| 17 | D0 | I/O | Parallel Data Bit 0 if PAR/$\overline{SER}$ HIGH; TAG data input if PAR/$\overline{SER}$ LOW. See Table I. |
| 18 | A1 | I/O | Channel Address. Input if CONTC LOW, output if CONTC HIGH. See Table I. |
| 19 | A0 | I/O | Channel Address. Input if CONTC LOW, output if CONTC HIGH. See Table I. |
| 20 | PAR/$\overline{SER}$ | I | Select Parallel or Serial Output. If HIGH, parallel data will be output on D0 thru D7. If LOW, serial data will be output on SDATA. See Table I and Figure 1. |
| 21 | BYTE | I | Byte Select. Only used with parallel data, when PAR/$\overline{SER}$ HIGH. Determines which byte is available on D0 thru D7. Changing BYTE with $\overline{CS}$ LOW and R/$\overline{C}$ HIGH will cause the data bus to change accordingly. LOW selects the 8 MSBs; HIGH selects the 8 LSBs. See Figures 2 and 3 |
| 22 | R/$\overline{C}$ | I | Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the output data bits if PAR/$\overline{SER}$ HIGH, or starts transmission of serial data if PAR/$\overline{SER}$ LOW and EXT/$\overline{INT}$ HIGH. |
| 23 | $\overline{CS}$ | I | Chip Select. Internally OR'd with R/$\overline{C}$. With CONTC LOW and R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH, a falling edge on $\overline{CS}$ will enable the output data bits if PAR/$\overline{SER}$ HIGH, or starts transmission of serial data if PAR/$\overline{SER}$ LOW and EXT/$\overline{INT}$ HIGH. |
| 24 | $\overline{BUSY}$ | O | Busy Output. Falls when conversion is started; remains LOW until the conversion is completed and the data is latched into the output register. In parallel output mode, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data. |
| 25 | CONTC | I | Continuous Conversion Input. If LOW, conversions will occur normally when initiated using $\overline{CS}$ and R/$\overline{C}$; if HIGH, acquisition and conversions will take place continually, cycling through all four input channels, as long as $\overline{CS}$, R/$\overline{C}$ and PWRD are LOW. See Table I. For serial mode only. |
| 26 | PWRD | I | Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output register. In the continuous conversion mode, the multiplexer address channel is reset to channel 0. |
| 27 | $V_{S2}$ | | Supply Input. Nominally +5V. Connect directly to pin 28. Decouple to ground with 0.1µF ceramic and 10µF Tantalum capacitors. |
| 28 | $V_{S1}$ | | Supply Input. Nominally +5V. Connect directly to pin 27. |

BURR - BROWN®




# ADS7831

www.burr-brown.com/databook/ADS7831.html

# 12-Bit 600kHz Sampling CMOS ANALOG-to-DIGITAL CONVERTER

## FEATURES

- 600kHz THROUGHPUT RATE
- STANDARD ±2.5V INPUT RANGE
- 69dB min SINAD WITH 250kHz INPUT
- COMPLETE WITH S/H, REF, CLOCK, ETC.
- PARALLEL DATA w/LATCHES
- FULLY SPECIFIED –40°C TO +85°C
- 15MHz –3dB BANDWIDTH
- 28-PIN 0.3" PDIP AND SOIC

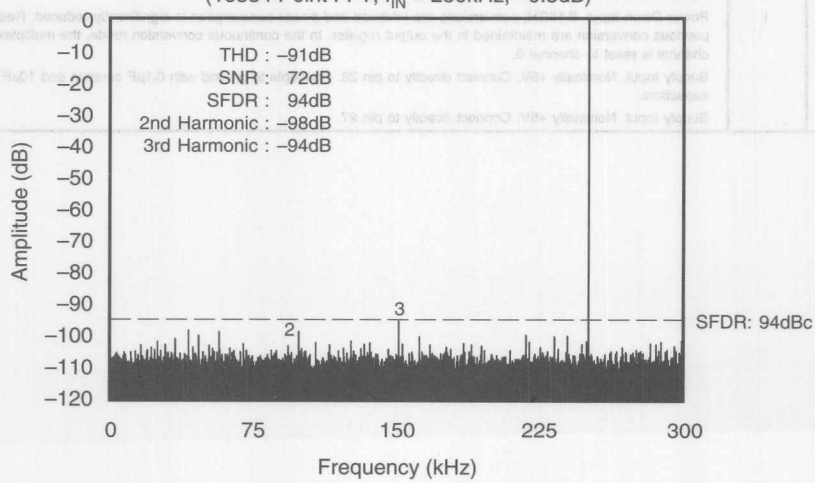
## DESCRIPTION

The ADS7831 is a complete 12-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 12-bit capacitor-based SAR A/D with inherent S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7831 is specified at a 600kHz sampling rate, and guaranteed over the full temperature range. A ±2.5V input range and excellent Nyquist performance provide an optimum solution in ±5V supply systems.

The 28-pin ADS7831 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.

FREQUENCY SPECTRUM
(16384 Point FFT; $f_{IN}$ = 250kHz, –0.5dB)



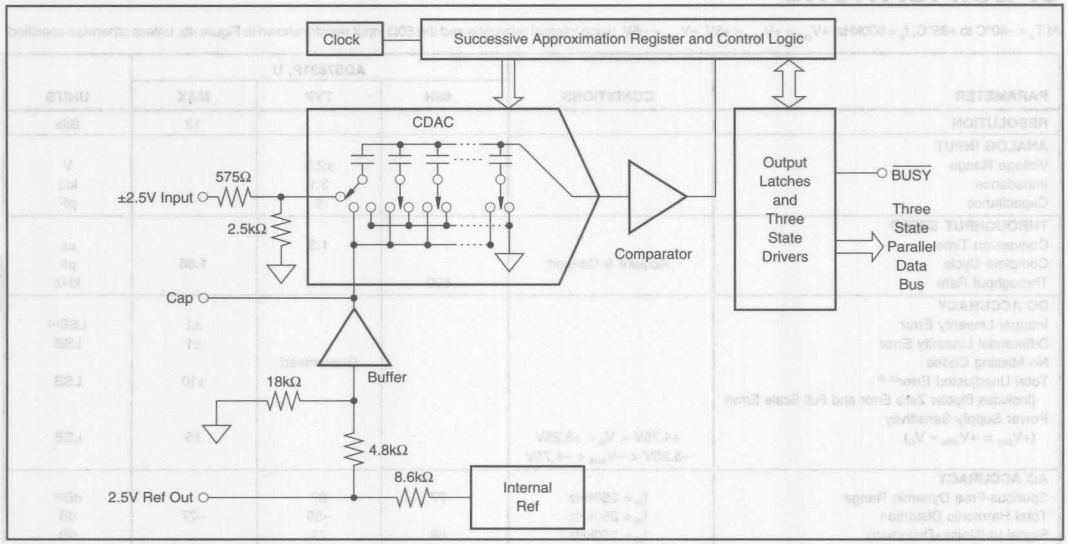

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = –40°C to +85°C, $f_S$ = 600kHz, $+V_{DIG} = +V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference and the 50Ω input resistor shown in Figure 4b, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7831P, U MIN | ADS7831P, U TYP | ADS7831P, U MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | | 12 | Bits |
| **ANALOG INPUT** | | | | | |
| Voltage Range | | | ±2.5 | | V |
| Impedance | | | 3.1 | | kΩ |
| Capacitance | | | 5 | | pF |
| **THROUGHPUT SPEED** | | | | | |
| Conversion Time | | | 1.3 | | µs |
| Complete Cycle | Acquire & Convert | | | 1.66 | µs |
| Throughput Rate | | 600 | | | kHz |
| **DC ACCURACY** | | | | | |
| Integral Linearity Error | | | | ±1 | LSB[1] |
| Differential Linearity Error | | | | ±1 | LSB |
| No Missing Codes | | | Guaranteed | | |
| Total Unadjusted Error[2, 3] (Includes Bipolar Zero Error and Full Scale Error) | | | | ±10 | LSB |
| Power Supply Sensitivity ($+V_{DIG} = +V_{ANA} = V_D$) | +4.75V < $V_D$ < +5.25V<br>–5.25V < $-V_{ANA}$ < –4.75V | | | ±5 | LSB |
| **AC ACCURACY** | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 250kHz | 77 | 87 | | dB[4] |
| Total Harmonic Distortion | $f_{IN}$ = 250kHz | | –85 | –77 | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 250kHz | 69 | 71 | | dB |
| Signal-to-Noise | $f_{IN}$ = 250kHz | 69 | 72 | | dB |
| Usable Bandwidth[5] | | | 1.6 | | MHz |
| Full-Power Bandwidth | | | 15 | | MHz |
| **SAMPLING DYNAMICS** | | | | | |
| Aperture Delay | | | 20 | | ns |
| Aperture Jitter | | | 10 | | ps |
| Transient Response | FS Step | | 200 | | ns |
| Overvoltage Recovery[6] | | | 250 | | ns |
| **REFERENCE** | | | | | |
| Reference Voltage | | 2.45 | 2.5 | 2.55 | V |
| Reference DC Source Current (External load should be static) | | | 100 | | µA |
| **DIGITAL INPUTS** | | | | | |
| Logic Levels | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | V |
| $V_{IH}$ | | +2.4 | | $V_D$ + 0.3 | V |
| $I_{IL}$ | $V_{IL}$ = 0V | | | ±10 | µA |
| $I_{IH}$ | $V_{IH}$ = 5V | | | ±10 | µA |
| **DIGITAL OUTPUTS** | | | | | |
| Data Format | | | Parallel 12-bits | | |
| Data Coding | | | Binary Two's Complement | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +2.8 | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_{DIG}$ | | | ±5 | µA |
| Output Capacitance | High-Z State | | | 15 | pF |
| **DIGITAL TIMING** | | | | | |
| Bus Access Time | | | | 62 | ns |
| Bus Relinquish Time | | | | 83 | ns |
| **POWER SUPPLIES** | | | | | |
| Specified Performance | | | | | |
| $+V_{DIG} = +V_{ANA}$ | | +4.75 | +5 | +5.25 | V |
| $-V_{ANA}$ | | –5.25 | –5 | –4.75 | V |
| $+I_{DIG}$ | | | +16 | | mA |
| $+I_{ANA}$ | | | +16 | | mA |
| $-I_{ANA}$ | | | –12 | | mA |
| Power Dissipation | $f_S$ = 600kHz | | 220 | 275 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified Performance | | –40 | | +85 | °C |
| Storage | | –65 | | +150 | °C |
| Thermal Resistance ($\theta_{JA}$) | | | | | |
| Plastic DIP | | | 75 | | °C/W |
| SOIC | | | 75 | | °C/W |

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, ±2.5V input ADS7831, one LSB is 1.22mV. (2) Measured with 50Ω in series with analog input. Adjustable to zero with external potentiometers. (3) Total unadjusted error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions and includes the effect of offset error. (4) All specifications in dB are referred to a full-scale ±2.5V input. (5) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. 6) Recovers to specified performance after 2 x FS input over voltage.




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $V_{IN}$ | ±25V |
| REF | $+V_{ANA}$ +0.3V to AGND2 –0.3V |
| CAP | Indefinite Short to AGND2, Momentary Short to $+V_{ANA}$ |
| Ground Voltage Differences: DGND, AGND1, AGND2 | ±0.3V |
| $+V_{ANA}$ | +7V |
| $+V_{DIG}$ to $+V_{ANA}$ | +0.3V |
| $+V_{DIG}$ | 7V |
| $-V_{ANA}$ | –7V |
| Digital Inputs | –0.3V to $+V_{DIG}$ +0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |

## PACKAGE AND ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| ADS7831P | 28-Pin Plastic DIP | 246 |
| ADS7831U | 28-Pin SOIC | 217 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

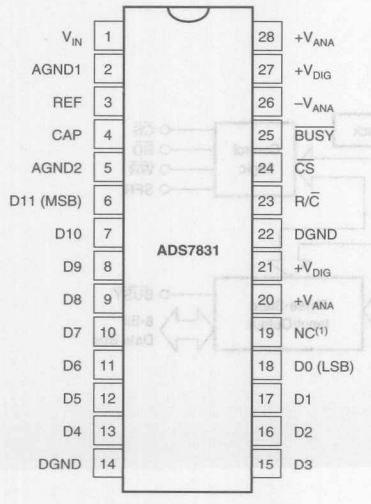
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## PIN ASSIGNMENTS

| PIN # | NAME | DIGITAL I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $V_{IN}$ | | Analog Input. Connect via 50Ω to analog input. Full-scale input range is ±2.5V. |
| 2 | AGND1 | | Analog Ground. Used internally as ground reference point. Minimal current flow. |
| 3 | REF | | Reference Input/Output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, decouple to ground with a 0.1µF ceramic capacitor. |
| 4 | CAP | | Reference Buffer Output. 10µF tantalum capacitor to ground. Nominally +2V. |
| 5 | AGND2 | | Analog Ground. |
| 6 | D11 (MSB) | O | Data Bit 11. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 7 | D10 | O | Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 8 | D9 | O | Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 9 | D8 | O | Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 10 | D7 | O | Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 11 | D6 | O | Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 12 | D5 | O | Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 13 | D4 | O | Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 14 | DGND | | Digital Ground. |
| 15 | D3 | O | Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 16 | D2 | O | Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 17 | D1 | O | Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 18 | D0 (LSB) | O | Data Bit 0. Least Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 19 | | | Not internally connected. |
| 20 | $+V_{ANA}$ | | Analog Positive Supply Input. Nominally +5V. Connect directly to pins 21, 27 and 28. |
| 21 | $+V_{DIG}$ | | Digital Supply Input. Nominally +5V. Connect directly to pins 20, 27 and 28. |
| 22 | DGND | | Digital ground. |
| 23 | R/$\overline{C}$ | I | Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW and no conversion in progress, a rising edge on R/$\overline{C}$ enables the output data bits. |
| 24 | $\overline{CS}$ | I | Chip Select. With R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH and no conversion in progress, a falling edge on $\overline{CS}$ will enable the output data bits. |
| 25 | $\overline{BUSY}$ | O | Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output register. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data. |
| 26 | $-V_{ANA}$ | | Analog Negative Supply Input. Nominally –5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors. |
| 27 | $+V_{DIG}$ | | Digital Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 28. |
| 28 | $+V_{ANA}$ | | Analog Positive Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 27, and decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors. |

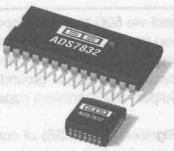
## PIN CONFIGURATION

Top View DIP/SOIC




NOTE: (1) Not Internally Connected.

BURR-BROWN®



# ADS7832

www.burr-brown.com/databook/ADS7832.html

# Autocalibrating, 4-Channel, 12-Bit ANALOG-TO-DIGITAL CONVERTER

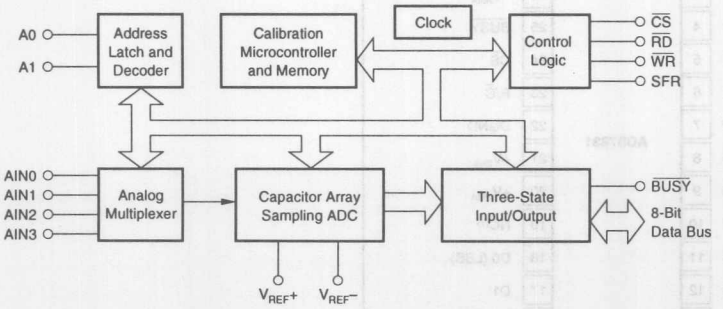
## FEATURES

- PIN COMPATIBLE TO ADC7802 AND ADS7803
- SINGLE SUPPLY: +5V OR +3.3V
- LOW POWER: 14mW plus Power Down
- SIGNAL-TO-(NOISE + DISTORTION) RATIO OVER TEMPERATURE:
  69dB min with $f_{IN}$ = 1kHz
  66dB min with $f_{IN}$ = 50kHz
- FAST CONVERSION TIME: 8.5µs Including Acquisition (117kHz Sampling Rate)
- FOUR-CHANNEL INPUT MULTIPLEXER
- AUTOCAL: No offset or Gain Adjust Required

## DESCRIPTION

The ADS7832 is a monolithic CMOS 12-bit analog-to-digital converter with internal sample/hold and four-channel multiplexer. It is designed and tested for full dynamic performance with input signals to 50kHz. The 5V single-supply requirements and standard $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ control signals make the part easy to use in microprocessor applications. Conversion results are available in two bytes through an 8-bit three-state output bus.

The ADS7832 is available in a 28-pin plastic DIP and 28-lead PLCC, fully specified for operation over the industrial –40°C to +85°C temperature range.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ADS7832 Electrical Specifications with 3.3V Supply

$V_A = V_D = V_{REF}+ = 3.3V \pm 10\%$; $V_{REF}- = AGND = DGND = 0V$; CLK = 1MHz external, $T_A = -40°C$ to $+85°C$, after calibration at any temperature, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7832BP/ADS7832BN MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | | 12 | Bits |
| **ANALOG INPUT** | $V_A = V_D = V_{REF+} = 3.0V$ | | | | |
| Voltage Input Range | | 0 | | $V_{REF+}$ | V |
| Input Capacitance | | | 40 | | pF |
| On State Bias Current | | | | 100 | nA |
| Off State Bias Current | $T_A = +25°C$ | | | 10 | nA |
| | $T_A = -40°C$ to $+85°C$ | | | 100 | nA |
| On Resistance Multiplexer | | | 400 | | Ω |
| Off Resistance Multiplexer | | | 10 | | MΩ |
| Channel Separation | $F_{IN}$ = 1kHz, $V_{REF}+ = 3.0V$ | | 0.5 | | LSB |
| **REFERENCE INPUT** | | | | | |
| For Specified Performance: $V_{REF}+$ | | | $V_A$ | | V |
| $V_{REF}-$ | | | 0 | | V |
| For Derated Performance[2]: $V_{REF}+$ | $(V_{REF}+) - (V_{REF}-) \geq 2.5V$ | 2.5 | | $V_A$ | V |
| $V_{REF}-$ | | 0 | | 0.5 | V |
| Input Reference Current | | | 100 | 200 | µA |
| **THROUGHPUT SPEED** | | | | | |
| Conversion Time With External Clock (Including Multiplexer Settling Time and Acquisition Time) | CLK = 1MHz | | | 17 | µs |
| | CLK = 500kHz | | | 34 | µs |
| With Internal Clock Using Recommended Clock Components | $T_A = +25°C$ | | 30 | | µs |
| | $T_A = -40°C$ to $+85°C$ | | 30 | | µs |
| Slew Rate | | | 2 | | V/µs |
| Multiplexer Settling Time to 1/2 LSB | | | 0.5 | | µs |
| Multiplexer Access Time | | | 20 | | ns |
| **SAMPLING DYNAMICS** | | | | | |
| Full Power Bandwidth | –3dB | | 2 | | MHz |
| Aperture Jitter | | | | | ps |
| Aperture Delay | SRF D2 LOW[3] | | 5 | | µs |
| | SFR D2 HIGH | | 5 | | ns |
| **DC ACCURACY** | | | | | |
| Integral Nonlinearity, All Channels | SFR D2 LOW | | | ±0.75 | LSB[4] |
| | SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock | | ±0.5 | | LSB |
| | SFR D2 HIGH, Sampling Command Asynchronous to External Clock | | ±0.6 | | LSB |
| Differential Nonlinearity | | | | ±0.75 | LSB |
| No Missing Codes | | | Guaranteed | | |
| Gain Error | All Channels | | | ±0.5 | LSB |
| Gain Error Drift | Between Calibration Cycles | | ±0.2 | | ppm/°C |
| Offset Error | All Channels | | | | |
| | SFR D2 LOW | | | ±0.75 | LSB |
| | SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock | | ±1 | | LSB |
| | SFR D2 HIGH, Sampling Command Asynchronous to External Clock | | ±4 | | LSB |
| Offset Error Drift | Between Calibration Cycles | | | | |
| | SFR D2 LOW | | ±0.2 | | ppm/°C |
| | SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock | | ±0.5 | | ppm/°C |
| | SFR D2 HIGH, Sampling Command Asynchronous to External Clock | | ±1 | | ppm/°C |
| Channel-to-Channel Mismatch | SFR D2 LOW | | ±0.25 | | LSB |
| | SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock | | ±0.5 | | LSB |
| | SFR D2 HIGH, Sampling Command Asynchronous to External Clock | | ±1 | | LSB |
| Power Supply Sensitivity | $V_D = V_A = +3.3V \pm 10\%$ (without recalibration) | | ±0.125 | | LSB |
| **AC ACCURACY** | | | | | |
| Signal-to-(Noise + Distortion) Ratio | $f_{IN}$ = 1kHz | 69 | 71 | | dB[1] |
| | $f_{IN}$ = 50kHz | 66 | 69 | | dB |
| Total Harmonic Distortion | $f_{IN}$ = 50kHz | | –75 | | dB |
| Signal-to-Noise Ratio | $f_{IN}$ = 50kHz | | 70 | | dB |
| Spurious Free Dynamic Range | $f_{IN}$ = 1kHz | | 85 | | dB |
| | $f_{IN}$ = 50kHz | | 82 | | dB |

## ADS7832 Electrical Specifications with 3.3V Supply

$V_A = V_D = V_{REF}+ = 3.3V \pm 10\%$; $V_{REF}- = AGND = DGND = 0V$; CLK = 1MHz external, $T_A = -40°C$ to $+85°C$, after calibration at any temperature, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7832BP/ADS7832BN MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **DIGITAL INPUTS** | | | | | |
| Voltage Levels: $V_{IL}$ | | –0.3 | | +0.8 | V |
| $V_{IH}$ | | 0.7 • $V_D$ | | $V_D$ +0.3V | V |
| Current Levels: $I_{IL}$ | CAL (Internal Pull-Up) | | 10 | | µA |
| $I_{IL}$ | All Other Inputs | | | ±10 | µA |
| $I_{IH}$ | SFR (Internal Pull-Down) | | 90 | | µA |
| $I_{IH}$ | CLK | | | 1.5 | mA |
| $I_{IH}$ | All Other Inputs | | | ±10 | µA |
| $I_{IH}$ | Power Down Mode (SFR D3 HIGH) | | | ±100 | nA |
| **DIGITAL OUTPUTS** | | | | | |
| Data Format | | | Parallel 12 Bits in Two Bytes | | |
| Data Coding | | | Straight Binary | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | 0.2 • $V_D$ | V |
| $V_{OH}$ | $I_{SOURCE}$ = 200µA | 0.8 • $V_D$ | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_D$ | | | ±1 | µA |
| Output Capacitance | High-Z State | | 4 | | pF |
| **CALIBRATION TIMING** | | | | | |
| Calibration Cycle | Power On or Power Failure | | | 37393 | Clock Cycles |
| Calibration Cycle | During Normal Operation | | | 4625 | Clock Cycles |
| **DIGITAL TIMING** | | | | | |
| Bus Access Time | | | | 83 | ns |
| Bus Relinquish Time | | | | 83 | ns |
| **POWER SUPPLIES** | | | | | |
| Supply Voltage for Specified Performance: $V_A$ | Tested at 3.0V | 3 | 3.3 | | V |
| $V_D$ | Tested at 3.0V | 3 | 3.3 | | V |
| Supply Current: $I_A$ | | | 2.5 | 3 | mA |
| $I_D$ | | | 300 | 500 | µA |
| Power Dissipation | Power Up Mode or During Conversion | | 7.5 | | mW |
| | Power Down Mode, No Clock Running | | 50 | | µW |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –40 | | +85 | °C |
| Storage | | –65 | | +150 | °C |

* These specifications need to be added based on performance of final silicon.

NOTES: (1) All specifications in dB are referred to a full-scale input range. (2) Over this range, total error will typically not exceed ±1LSB. (3) In this mode, the ADS7832 acquires the input signal for five clock cycles after a start command, before the input is held and conversion begins. (4) LSB means Least Significant Bit. For a 0V to 5V input range, one LSB is 1.22mV. For a 0V to 2.5V input range, one LSB is 610µV.

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# SPECIFICATIONS

## ADS7832 Electrical Specifications with 5V Supply

$V_A = V_D = 5V$ ±10%; $V_{REF}+ = 5.0V$; $V_{REF}-$ = AGND = DGND = 0V; CLK = 1MHz external 50% ±2% Duty Cycle, $T_A$ = –40°C to +85°C, after calibration at any temperature, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7832BP/ADS7832BN MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | | 12 | Bits |
| **ANALOG INPUT** | | | | | |
| Voltage Input Range | $V_D = V_A = V_{REF}+ = 5V$ | 0 | | 5 | V |
| Input Capacitance | | | 40 | | pF |
| On State Bias Current | | | | 100 | nA |
| Off State Bias Current | $T_A$ = +25°C | | | 10 | nA |
| | $T_A$ = –40°C to +85°C | | | 100 | nA |
| On Resistance Multiplexer | | | 400 | | Ω |
| Off Resistance Multiplexer | | | 10 | | MΩ |
| Channel Separation | $F_{IN}$ = 1kHz, $V_D = V_A = V_{REF}+ = 5V$ | | 0.5 | | LSB |
| **REFERENCE INPUT** | | | | | |
| For Specified Performance: | $V_{REF} = V_A = 5V$ | | | | |
| $V_{REF}+$ | | | $V_A$ | | V |
| $V_{REF}-$ | | | 0 | | V |
| For Derated Performance[2]: | $(V_{REF}+) - (V_{REF}-) \geq 2.5V$ | | | | |
| $V_{REF}+$ | | 2.5 | | $V_A$ | V |
| $V_{REF}-$ | | 0 | | 1 | V |
| Input Reference Current | | | 100 | 200 | µA |
| **THROUGHPUT SPEED** | | | | | |
| Conversion Time With External Clock (Including Multiplexer Settling Time and Acquisition Time) | CLK = 2MHz | | | 8.5 | µs |
| | CLK = 1MHz | | | 17 | µs |
| | CLK = 500kHz | | | 34 | µs |
| With Internal Clock Using Recommended Clock Components | $T_A$ = +25°C | | 30 | | µs |
| | $T_A$ = –40°C to +85°C | | 30 | | µs |
| Slew Rate | | 2 | | | mV/µs |
| Multiplexer Settling Time to 1/2 LSB | | | 0.5 | | µs |
| Multiplexer Access Time | | | 20 | | ns |
| **SAMPLING DYNAMICS** | | | | | |
| Full Power Bandwidth | –3dB | | 4 | | MHz |
| Aperture Jitter | | | 10 | | ps |
| Aperture Delay | SRF D2 LOW[3] | | 2.5 | | µs |
| | SFR D2 HIGH | | 5 | | ns |
| **DC ACCURACY** | | | | | |
| Integral Nonlinearity, All Channels | SFR D2 LOW | | | ±0.75 | LSB[4] |
| | SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock | | ±0.5 | | LSB |
| | SFR D2 HIGH, Sampling Command Asynchronous to External Clock | | ±0.6 | | LSB |
| Differential Nonlinearity | | | | ±0.75 | LSB |
| No Missing Codes | | | Guaranteed | | |
| Gain Error | All Channels | | | ±0.75 | LSB |
| Gain Error Drift | Between Calibration Cycles | | ±0.2 | | ppm/°C |
| Offset Error | All Channels | | | | |
| | SFR D2 LOW | | | ±0.75 | LSB |
| | SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock | | ±1 | | LSB |
| | SFR D2 HIGH, Sampling Command Asynchronous to External Clock | | ±4 | | LSB |
| Offset Error Drift | Between Calibration Cycles | | | | |
| | SFR D2 LOW | | ±0.2 | | ppm/°C |
| | SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock | | ±0.5 | | ppm/°C |
| | SFR D2 HIGH, Sampling Command Asynchronous to External Clock | | ±1 | | ppm/°C |
| Channel-to-Channel Mismatch | SFR D2 LOW | | ±0.25 | | LSB |
| | SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock | | ±0.5 | | LSB |
| | SFR D2 HIGH, Sampling Command Asynchronous to External Clock | | ±1.0 | | LSB |
| Power Supply Sensitivity | $V_D = V_A$ = +5V ±10% (without recalibration) | | ±0.125 | | LSB |

# SPECIFICATIONS (CONT)

## ADS7832 Electrical Specifications with 5V Supply

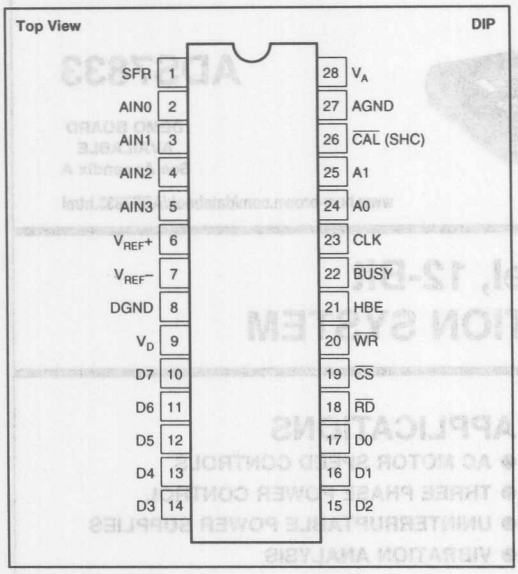
$V_A = V_D = 5V \pm 10\%$; $V_{REF}+ = 2.5V$; $V_{REF}- = AGND = DGND = 0V$; CLK = 1MHz external 50% ±2% Duty Cycle, $T_A = -40°C$ to $+85°C$, after calibration at any temperature, unless otherwise specified.

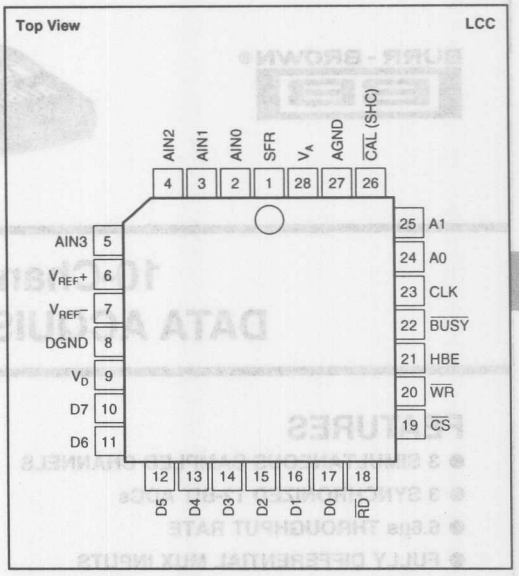
| PARAMETER | CONDITIONS | ADS7832BP/ADS7832BN MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **AC ACCURACY** | | | | | |
| Signal-to-(Noise + Distortion) Ratio | $f_{IN}$ = 1kHz | 69 | 71 | | dB(1) |
| | $f_{IN}$ = 50kHz | 66 | 69 | | dB |
| Total Harmonic Distortion | $f_{IN}$ = 50kHz | | –75 | | dB |
| Signal-to-Noise Ratio | $f_{IN}$ = 50kHz | | 70 | | dB |
| Spurious Free Dynamic Range | $f_{IN}$ = 1kHz | | 85 | | dB |
| | $f_{IN}$ = 50kHz | | 82 | | dB |
| **DIGITAL INPUTS** | | | | | |
| Voltage Levels: $V_{IL}$ | CLK | –0.3 | | 0.8 | V |
| $V_{IH}$ | CLK | 3.5 | | $V_D$ +0.3V | V |
| $V_{IL}$ | All Others | –0.3 | | 0.8 | V |
| $V_{IH}$ | All Others | 2.4 | | $V_D$ +0.3V | V |
| Current Levels: $I_{IL}$ | CAL (Internal Pull-Up) | | 10 | | µA |
| $I_{IL}$ | All Other Inputs | | | ±10 | µA |
| $I_{IH}$ | SFR (Internal Pull-Down) | | 90 | | µA |
| $I_{IH}$ | CLK | | | 1.5 | mA |
| $I_{IH}$ | All Other Inputs | | | ±10 | µA |
| $I_{IH}$ | Power Down Mode (SFR D3 HIGH) | | | ±100 | nA |
| **DIGITAL OUTPUTS** | | | | | |
| Data Format | Parallel 12 Bits in Two Bytes | | | | |
| Data Coding | Straight Binary | | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | 0.4 | V |
| $V_{OH}$ | $I_{SOURCE}$ = 200µA | 4 | | | V |
| Leakage Current | High-Z State | | | ±1 | µA |
| Output Capacitance | High-Z State | | 4 | | pF |
| **CALIBRATION TIMING** | | | | | |
| Calibration Cycle | Power On or Power Failure | | | 37393 | Clock Cycles |
| Calibration Cycle | During Normal Operation | | | 4625 | Clock Cycles |
| **DIGITAL TIMING** | | | | | |
| Bus Access Time | | | | 83 | ns |
| Bus Relinquish Time | | | | 83 | ns |
| **POWER SUPPLIES** | | | | | |
| Supply Voltage for Specified Performance: $V_A$ | Tested at 5.5V | | 5 | 5.5 | V |
| $V_D$ | Tested at 5.5V | | 5 | 5.5 | V |
| Supply Current: $I_A$ | Tested at 5.5V | | 2.5 | 5.5 | mA |
| $I_D$ | Tested at 5.5V | | 300 | 500 | µA |
| Power Dissipation | Power Up Mode or During Conversion | | 14 | | mW |
| | Power Down Mode, No Clock Running | | 50 | | µW |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –40 | | 85 | °C |
| Storage | | –65 | | 150 | °C |

*These specifications need to be added based on performance of final silicon.

NOTES: (1) All specifications in dB are referred to a full-scale input range. (2) Over this range, total error will typically not exceed ±1LSB. (3) In this mode, the ADS7832 acquires the input signal for five clock cycles after a start command, before the input is held and conversion begins. (4) LSB means Least Significant Bit. For a 0V to 5V input range, one LSB is 1.22mV. For a 0V to 2.5V input range, one LSB is 610µV.

## PIN CONFIGURATIONS




## PACKAGE/ORDERING INFORMATION

| PRODUCT | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO, dB | INTEGRAL NONLINEARITY MAXIMUM LSB | SPECIFICATION TEMPERATURE RANGE | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|---|---|---|
| ADS7832BN | 69 | ±3/4 | –40°C to +85°C | 28-Pin LCC | 251 |
| ADS7832BP | 69 | ±3/4 | –40°C to +85°C | 28-Pin Plastic DIP | 215 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $V_A$ to Analog Ground | 7V |
| $V_D$ to Digital Ground | 7V |
| $V_A$ to $V_D$ | ±0.3V |
| Analog Ground to Digital Ground | ±0.3V |
| Control Inputs to Digital Ground | –0.3V to $V_D$ + 0.3V |
| Analog Input Voltage to Analog Ground | –0.3V to $V_A$ + 0.3V |
| Maximum Junction Temperature | 150°C |
| Internal Power Dissipation | 875mW |
| Lead Temperature (soldering, 10s) | +260°C |
| (soldering, 3s) | +360°C |
| Thermal Resistance, $\theta_{JA}$ | 75°C/W |
| Maximum Input Current to Any Pin | ±50mA |
| ESD: Human Body Model | 1kV |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®




# ADS7833

**DEMO BOARD AVAILABLE**
**See Appendix A**

www.burr-brown.com/databook/ADS7833.html

# 10-Channel, 12-Bit DATA ACQUISITION SYSTEM

## FEATURES

- 3 SIMULTANEOUS SAMPLED CHANNELS
- 3 SYNCHRONIZED 12-BIT ADCs
- 6.6µs THROUGHPUT RATE
- FULLY DIFFERENTIAL MUX INPUTS
- DIGITALLY SELECTABLE INPUT RANGES
- ±5V POWER SUPPLIES
- SERIAL DIGITAL INPUT/OUTPUTS
- 2 SIMULTANEOUS SAMPLED AUXILIARY CHANNELS
- DIRECT INTERFACE TO MOTOROLA'S DSP56004/7

## APPLICATIONS

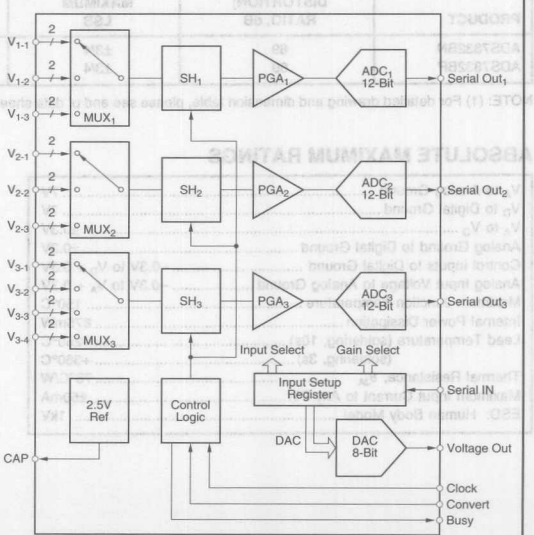
- AC MOTOR SPEED CONTROLS
- THREE PHASE POWER CONTROL
- UNINTERRUPTABLE POWER SUPPLIES
- VIBRATION ANALYSIS
- PC DATA ACQUISITION
- MEDICAL INSTRUMENTATION

## DESCRIPTION

The ADS7833 consists of three 12-bit analog-to-digital converters preceded by three simultaneously operating sample-hold amplifiers, and multiplexers for 10 differential inputs. The ADCs have simultaneous serial outputs for high speed data transfer and data processing.

The ADS7833 also offers a programmable gain amplifier with programmable gains of 1.0V/V, 1.25V/V, 2.5V/V, and 5.0V/V. Channel selection and gain selection are selectable through the serial input control word. The high through put rate is maintained by simultaneously clocking in the 13-bit input control word for the next conversion while the present conversions are clocked out.

The part also contains an 8-bit digital-to-analog converter whose digital input is supplied as part of the input control word.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
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# SPECIFICATIONS

At $V_{ANA+}$ = +5V, $V_{ANA-}$ = –5V, $V_{DIG+}$ = +5V, $V_{DIG-}$ = –5V, and $T_A$ = –40°C to +85°C, using internal reference, $f_{CLOCK}$ = 2.1MHz.

## ANALOG-TO-DIGITAL CONVERTER CHANNELS

| PARAMETER | CONDITIONS | ADS7833N MIN | ADS7833N TYP | ADS7833N MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | 12 | | | Bit |
| **ANALOG INPUT** | | | | | |
| Full Scale Voltage, Differential | G = 1.0V/V | | ±2.5 | | V |
| | G = 1.25V/V | | ±2.0 | | V |
| | G = 2.5V/V | | ±1.0 | | V |
| | G = 5.0V/V | | ±0.5 | | V |
| Common-Mode Voltage | | ±0.5 | See Table VII | | V |
| Impedance | | | $10^{12}$ | | Ω |
| Capacitance | | | 20 | | pF |
| **THROUGHPUT SPEED** | | | | | |
| Conversion Time | CLK = 2.1MHz | | | 6.1 | µs |
| Complete Cycle | Acquire and Convert | | | 6.6 | µs |
| Throughput Rate | | 150 | 200 | | kHz |
| **SAMPLING DYNAMICS** | | | | | |
| S/H Droop Rate | | | 0.1 | | µV/µs |
| S/H Acquisition Time | | | 0.5 | | µs |
| S/H Aperture Delay | | | 50 | | ns |
| S/H Aperture Jitter | | | 50 | | ps |
| Sampling Skew, Channel-to-Channel | | | 3 | | ns |
| **DC ACCURACY** | | | | | |
| Integral Linearity - ADC | | | ±0.5 | ±2 | LSB |
| Differential Linearity - ADC | | | ±0.5 | | LSB |
| No Missing Codes | | 12 | | | Bits |
| Integral Linearity - Asynchronous, Synchronous | | | 0.5 | ±3 | LSB |
| Differential Linearity - Asynchronous, Synchronous | | | 0.5 | ±3 | LSB |
| Full Scale Error | G = 1.0V/V | | | 2 | % of FSR |
| Full Scale Error Other Gains | | | | 4 | % of FSR |
| Full Scale Error Drift | G = 1.0V/V | | ±10 | ±100 | ppm/°C |
| | G = 2.5V/V | | ±10 | ±100 | ppm/°C |
| Zero Error - ADC | G = 1.0V/V | | ±0.5 | ±15 | LSB |
| Zero Error - Asynchronous, Synchronous | G = 1.0V/V | | ±0.5 | ±20 | LSB |
| Zero Error Drift | G = 1.0V/V | | ±0.5 | | ppm/°C |
| **AC ACCURACY** | | | | | |
| Total Harmonic Distortion | | | | | |
| $f_{IN}$ = 1kHz | | | 92 | | dB |
| $f_{IN}$ = 1MHz | | | 72 | | dB |
| CMR | $V_{CM}$ = 1V, $f_{CM}$ = 1MHz | | 40 | | dB |
| **REFERENCE** | | | | | |
| Internal Reference Voltage | | | 2.5 | | V |
| Internal Reference Accuracy | | | ±0.25 | | % |
| Internal Reference Drift | | | ±10 | | ppm/°C |
| Internal Reference Source Current | | | 10 | | µA |
| External Reference Voltage Range for Specified Linearity | | 2.25 | 2.5 | 2.75 | V |
| External Reference Current Drain | | | 10 | | µA |
| **DIGITAL INPUTS** | | | | | |
| Logic Levels | | | | | |
| $V_{IL}$ | | 0 | | 1.5 | V |
| $V_{IH}$ | | +3.5 | | +5 | V |
| $I_{IL}$ | | | | ±10 | µA |
| $I_{IH}$ | | | | ±10 | µA |
| Input Capacitance | At All Digital Input Pins | | | 15 | pF |
| **DIGITAL OUTPUTS** | | | | | |
| Data Format | | | 12-Bit Serial | | |
| Data Coding | | | BTC | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | 0 | | 0.4 | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | 4.2 | | 5 | V |
| Leakage Current | | | | ±5 | µA |
| Output Capacitance | At All Digital Output Pins | | | 15 | pF |

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

# SPECIFICATIONS (CONT)

At $V_{ANA+}$ = +5V, $V_{ANA-}$ = –5V, $V_{DIG+}$ = +5V, $V_{DIG-}$ = –5V, and $T_A$ = –40°C to +85°C, using internal reference, $f_{CLOCK}$ = 2.1MHz.

## ANALOG-TO-DIGITAL CONVERTER CHANNELS

| PARAMETER | CONDITIONS | ADS7833N MIN | ADS7833N TYP | ADS7833N MAX | UNITS |
|---|---|---|---|---|---|
| **POWER SUPPLIES** | Specified Performance | | | | |
| $V_{ANA+}$ | | +4.75 | +5.0 | +5.25 | V |
| $V_{ANA-}$ | | –4.75 | –5.0 | –5.25 | V |
| $V_{DIG+}$ | | +4.75 | +5.0 | +5.25 | V |
| $V_{DIG-}$ | | –4.75 | –5.0 | –5.25 | V |
| $I_{ANA+}$ | | | 15 | 25 | mA |
| $I_{ANA-}$ | | | 8 | 10 | mA |
| $I_{DIG+}$ | | | 3 | 5 | mA |
| $I_{DIG-}$ | | | 1 | 2 | mA |
| Power Dissipation | | | 125 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified Performance | | –40 | | +85 | °C |
| Derated Performance | | –55 | | +125 | °C |
| Storage | | –65 | | +150 | °C |

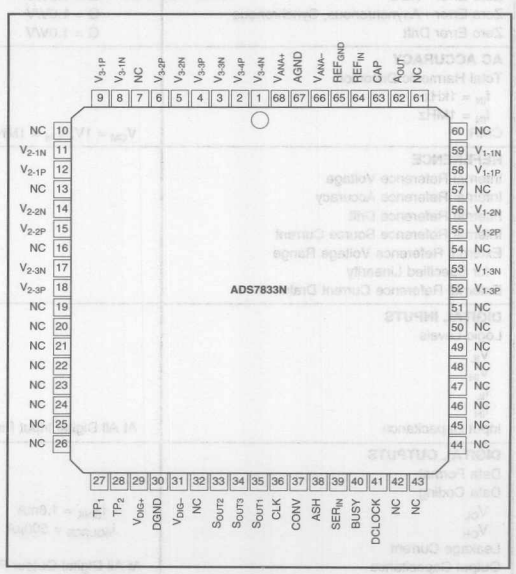
## DIGITAL-TO-ANALOG CONVERTER

| PARAMETER | CONDITIONS | ADS7833N MIN | ADS7833N TYP | ADS7833N MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | 8-Bits | | | |
| Output Range | | 0 | | +2.5 | V |
| Output Settling Time | To 0.5LSB | | | 1 | µs |
| Linearity Error | | | | ±1 | LSB |
| Differential Linearity | | | | ±1 | LSB |
| Output Current | | | 200 | | µA |
| Offset Error | | | ±1 | 10 | mV |
| Full Scale Error | | | | 2 | % |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Input Voltage | ±25V |
| Ground Voltage Difference: AGND and DGND | ±0.3V |
| Power Supply Voltages: | |
| $V_{ANA+}$ | +7V |
| $V_{ANA-}$ | –7V |
| $V_{DIG+}$ | +7V |
| $V_{DIG-}$ | –7V |
| Digital Inputs | –0.3V to $V_{DIG}$ +0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |

## PIN CONFIGURATION




## CONVERSION AND DATA TIMING

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | A/D Conversion Time | 6.6 | 4.0 | | µs |
| CLK | A/D Conversion Clock | 2.1 | 2.8 | | MHz |
| $t_1$ | Setup Time for Conversion Before Rising Edge of Clock | 50 | | | ns |
| $t_2$ | Hold Time for Conversion After Rising Edge of Clock | 50 | | | ns |
| $t_3$ | Setup Time for Serial Out | | | 25 | ns |
| $t_4$ | Setup Time for Serial Input | 30 | | | ns |
| $t_5$ | Hold Time for Serial Input | 30 | | | ns |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ADS7833N | 68-Lead PLCC | 312 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN DEFINITIONS

| PIN NO | NAME | TYPE[1] | DESCRIPTION | PIN NO | NAME | TYPE[1] | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| 1 | $V_{3-4N}$ | AI | Voltage Input, Channel 3, Mux I/P 4, Negative Side | 35 | $S_{OUT1}$ | DO | Serial Digital Output, Channel 1 |
| | | | | 36 | CLK | DI | Clock for A/D Converters |
| 2 | $V_{3-4P}$ | AI | Voltage Input, Channel 3, Mux IP 4, Positive Side | 37 | CONV | DI | Start A/D Converters. When CONV goes to "0" (low) the next rising edge of CLK starts the conversion. |
| 3 | $V_{3-3N}$ | AI | Voltage Input, Channel 3, Mux I/P 3, Negative Side | 38 | ASH | DI | Digital Control for Asynchronous Sample Hold. If signal is "1" (high), signals are sampled. |
| 4 | $V_{3-3P}$ | AI | Voltage Input, Channel 3, Mux I/P 3, Positive Side | | | | |
| | | | | 39 | $SER_{IN}$ | DI | Serial Digital Input for Input Control Word |
| 5 | $V_{3-2N}$ | AI | Voltage Input, Channel 3, Mux I/P 2, Negative Side | 40 | BUSY | DO | A/D Converters Busy. Busy if signal is "0" (low). |
| 6 | $V_{3-2P}$ | AI | Voltage Input, Channel 3, Mux I/P 2, Positive Side | 41 | DCLOCK | DO | A Delayed and Truncated Version of the CLK Signals. It is Delayed 50ns from the CLK Signal and Stays Low after 13 DCLOCK Cycles. |
| 7 | NC | — | No Connection | | | | |
| 8 | $V_{3-1N}$ | AI | Voltage Input, Channel 3, Mux I/P 1, Negative Side | 42 | NC | — | No Connection |
| 9 | $V_{3-1P}$ | AI | Voltage Input, Channel 3, Mux I/P 1, Positive Side | 43 | NC | — | No Connection |
| | | | | 44 | NC | — | No Connection |
| 10 | NC | — | No Connection | 45 | NC | — | No Connection |
| 11 | $V_{2-1N}$ | AI | Voltage Input, Channel 2, Mux I/P 1, Negative Side | 46 | NC | — | No Connection |
| | | | | 47 | NC | — | No Connection |
| 12 | $V_{2-1P}$ | AI | Voltage Input, Channel 2, Mux I/P 1, Positive Side | 48 | NC | — | No Connection |
| | | | | 49 | NC | — | No Connection |
| 13 | NC | — | No Connection | 50 | NC | — | No Connection |
| 14 | $V_{2-2N}$ | AI | Voltage Input, Channel 2, Mux I/P 2, Negative Side | 51 | NC | — | No Connection |
| | | | | 52 | $V_{1-3P}$ | AI | Voltage Input, Channel 1, Mux I/P 3, Positive Side |
| 15 | $V_{2-2P}$ | AI | Voltage Input, Channel 2, Mux I/P 2, Positive Side | 53 | $V_{1-3N}$ | AI | Voltage Input, Channel 1, Mux I/P 3, Negative Side |
| 16 | NC | — | No Connection | | | | |
| 17 | $V_{2-3N}$ | AI | Voltage Input, Channel 2, Mux I/P 3, Negative Side. | 54 | NC | — | No Connection |
| | | | | 55 | $V_{1-2P}$ | AI | Voltage Input, Channel 1, Mux I/P 2, Positive Side |
| 18 | $V_{2-3P}$ | AI | Voltage Input, Channel 2, Mux I/P 3, Positive Side | 56 | $V_{1-2N}$ | AI | Voltage Input, Channel 1, Mux I/P 2, Negative Side |
| 19 | NC | — | No Connection | | | | |
| 20 | NC | — | No Connection | 57 | NC | — | No Connection |
| 21 | NC | — | No Connection | 58 | $V_{1-1P}$ | AI | Voltage Input, Channel 1, Mux I/P 1, Positive Side |
| 22 | NC | — | No Connection | | | | |
| 23 | NC | — | No Connection | 59 | $V_{1-1N}$ | AI | Voltage Input, Channel 1, Mux I/P 1, Negative Side |
| 24 | NC | — | No Connection | | | | |
| 25 | NC | — | No Connection | 60 | NC | — | No Connection |
| 26 | NC | — | No Connection | 61 | NC | — | No Connection |
| 27 | TP1 | — | Test Point 1, Make No Connection | 62 | $A_{OUT}$ | AO | Output of DAC |
| 28 | TP2 | — | Test Point 2, Make No Connection | 63 | CAP | AO | Decoupling Point for Internal Reference |
| 29 | $V_{DIG+}$ | P | Digital Supply Voltage, +5V | 64 | $REF_{IN}$ | AI | Input Pin for External Reference |
| 30 | DGND | P | Digital Supply Voltage, Ground | 65 | $REF_{GND}$ | P | Ground Pin for External Reference |
| 31 | $V_{DIG-}$ | P | Digital Supply Voltage, –5V | 66 | $V_{ANA-}$ | P | Analog Supply Voltage, –5V |
| 32 | NC | — | No Connection | 67 | AGND | P | Analog Supply Voltage, Ground |
| 33 | $S_{OUT2}$ | DO | Serial Digital Output, Channel 2 | 68 | $V_{ANA+}$ | P | Analog Supply Voltage, +5V |
| 34 | $S_{OUT3}$ | DO | Serial Digital Output, Channel 3 | | | | |

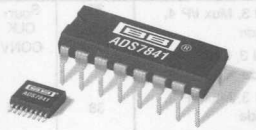
NOTE: (1) AI is Analog Input, AO is Analog Output, DI is Digital Input, DO is Digital Output, P is Power Supply Connection.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR - BROWN®



# ADS7841

www.burr-brown.com/databook/ADS7841.html

# 12-Bit, 4-Channel Serial Output Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- SINGLE SUPPLY: 2.7V to 5V
- 4-CHANNEL SINGLE-ENDED OR 2-CHANNEL DIFFERENTIAL INPUT
- UP TO 200kHz CONVERSION RATE
- ±1 LSB MAX INL AND DNL
- GUARANTEED NO MISSING CODES
- 72dB SINAD
- SERIAL INTERFACE
- 16-PIN PDIP OR 16-LEAD SSOP PACKAGE
- ALTERNATE SOURCE FOR MAX1247

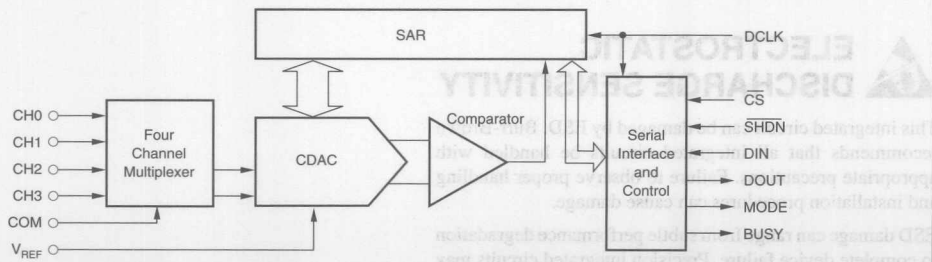
## APPLICATIONS

- DATA ACQUISITION
- TEST AND MEASUREMENT
- INDUSTRIAL PROCESS CONTROL
- PERSONAL DIGITAL ASSISTANTS
- BATTERY-POWERED SYSTEMS

## DESCRIPTION

The ADS7841 is a 4-channel, 12-bit sampling analog-to-digital converter (ADC) with a synchronous serial interface. The resolution is programmable to either 8 or 12 bits. Typical power dissipation is 2mW at a 200kHz throughput rate and a +5V supply. The reference voltage ($V_{REF}$) can be varied between 100mV and $V_{CC}$, providing a corresponding input voltage range of 0V to $V_{REF}$. The device includes a shutdown mode which reduces power dissipation to under 15µW. The ADS7841 is guaranteed down to 2.7V operation.

Low power, high speed, and on-board multiplexer make the ADS7841 ideal for battery operated systems such as personal digital assistants, portable multi-channel data loggers, and measurement equipment. The serial interface also provides low-cost isolation for remote data acquisition. The ADS7841 is available in a 16-pin PDIP or a 16-lead SSOP package and is guaranteed over the –40°C to +85°C temperature range.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132



BURR - BROWN®

# SPECIFICATION: +5V

At $T_A$ = –40°C to +85°C, $+V_{CC}$ = +5V, $V_{REF}$ = +5V, $f_{SAMPLE}$ = 200kHz, and $f_{CLK}$ = 16 • $f_{SAMPLE}$ = 3.2MHz, unless otherwise noted.

| PARAMETER | CONDITIONS | ADS7841E, P | | | ADS7841EB, PB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ANALOG INPUT** | | | | | | | | |
| Full-Scale Input Span | Positive Input - Negative Input | 0 | | $V_{REF}$ | * | | * | V |
| Absolute Input Range | Positive Input | –0.2 | | $+V_{CC}$ +0.2 | * | | * | V |
| | Negative Input | –0.2 | | +1.25 | * | | * | V |
| Capacitance | | | 25 | | | * | | pF |
| Leakage Current | | | ±1 | | | * | | µA |
| **SYSTEM PERFORMANCE** | | | | | | | | |
| Resolution | | | 12 | | | * | | Bits |
| No Missing Codes | | 12 | | | 12 | | | Bits |
| Integral Linearity Error | | | | ±2 | | | ±1 | LSB[1] |
| Differential Linearity Error | | | ±0.8 | | | ±0.5 | ±1 | LSB |
| Offset Error | | | | ±3 | | | * | LSB |
| Offset Error Match | | | 0.15 | 1.0 | | * | * | LSB |
| Gain Error | | | | ±4 | | | ±3 | LSB |
| Gain Error Match | | | 0.1 | 1.0 | | * | * | LSB |
| Noise | | | 30 | | | * | | µVrms |
| Power Supply Rejection | | | 70 | | | * | | dB |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Conversion Time | | | | 12 | | | * | Clk Cycles |
| Acquisition Time | | 3 | | | * | | | Clk Cycles |
| Throughput Rate | | | | 200 | | | * | kHz |
| Multiplexer Settling Time | | | 500 | | | * | | ns |
| Aperture Delay | | | 30 | | | * | | ns |
| Aperture Jitter | | | 100 | | | * | | ps |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | |
| Total Harmonic Distortion[2] | $V_{IN}$ = 5Vp-p at 10kHz | | –78 | –72 | | –80 | –76 | dB |
| Signal-to-(Noise + Distortion) | $V_{IN}$ = 5Vp-p at 10kHz | 68 | 71 | | 70 | 72 | | dB |
| Spurious Free Dynamic Range | $V_{IN}$ = 5Vp-p at 10kHz | 72 | 79 | | 76 | 81 | | dB |
| Channel-to-Channel Isolation | $V_{IN}$ = 5Vp-p at 50kHz | | 120 | | | * | | dB |
| **REFERENCE INPUT** | | | | | | | | |
| Range | | 0.1 | | $+V_{CC}$ | * | | * | V |
| Resistance | DCLK Static | | 5 | | | * | | GΩ |
| Input Current | | | 40 | 100 | | * | * | µA |
| | $f_{SAMPLE}$ = 12.5kHz | | 2.5 | | | * | | µA |
| | DCLK Static | | 0.001 | 3 | | * | * | µA |
| **DIGITAL INPUT/OUTPUT** | | | | | | | | |
| Logic Family | | | CMOS | | | * | | |
| Logic Levels | | | | | | | | |
| $V_{IH}$ | $\lvert I_{IH} \rvert \leq +5\mu A$ | 3.0 | | 5.5 | * | | * | V |
| $V_{IL}$ | $\lvert I_{IL} \rvert \leq +5\mu A$ | –0.3 | | +0.8 | * | | * | V |
| $V_{OH}$ | $I_{OH}$ = –250µA | 3.5 | | | * | | | V |
| $V_{OL}$ | $I_{OL}$ = 250µA | | | 0.4 | | | * | V |
| Data Format | | | Straight Binary | | | * | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | |
| $+V_{CC}$ | Specified Performance | 4.75 | | 5.25 | * | | * | V |
| Quiescent Current | | | 550 | 900 | | | * | µA |
| | $f_{SAMPLE}$ = 12.5kHz | | 300 | | | * | | µA |
| | Power-Down Mode[3], $\overline{CS}$ = $+V_{CC}$ | | | 3 | | | * | µA |
| Power Dissipation | | | | 4.5 | | | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | °C |

* Same specifications as ADS7841E, P.

NOTE: (1) LSB means Least Significant Bit. With $V_{REF}$ equal to +5.0V, one LSB is 1.22mV. (2) First five harmonics of the test frequency. (3) Auto power-down mode (PD1 = PD0 = 0) active or $\overline{SHDN}$ = GND.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

# SPECIFICATION: +2.7V

At $T_A$ = –40°C to +85°C, $+V_{CC}$ = +2.7V, $V_{REF}$ = +2.5V, $f_{SAMPLE}$ = 125kHz, and $f_{CLK} = 16 \bullet f_{SAMPLE}$ = 2MHz, unless otherwise noted.

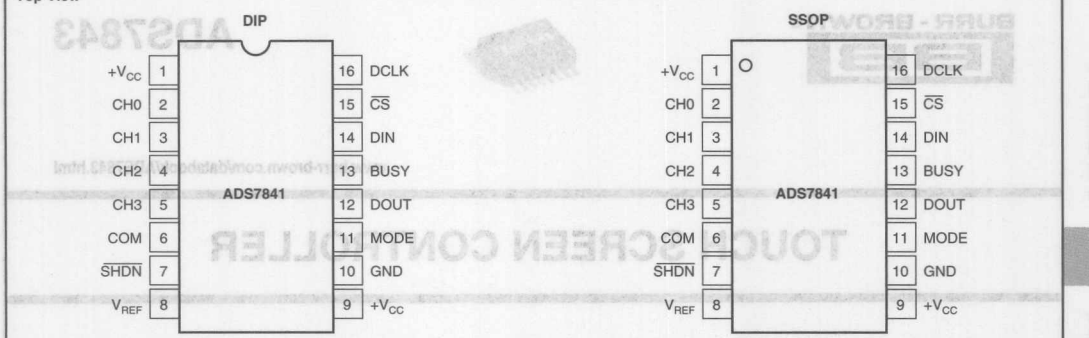
| PARAMETER | CONDITIONS | ADS7841E, P | | | ADS7841EB, PB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ANALOG INPUT** | | | | | | | | |
| Full-Scale Input Span | Positive Input - Negative Input | 0 | | $V_{REF}$ | * | | * | V |
| Absolute Input Range | Positive Input | –0.2 | | $+V_{CC}$ +0.2 | * | | * | V |
| | Negative Input | –0.2 | | +0.2 | * | | * | V |
| Capacitance | | | 25 | | | * | | pF |
| Leakage Current | | | ±1 | | | * | | µA |
| **SYSTEM PERFORMANCE** | | | | | | | | |
| Resolution | | | 12 | | | * | | Bits |
| No Missing Codes | | 12 | | | 12 | | | Bits |
| Integral Linearity Error | | | | ±2 | | | ±1 | LSB[1] |
| Differential Linearity Error | | | ±0.8 | | | ±0.5 | ±1 | LSB |
| Offset Error | | | | ±3 | | | * | LSB |
| Offset Error Match | | | 0.15 | 1.0 | | * | * | LSB |
| Gain Error | | | | ±4 | | | ±3 | LSB |
| Gain Error Match | | | 0.1 | 1.0 | | * | * | LSB |
| Noise | | | 30 | | | * | | µVrms |
| Power Supply Rejection | | | 70 | | | * | | dB |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Conversion Time | | | | 12 | | | * | Clk Cycles |
| Acquisition Time | | 3 | | | * | | | Clk Cycles |
| Throughput Rate | | | | 125 | | | * | kHz |
| Multiplexer Settling Time | | | 500 | | | * | | ns |
| Aperture Delay | | | 30 | | | * | | ns |
| Aperture Jitter | | | 100 | | | * | | ps |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | |
| Total Harmonic Distortion[2] | $V_{IN}$ = 2.5Vp-p at 10kHz | | –77 | –72 | | –79 | –76 | dB |
| Signal-to-(Noise + Distortion) | $V_{IN}$ = 2.5Vp-p at 10kHz | 68 | 71 | | 70 | 72 | | dB |
| Spurious Free Dynamic Range | $V_{IN}$ = 2.5Vp-p at 10kHz | 72 | 78 | | 76 | 80 | | dB |
| Channel-to-Channel Isolation | $V_{IN}$ = 2.5Vp-p at 50kHz | | 100 | | | * | | dB |
| **REFERENCE INPUT** | | | | | | | | |
| Range | | 0.1 | | $+V_{CC}$ | * | | * | V |
| Resistance | DCLK Static | | 5 | | | * | | GΩ |
| Input Current | | | 13 | 40 | | * | * | µA |
| | $f_{SAMPLE}$ = 12.5kHz | | 2.5 | | | * | | µA |
| | DCLK Static | | 0.001 | 3 | | * | * | µA |
| **DIGITAL INPUT/OUTPUT** | | | | | | | | |
| Logic Family | | | CMOS | | | * | | |
| Logic Levels | | | | | | | | |
| $V_{IH}$ | $I I_{IH} I \leq +5\mu A$ | $+V_{CC} \bullet 0.7$ | | 5.5 | * | | * | V |
| $V_{IL}$ | $I I_{IL} I \leq +5\mu A$ | –0.3 | | +0.8 | * | | * | V |
| $V_{OH}$ | $I_{OH}$ = –250µA | $+V_{CC} \bullet 0.8$ | | | * | | | V |
| $V_{OL}$ | $I_{OL}$ = 250µA | | | 0.4 | | | * | V |
| Data Format | | | Straight Binary | | | * | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | |
| $+V_{CC}$ | Specified Performance | 2.7 | | 3.6 | * | | * | V |
| Quiescent Current | | | 280 | 650 | | * | * | µA |
| | $f_{SAMPLE}$ = 12.5kHz | | 220 | | | * | | µA |
| | Power-Down Mode[3], $\overline{CS}$ = $+V_{CC}$ | | | 3 | | | * | µA |
| Power Dissipation | | | | 1.8 | | | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | °C |

* Same specifications as ADS7841E, P.

NOTE: (1) LSB means Least Significant Bit. With $V_{REF}$ equal to +2.5V, one LSB is 610mV. (2) First five harmonics of the test frequency. (3) Auto power-down mode (PD1 = PD0 = 0) active or $\overline{SHDN}$ = GND.

## PIN CONFIGURATIONS

Top View




## PIN DESCRIPTIONS

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | $+V_{CC}$ | Power Supply, 2.7V to 5V. |
| 2 | CH0 | Analog Input Channel 0. |
| 3 | CH1 | Analog Input Channel 1. |
| 4 | CH2 | Analog Input Channel 2. |
| 5 | CH3 | Analog Input Channel 3. |
| 6 | COM | Ground Reference for Analog Inputs. Sets zero code voltage in single-ended mode. Connect this pin to ground or ground reference point. |
| 7 | $\overline{SHDN}$ | Shutdown. When LOW, the device enters a very low power shutdown mode. |
| 8 | $V_{REF}$ | Voltage Reference Input |
| 9 | $+V_{CC}$ | Power Supply, 2.7V to 5V. |
| 10 | GND | Ground |
| 11 | MODE | Conversion Mode. When LOW, the device always performs a 12-bit conversion. When HIGH, the resolution is set by the MODE bit in the CONTROL byte. |
| 12 | DOUT | Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when $\overline{CS}$ is HIGH. |
| 13 | BUSY | Busy Output. This output is high impedance when $\overline{CS}$ is HIGH. |
| 14 | DIN | Serial Data Input. If $\overline{CS}$ is LOW, data is latched on rising edge of DCLK. |
| 15 | $\overline{CS}$ | Chip Select Input. Controls conversion timing and enables the serial input/output register. |
| 16 | DCLK | External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O. |

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| $+V_{CC}$ to GND | –0.3V to +6V |
| Analog Inputs to GND | –0.3V to $+V_{CC}$ + 0.3V |
| Digital Inputs to GND | –0.3V to +6V |
| Power Dissipation | 250mW |
| Maximum Junction Temperature | +150°C |
| Operating Temperature Range | –40°C to +85°C |
| Storage Temperature Range | –65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) (dB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|---|---|---|
| ADS7841E | ±2 | 68 | –40°C to +85°C | 16-Lead SSOP | 322 |
| ADS7841P | ±2 | 68 | –40°C to +85°C | 16-Pin PDIP | 180 |
| ADS7841EB | ±1 | 70 | –40°C to +85°C | 16-Lead SSOP | 322 |
| ADS7841PB | ±1 | 70 | –40°C to +85°C | 16-Pin PDIP | 180 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# ADS7843

www.burr-brown.com/databook/ADS7843.html

# TOUCH SCREEN CONTROLLER

## FEATURES

- 4-WIRE TOUCH SCREEN INTERFACE
- RATIOMETRIC CONVERSION
- SINGLE SUPPLY: 2.7V to 5V
- UP TO 125kHz CONVERSION RATE
- SERIAL INTERFACE
- PROGRAMMABLE 8- OR 12-BIT RESOLUTION
- 2 AUXILIARY ANALOG INPUTS
- FULL POWER-DOWN CONTROL

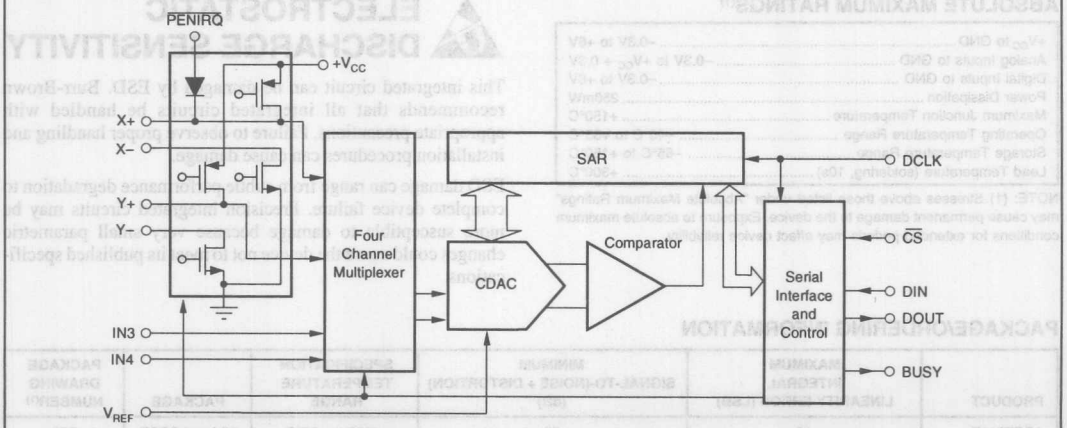
## APPLICATIONS

- PERSONAL DIGITAL ASSISTANTS
- PORTABLE INSTRUMENTS

## DESCRIPTION

The ADS7843 is a 12-bit sampling analog-to-digital converter (ADC) with a synchronous serial interface and low on-resistance switches for driving touch screens. Typical power dissipation is 750µW at a 125kHz throughput rate and a +2.7V supply. The reference voltage ($V_{REF}$) can be varied between 1V and $+V_{CC}$, providing a corresponding input voltage range of 0V to $V_{REF}$. The device includes a shutdown mode which reduces typical power dissipation to under 0.5µW. The ADS7843 is guaranteed down to 2.7V operation.

Low power, high speed, and on-board switches make the ADS7843 ideal for battery operated systems such as personal digital assistants with resistive touch screens and other portable equipment. The ADS7843 is available in a 16-lead SSOP package and is guaranteed over the –40°C to +85°C temperature range.




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# SPECIFICATIONS

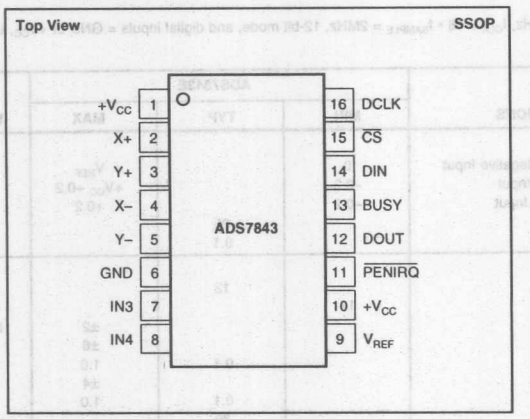
At $T_A$ =–40°C to +85°C, $+V_{CC}$ = +2.7V, $V_{REF}$ = +2.5V, $f_{SAMPLE}$ = 125kHz, $f_{CLK}$ = 16 • $f_{SAMPLE}$ = 2MHz, 12-bit mode, and digital inputs = GND or $+V_{CC}$, unless otherwise noted.

| PARAMETER | CONDITIONS | ADS7843E MIN | ADS7843E TYP | ADS7843E MAX | UNITS |
|---|---|---|---|---|---|
| **ANALOG INPUT** | | | | | |
| Full-Scale Input Span | Positive Input - Negative Input | 0 | | $V_{REF}$ | V |
| Absolute Input Range | Positive Input | –0.2 | | $+V_{CC}$ +0.2 | V |
| | Negative Input | –0.2 | | +0.2 | V |
| Capacitance | | | 25 | | pF |
| Leakage Current | | | 0.1 | | µA |
| **SYSTEM PERFORMANCE** | | | | | |
| Resolution | | | 12 | | Bits |
| No Missing Codes | | 11 | | | Bits |
| Integral Linearity Error | | | | ±2 | LSB(1) |
| Offset Error | | | | ±6 | LSB |
| Offset Error Match | | | 0.1 | 1.0 | LSB |
| Gain Error | | | | ±4 | LSB |
| Gain Error Match | | | 0.1 | 1.0 | LSB |
| Noise | | | 30 | | µVrms |
| Power Supply Rejection | | | 70 | | dB |
| **SAMPLING DYNAMICS** | | | | | |
| Conversion Time | | | | 12 | Clk Cycles |
| Acquisition Time | | 3 | | | Clk Cycles |
| Throughput Rate | | | | 125 | kHz |
| Multiplexer Settling Time | | | 500 | | ns |
| Aperture Delay | | | 30 | | ns |
| Aperture Jitter | | | 100 | | ps |
| Channel-to-Channel Isolation | $V_{IN}$ = 2.5Vp-p at 50kHz | | 100 | | dB |
| **SWITCH DRIVERS** | | | | | |
| On-Resistance | | | | | |
| Y+, X+ | | | 5 | | Ω |
| Y–, X– | | | 6 | | Ω |
| **REFERENCE INPUT** | | | | | |
| Range | | 1.0 | | $+V_{CC}$ | V |
| Resistance | $\overline{CS}$ = GND or $+V_{CC}$ | | 5 | | GΩ |
| Input Current | | | 13 | 40 | µA |
| | $f_{SAMPLE}$ = 12.5kHz | | 2.5 | | µA |
| | $\overline{CS}$ = $+V_{CC}$ | | 0.001 | 3 | µA |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic Family | | | CMOS | | |
| Logic Levels, Except $\overline{PENIRQ}$ | | | | | |
| $V_{IH}$ | $\lvert I_{IH} \rvert \leq +5\mu A$ | $+V_{CC}$ • 0.7 | | $+V_{CC}$ +0.3 | |
| $V_{IL}$ | $\lvert I_{IL} \rvert \leq +5\mu A$ | –0.3 | | +0.8 | V |
| $V_{OH}$ | $I_{OH}$ = –250µA | $+V_{CC}$ • 0.8 | | | V |
| $V_{OL}$ | $I_{OL}$ = 250µA | | | 0.4 | V |
| $\overline{PENIRQ}$ | | | | | |
| $V_{OL}$ | $T_A$ = 0°C to +85°C, 100kΩ Pull-Up | | | 0.8 | V |
| Data Format | | | Straight Binary | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| $+V_{CC}$ | Specified Performance | 2.7 | | 3.6 | V |
| Quiescent Current | | | 280 | 650 | µA |
| | $f_{SAMPLE}$ = 12.5kHz | | 220 | | µA |
| | Shut Down Mode with DCLK = DIN = $+V_{CC}$ | | | 3 | µA |
| Power Dissipation | $+V_{CC}$ = +2.7V | | | 1.8 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified Performance | | –40 | | +85 | °C |

NOTE: (1) LSB means Least Significant Bit. With $V_{REF}$ equal to +2.5V, one LSB is 610µV.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN CONFIGURATION




## PIN DESCRIPTION

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | $+V_{CC}$ | Power Supply, 2.7V to 5V. |
| 2 | X+ | X+ Position Input. ADC input Channel 1. |
| 3 | Y+ | Y+ Position Input. ADC input Channel 2. |
| 4 | X– | X– Position Input. |
| 5 | Y– | Y– Position Input. |
| 6 | GND | Ground |
| 7 | IN3 | Auxiliary Input 1. ADC input Channel 3. |
| 8 | IN4 | Auxiliary Input 2. ADC input Channel 4. |
| 9 | $V_{REF}$ | Voltage Reference Input |
| 10 | $+V_{CC}$ | Power Supply, 2.7V to 5V. |
| 11 | $\overline{PENIRQ}$ | Pen Interrupt. Open anode output (requires 10kΩ to 100kΩ pull-up resistor externally). |
| 12 | DOUT | Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when $\overline{CS}$ is HIGH. |
| 13 | BUSY | Busy Output. This output is high impedance when $\overline{CS}$ is HIGH. |
| 14 | DIN | Serial Data Input. If $\overline{CS}$ is LOW, data is latched on rising edge of DCLK. |
| 15 | $\overline{CS}$ | Chip Select Input. Controls conversion timing and enables the serial input/output register. |
| 16 | DCLK | External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O. |

## ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|---|
| $+V_{CC}$ to GND | –0.3V to +6V |
| Analog Inputs to GND | –0.3V to $+V_{CC}$ + 0.3V |
| Digital Inputs to GND | –0.3V to $+V_{CC}$ + 0.3V |
| Power Dissipation | 250mW |
| Maximum Junction Temperature | +150°C |
| Operating Temperature Range | –40°C to +85°C |
| Storage Temperature Range | –65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

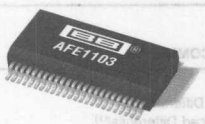
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE | PACKAGE DRAWING NUMBER(1) | TRANSPORT MEDIA(2) |
|---|---|---|---|---|---|
| ADS7843E | ±2 | –40°C to +85°C | 16-Lead SSOP | 322 | Rails - 100 |
| ADS7843E/2K5 | ±2 | –40°C to +85°C | 16-Lead SSOP | 322 | Tape and Reel - 2500 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Smaller quantities are available through authorized distribution.

BURR-BROWN®



# AFE1103

www.burr-brown.com/databook/AFE1103.html



# HDSL/MDSL ANALOG FRONT END

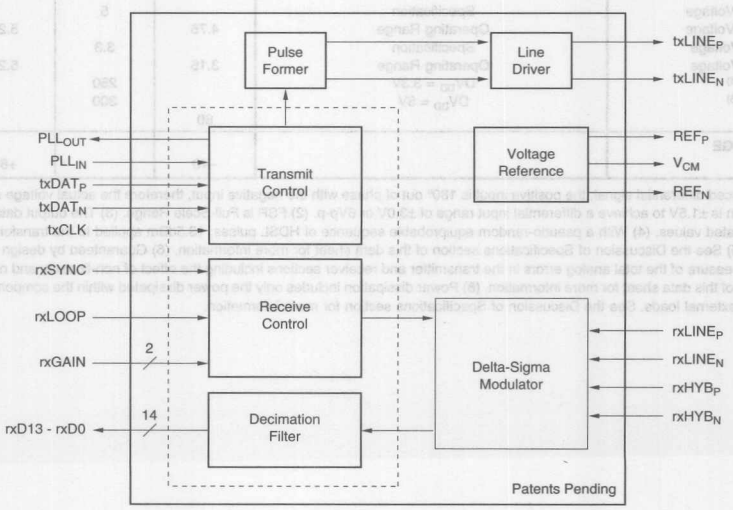
## FEATURES

- COMPLETE ANALOG INTERFACE
- T1, E1, AND MDSL OPERATION
- CLOCK SCALEABLE SPEED
- SINGLE CHIP SOLUTION
- +5V ONLY (5V OR 3.3V DIGITAL)
- 250mW POWER DISSIPATION
- 48-PIN SSOP
- –40°C TO +85°C OPERATION
- SECOND SOURCED BY BROOKTREE Bt8921

## DESCRIPTION

Burr-Brown's Analog Front End greatly reduces the size and cost of an HDSL or MDSL system by providing all of the active analog circuitry needed to connect the Brooktree Bt8952 HDSL digital signal processor to an external compromise hybrid and a 1:2 HDSL line transformer. All internal filter responses as well as the pulse former output scale with clock frequency—allowing the AFE1103 to operate over a range of bit rates from 196kbps to 1.168Mbps.

Functionally, this unit is separated into a transmit and a receive section. The transmit section generates, filters, and buffers outgoing 2B1Q data. The receive section filters and digitizes the symbol data received on the telephone line and passes it to the Bt8952. The HDSL Analog Interface is a monolithic device fabricated on 0.6µCMOS. It operates on a single +5V supply. It is housed in a 48-pin SSOP package. This unit is second sourced by Brooktree's Bt8921.




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# SPECIFICATIONS

Typical at 25°C, $AV_{DD}$ = +5V, $DV_{DD}$ = +3.3V, $f_{tx}$ = 584kHz (E1 rate), unless otherwise specified.

| PARAMETER | COMMENTS | AFE1103E MIN | AFE1103E TYP | AFE1103E MAX | UNITS |
|---|---|---|---|---|---|
| **RECEIVE CHANNEL** | | | | | |
| Number of Inputs | Differential | 2 | | | |
| Input Voltage Range | Balanced Differential(1) | | ±3.0 | | V |
| Common-Mode Voltage | 1.5V CMV Recommended | | +1.5 | | V |
| Input Impedance | All Inputs | | See Typical Performance Curves | | |
| Input Capacitance | | | 10 | | pF |
| Input Gain Matching | Line Input vs Hybrid Input | | ±2 | | % |
| Resolution | | 14 | | | Bits |
| Programmable Gain | Four Gains: 0dB, 3.25dB, 6dB, and 9dB | 0 | | 9 | dB |
| Settling Time for Gain Change | | | 6 | | Symbol Periods |
| Gain + Offset Error | Tested at Each Gain Range | | 5 | | %FSR(2) |
| Output Data Coding | | | Offset Binary | | |
| Output Data Rate, rxSYNC(3) | | 98 | | 584 | kHz |
| **TRANSMIT CHANNEL** | | | | | |
| Transmit Symbol Rate, $f_{tx}$ | | 98 | | 584 | kHz |
| T1 Transmit –3dB Point | Bellcore TA-NWT-3017 Compliant | | 196 | | kHz |
| T1 Rate Power Spectral Density(4) | | | See Typical Performance Curves | | |
| E1 Transmit –3dB Point | ETSI RTR/TM-03036 Compliant | | 292 | | kHz |
| E1 Rate Power Spectral Density(4) | | | See Typical Performance Curves | | |
| Transmit Power(4, 5) | | 13 | | 14 | dBm |
| Pulse Output | | | See Typical Performance Curves | | |
| Common-Mode Voltage, $V_{CM}$ | | | $AV_{DD}/2$ | | V |
| Output Resistance(6) | DC to 1MHz | | 1 | | Ω |
| **TRANSCEIVER PERFORMANCE** | | | | | |
| Uncancelled Echo(7) | rxGAIN = 0dB, Loopback Enabled | | | –67 | dB |
| | rxGAIN = 0dB, Loopback Disabled | | | –67 | dB |
| | rxGAIN = 3.25dB, Loopback Disabled | | | –69 | dB |
| | rxGAIN = 6dB, Loopback Disabled | | | –71 | dB |
| | rxGAIN = 9dB, Loopback Disabled | | | –73 | dB |
| **DIGITAL INTERFACE(6)** | | | | | |
| Logic Levels | | | | | |
| $V_{IH}$ | $\lvert I_{IH}\rvert$ < 10µA | $DV_{DD}$ –1 | | $DV_{DD}$ +0.3 | V |
| $V_{IL}$ | $\lvert I_{IL}\rvert$ < 10µA | –0.3 | | +0.8 | V |
| $V_{OH}$ | $I_{OH}$ = –20µA | $DV_{DD}$ –0.5 | | | V |
| $V_{OL}$ | $I_{OL}$ = 20µA | | | +0.4 | V |
| Transmit/Receive Channel Interface | | | | | |
| $t_{tx1}$ | txCLK Period | 1.7 | | 10.2 | µs |
| $t_{tx2}$ | txCLK Pulse Width | $t_{tx1}/16$ | | $15t_{tx1}/16$ | ns |
| **POWER** | | | | | |
| Analog Power Supply Voltage | Specification | | 5 | | V |
| Analog Power Supply Voltage | Operating Range | 4.75 | | 5.25 | V |
| Digital Power Supply Voltage | Specification | | 3.3 | | V |
| Digital Power Supply Voltage | Operating Range | 3.15 | | 5.25 | V |
| Power Dissipation(4, 5, 8) | $DV_{DD}$ = 3.3V | | 250 | | mW |
| Power Dissipation(4, 5, 8) | $DV_{DD}$ = 5V | | 300 | | mW |
| PSRR | | 60 | | | dB |
| **TEMPERATURE RANGE** | | | | | |
| Operating(6) | | –40 | | +85 | °C |

NOTES: (1) With a balanced differential signal, the positive input is 180° out of phase with the negative input, therefore the actual voltage swing about the common mode voltage on each pin is ±1.5V to achieve a differential input range of ±3.0V or 6Vp-p. (2) FSR is Full-Scale Range. (3) The output data is available at twice the symbol rate with interpolated values. (4) With a pseudo-random equiprobable sequence of HDSL pulses; 13.5dBm applied to the transformer (27dBm output from $txLINE_P$ and $txLINE_N$). (5) See the Discussion of Specifications section of this data sheet for more information. (6) Guaranteed by design and characterization. (7) Uncancelled Echo is a measure of the total analog errors in the transmitter and receiver sections including the effect of non-linearity and noise. See the Discussion of Specifications section of this data sheet for more information. (8) Power dissipation includes only the power dissipated within the component and does not include power dissipated in the external loads. See the Discussion of Specifications section for more information.

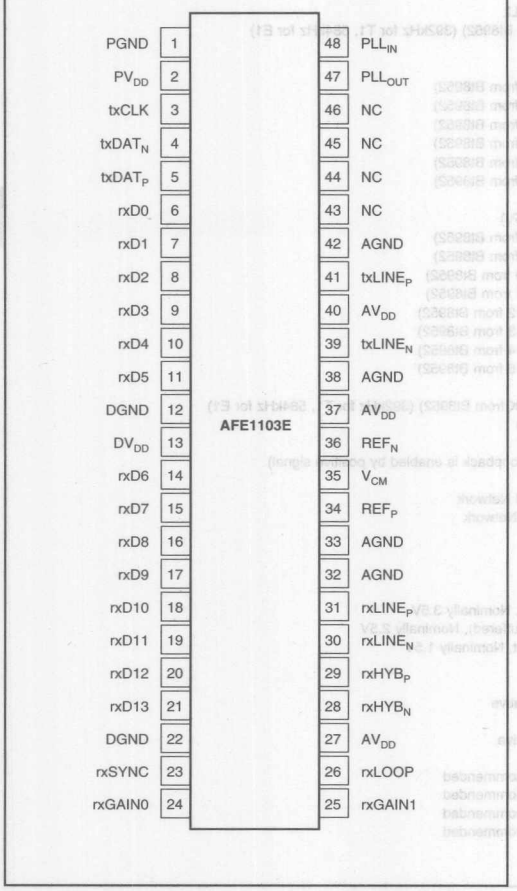
## PIN DESCRIPTIONS

| PIN # | TYPE | NAME | DESCRIPTION |
|---|---|---|---|
| 1 | Ground | PGND | Analog Ground for PLL |
| 2 | Power | $PV_{DD}$ | Analog Supply (+5V) for PLL |
| 3 | Input | txCLK | Symbol Clock (QCLK from Bt8952) (392kHz for T1, 584kHz for E1) |
| 4 | Input | $txDAT_N$ | XMITB Line from Bt8952 |
| 5 | Input | $txDAT_P$ | XMIT Line from Bt8952 |
| 6 | Output | rxD0 | ADC Output Bit-0 (RCV 2 from Bt8952) |
| 7 | Output | rxD1 | ADC Output Bit-1 (RCV 3 from Bt8952) |
| 8 | Output | rxD2 | ADC Output Bit-2 (RCV 4 from Bt8952) |
| 9 | Output | rxD3 | ADC Output Bit-3 (RCV 5 from Bt8952) |
| 10 | Output | rxD4 | ADC Output Bit-4 (RCV 6 from Bt8952) |
| 11 | Output | rxD5 | ADC Output Bit-5 (RCV 7 from Bt8952) |
| 12 | Ground | DGND | Digital Ground |
| 13 | Power | $DV_{DD}$ | Digital Supply (+3.3V to +5V) |
| 14 | Output | rxD6 | ADC Output Bit-6 (RCV 8 from Bt8952) |
| 15 | Output | rxD7 | ADC Output Bit-7 (RCV 9 from Bt8952) |
| 16 | Output | rxD8 | ADC Output Bit-8 (RCV 10 from Bt8952) |
| 17 | Output | rxD9 | ADC Output Bit-9 (RCV 11 from Bt8952) |
| 18 | Output | rxD10 | ADC Output Bit-10 (RCV 12 from Bt8952) |
| 19 | Output | rxD11 | ADC Output Bit-11 (RCV 13 from Bt8952) |
| 20 | Output | rxD12 | ADC Output Bit-12 (RCV 14 from Bt8952) |
| 21 | Output | rxD13 | ADC Output Bit-13 (RCV 15 from Bt8952) |
| 22 | Ground | DGND | Digital Ground |
| 23 | Input | rxSYNC | ADC Sync Signal (RCVCLK from Bt8952) (392kHz for T1, 584kHz for E1) |
| 24 | Input | rxGAIN0 | Receive Gain Control Bit-0 |
| 25 | Input | rxGAIN1 | Receive Gain Control Bit-1 |
| 26 | Input | rxLOOP | Loopback Control Signal (loopback is enabled by positive signal) |
| 27 | Power | $AV_{DD}$ | Analog Supply (+5V) |
| 28 | Input | $rxHYB_N$ | Negative Input from Hybrid Network |
| 29 | Input | $rxHYB_P$ | Positive Input from Hybrid Network |
| 30 | Input | $rxLINE_N$ | Negative Line Input |
| 31 | Input | $rxLINE_P$ | Positive Line Input |
| 32 | Ground | AGND | Analog Ground |
| 33 | Ground | AGND | Analog Ground |
| 34 | Output | $REF_P$ | Positive Reference Output, Nominally 3.5V |
| 35 | Output | $V_{CM}$ | Common-Mode Voltage (buffered), Nominally 2.5V |
| 36 | Output | $REF_N$ | Negative Reference Output, Nominally 1.5V |
| 37 | Power | $AV_{DD}$ | Analog Supply (+5V) |
| 38 | Ground | AGND | Analog Ground |
| 39 | Output | $txLINE_N$ | Transmit Line Output Negative |
| 40 | Power | $AV_{DD}$ | Analog Supply (+5V) |
| 41 | Output | $txLINE_P$ | Transmit Line Output Positive |
| 42 | Ground | AGND | Analog Ground |
| 43 | NC | NC | Connection to Ground Recommended |
| 44 | NC | NC | Connection to Ground Recommended |
| 45 | NC | NC | Connection to Ground Recommended |
| 46 | NC | NC | Connection to Ground Recommended |
| 47 | Output | $PLL_{OUT}$ | PLL Filter Output |
| 48 | Input | $PLL_{IN}$ | PLL Filter Input |

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## PIN CONFIGURATION

Top View SSOP




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: Current | ±100mA, Momentary |
| | ±10mA, Continuous |
| Voltage | AGND –0.3V to $AV_{DD}$ +0.3V |
| Analog Outputs Short Circuit to Ground (+25°C) | Continuous |
| $AV_{DD}$ to AGND | –0.3V to 6V |
| $PV_{DD}$ to PGND | –0.3V to 6V |
| $DV_{DD}$ to DGND | –0.3V to 6V |
| $PLL_{IN}$ or $PLL_{OUT}$ to PGND | –0.3V to $PV_{DD}$ +0.3V |
| Digital Input Voltage to DGND | –0.3V to $DV_{DD}$ +0.3V |
| Digital Output Voltage to DGND | –0.3V to $DV_{DD}$ +0.3V |
| AGND, DGND, PGND Differential Voltage | 0.3V |
| Junction Temperature ($T_J$) | +150°C |
| Storage Temperature Range | –40°C to +125°C |
| Lead Temperature (soldering, 3s) | +260°C |
| Power Dissipation | 700mW |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| AFE1103E | 48-Pin Plastic SSOP | 333 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# AFE1104

www.burr-brown.com/databook/AFE1104.html

# HDSL/MDSL ANALOG FRONT END

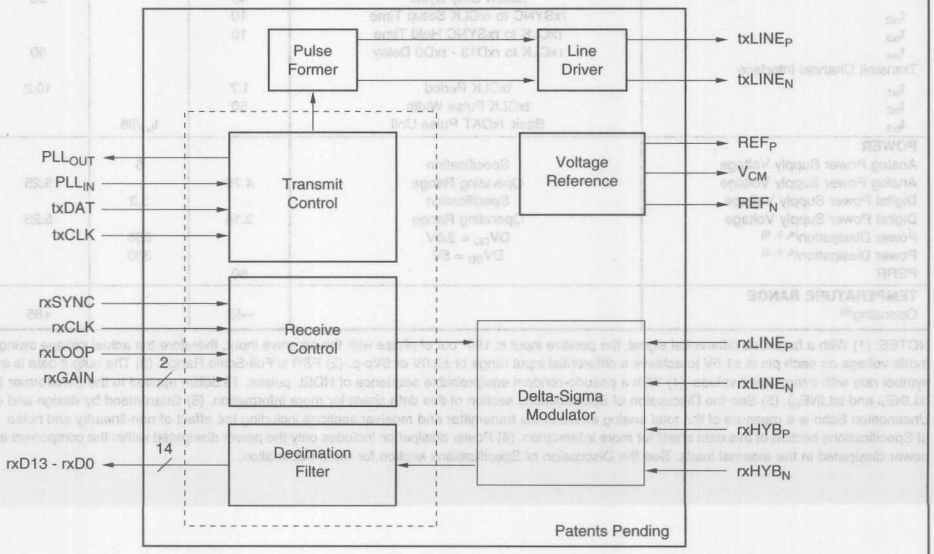
## FEATURES

- COMPLETE ANALOG INTERFACE
- T1, E1, AND MDSL OPERATION
- CLOCK SCALEABLE SPEED
- SINGLE CHIP SOLUTION
- +5V ONLY (5V OR 3.3V DIGITAL)
- 250mW POWER DISSIPATION
- 48-PIN SSOP
- –40°C TO +85°C OPERATION

## DESCRIPTION

Burr-Brown's Analog Front End greatly reduces the size and cost of an HDSL or MDSL system by providing all of the active analog circuitry needed to connect PairGain Technologies SPAROW HDSL digital signal processor to an external compromise hybrid and a 1:2 HDSL line transformer. All internal filter responses as well as the pulse former output scale with clock frequency—allowing the AFE1104 to operate over a range of bit rates from 196kbps to 1.168Mbps.

Functionally, this unit is separated into a transmit and a receive section. The transmit section generates, filters, and buffers outgoing 2B1Q data. The receive section filters and digitizes the symbol data received on the telephone line and passes it to the SPAROW. The HDSL Analog Interface is a monolithic device fabricated on 0.6µCMOS. It operates on a single +5V supply. It is housed in a 48-pin SSOP package.




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# SPECIFICATIONS

Typical at 25°C, $AV_{DD}$ = +5V, $DV_{DD}$ = +3.3V, $f_{tx}$ = 584kHz (E1 rate), unless otherwise specified.

| PARAMETER | COMMENTS | AFE1104E MIN | AFE1104E TYP | AFE1104E MAX | UNITS |
|---|---|---|---|---|---|
| **RECEIVE CHANNEL** | | | | | |
| Number of Inputs | Differential | 2 | | | |
| Input Voltage Range | Balanced Differential(1) | | ±3.0 | | V |
| Common-Mode Voltage | 1.5V CMV Recommended | | +1.5 | | V |
| Input Impedance | All Inputs | | See Typical Performance Curves | | |
| Input Capacitance | | | 10 | | pF |
| Input Gain Matching | Line Input vs Hybrid Input | | ±2 | | % |
| Resolution | | 14 | | | Bits |
| Programmable Gain | Four Gains: 0dB, 3.25dB, 6dB, and 9dB | 0 | | 9 | dB |
| Settling Time for Gain Change | | | 6 | | Symbol Periods |
| Gain + Offset Error | Tested at Each Gain Range | | 5 | | %FSR(2) |
| Output Data Coding | | | Two's Complement | | |
| Output Data Rate, rxSYNC(3) | | 98 | | 584 | kHz |
| **TRANSMIT CHANNEL** | | | | | |
| Transmit Symbol Rate, $f_{tx}$ | | 98 | | 584 | kHz |
| T1 Transmit –3dB Point | Bellcore TA-NWT-3017 Compliant | | 196 | | kHz |
| T1 Rate Power Spectral Density(4) | | | See Typical Performance Curves | | |
| E1 Transmit –3dB Point | ETSI RTR/TM-03036 Compliant | | 292 | | kHz |
| E1 Rate Power Spectral Density(4) | | | See Typical Performance Curves | | |
| Transmit Power(4, 5) | | 13 | | 14 | dBm |
| Pulse Output | | | See Typical Performance Curves | | |
| Common-Mode Voltage, $V_{CM}$ | | | $AV_{DD}/2$ | | V |
| Output Resistance(6) | DC to 1MHz | | 1 | | Ω |
| **TRANSCEIVER PERFORMANCE** | | | | | |
| Uncanceled Echo(7) | rxGAIN = 0dB, Loopback Enabled | | | –67 | dB |
| | rxGAIN = 0dB, Loopback Disabled | | | –67 | dB |
| | rxGAIN = 3.25dB, Loopback Disabled | | | –69 | dB |
| | rxGAIN = 6dB, Loopback Disabled | | | –71 | dB |
| | rxGAIN = 9dB, Loopback Disabled | | | –73 | dB |
| **DIGITAL INTERFACE(6)** | | | | | |
| Logic Levels | | | | | |
| $V_{IH}$ | $\lvert I_{IH}\rvert$ < 10µA | $DV_{DD}$ –1 | | $DV_{DD}$ +0.3 | V |
| $V_{IL}$ | $\lvert I_{IL}\rvert$ < 10µA | –0.3 | | +0.8 | V |
| $V_{OH}$ | $I_{OH}$ = –20µA | $DV_{DD}$ –0.5 | | | V |
| $V_{OL}$ | $I_{OL}$ = 20µA | | | +0.4 | V |
| Receive Channel Interface | | | | | |
| $t_{rx1}$ | rxCLK Period | 35 | | 215 | ns |
| | rxCLK Duty Cycle | 45 | | 55 | % |
| $t_{rx2}$ | rxSYNC to rxCLK Setup Time | 10 | | | ns |
| $t_{rx3}$ | rxCLK to rxSYNC Hold Time | 10 | | | ns |
| $t_{rx4}$ | rxCLK to rxD13 - rxD0 Delay | | | 50 | ns |
| Transmit Channel Interface | | | | | |
| $t_{tx1}$ | txCLK Period | 1.7 | | 10.2 | µs |
| $t_{tx2}$ | txCLK Pulse Width | 50 | | | ns |
| $t_{tx3}$ | Basic txDAT Pulse Unit | | $t_{tx1}/96$ | | ns |
| **POWER** | | | | | |
| Analog Power Supply Voltage | Specification | | 5 | | V |
| Analog Power Supply Voltage | Operating Range | 4.75 | | 5.25 | V |
| Digital Power Supply Voltage | Specification | | 3.3 | | V |
| Digital Power Supply Voltage | Operating Range | 3.15 | | 5.25 | V |
| Power Dissipation(4, 5, 8) | $DV_{DD}$ = 3.3V | | 250 | | mW |
| Power Dissipation(4, 5, 8) | $DV_{DD}$ = 5V | | 300 | | mW |
| PSRR | | 60 | | | dB |
| **TEMPERATURE RANGE** | | | | | |
| Operating(6) | | –40 | | +85 | °C |

NOTES: (1) With a balanced differential signal, the positive input is 180° out of phase with the negative input, therefore the actual voltage swing about the common mode voltage on each pin is ±1.5V to achieve a differential input range of ±3.0V or 6Vp-p. (2) FSR is Full-Scale Range. (3) The output data is available at twice the symbol rate with interpolated values. (4) With a pseudo-random equiprobable sequence of HDSL pulses; 13.5dBm applied to the transformer (27dBm output from $txLINE_P$ and $txLINE_N$). (5) See the Discussion of Specifications section of this data sheet for more information. (6) Guaranteed by design and characterization. (7) Uncanceled Echo is a measure of the total analog errors in the transmitter and receiver sections including the effect of non-linearity and noise. See the Discussion of Specifications section of this data sheet for more information. (8) Power dissipation includes only the power dissipated within the component and does not include power dissipated in the external loads. See the Discussion of Specifications section for more information.

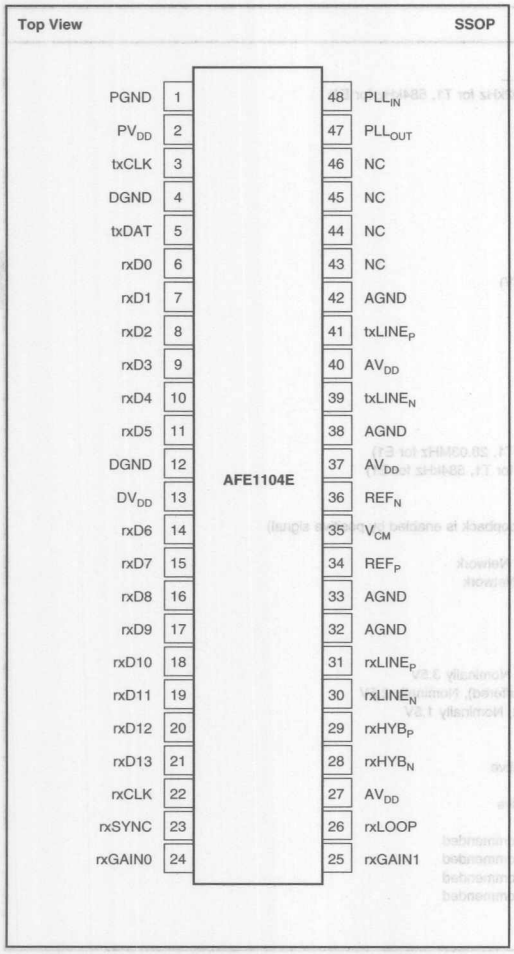
## PIN DESCRIPTIONS

| PIN # | TYPE | NAME | DESCRIPTION |
|---|---|---|---|
| 1 | Ground | PGND | Analog Ground for PLL |
| 2 | Power | $PV_{DD}$ | Analog Supply (+5V) for PLL |
| 3 | Input | txCLK | Transmit Symbol Clock (392kHz for T1, 584kHz for E1) |
| 4 | Ground | DGND | Digital Ground |
| 5 | Input | txDAT | DAC+ Line from SPAROW |
| 6 | Output | rxD0 | ADC Output Bit-0 |
| 7 | Output | rxD1 | ADC Output Bit-1 |
| 8 | Output | rxD2 | ADC Output Bit-2 |
| 9 | Output | rxD3 | ADC Output Bit-3 |
| 10 | Output | rxD4 | ADC Output Bit-4 |
| 11 | Output | rxD5 | ADC Output Bit-5 |
| 12 | Ground | DGND | Digital Ground |
| 13 | Power | $DV_{DD}$ | Digital Supply (+3.3V to +5V) |
| 14 | Output | rxD6 | ADC Output Bit-6 |
| 15 | Output | rxD7 | ADC Output Bit-7 |
| 16 | Output | rxD8 | ADC Output Bit-8 |
| 17 | Output | rxD9 | ADC Output Bit-9 |
| 18 | Output | rxD10 | ADC Output Bit-10 |
| 19 | Output | rxD11 | ADC Output Bit-11 |
| 20 | Output | rxD12 | ADC Output Bit-12 |
| 21 | Output | rxD13 | ADC Output Bit-13 |
| 22 | Input | rxCLK | A/D Clock (18.816MHz for T1, 28.03MHz for E1) |
| 23 | Input | rxSYNC | ADC Sync Signal (392kHz for T1, 584kHz for E1) |
| 24 | Input | rxGAIN0 | Receive Gain Control Bit-0 |
| 25 | Input | rxGAIN1 | Receive Gain Control Bit-1 |
| 26 | Input | rxLOOP | Loopback Control Signal (loopback is enabled by positive signal) |
| 27 | Power | $AV_{DD}$ | Analog Supply (+5V) |
| 28 | Input | $rxHYB_N$ | Negative Input from Hybrid Network |
| 29 | Input | $rxHYB_P$ | Positive Input from Hybrid Network |
| 30 | Input | $rxLINE_N$ | Negative Line Input |
| 31 | Input | $rxLINE_P$ | Positive Line Input |
| 32 | Ground | AGND | Analog Ground |
| 33 | Ground | AGND | Analog Ground |
| 34 | Output | $REF_P$ | Positive Reference Output, Nominally 3.5V |
| 35 | Output | $V_{CM}$ | Common-Mode Voltage (buffered), Nominally 2.5V |
| 36 | Output | $REF_N$ | Negative Reference Output, Nominally 1.5V |
| 37 | Power | $AV_{DD}$ | Analog Supply (+5V) |
| 38 | Ground | AGND | Analog Ground |
| 39 | Output | $txLINE_N$ | Transmit Line Output Negative |
| 40 | Power | $AV_{DD}$ | Analog Supply (+5V) |
| 41 | Output | $txLINE_P$ | Transmit Line Output Positive |
| 42 | Ground | AGND | Analog Ground |
| 43 | NC | NC | Connection to Ground Recommended |
| 44 | NC | NC | Connection to Ground Recommended |
| 45 | NC | NC | Connection to Ground Recommended |
| 46 | NC | NC | Connection to Ground Recommended |
| 47 | Output | $PLL_{OUT}$ | PLL Filter Output |
| 48 | Input | $PLL_{IN}$ | PLL Filter Input |

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN CONFIGURATION

**Top View** **SSOP**




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: Current | ±100mA, Momentary |
| | ±10mA, Continuous |
| Voltage | AGND –0.3V to $AV_{DD}$ +0.3V |
| Analog Outputs Short Circuit to Ground (+25°C) | Continuous |
| $AV_{DD}$ to AGND | –0.3V to 6V |
| $PV_{DD}$ to PGND | –0.3V to 6V |
| $DV_{DD}$ to DGND | –0.3V to 6V |
| $PLL_{IN}$ or $PLL_{OUT}$ to PGND | –0.3V to $PV_{DD}$ +0.3V |
| Digital Input Voltage to DGND | –0.3V to $DV_{DD}$ +0.3V |
| Digital Output Voltage to DGND | –0.3V to $DV_{DD}$ +0.3V |
| AGND, DGND, PGND Differential Voltage | 0.3V |
| Junction Temperature ($T_J$) | +150°C |
| Storage Temperature Range | –40°C to +125°C |
| Lead Temperature (soldering, 3s) | +260°C |
| Power Dissipation | 700mW |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| AFE1104E | 48-Pin Plastic SSOP | 333 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# AFE1105

www.burr-brown.com/databook/AFE1105.html

# HDSL/MDSL ANALOG FRONT END

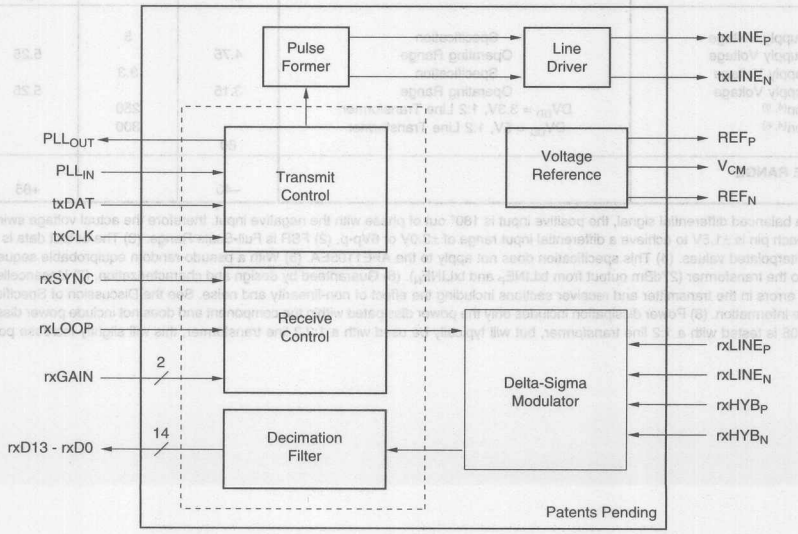
## FEATURES

- COMPLETE ANALOG INTERFACE
- T1, E1, AND MDSL OPERATION
- CLOCK SCALEABLE SPEED
- SINGLE CHIP SOLUTION
- +5V ONLY (5V OR 3.3V DIGITAL)
- 250mW POWER DISSIPATION
- 48-PIN SSOP
- –40°C TO +85°C OPERATION

## DESCRIPTION

Burr-Brown's Analog Front End greatly reduces the size and cost of an HDSL or MDSL system by providing all of the active analog circuitry needed to connect the Metalink MtH1210B HDSL digital signal processor to an external compromise hybrid and a 1:2.3 HDSL line transformer. All internal filter responses as well as the pulse former output scale with clock frequency—allowing the AFE1105 to operate over a range of bit rates from 196kbps to 1.168Mbps.

Functionally, this unit is separated into a transmit and a receive section. The transmit section generates, filters, and buffers outgoing 2B1Q data. The receive section filters and digitizes the symbol data received on the telephone line and passes it to the MtH1210B. The HDSL Analog Interface is a monolithic device fabricated on 0.6µCMOS. It operates on a single +5V supply. It is housed in a 48-pin SSOP package.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

Typical at 25°C, $AV_{DD}$ = +5V, $DV_{DD}$ = +3.3V, $f_{tx}$ = 584kHz (E1 rate), unless otherwise specified.

| PARAMETER | COMMENTS | AFE1105E MIN | AFE1105E TYP | AFE1105E MAX | UNITS |
|---|---|---|---|---|---|
| **RECEIVE CHANNEL** | | | | | |
| Number of Inputs | Differential | 2 | | | |
| Input Voltage Range | Balanced Differential(1) | | ±3.0 | | V |
| Common-Mode Voltage | 1.5V CMV Recommended | | +1.5 | | V |
| Input Impedance | All Inputs | | See Typical Performance Curves | | |
| Input Capacitance | | | 10 | | pF |
| Input Gain Matching | Line Input vs Hybrid Input | | ±2 | | % |
| Resolution | | 14 | | | Bits |
| Programmable Gain | Four Gains: 0dB, 3.25dB, 6dB, and 9dB | 0 | | 9 | dB |
| Settling Time for Gain Change | | | 6 | | Symbol Periods |
| Gain + Offset Error | Tested at Each Gain Range | | 5 | | %FSR(2) |
| Output Data Coding | | | Two's Complement | | |
| Output Data Rate, rxSYNC(3) | | 98 | | 584(4) | kHz |
| **TRANSMIT CHANNEL** | | | | | |
| Transmit Symbol Rate, $f_{tx}$ | | 98 | | 584(4) | kHz |
| T1 Transmit –3dB Point | Bellcore TA-NWT-3017 Compliant | | 196 | | kHz |
| T1 Rate Power Spectral Density(5) | | | See Typical Performance Curves | | |
| E1 Transmit –3dB Point | ETSI RTR/TM-03036 Compliant | | 292 | | kHz |
| E1 Rate Power Spectral Density(5) | | | See Typical Performance Curves | | |
| Transmit Power(5) | | 13 | | 14 | dBm |
| Pulse Output | | | See Typical Performance Curves | | |
| Common-Mode Voltage, $V_{CM}$ | | | $AV_{DD}/2$ | | V |
| Output Resistance(6) | DC to 1MHz | | 1 | | Ω |
| **TRANSCEIVER PERFORMANCE** | | | | | |
| Uncancelled Echo(7) | rxGAIN = 0dB, Loopback Enabled | | | –67 | dB |
| | rxGAIN = 0dB, Loopback Disabled | | | –67 | dB |
| | rxGAIN = 3.25dB, Loopback Disabled | | | –69 | dB |
| | rxGAIN = 6dB, Loopback Disabled | | | –71 | dB |
| | rxGAIN = 9dB, Loopback Disabled | | | –73 | dB |
| **DIGITAL INTERFACE(6)** | | | | | |
| Logic Levels | | | | | |
| $V_{IH}$ | $\lvert I_{IH}\rvert$ < 10µA | $DV_{DD}$ –1 | | $DV_{DD}$ +0.3 | V |
| $V_{IL}$ | $\lvert I_{IL}\rvert$ < 10µA | –0.3 | | +0.8 | V |
| $V_{OH}$ | $I_{OH}$ = –20µA | $DV_{DD}$ –0.5 | | | V |
| $V_{OL}$ | $I_{OL}$ = 20µA | | | +0.4 | V |
| Transmit/Receive Channel Interface | | | | | |
| $t_{tx1}$ | txCLK Period | 1.7 | | 10.2 | µs |
| $t_{tx2}$ | txCLK Pulse Width | $t_{tx1}$/16 | | 15$t_{tx1}$/16 | ns |
| **POWER** | | | | | |
| Analog Power Supply Voltage | Specification | | 5 | | V |
| Analog Power Supply Voltage | Operating Range | 4.75 | | 5.25 | V |
| Digital Power Supply Voltage | Specification | | 3.3 | | V |
| Digital Power Supply Voltage | Operating Range | 3.15 | | 5.25 | V |
| Power Dissipation(4, 8) | $DV_{DD}$ = 3.3V, 1:2 Line Transformer | | 250 | | mW |
| Power Dissipation(4, 8) | $DV_{DD}$ = 5V, 1:2 Line Transformer | | 300 | | mW |
| PSRR | | 60 | | | dB |
| **TEMPERATURE RANGE** | | | | | |
| Operating(6) | | –40 | | +85 | °C |

NOTES: (1) With a balanced differential signal, the positive input is 180° out of phase with the negative input, therefore the actual voltage swing about the common mode voltage on each pin is ±1.5V to achieve a differential input range of ±3.0V or 6Vp-p. (2) FSR is Full-Scale Range. (3) The output data is available at twice the symbol rate with interpolated values. (4) This specification does not apply to the AFE1105EA. (5) With a pseudo-random equiprobable sequence of HDSL pulses; 13.5dBm applied to the transformer (27dBm output from $txLINE_P$ and $txLINE_N$). (6) Guaranteed by design and characterization. (7) Uncancelled Echo is a measure of the total analog errors in the transmitter and receiver sections including the effect of non-linearity and noise. See the Discussion of Specifications section of this data sheet for more information. (8) Power dissipation includes only the power dissipated within the component and does not include power dissipated in the external loads. The AFE1105 is tested with a 1:2 line transformer, but will typically be used with a 1:2.3 line transformer, this will slightly increase power dissipation.

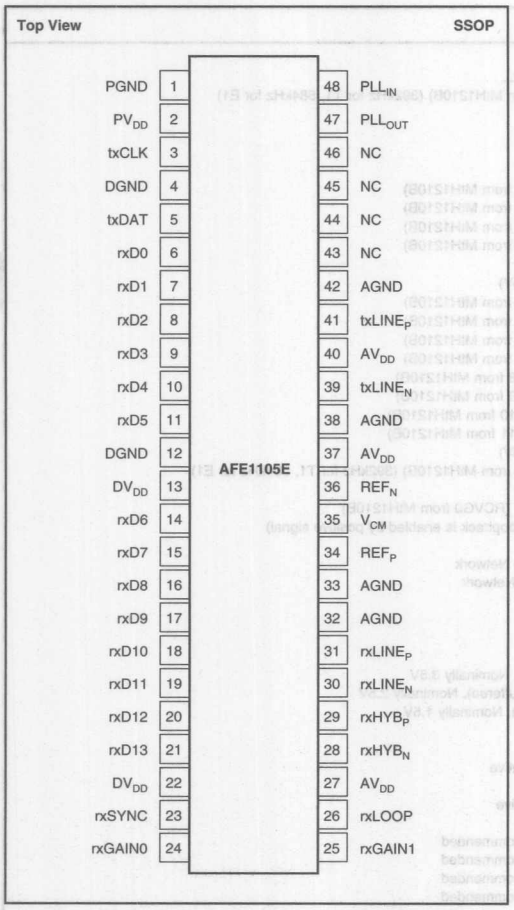
## PIN DESCRIPTIONS

| PIN # | TYPE | NAME | DESCRIPTION |
|---|---|---|---|
| 1 | Ground | PGND | Analog Ground for PLL |
| 2 | Power | $PV_{DD}$ | Analog Supply (+5V) for PLL |
| 3 | Input | txCLK | Symbol Clock (XMTLE from MtH1210B) (392kHz for T1, 584kHz for E1) |
| 4 | Ground | DGND | Digital Ground |
| 5 | Input | txDAT | XMTDA from MtH1210B |
| 6 | Output | rxD0 | ADC Output Bit-0 |
| 7 | Output | rxD1 | ADC Output Bit-1 |
| 8 | Output | rxD2 | ADC Output Bit-2 (RCVD0 from MtH1210B) |
| 9 | Output | rxD3 | ADC Output Bit-3 (RCVD1 from MtH1210B) |
| 10 | Output | rxD4 | ADC Output Bit-4 (RCVD2 from MtH1210B) |
| 11 | Output | rxD5 | ADC Output Bit-5 (RCVD3 from MtH1210B) |
| 12 | Ground | DGND | Digital Ground |
| 13 | Power | $DV_{DD}$ | Digital Supply (+3.3V to +5V) |
| 14 | Output | rxD6 | ADC Output Bit-6 (RCVD4 from MtH1210B) |
| 15 | Output | rxD7 | ADC Output Bit-7 (RCVD5 from MtH1210B) |
| 16 | Output | rxD8 | ADC Output Bit-8 (RCVD6 from MtH1210B) |
| 17 | Output | rxD9 | ADC Output Bit-9 (RCVD7 from MtH1210B) |
| 18 | Output | rxD10 | ADC Output Bit-10 (RCVD8 from MtH1210B) |
| 19 | Output | rxD11 | ADC Output Bit-11 (RCVD9 from MtH1210B) |
| 20 | Output | rxD12 | ADC Output Bit-12 (RCVD10 from MtH1210B) |
| 21 | Output | rxD13 | ADC Output Bit-13 (RCVD11 from MtH1210B) |
| 22 | Power | $DV_{DD}$ | Digital Supply (+3.3V to +5V) |
| 23 | Input | rxSYNC | ADC Sync Signal (RCVCK from MtH1210B) (392kHz for T1, 584kHz for E1) |
| 24 | Input | rxGAIN0 | Receive Gain Control Bit-0 |
| 25 | Input | rxGAIN1 | Receive Gain Control Bit-1 (RCVG0 from MtH1210B) |
| 26 | Input | rxLOOP | Loopback Control Signal (loopback is enabled by positive signal) |
| 27 | Power | $AV_{DD}$ | Analog Supply (+5V) |
| 28 | Input | $rxHYB_N$ | Negative Input from Hybrid Network |
| 29 | Input | $rxHYB_P$ | Positive Input from Hybrid Network |
| 30 | Input | $rxLINE_N$ | Negative Line Input |
| 31 | Input | $rxLINE_P$ | Positive Line Input |
| 32 | Ground | AGND | Analog Ground |
| 33 | Ground | AGND | Analog Ground |
| 34 | Output | $REF_P$ | Positive Reference Output, Nominally 3.5V |
| 35 | Output | $V_{CM}$ | Common-Mode Voltage (buffered), Nominally 2.5V |
| 36 | Output | $REF_N$ | Negative Reference Output, Nominally 1.5V |
| 37 | Power | $AV_{DD}$ | Analog Supply (+5V) |
| 38 | Ground | AGND | Analog Ground |
| 39 | Output | $txLINE_N$ | Transmit Line Output Negative |
| 40 | Power | $AV_{DD}$ | Analog Supply (+5V) |
| 41 | Output | $txLINE_P$ | Transmit Line Output Positive |
| 42 | Ground | AGND | Analog Ground |
| 43 | NC | NC | Connection to Ground Recommended |
| 44 | NC | NC | Connection to Ground Recommended |
| 45 | NC | NC | Connection to Ground Recommended |
| 46 | NC | NC | Connection to Ground Recommended |
| 47 | Output | $PLL_{OUT}$ | PLL Filter Output |
| 48 | Input | $PLL_{IN}$ | PLL Filter Input |

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## PIN CONFIGURATION

Top View — SSOP




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: Current | ±100mA, Momentary |
| | ±10mA, Continuous |
| Voltage | AGND –0.3V to $AV_{DD}$ +0.3V |
| Analog Outputs Short Circuit to Ground (+25°C) | Continuous |
| $AV_{DD}$ to AGND | –0.3V to 6V |
| $PV_{DD}$ to PGND | –0.3V to 6V |
| $DV_{DD}$ to DGND | –0.3V to 6V |
| $PLL_{IN}$ or $PLL_{OUT}$ to PGND | –0.3V to $PV_{DD}$ +0.3V |
| Digital Input Voltage to DGND | –0.3V to $DV_{DD}$ +0.3V |
| Digital Output Voltage to DGND | –0.3V to $DV_{DD}$ +0.3V |
| AGND, DGND, PGND Differential Voltage | 0.3V |
| Junction Temperature ($T_J$) | +150°C |
| Storage Temperature Range | –40°C to +125°C |
| Lead Temperature (soldering, 3s) | +260°C |
| Power Dissipation | 700mW |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | MAXIMUM BIT RATE | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|---|
| AFE1105E | 1.168Mbps | 48-Pin Plastic SSOP | 333 | –40°C to +85°C |
| AFE1105EA | 512kbps | 48-Pin Plastic SSOP | 333 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# AFE1115

www.burr-brown.com/databook/AFE1115.html

# HDSL/MDSL ANALOG FRONT END WITH VCXO

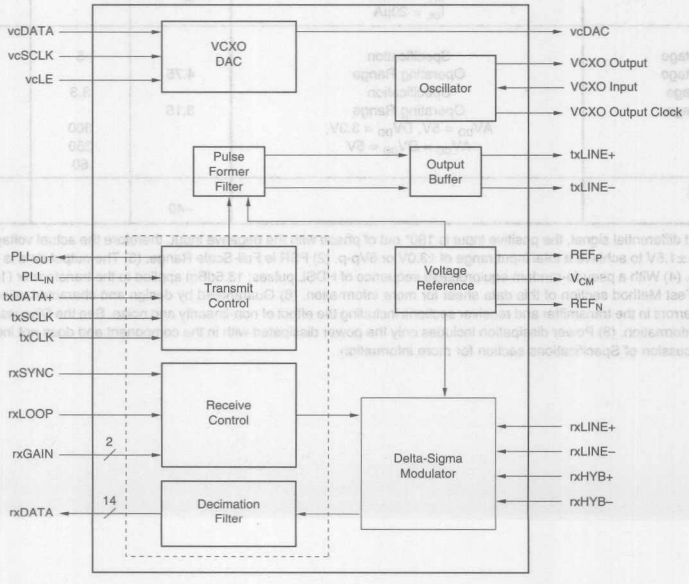
## FEATURES

- COMPLETE HDSL ANALOG INTERFACE
- E1, T1 AND MDSL OPERATION
- VCXO AND VCXO CONTROL CIRCUITRY
- +5V ONLY (5V or 3.3V Digital)
- SCALEABLE DATA RATE
- 300mW POWER DISSIPATION
- 56-PIN SSOP

## DESCRIPTION

Burr-Brown's Analog Front End greatly reduces the size and cost of an HDSL (High bit rate Digital Subscriber Line) system by providing all of the active analog circuitry needed to connect an HDSL digital signal processor to an external compromise hybrid and a HDSL line transformer. The transmit and receive filter responses automatically change with clock frequency—allowing the AFE1115 to operate over a range of data rates from 196kbps to 1.168Mbps.

Functionally, this unit consists of a transmit and a receive section with a VCXO (Voltage Controlled Crystal Oscillator) control DAC and VCXO circuitry. The transmit section generates, filters, and buffers outgoing 2B1Q data. The receive section filters and digitizes the symbol data received on the telephone line. Data to the VCXO and symbol data are sent to the AFE1115 via two serial interfaces; the receive data is available as a 14-bit parallel word. This IC operates on a single 5V supply. The digital circuitry in the unit can be connected to a supply from 3.3V to 5V. It is housed in a small 56-pin SSOP package.



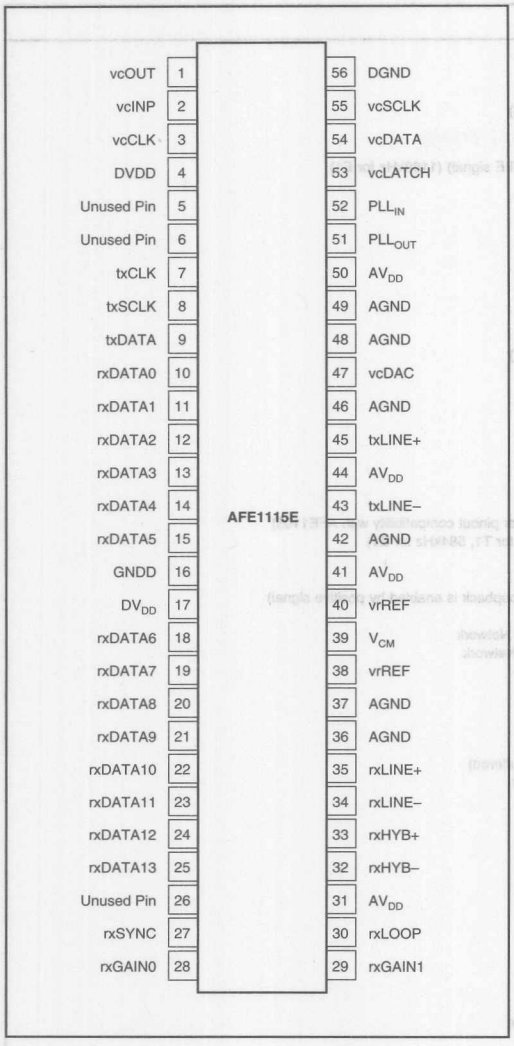

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$DV_{DD}$ = 3.3V, $AV_{DD}$ = 5.0V, $f_{tx}$ = 384kHz (E1 rate), unless otherwise specified.

| PARAMETER | COMMENTS | AFE1115E MIN | AFE1115E TYP | AFE1115E MAX | UNITS |
|---|---|---|---|---|---|
| **RECEIVE CHANNEL** | | | | | |
| Number of Inputs | Differential | 2 | | | |
| Input Voltage Range | Balanced Differential(1) | | ±3.0 | | V |
| Common-Mode Voltage | | | +2.5 | | V |
| Input Impedance All Inputs | | | See Typical Performance Curves | | |
| Input Capacitance | | | 10 | | pF |
| Input Gain Matching | Line Input vs Hybrid Input | | ±2 | | % |
| Resolution | | 14 | | | Bits |
| Programmable Gain | Three Gains: –3dB, 3dB, and 9dB | –3 | | +9 | dB |
| Settling Time for Gain Change | | | 6 | | Symbol Periods |
| Gain + Offset Error | Tested at Each Gain Range | | 5 | | %FSR(2) |
| Output Data Coding | Two's Complement | | | | |
| Output Data Rate, rxSYNC(3) | | 98 | | 584 | kHz |
| **TRANSMIT CHANNEL** | | | | | |
| Transmit Clock Rate, $f_{tx}$ | Symbol Rate | 98 | | 584 | kHz |
| T1 Transmit –3dB Point | Bellcore TA-NWT-3017 Compliant | | 196 | | kHz |
| T1 Rate Power(4, 5) | See Test Method Section | 13 | | 14 | dBm |
| E1 Transmit –3dB Point | ETSI RTR/TM-03036 Compliant | | 292 | | kHz |
| E1 Transmit Power(4, 5) | See Test Method Section | 13 | | 14 | dBm |
| Pulse Output | | | See Typical Performance Curves | | |
| Common-Mode Voltage, $V_{CM}$ | | | $AV_{DD}/2$ | | V |
| Output Resistance(6) | DC to 1MHz | | 1 | | Ω |
| **TRANSCEIVER PERFORMANCE** | | | | | |
| Uncancelled Echo(7) | rxGAIN = –3dB, Loopback Enabled | | | –67 | dB |
| | rxGAIN = –3dB, Loopback Disabled | | | –67 | dB |
| | rxGAIN = 3dB, Loopback Disabled | | | –71 | dB |
| | rxGAIN = 9dB, Loopback Disabled | | | –73 | dB |
| **VCXO PERFORMANCE** | | | | | |
| VCXO Control DAC Resolution | | 8 | | | Bits |
| VCXO Control DAC Output | Positive Full Scale Output | | 4.5 | | V |
| VCXO Control DAC Output | Negative Full Scale Output | | 0.5 | | V |
| VCXO Performance | See VCXO Circuit and Layout Section | | | | |
| **DIGITAL INTERFACE(6)** | | | | | |
| Logic Levels | | | | | |
| $V_{IH}$ | $\lvert I_{IH}\rvert$ < 10µA | $DV_{DD}$ –1 | | $DV_{DD}$ +0.3 | V |
| $V_{IL}$ | $\lvert I_{IL}\rvert$ < 10µA | –0.3 | | +0.8 | V |
| $V_{OH}$ | $I_{OH}$ = –20µA | $DV_{DD}$ –0.5 | | | V |
| $V_{OL}$ | $I_{OL}$ = 20µA | | | +0.4 | V |
| **POWER** | | | | | |
| Analog Power Supply Voltage | Specification | | 5 | | V |
| Analog Power Supply Voltage | Operating Range | 4.75 | | 5.25 | V |
| Digital Power Supply Voltage | Specification | | 3.3 | | V |
| Digital Power Supply Voltage | Operating Range | 3.15 | | 5.25 | V |
| Power Dissipation(4, 5, 8) | $AV_{DD}$ = 5V, $DV_{DD}$ = 3.3V, | | 300 | | mW |
| Power Dissipation(4, 5, 8) | $AV_{DD}$ = $DV_{DD}$ = 5V | | 350 | | mW |
| PSRR | | | 60 | | dB |
| **TEMPERATURE RANGE** | | | | | |
| Operating(6) | | –40 | | +85 | °C |

NOTES: (1) With a balanced differential signal, the positive input is 180° out of phase with the negative input, therefore the actual voltage swing about the common-mode voltage on each pin is ±1.5V to achieve a total input range of ±3.0V or 6Vp-p. (2) FSR is Full-Scale Range. (3) The output data is available at twice the symbol rate with interpolated values. (4) With a pseudo-random equiprobable sequence of HDSL pulses; 13.5dBm applied to the transformer (16.5dBm output from txLINEP and txLINEN). (5) See the Test Method section of this data sheet for more information. (6) Guaranteed by design and characterization. (7) Uncancelled Echo is a measure of the total analog errors in the transmitter and receiver sections including the effect of non-linearity and noise. See the Discussion of Specifications sections of this data sheet for more information. (8) Power dissipation includes only the power dissipated with in the component and does not include power dissipated in the external loads. See the Discussion of Specifications section for more information.

## PIN CONFIGURATION




## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| AFE1115E | 56-Pin Plastic SSOP | 346 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN DESCRIPTIONS

| PIN # | TYPE | NAME | DESCRIPTION |
|---|---|---|---|
| 1 | Output | vcOUT | VCXO Output |
| 2 | Input | vcINP | VCXO Input |
| 3 | Output | vcCLK | VCXO Output Clock |
| 4 | Power | DVDD | Digital Supply (+3.3 to +5V) |
| 5 | NC | Unused Pin | |
| 6 | NC | Unused Pin | |
| 7 | Input | txCLK | Transmit Baud Clock (XMTLE signal) (1168kHz for E1) |
| 8 | Input | txSCLK | Transmit Serial Clock |
| 9 | Input | txDATA | Transmit Data Input |
| 10 | Output | rxDATA0 | ADC Output Bit-0 |
| 11 | Output | rxDATA1 | ADC Output Bit-1 |
| 12 | Output | rxDATA2 | ADC Output Bit-2 |
| 13 | Output | rxDATA3 | ADC Output Bit-3 |
| 14 | Output | rxDATA4 | ADC Output Bit-4 |
| 15 | Output | rxDATA5 | ADC Output Bit-5 |
| 16 | Ground | GNDD | Digital Ground |
| 17 | Power | $DV_{DD}$ | Digital Supply (+3.3 to +5V) |
| 18 | Output | rxDATA6 | ADC Output Bit-6 |
| 19 | Output | rxDATA7 | ADC Output Bit-7 |
| 20 | Output | rxDATA8 | ADC Output Bit-8 |
| 21 | Output | rxDATA9 | ADC Output Bit-9 |
| 22 | Output | rxDATA10 | ADC Output Bit-10 |
| 23 | Output | rxDATA11 | ADC Output Bit-11 |
| 24 | Output | rxDATA12 | ADC Output Bit-12 |
| 25 | Output | rxDATA13 | ADC Output Bit-13 |
| 26 | NC | Unused Pin | ($DV_{DD}$ may be connected for pinout compatibility with AFE1105) |
| 27 | Input | rxSYNC | ADC Sync Signal (392kHz for T1, 584kHz for E1) |
| 28 | Input | rxGAIN0 | Receive Gain Control Bit-0 |
| 29 | Input | rxGAIN1 | Receive Gain Control Bit-1 |
| 30 | Input | rxLOOP | Loopback Control Signal (loopback is enabled by positive signal) |
| 31 | Power | $AV_{DD}$ | Analog Supply (+5V) |
| 32 | Input | rxHYB– | Negative Input from Hybrid Network |
| 33 | Input | rxHYB+ | Positive Input from Hybrid Network |
| 34 | Input | rxLINE– | Negative Line Input |
| 35 | Input | rxLINE+ | Positive Line Input |
| 36 | Ground | AGND | Analog Ground |
| 37 | Ground | AGND | Analog Ground |
| 38 | Output | vrREFP | Positive Reference Output |
| 39 | Output | $V_{CM}$ | Common-mode Voltage (buffered) |
| 40 | Output | vrREFN | Negative Reference Output |
| 41 | Power | $AV_{DD}$ | Analog Supply (+5V) |
| 42 | Ground | AGND | Analog Ground |
| 43 | Output | txLINE– | Negative Line Output |
| 44 | Power | $AV_{DD}$ | Analog Supply (+5V) |
| 45 | Output | txLINE+ | Positive Line Output |
| 46 | Ground | AGND | Analog Ground |
| 47 | Output | vcDAC | VCXO Control |
| 48 | Ground | AGND | Analog Ground |
| 49 | Ground | AGND | PLL Ground |
| 50 | Power | $AV_{DD}$ | PLL Supply |
| 51 | Output | $PLL_{OUT}$ | PLL Filter Output |
| 52 | Input | $PLL_{IN}$ | PLL Filter Input |
| 53 | Input | vcLATCH | VCXO Control Latch Enable |
| 54 | Input | vcDATA | VCXO Control Data |
| 55 | Input | vcSCLK | VCXO Control Serial Clock |
| 56 | Ground | DGND | Digital Ground |

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# AFE1124

www.burr-brown.com/databook/AFE1124.html

# HDSL/MDSL ANALOG FRONT END

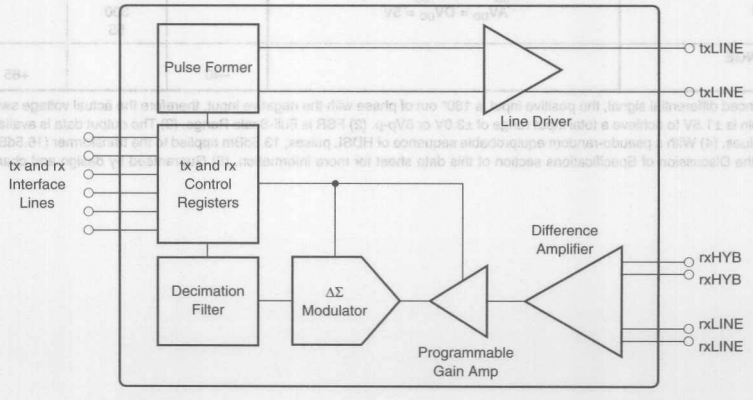
## FEATURES

- SERIAL DIGITAL INTERFACE
- 28-PIN SSOP
- E1, T1 AND MDSL OPERATION
- 64kbps TO 1168kbps OPERATION
- SCALEABLE DATA RATE
- 250mW POWER DISSIPATION
- COMPLETE HDSL ANALOG INTERFACE
- +5V POWER (5V or 3.3V Digital)

## DESCRIPTION

Burr-Brown's Analog Front End chip greatly reduces the size and cost of an xDSL (Digital Subscriber Line) system by providing all of the active analog circuitry needed to connect a digital signal processor to an external compromise hybrid and line transformer. The AFE1124 is optimized for HDSL (High bit rate DSL) and for lower speed MDSL (Medium speed DSL) and RADSL (Rate Adaptive DSL) applications. Because the transmit and receive filter responses automatically change with clock frequency, the AFE1124 is particularly suitable for RADSL and multiple rate DSL systems. The device operates over a wide range of data rates from 64kbps to 1168kbps.

Functionally, this unit consists of a transmit and a receive section. The transmit section generates analog signals from 2-bit digital symbol data and filters the analog signals to create 2B1Q symbols. The on board differential line driver provides a 13.5dBm signal to the telephone line. The receive section filters and digitizes the symbol data received on the telephone line. This IC operates on a single 5V supply. The digital circuitry in the unit can be connected to a supply from 3.3V to 5V. It is housed in a 28-pin SSOP package.




AFE1124

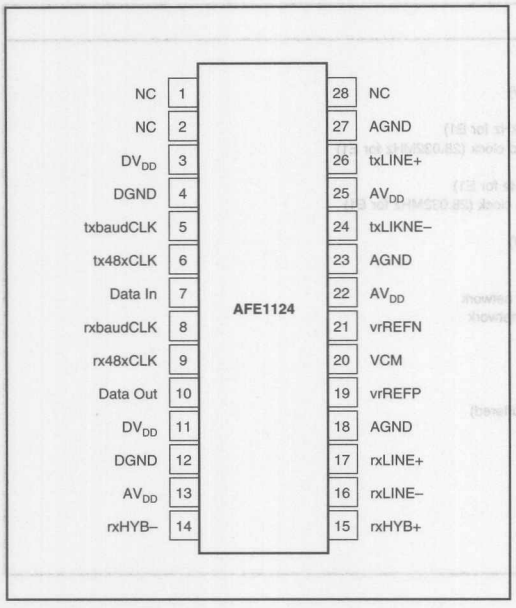
Patents Pending

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| PARAMETER | COMMENTS | AFE1124E | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **RECEIVE CHANNEL** | | | | | |
| Number of Inputs | Differential | 2 | | | |
| Input Voltage Range | Balanced Differential[1] | | ±3.0 | | V |
| Common-Mode Voltage | | | $AV_{DD}/2$ | | V |
| Input Impedance All Inputs | | | See Typical Performance Curves | | |
| Input Capacitance | | | 10 | | pF |
| Input Gain Matching | Line Input vs Hybrid Input | | ±2 | | % |
| Resolution | | 14 | | | Bits |
| Programmable Gain | 0dB, 3dB, 6dB, 9dB and 12dB | 0 | | +12 | dB |
| Settling Time for Gain Change | | | 6 | | Symbol Periods |
| Gain + Offset Error | Tested at Each Gain Range | | 5 | | %FSR[2] |
| Output Data Coding | Two's Complement | | | | |
| Output Symbol Rate, rxSYNC[3] | | 32 | | 584 | kHz |
| Output Bit Rate, rxSYNC[3] | | 64 | | 1168 | kbits/sec |
| **TRANSMIT CHANNEL** | | | | | |
| Transmit Clock Rate, $f_{tx}$ | Symbol Rate | 32 | | 584 | kHz |
| T1 Transmit –3dB Point | ETSI RTR/TM – Compliant | | 196 | | kHz |
| T1 Rate Power[4, 5] | See Test Method Section, txBoost = 0 | 13 | | 14 | dBm |
| E1 Transmit –3dB Point | ETSI RTR/TM – Compliant | | 292 | | kHz |
| E1 Transmit Power[4, 5] | See Test Method Section, txBoost = 0 | 13 | | 14 | dBm |
| Pulse Output | | | See Typical Performance Curves | | |
| Common-Mode Voltage, $V_{CM}$ | | | $AV_{DD}/2$ | | V |
| Output Resistance[6] | DC to 1MHz | | 1 | | Ω |
| **TRANSCEIVER PERFORMANCE** | | | | | |
| Uncancelled Echo[5] | rxGAIN = 0dB, Loopback Enabled | | –71 | –68.5 | dB |
| | rxGAIN = 0dB, Loopback Disabled | | –71 | –68.5 | dB |
| | rxGAIN = 3dB, Loopback Disabled | | –74 | –71 | dB |
| | rxGAIN = 6dB, Loopback Disabled | | –76 | –73.5 | dB |
| | rxGAIN = 9dB, Loopback Disabled | | –78 | –75.5 | dB |
| | rxGAIN = 12dB, Loopback Disabled | | –80 | –77.5 | dB |
| **DIGITAL INTERFACE[6]** | | | | | |
| Logic Levels | | | | | |
| $V_{IH}$ | $\lvert I_{IH}\rvert < 10\mu A$ | $DV_{DD}$ –1 | | $DV_{DD}$ +0.3 | V |
| $V_{IL}$ | $\lvert I_{IL}\rvert < 10\mu A$ | –0.3 | | +0.8 | V |
| $V_{OH}$ | $I_{OH} = -20\mu A$ | $DV_{DD}$ –0.5 | | | V |
| $V_{OL}$ | $I_{OL} = 20\mu A$ | | | +0.4 | V |
| $t_{rx1}$ Interface | | 9 | | 14 | ns |
| **POWER** | | | | | |
| Analog Power Supply Voltage | Specification | | 5 | | V |
| Analog Power Supply Voltage | Operating Range | 4.75 | | 5.25 | V |
| Digital Power Supply Voltage | Specification | | 3.3 | | V |
| Digital Power Supply Voltage | Operating Range | 3.15 | | 5.25 | V |
| Power Dissipation[4, 5] | $AV_{DD}$ = 5V, $DV_{DD}$ = 3.3V, | | 250 | | mW |
| Power Dissipation[4, 5] | $AV_{DD} = DV_{DD}$ = 5V | | 300 | | mW |
| PSRR | | | 55 | | dB |
| **TEMPERATURE RANGE** | | | | | |
| Operating[6] | | –40 | | +85 | °C |

NOTES: (1) With a balanced differential signal, the positive input is 180° out of phase with the negative input, therefore the actual voltage swing about the common-mode voltage on each pin is ±1.5V to achieve a total input range of ±3.0V or 6Vp-p. (2) FSR is Full-Scale Range. (3) The output data is available at twice the symbol rate with interpolated values. (4) With a pseudo-random equiprobable sequence of HDSL pulses; 13.5dBm applied to the transformer (16.5dBm output from txLINEP and txLINEN). (5) See the Discussion of Specifications section of this data sheet for more information. (6) Guaranteed by design and characterization.

## PIN CONFIGURATION




## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| AFE1124E | 28-Pin SSOP | 324 | –40 to +85 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: Current | ±100mA, Momentary |
| | ±10mA, Continuous |
| Voltage | AGND –0.3V to $AV_{DD}$ +0.3V |
| Analog Outputs Short Circuit to Ground (+25°C) | Continuous |
| $AV_{DD}$ to AGND | –0.3V to 6V |
| $DV_{DD}$ to DGND | –0.3V to 6V |
| Digital Input Voltage to DGND | –0.3V to $DV_{DD}$ +0.3V |
| Digital Output Voltage to DGND | –0.3V to $DV_{DD}$ +0.3V |
| AGND, DGND, Differential Voltage | 0.3V |
| Junction Temperature ($T_J$) | +150°C |
| Storage Temperature Range | –40°C to +125°C |
| Lead Temperature (soldering, 3s) | +260°C |
| Power Dissipation | 700mW |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

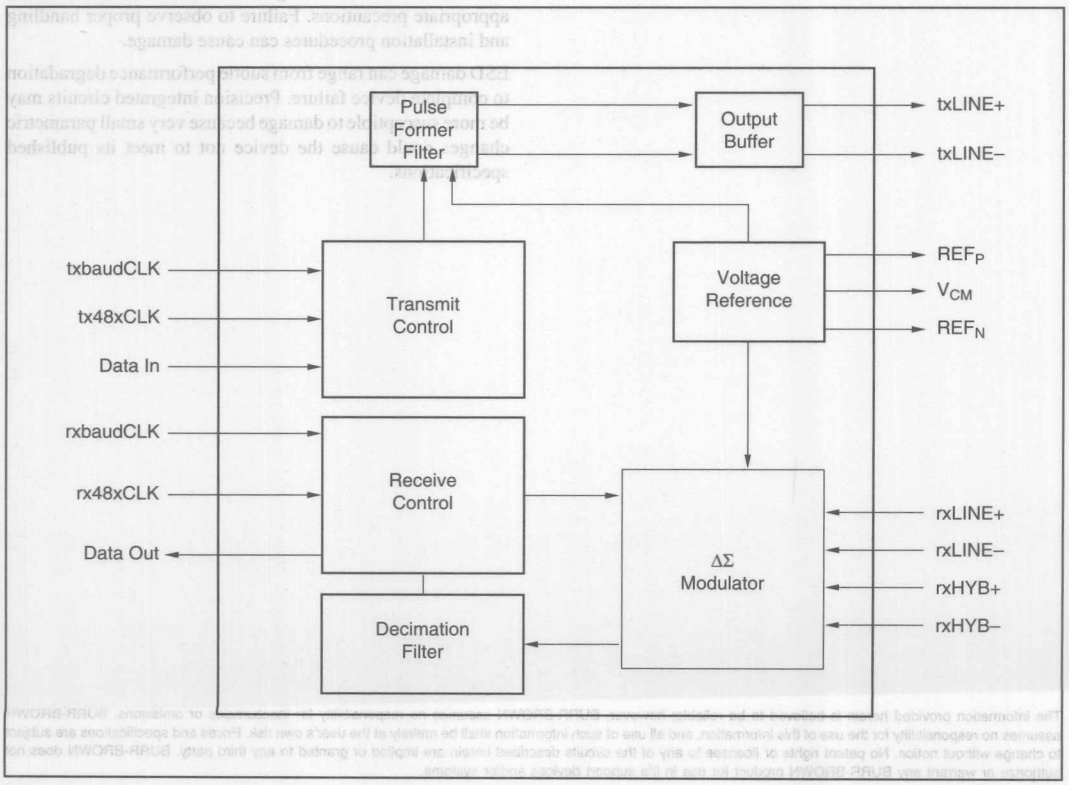
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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## PIN DESCRIPTIONS

| PIN # | TYPE | NAME | DESCRIPTION |
|---|---|---|---|
| 1 | No Connection | NC | |
| 2 | No Connection | NC | |
| 3 | Power | $DV_{DD}$ | Digital Supply (+3.3 to +5V) |
| 4 | Ground | DGND | Digital Ground |
| 5 | Input | txbaudCLK | Transmit Baud Clock (584kHz for E1) |
| 6 | Input | tx48xCLK | Transmit Clock at 48x baud clock (28.032MHz for E1) |
| 7 | Input | Data In | Input Data Word |
| 8 | Input | rxbaudCLK | Receive baud clock (584kHz for E1) |
| 9 | Input | rx48xCLK | Receive clock at 48x baud clock (28.032MHz for E1) |
| 10 | Output | Data Out | Output Data Word |
| 11 | Power | $DV_{DD}$ | Digital Supply (+3.3 to +5V) |
| 12 | Ground | DGND | Digital Ground |
| 13 | Power | $AV_{DD}$ | Analog Supply (+5V) |
| 14 | Input | rxHYB– | Negative input from hybrid network |
| 15 | Input | rxHYB+ | Positive input from hybrid network |
| 16 | Input | rxLINE– | Negative line input |
| 17 | Input | rxLINE+ | Positive line input |
| 18 | Ground | AGND | Analog Ground |
| 19 | Output | vrREFP | Positive reference output |
| 20 | Output | VCM | Common-mode voltage (buffered) |
| 21 | Output | vrREFN | Negative reference output |
| 22 | Power | AVDD | Analog Supply (+5V) |
| 23 | Ground | AGND | Analog Ground |
| 24 | Output | txLINE– | Negative line output |
| 25 | Power | $AV_{DD}$ | Output buffer supply (+5V) |
| 26 | Output | txLINE+ | Positive line output |
| 27 | Ground | AGND | Output buffer ground |
| 28 | No Connection | NC | |

## BLOCK DIAGRAM



BURR-BROWN®



# DDC101

www.burr-brown.com/databook/DDC101.html



# 20-BIT ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- MONOLITHIC CHARGE INPUT ADC
- DIGITAL FILTER NOISE REDUCTION: 0.9ppm, rms
- DIGITAL ERROR CORRECTION: CDS
- CONVERSION RATE: Up to 15kHz
- USER FRIENDLY EVALUATION FIXTURE

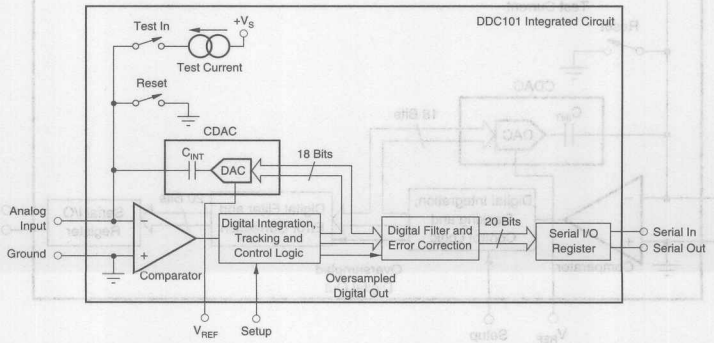
## APPLICATIONS

- DIRECT PHOTOSENSOR DIGITIZATION
- PRECISION INSTRUMENTATION
- INFRARED PYROMETRY
- PRECISION PROCESS CONTROL
- CT SCANNER DAS
- CHEMICAL ANALYZERS

## DESCRIPTION

The DDC101 is a precision, wide dynamic range, charge digitizing A/D converter with 20-bit resolution. Low level current output devices, such as photosensors, can be directly connected to its input. The most stringent accuracy requirements of many unipolar output sensor applications occur at low signal levels. To meet this requirement, Burr-Brown developed the adaptive delta modulation architecture of the DDC101 to provide linearly improving noise and linearity errors as the input signal level decreases. The DDC101 combines the functions of current-to-voltage conversion, integration, input programmable gain amplification, A/D conversion, and digital filtering to produce precision, wide dynamic range results. The input signal can be a low level current connected directly into the unit or a voltage connected through a user selected resistor. Although the DDC101 is optimized for unipolar signals, it can also accurately digitize bipolar input signals. The patented delta modulation topology combines charge integration and digitization functions. Oversampling and digital filtering reduce system noise dramatically. Correlated Double Sampling (CDS) captures and eliminates steady state and conversion cycle dependent offset and switching errors that are not eliminated with conventional analog circuits.

The DDC101 block diagram is shown below. During conversion, the input signal is collected on the internal integration capacitance for a user determined integration period. A high precision, autozeroed comparator samples the analog input node. Tracking logic updates the internal high resolution D/A converter at a 2MHz rate to maintain the analog input at virtual ground. A user programmable digital filter oversamples the tracking logic's output. The digital filter passes a low noise, high resolution digital output to the serial I/O register. The serial outputs of multiple DDC101 units can be easily connected together in series or parallel if desired to minimize interconnections.




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Section 1 ..... Basic Theory of Operation
2 ..... Specifications
3 ..... Pin Descriptions
4 ..... Timing Diagrams
5 ..... Discussion of Specifications
6 ..... Detailed Theory of Operation
7 ..... Applications Information
8 ..... Mechanical

# SECTION 1
# BASIC THEORY OF OPERATION

The basic function of the DDC101 is illustrated in the Simplified Equivalent Circuit shown in Figure 1. The operation is equivalent to the functions performed by a very high quality, low bias current switched integrator followed by a precision floating point programmable gain amplifier and ending with a high resolution A/D converter.

monolithically. During each conversion, the input signal current is collected on the internal integration capacitance, $C_{INT}$, as charge for a user determined integration period, $T_{INT}$. As the integration capacitor collects input charge, the tracking logic updates the internal high resolution D/A converter at a 2MHz rate to maintain the analog input node at virtual ground.

The digital filter oversamples the tracking logic's output at the beginning and end of each integration period to produce two oversampled data points. The DDC101 measures the charge accumulated in the integration and performs correlated double sampling (CDS) by subtracting these two data points. CDS eliminates integration cycle dependent errors such as charge injection, offset voltage, and reset noise since these errors are measured with the signal at each of the two data points. The number of oversamples, and thus the frequency response of the digital filter, is user programmable.

The digital filter passes a low noise, high resolution digital output to the serial I/O register. Since the timing control of the serial I/O register is independent of the DDC101 conversion process, the outputs of multiple DDC101 units can be connected together in series or parallel to minimize interconnections.

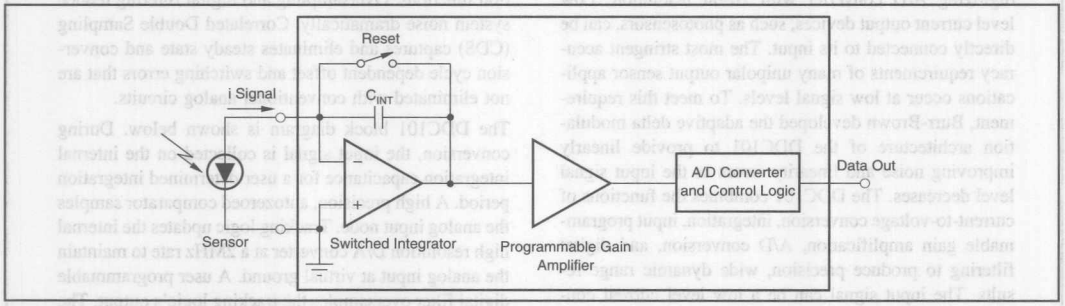



FIGURE 1. Simplified Equivalent Circuit of DDC101 to Illustrate Function.

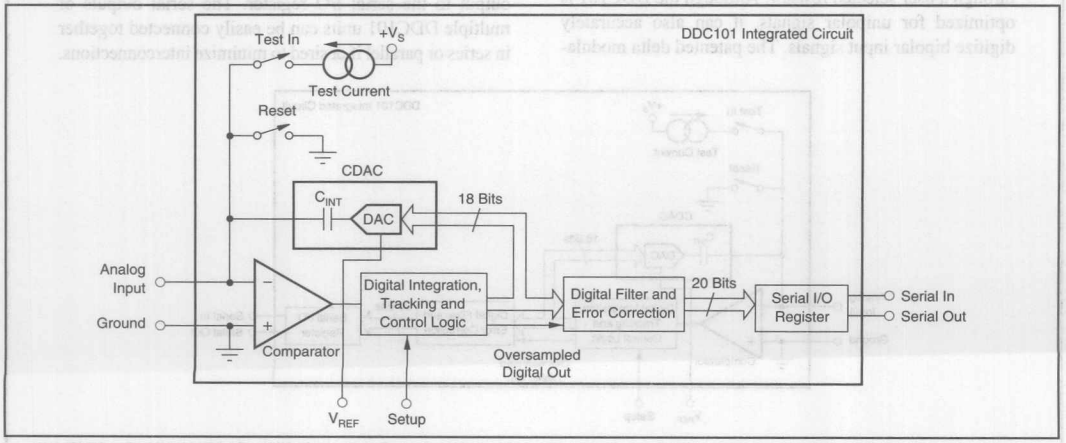



FIGURE 2. DDC101 Block Diagram.

An internal test current source is provided for basic functionality testing and diagnostics. This approximately 100nA current source is pin activated and sums with the external input current.

Figure 3 shows a more detailed circuit configuration of the DDC101. The single integration capacitor, $C_{INT}$, and the D/A converter have been replaced with a high resolution Capacitor Digital-to-Analog Converter (CDAC). By switching between ground and $V_{REF}$ the binary weighted capacitor array of the CDAC accumulates the input signal's charge to keep the comparator input at virtual ground.

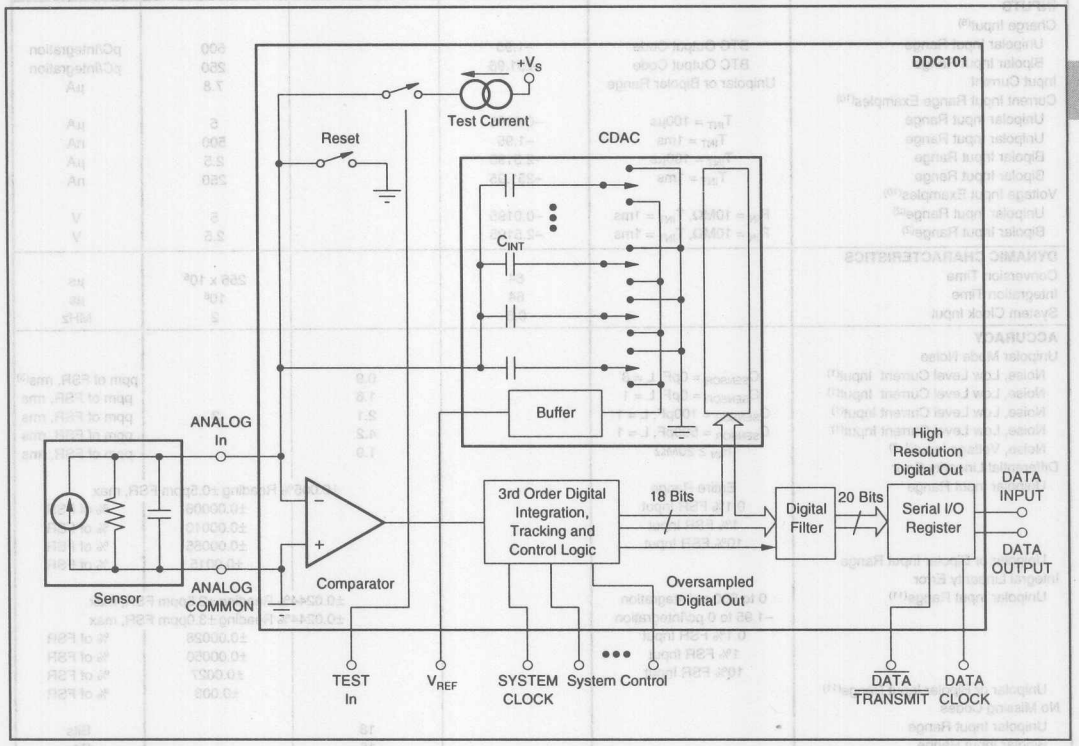



FIGURE 3. DDC101 Detailed Circuit Diagram.

# SECTION 2
# SPECIFICATIONS

## ELECTRICAL

All specifications with unipolar current input range, $T_{INT}$ = 1ms, correlated double sampling enabled, System Clock = 2MHz, $V_{REF}$ = –2.5V, $T_A$ = +25°C and $V_S$ = ±5VDC, unless otherwise noted.

| PARAMETER | CONDITIONS | DDC101 MIN | DDC101 TYP | DDC101 MAX | UNITS |
|---|---|---|---|---|---|
| **INPUTS** | | | | | |
| Charge Input[6] | | | | | |
| Unipolar Input Range | BTC Output Code | –1.95 | | 500 | pC/Integration |
| Bipolar Input Range | BTC Output Code | –251.95 | | 250 | pC/Integration |
| Input Current | Unipolar or Bipolar Range | | | 7.8 | µA |
| Current Input Range Examples[10] | | | | | |
| Unipolar Input Range | $T_{INT}$ = 100µs | –0.0195 | | 5 | µA |
| Unipolar Input Range | $T_{INT}$ = 1ms | –1.95 | | 500 | nA |
| Bipolar Input Range | $T_{INT}$ = 100µs | –2.5195 | | 2.5 | µA |
| Bipolar Input Range | $T_{INT}$ = 1ms | –251.95 | | 250 | nA |
| Voltage Input Examples[10] | | | | | |
| Unipolar Input Range[2] | $R_{IN}$ = 10MΩ, $T_{INT}$ = 1ms | –0.0195 | | 5 | V |
| Bipolar Input Range[2] | $R_{IN}$ = 10MΩ, $T_{INT}$ = 1ms | –2.5195 | | 2.5 | V |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Conversion Time | | 64 | | $256 \times 10^6$ | µs |
| Integration Time | | 64 | | $10^6$ | µs |
| System Clock Input | | 0.5 | | 2 | MHz |
| **ACCURACY** | | | | | |
| Unipolar Mode Noise | | | | | |
| Noise, Low Level Current Input[1] | $C_{SENSOR}$ = 0pF, L = 8 | | 0.9 | | ppm of FSR, rms[3] |
| Noise, Low Level Current Input[1] | $C_{SENSOR}$ = 0pF, L = 1 | | 1.6 | | ppm of FSR, rms |
| Noise, Low Level Current Input[1] | $C_{SENSOR}$ = 100pF, L = 1 | | 2.1 | 3 | ppm of FSR, rms |
| Noise, Low Level Current Input[1] | $C_{SENSOR}$ = 500pF, L = 1 | | 4.2 | | ppm of FSR, rms |
| Noise, Voltage Input[1, 2] | $R_{IN} \geq 20M\Omega$ | | 1.9 | | ppm of FSR, rms |
| Differential Linearity Error | | | | | |
| Unipolar Input Range | Entire Range | | ±0.005% Reading ±0.5ppm FSR, max | | |
| | 0.1% FSR Input | | | ±0.00006 | % of FSR |
| | 1% FSR Input | | | ±0.00010 | % of FSR |
| | 10% FSR Input | | | ±0.00055 | % of FSR |
| Unipolar or Bipolar Input Range | | | | ±0.0015 | % of FSR |
| Integral Linearity Error | | | | | |
| Unipolar Input Range[11] | 0 to 500 pc/Integration | | ±0.0244% Reading ±2.5ppm FSR, max | | |
| | –1.95 to 0 pc/Integration | | ±0.0244% Reading ±3.0ppm FSR, max | | |
| | 0.1% FSR Input | | | ±0.00028 | % of FSR |
| | 1% FSR Input | | | ±0.00050 | % of FSR |
| | 10% FSR Input | | | ±0.0027 | % of FSR |
| Unipolar or Bipolar Input Range[11] | | | | ±0.003 | % of FSR |
| No Missing Codes | | | | | |
| Unipolar Input Range | | | 18 | | Bits |
| Bipolar Input Range | | | 16 | | Bits |
| Input Bias Current | $T_A$ = +25°C | | 3 | 10 | pA |
| DC Gain Error | | | ±0.5 | ±2 | % of FSR |
| Output Offset Error[8] | | | ±0.5 | | ppm of FSR |
| Input Offset Voltage[8] | | | ±0.5 | ±2 | mV |
| External Voltage Reference, $V_{REF}$ | | | –2.5 | | VDC |
| Internal Test Signal | | | 100 | | nA |
| Internal Test Signal Accuracy | | | ±20 | | nA |
| Gain Sensitivity to $V_{REF}$ | $V_{REF}$ = 2.5V ±0.1V | | 1:1 | | |
| PSRR | | 80 | 90 | | dB |
| **PERFORMANCE OVER TEMPERATURE** | | | | | |
| Output Offset Drift[8] | not including bias current drift | | 0 | | µV/°C |
| Input Offset Voltage Drift[8] | | | 1 | | µV/°C |
| Input Bias Current Drift | +25°C to +45°C | | 0.1 | 0.5 | pA/°C |
| Input Bias Current | $T_A$ = +85°C | | 8 | 40 | pA |
| Gain Drift[4] | | | ±15 | | ppm/°C |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic Family | | | TTL Compatible CMOS | | |
| Logic Level: $V_{IH}$ | $I_{IH}$ = +5µA | +2.0 | | $+V_{CC}$ | V |
| $V_{IL}$ | $I_{IL}$ = +5µA | –0.3 | | +0.8 | V |
| $V_{OH}$ | $I_{OH}$ = 2 TTL Loads | +2.4 | | $+V_{CC}$ | V |
| $V_{OL}$ | $I_{OL}$ = 2 TTL Loads | 0.0 | | 0.4 | V |
| Data Clock | | | | | |
| Data I/O | | | | 8 | MHz |
| SETUP Code I/O[9] | | | | 4 | MHz |
| Data Format | | | | | |
| Straight Binary | Unipolar or Bipolar Range | | 20 | | Bits |
| Two's Complement | Unipolar or Bipolar Range | | 21 | | Bits |

# SPECIFICATIONS (CONT)

## ELECTRICAL

All specifications with unipolar current input range, $T_{INT}$ = 1ms, correlated double sampling enabled, System Clock = 2MHz, $V_{REF}$ = –2.5V, $T_A$ = +25°C and $V_S$ = ±5VDC, unless otherwise noted.

| PARAMETER | CONDITIONS | DDC101 MIN | DDC101 TYP | DDC101 MAX | UNITS |
|---|---|---|---|---|---|
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Operation[5] | | ±4.75 | ±5 | ±5.25 | VDC |
| Quiescent Current, Positive Supply | $V_S$+ = +5VDC, $V_{DD}$+ = +5VDC | | 15.6 | 19.5 | mA |
| Analog, $V_S$+ | | | 8.9 | | mA |
| Digital, $V_{DD}$+ | | | 6.7 | | mA |
| Quiescent Current, Negative Supply | $V_S$– = –5VDC | | 18.0 | 22.5 | mA |
| Operating Power | | | 170 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –40 | | +85 | °C |
| Storage | | –60 | | +100 | °C |

NOTES: (1) Input = low level (less than 1% of Full Scale); Full Scale $I_{IN}$ = 500nA: $T_{INT}$ = 1ms; Unipolar Input Range; Acquisition Time = 16 clock cycles, Oversampling = 128. (2) Voltage input is converted through user provided input resistor, $R_{IN}$. (3) FSR is Full Scale Range. (4) Gain Drift does not include the drift of the external reference. (5) $V_{DD}$+ must be less than or equal to $V_S$+. See Section 7 for recommended connections. (6) Straight Binary output code has slightly different Charge Range. See Section 6. (8) Input offset voltage is nulled by autozero circuitry and causes no output error. See Section 6 (Internal Error Correction). (9) This is the maximum clock frequency at which SETUP codes can be written to and read from the DDC101. (10) For other input current and voltage configurations, see Discussion of Specifications and Detailed Theory of Operation sections. (11) A best-fit straight line method is used to determine linearity. Two different best-fit straight lines are used for the two unipolar integral linearity specifications. Acquisition Time = 16 clock cycles, Oversampling = 128.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | THERMAL RESISTANCE ($\theta_{JA}$) (°C/W) |
|---|---|---|---|
| DDC101U | 24-Lead SOIC | 239 | 100 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

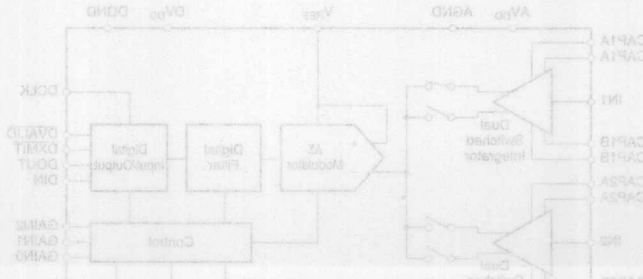
## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs | |
| Input Current | 100mA, momentary |
| Input Current | 10mA, continuous |
| Input Voltage | $V_S$+ +0.5V to $V_S$– –0.5V |
| Power Supply | |
| $V_S$+ | + 7V |
| $V_S$– | –7V |
| $V_{DD}$+ | must be ≤ $V_S$+ |
| Maximum Junction Temperature | +165°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.



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# DDC112



PRELIMINARY INFORMATION
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www.burr-brown.com/databook/DDC112.html

# Dual Input 20-Bit ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- MONOLITHIC CHARGE MEASUREMENT ADC
- DIGITAL FILTER NOISE REDUCTION: 3.2ppm, rms
- CONVERSION RATE: 2kHz
- DIFFERENTIAL LINEARITY: ±0.005% Reading + 0.5ppm FSR, max
- HIGH PRECISION, TRUE INTEGRATING FUNCTION
- SINGLE SUPPLY

## APPLICATIONS

- DIRECT PHOTOSENSOR DIGITIZATION
- CT SCANNER DAS
- INFRARED PYROMETER
- PRECISION PROCESS CONTROL
- LIQUID/GAS CHROMOTOGRAPHY
- BLOOD ANALYSIS

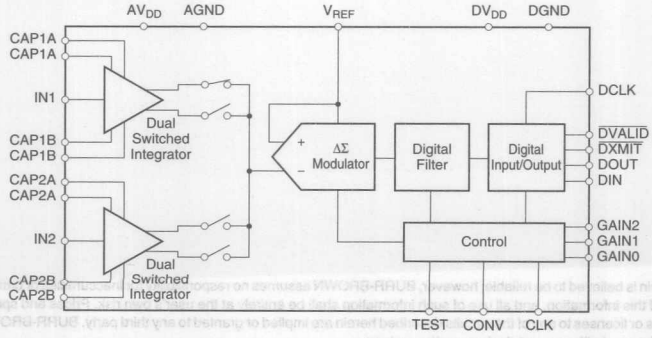
## DESCRIPTION

The DDC112 is a dual input, wide dynamic range, charge digitizing analog-to-digital converter (ADC) with 20-bit resolution. Low level current output devices, such as photosensors, can be directly connected to its input. Charge integration is continuous as each channel contains two integrators; while one is being digitized, the other is integrating.

For each of its two inputs, the DDC112 combines current-to-voltage conversion, continuous integration, programmable full-scale range, analog-to-digital conversion, and digital filtering to achieve a precision, wide dynamic range digital result. Oversampling and digital filtering substantially reduces system noise. In addition, external integrating capacitors allow an additional user-settable full-scale range.

To provide single-supply operation, the internal ADC utilizes a differential input, with the non-inverting input tied to $V_{REF}$. When the integration capacitor is reset at the beginning of each integration cycle, the capacitor obtains a charge that is proportional to $V_{REF}$. This charge is removed in proportion to the input current. At the end of the integration cycle, the remaining voltage is compared to $V_{REF}$.

The high-speed serial shift register holds the result of the last conversion and is independent of the conversion process. The DIN input allows multiple DDC112 units to be cascaded, minimizing interconnections. The DDC112 is available in a 28-lead SOIC package and is guaranteed over the –40°C to +85°C temperature range.




Patents Pending

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

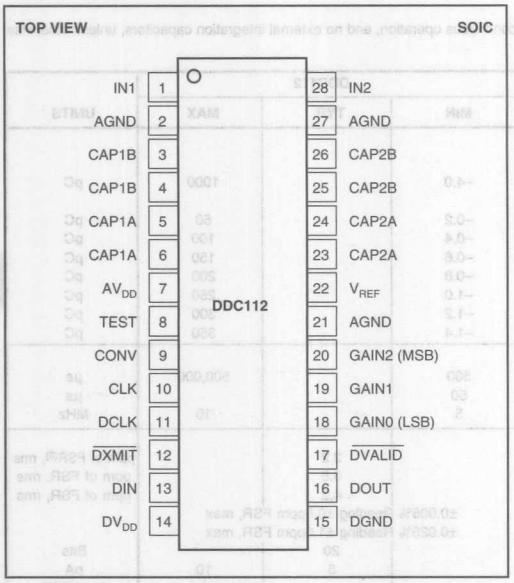
At $T_A$ = +25°C, $AV_{DD}$ = $DV_{DD}$ = +5V, $T_{INT}$ = 500µs, $f_{CLK}$ = 10MHz, $V_{REF}$ = +4.096V, continuous operation, and no external integration capacitors, unless otherwise noted.

| PARAMETER | CONDITIONS | DDC112 MIN | DDC112 TYP | DDC112 MAX | UNITS |
|---|---|---|---|---|---|
| **ANALOG INPUTS** | | | | | |
| External | | | | | |
| Range 0[1] | Integration Capacitor = 250pF | –4.0 | | 1000 | pC |
| Internal | | | | | |
| Range 1[1] | | –0.2 | | 50 | pC |
| Range 2[1] | | –0.4 | | 100 | pC |
| Range 3[1] | | –0.6 | | 150 | pC |
| Range 4[1] | | –0.8 | | 200 | pC |
| Range 5[1] | | –1.0 | | 250 | pC |
| Range 6[1] | | –1.2 | | 300 | pC |
| Range 7[1] | | –1.4 | | 350 | pC |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Integration Time, $T_{INT}$ | Continuous | 500 | | 500,000 | µs |
| Integration Time, $T_{INT}$ | Non-continuous | 50 | | | µs |
| System Clock Input | | 5 | | 10 | MHz |
| **ACCURACY** | | | | | |
| Noise, Low Level Current Input[2] | $C_{SENSOR}$ = 0pF, Range 5 (250pC) | | 3.2 | | ppm of FSR[3], rms |
| | $C_{SENSOR}$ = 25pF, Range 5 (250pC) | | 3.8 | | ppm of FSR, rms |
| | $C_{SENSOR}$ = 50pF, Range 5 (250pC) | | 4.2 | | ppm of FSR, rms |
| Differential Linearity Error | | | ±0.005% Reading ±0.5ppm FSR, max | | |
| Integral Linearity Error | | | ±0.025% Reading ±1.0ppm FSR, max | | |
| No Missing Codes | | | 20 | | Bits |
| Input Bias Current | $T_A$ = +25°C | | 5 | 10 | pA |
| Gain Error | Range 5 (250pC) | | | 5 | % of FSR |
| Gain Error Match | Range 5 (250pC) | | 0.1 | 0.5 | % of FSR |
| Gain Sensitivity to $V_{REF}$ | $V_{REF}$ = 4.096 ±0.1V | | 1:1 | | |
| Offset Error | | | 200 | | ppm of FSR |
| Offset Error Match | | | 100 | | ppm of FSR |
| DC Bias Voltage | Applied to Sensor Input | | 0.2 | | mV |
| Power Supply Rejection Ratio | | | 100 | | ppm/V |
| **PERFORMANCE OVER TEMPERATURE** | | | | | |
| Offset Drift | | | TBD | | ppm/°C |
| Offset Drift Stability | | | 0.01 | | ppm/minute |
| DC Bias Voltage Drift | Applied to Sensor Input | | 1 | | µV/°C |
| Input Bias Current Drift | +25°C to +45°C | | | 1 | pA/°C |
| Input Bias Current | $T_A$ = +75°C | | TBD | TBD | pA |
| Gain Drift[4] | Range 5 (250pC) | | ±20 | | ppm/°C |
| Gain Drift Match | Range 5 (250pC) | | TBD | | ppm/°C |
| **REFERENCE** | | | | | |
| Voltage | | | 4.096 | | V |
| Input Current[5] | | | 150 | | µA |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic Family | | | CMOS | | |
| Logic Levels | | | | | |
| $V_{IH}$ | $I_{IH}$ = ±10µA | 3.0 | | $DV_{DD}$ +0.3 | V |
| $V_{IL}$ | $I_{IL}$ = ±10µA | –0.3 | | +0.8 | V |
| $V_{OH}$ | $I_{OH}$ = –500µA | 3.6 | | | V |
| $V_{OL}$ | $I_{OL}$ = 500µA | | | 0.4 | V |
| Data Clock | | | | 10 | MHz |
| Data Format[6] | | | Straight Binary | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Power Supply Voltage | $AV_{DD}$ and $DV_{DD}$ | 4.75 | | 5.25 | V |
| Supply Current | | | | | |
| Analog Current | $AV_{DD}$ = +5V | | 14.5 | | µA |
| Digital Current | $DV_{DD}$ = +5V | | 1.5 | | µA |
| Power Dissipation | | | 80 | TBD | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified Performance | | –40 | | +85 | °C |
| Storage | | –60 | | +100 | °C |

NOTES: (1) Ideal input range, does not take into account gain and offset error. (2) Input is less than 1% of full scale. (3) FSR is Full-Scale Range. (4) Gain drift does not include external reference drift. (5) Input reference current decreases with increasing $T_{INT}$. (6) Data format is Straight Binary with small offset (see text).

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN CONFIGURATION




## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| $AV_{DD}$ to $DV_{DD}$ | –0.3V to +6V |
| $AV_{DD}$ to AGND | –0.3V to +6V |
| $DV_{DD}$ to DGND | –0.3V to +6V |
| AGND to DGND | ±0.3V |
| $V_{REF}$ Voltage to AGND | –0.3V to $AV_{DD}$ +0.3V |
| Digital Input Voltage to DGND | –0.3V to $DV_{DD}$ +0.3V |
| Digital Output Voltage to DGND | –0.3V to $DV_{DD}$ +0.3V |
| Package Power Dissipation | $(T_{JMAX} - T_A)/\theta_{JA}$ |
| Maximum Junction Temperature ($T_{JMAX}$) | +150°C |
| Thermal Resistance, $\theta_{JA}$ | 150°C/W |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## PIN DESCRIPTIONS

| PIN | LABEL | DESCRIPTION |
|---|---|---|
| 1 | IN1 | Analog Input for Integrators 1A and 1B. The integrator that is active is set by the CONV input. |
| 2 | AGND | Analog Ground. |
| 3 | CAP1B | External Capacitor for Integrator 1B. |
| 4 | CAP1B | External Capacitor for Integrator 1B. |
| 5 | CAP1A | External Capacitor for Integrator 1A. |
| 6 | CAP1A | External Capacitor for Integrator 1A. |
| 7 | $AV_{DD}$ | Analog Supply, +5V nominal. |
| 8 | TEST | Test Control Input. When HIGH, a test charge is applied to the A or B integrators on the next CONV transition. |
| 9 | CONV | Asynchronous Convert Input. A transition on this input switches the integrate/measure mode for the integrators. When HIGH, integrators 1A and 2A are integrating and 1B and 2B are waiting to be measured. The opposite is true when CONV is LOW. |
| 10 | CLK | System Clock Input, 10MHz nominal. |
| 11 | DCLK | Serial Data Clock Input. This input operates the serial I/O shift register exclusively. |
| 12 | $\overline{DXMIT}$ | Serial Data Transmit Enable Input. When LOW, this input enables the internal serial shift register. |
| 13 | DIN | Serial Digital Input. Used to cascade multiple DDC112s. |
| 14 | $DV_{DD}$ | Digital Supply, +5V nominal. |
| 15 | DGND | Digital Ground. |
| 16 | DOUT | Serial Data Output, Hi-Z when $\overline{DXMIT}$ is HIGH. |
| 17 | $\overline{DVALID}$ | Data Valid Output. A LOW value indicates valid data is available in the serial I/O register. |
| 18 | GAIN0 | Gain Control Input 0 (least significant bit). |
| 19 | GAIN1 | Gain Control Input 1. |
| 20 | GAIN2 | Gain Control Input 2 (most significant bit). |
| 21 | AGND | Analog Ground. |
| 22 | $V_{REF}$ | External Reference Input, +4.096V nominal. |
| 23 | CAP2A | External Capacitor for Integrator 2A. |
| 24 | CAP2A | External Capacitor for Integrator 2A. |
| 25 | CAP2B | External Capacitor for Integrator 2B. |
| 26 | CAP2B | External Capacitor for Integrator 2B. |
| 27 | AGND | Analog Ground. |
| 28 | IN2 | Analog Input for Integrators 2A and 2B. The integrator that is active is set by the CONV input. |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | MAXIMUM DIFFERENTIAL LINEARITY ERROR | MAXIMUM INTEGRAL LINEARITY ERROR | SPECIFICATION TEMPERATURE RANGE | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|---|---|---|
| DDC112U | ±0.005% Reading ±0.5ppm FSR | ±0.025% Reading ±1.0ppm FSR | –40°C to +85°C | 28-Lead SOIC | 217 |

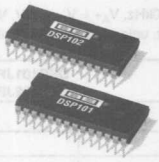
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®



# DSP101
# DSP102

www.burr-brown.com/databook/DSP101.html

# DSP-Compatible Sampling Single/Dual ANALOG-TO-DIGITAL CONVERTERS

## FEATURES

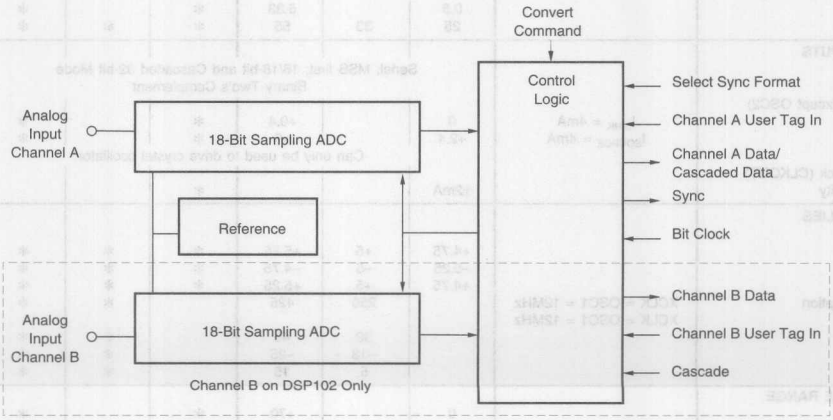
- ZERO-CHIP INTERFACE TO STANDARD DSP ICs: AD, AT&T, MOTOROLA, TI
- SINGLE CHANNEL: DSP101
- DUAL CHANNEL: DSP102
  Two Serial Outputs or Cascade to Single 32-Bit Word
- SAMPLING RATE TO 200kHz
- DYNAMIC SPECIFICATIONS:
  Signal/(Noise + Distortion) = 88dB;
  Spurious-Free Dynamic Range = 94dB;
  THD = –91dB
- SERIAL OUTPUT DATA COMPATIBLE WITH 16-, 24-, AND 32-BIT DSP IC FORMATS

## DESCRIPTION

The DSP101 and DSP102 are high performance sampling analog-to-digital converters designed for simplicity of use with modern digital signal processing ICs. Both are complete with all interface logic for use directly with DSP ICs, and provide full sampling and conversion at rates up to 200kHz.

The DSP101 offers a single conversion channel, with 18 bits of serial data output, allowing the user to drive 16-bit, 24-bit, or 32-bit DSP ports. The DSP102 offers two complete conversion channels, with either two full 18-bit output ports, or a mode to cascade two 16-bit conversions into a 32-bit port as one word.

Both the DSP101 and DSP102 are packaged in standard, low-cost 28-pin plastic DIP packages. Each is offered in two performance grades to match application requirements.




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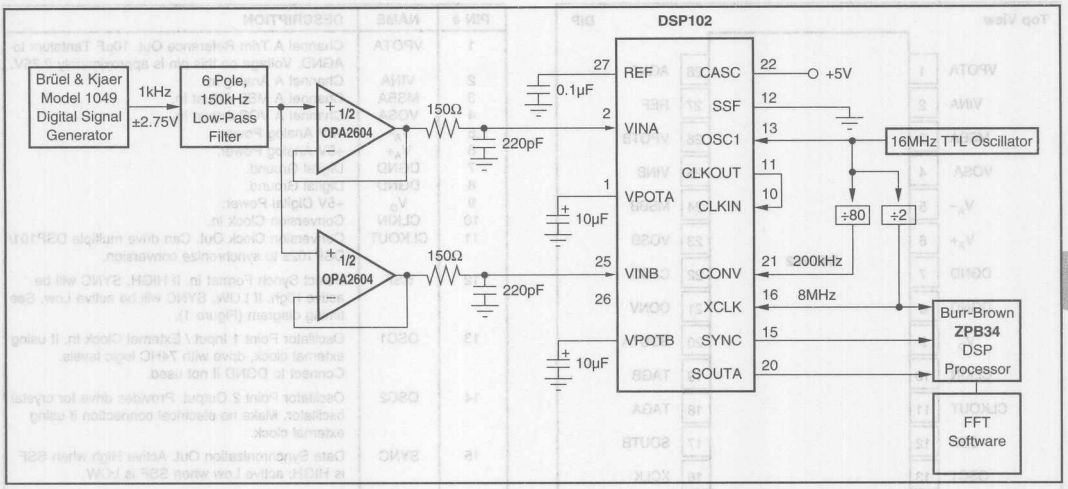
At $T_A$ = 0°C to 70°C, ±2.75V input signal, sampling frequency ($f_S$) = 200kHz, $V_A+ = V_D = +5V$, $V_A- = -5V$, 16MHz external clock on OSC1, CLKOUT tied to CLKIN, 8MHzdata transfer clock on XCLK, data analysis band-limited to 20kHz, unless otherwise specified.

| PARAMETER | CONDITIONS | DSP101JP DSP102JP | | | DSP101KP DSP102KP | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | | 18 | | | * | Bits |
| **ANALOG INPUT** | | | | | | | | |
| Voltage Range | | | ±2.75V | | | * | | V |
| Impedance | | | 1 | | | * | | kΩ |
| Capacitance | | | 20 | | | * | | pF |
| **THROUGHPUT SPEED** | | | | | | | | |
| Complete Cycle | Acquisition + Conversion | | | 5 | | | * | µs |
| Throughput Rate | | 200 | | | * | | | kHz |
| **AC ACCURACY**(1) | | | | | | | | |
| Signal-to-(Noise + Distortion) Ratio | $f_{IN}$ = 1kHz | 83 | 86 | | 86 | 88 | | dB(2) |
| | $f_{IN}$ = 1kHz (–60dB) | | 32 | | | * | | dB |
| | $f_{IN}$ = 25kHz | | 82 | | | * | | dB |
| Total Harmonic Distortion | $f_{IN}$ = 1kHz | | –90 | –86 | | –91 | –89 | dB |
| Spurious-Free Dynamic Range | $f_{IN}$ = 1kHz | 89 | 92 | | 92 | 94 | | dB |
| Signal-to-Noise Ratio (SNR) | $f_{IN}$ = 1kHz | 84 | 88 | | 87 | 89 | | dB |
| **DC ACCURACY** | | | | | | | | |
| Gain Error | | | | ±5 | | * | | % |
| Gain Error Mismatch | DSP102 Channels | | | ±2 | | * | | % |
| Integral Linearity | ±2.75V Input Range | | Sufficient to meet AC Accuracy Specifications | | | | | |
| Differential Linearity | ±2.75V Input Range | | Sufficient to meet AC Accuracy Specifications | | | | | |
| Integral Linearity Error | ±0.7V Input Range | | ±0.003 | | | * | | % |
| Differential Linearity Error | ±0.7V Input Range | | ±0.002 | | | * | | % |
| No Missing Codes | ±0.7V Input Range | | 14 | | | * | | Bits |
| Bipolar Zero Error (3) | | | ±2 | | | | | mV |
| Bipolar Zero Mismatch (3) | DSP102 Channels | | ±2 | | | | | mV |
| Power Supply Sensitivity | $-5.25V < V_A- < -4.75V$ | | –60 | | | * | | dB |
| | $+4.75V < V_A+, V_D+ < +5.25V$ | | –60 | | | * | | dB |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Aperture Delay | | | 30 | | | * | | ns |
| Aperture Jitter | | | 100 | | | * | | ps, rms |
| Transient Response | | | 1 | | | * | | µs |
| Overvoltage Recovery | | | 5 | | | * | | µs |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Levels (Except OSC1) | | | | | | | | |
| $V_{IL}$ | $I_L$ = ±10µA | 0 | | +0.8 | * | | * | V |
| $V_{IH}$ | $I_H$ = ±10µA | +2.4 | | +5 | * | | * | V |
| OSC1 Clock | | | 74HC Compatible | | | | | |
| Frequency | | | | 16 | | | | MHz |
| Data Transfer Clock (XCLK) | | | | | | | | |
| Frequency | | 0.1 | | 12 | * | | * | MHz |
| Duty Cycle | | 40 | 50 | 60 | * | | * | % |
| Conversion Clock (CLKIN) | | | | | | | | |
| Frequency | | 0.5 | | 5.33 | * | | * | MHz |
| Duty Cycle | | 25 | 33 | 55 | * | * | * | % |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Format | | | Serial; MSB first; 16/18-bit and Cascaded 32-bit Mode | | | | | |
| Coding | | | Binary Two's Complement | | | | | |
| Logic Levels (Except OSC2) | | | | | | | | |
| $V_{OL}$ | $I_{SINK}$ = 4mA | 0 | | +0.4 | * | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 4mA | +2.4 | | +5 | * | | * | V |
| OSC2 | | | Can only be used to drive crystal oscillator. | | | | | |
| Conversion Clock (CLKOUT) | | | | | | | | |
| Drive Capability | | ±2mA | | | * | | | mA |
| **POWER SUPPLIES** | | | | | | | | |
| Rated Voltage | | | | | | | | |
| $V_A+$ | | +4.75 | +5 | +5.25 | * | * | * | V |
| $V_A-$ | | –5.25 | –5 | –4.75 | * | * | * | V |
| $V_D$ | | +4.75 | +5 | +5.25 | * | * | * | V |
| Power Consumption | XCLK = OSC1 = 12MHz | | 250 | 425 | | * | * | mW |
| Supply Current | XCLK = OSC1 = 12MHz | | | | | | | |
| $I_A+$ | | | 30 | 45 | | * | * | mA |
| $I_A-$ | | | –18 | –25 | | * | * | mA |
| $I_D$ | | | 5 | 15 | | * | * | mA |
| ***TEMPERATURE RANGE*** | | | | | | | | |
| Specification | | 0 | | +70 | * | | * | °C |
| Storage | | –65 | | +125 | * | | * | °C |

* Specifications same as DSP101JP, DSP102JP.

NOTES: (1) All dynamic specifications are based on 2048-point FFTs, using four-term Blackman-Harris window. (2) All specifications in dB are referred to a full-scale input, ±2.75Vp-p. (3) Adjustable to zero with external potentiometer.

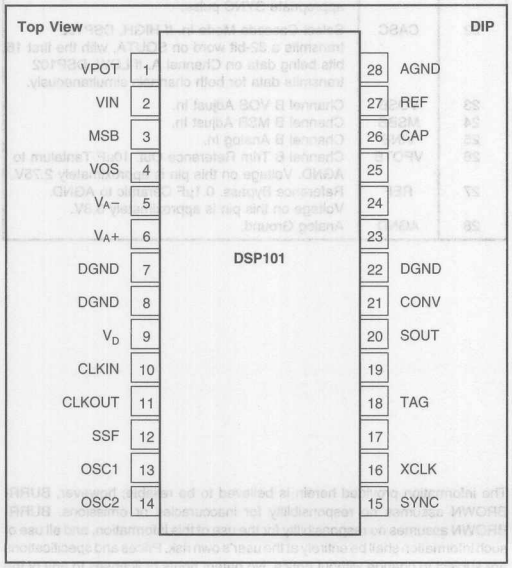
## TYPICAL DSP102 FFT SETUP




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $V_A$+ to Analog Common | +7V |
| $V_A$– to Analog Common | –7V |
| $V_D$ to Digital Common | +7V |
| Analog Common to Digital Common | ±1V |
| Control Inputs to Digital Common | –0.5 to $V_D$ + 0.5V |
| Analog Input Voltage | ±5V |
| Maximum Junction Temperature | 150°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |
| Thermal Resistance, $\theta_{JA}$, Plastic DIP | 50°C/W |

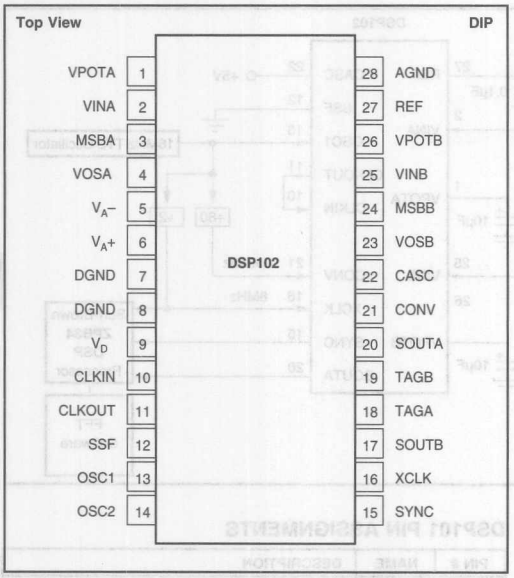
## DSP101 PIN CONFIGURATION




## DSP101 PIN ASSIGNMENTS

| PIN # | NAME | DESCRIPTION |
|---|---|---|
| 1 | VPOT | Trim Reference Out. 10µF Tantalum to AGND. Voltage on this pin is approximately 2.75V. |
| 2 | VIN | Analog In. |
| 3 | MSB | MSB Adjust In. |
| 4 | VOS | VOS Adjust In. |
| 5 | $V_A$– | –5V Analog Power. |
| 6 | $V_A$+ | +5V Analog Power. |
| 7 | DGND | Digital Ground. |
| 8 | DGND | Digital Ground. |
| 9 | $V_D$ | +5V Digital Power. |
| 10 | CLKIN | Conversion Clock In. |
| 11 | CLKOUT | Conversion Clock Out. Can drive multiple DSP101/DSP102s to synchronize conversion. |
| 12 | SSF | Select Synch Format In. If HIGH, SYNC will be active High. If LOW, SYNC will be active Low. See timing diagram (Figure 1). |
| 13 | OSC1 | Oscillator Point 1 Input/External Clock In. If using external clock, drive with 74HC logic levels. Connect to DGND if not used. |
| 14 | OSC2 | Oscillator Point 2 Output. Provides drive for crystal oscillator. Make no electrical connection if using external clock. |
| 15 | SYNC | Data Synchronization Out. Active High when SSF is HIGH; active Low when SSF is LOW. |
| 16 | XCLK | Data Transfer Clock In. |
| 17 | | No Internal Connection. |
| 18 | TAG | User Tag In. Data clocked into this pin is appended to the conversion results on SOUT. See timing diagram (Figure 1). |
| 19 | | No Internal Connection. |
| 20 | SOUT | Serial Data Out. MSB first, Binary Two's Complement format. |
| 21 | CONV | Convert Command In. Falling edge puts converter into hold state, initiates conversion, and transmits previous conversion results to DSP IC with appropriate SYNC pulse. |
| 22 | DGND | Digital Ground. |
| 23 | | No Internal Connection. |
| 24 | | No Internal Connection. |
| 25 | | No Internal Connection. |
| 26 | CAP | Bypass Capacitor. 10µF Tantalum to AGND. Voltage on this pin is approximately 2.7V. |
| 27 | REF | Reference Bypass. 0.1µF Ceramic to AGND. Voltage on this pin is approximately 3.8V. |
| 28 | AGND | Analog Ground. |

## DSP102 PIN CONFIGURATION




## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| DSP101JP | 28-Pin Plastic DIP | 215 |
| DSP101KP | 28-Pin Plastic DIP | 215 |
| DSP102JP | 28-Pin Plastic DIP | 215 |
| DSP102KP | 28-Pin Plastic DIP | 215 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

| PRODUCT | NUMBER OF CHANNELS | SIGNAL-TO-(NOISE + DIST.) RATIO dB min |
|---|---|---|
| DSP101JP | 1 | 83 |
| DSP101KP | 1 | 86 |
| DSP102JP | 2 | 83 |
| DSP102KP | 2 | 86 |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## DSP102 PIN ASSIGNMENTS

| PIN # | NAME | DESCRIPTION |
|---|---|---|
| 1 | VPOTA | Channel A Trim Reference Out. 10µF Tantalum to AGND. Voltage on this pin is approximately 2.75V. |
| 2 | VINA | Channel A Analog In. |
| 3 | MSBA | Channel A MSB Adjust In. |
| 4 | VOSA | Channel A VOS Adjust In. |
| 5 | $V_A-$ | –5V Analog Power. |
| 6 | $V_A+$ | +5V Analog Power. |
| 7 | DGND | Digital Ground. |
| 8 | DGND | Digital Ground. |
| 9 | $V_D$ | +5V Digital Power. |
| 10 | CLKIN | Conversion Clock In. |
| 11 | CLKOUT | Conversion Clock Out. Can drive multiple DSP101/DSP102s to synchronize conversion. |
| 12 | SSF | Select Synch Format In. If HIGH, SYNC will be active High. If LOW, SYNC will be active Low. See timing diagram (Figure 1). |
| 13 | OSC1 | Oscillator Point 1 Input / External Clock In. If using external clock, drive with 74HC logic levels. Connect to DGND if not used. |
| 14 | OSC2 | Oscillator Point 2 Output. Provides drive for crystal oscillator. Make no electrical connection if using external clock. |
| 15 | SYNC | Data Synchronization Out. Active High when SSF is HIGH; active Low when SSF is LOW. |
| 16 | XCLK | Data Transfer Clock In. |
| 17 | SOUTB | Channel B Serial Data Out. MSB first, Binary Two's Complement format. |
| 18 | TAGA | Channel A User Tag In. Data clocked into this pin is appended to the conversion results of SOUTA. See timing diagram (Figure 1). |
| 19 | TAGB | Channel B User Tag In. Data clocked into this pin is appended to the conversion results of SOUTB. See timing diagram (Figure 1). |
| 20 | SOUTA | Channel A Serial Data Out. MSB first, Binary Two's Complement format. If CASC is HIGH, 32 bits of data output, with first 16 bits being Channel A data. |
| 21 | CONV | Convert Command In. Falling edge puts converter into hold state, initiates conversion, and transmits previous conversion results to DSP IC with appropriate SYNC pulse. |
| 22 | CASC | Select Cascade Mode In. If HIGH, DSP102 transmits a 32-bit word on SOUTA, with the first 16 bits being data on Channel A. If LOW, DSP102 transmits data for both channels simultaneously. |
| 23 | VOSB | Channel B VOS Adjust In. |
| 24 | MSBB | Channel B MSB Adjust In. |
| 25 | VINB | Channel B Analog In. |
| 26 | VPOTB | Channel B Trim Reference Out. 10µF Tantalum to AGND. Voltage on this pin is approximately 2.75V. |
| 27 | REF | Reference Bypass. 0.1µF Ceramic to AGND. Voltage on this pin is approximately 3.8V. |
| 28 | AGND | Analog Ground. |

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# VSP2000

**PRELIMINARY INFORMATION
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www.burr-brown.com/databook/VSP2000.html

# CCD SIGNAL PROCESSOR FOR DIGITAL CAMERAS

## FEATURES

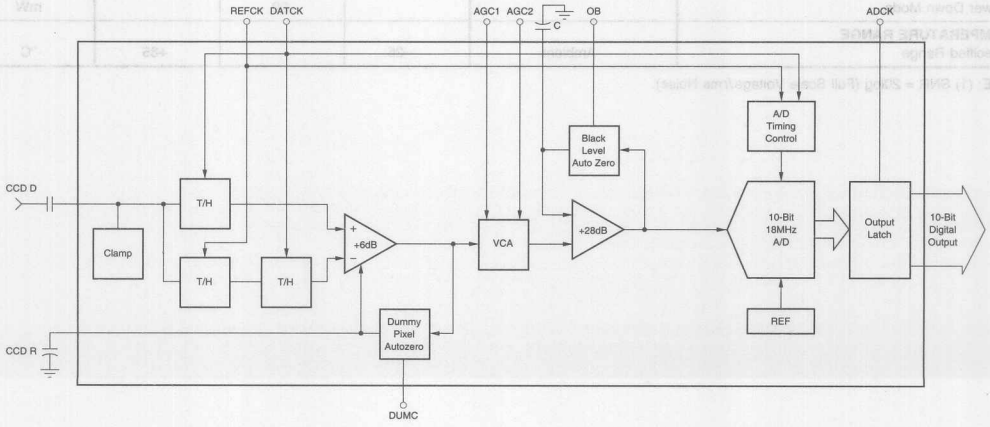
- **CCD SIGNAL PROCESSING:**
  - **Correlated Double Sampling**
  - **Black Level Clamping**
  - **0 to +34dB Gain Ranging**
  - **55dB SNR Referred to Full Well**
- **10-BIT A/D CONVERSION:**
  - **Up to 18MHz Conversion Rate**
  - **No Missing Codes**
- **PORTABLE OPERATION:**
  - **Low Voltage: Down to 2.7V**
  - **Low Power: 165mW at 2.7V**

## DESCRIPTION

The VSP2000 is a COMPLETE mixed-signal processing IC for digital cameras providing signal conditioning and 10-bit analog-to-digital conversion. The primary CCD channel provides correlated double sampling to extract the video information from the pixels, 0dB to +34dB gain ranging with analog control for varying background light conditions, and black level clamping for an accurate black level reference. The stable gain control is linear in dB. Also, the black level is quickly recovered after gain changes.

## APPLICATIONS

- **DIGITAL CAMERAS**
- **PC CAMERAS**
- **SECURITY CAMERAS**
- **VIDEO CAMERAS**

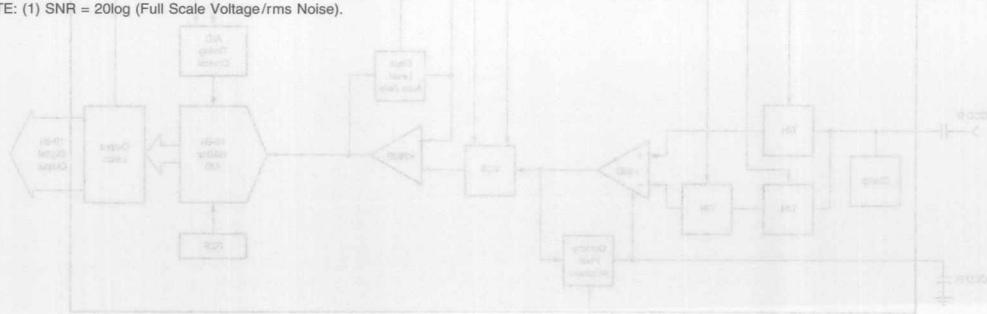



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$V_{DD2}$ = +5.0V, $DV_{DD}$ = $DV_{DD1}$ = $DRV_{DD1}$ = +3.0V, unless otherwise specified.

| PARAMETER | CONDITIONS | VSP2000 MIN | VSP2000 TYP | VSP2000 MAX | UNITS |
|---|---|---|---|---|---|
| **DIGITAL INPUT** | | | | | |
| Logic Family | | | CMOS | | |
| Logic Levels | Logic HI | $+V_{DD}/2$ | | $+V_{DD}$ | V |
| | Logic LO | 0 | | +0.4 | V |
| Logic Currents | Logic HI, $V_{IN} = +V_{DD}$ | | | 10 | µA |
| | Logic LO, $V_{IN} = 0V$ | | | 10 | µA |
| A/D Clock Duty Cycle | | | 50 | | % |
| **DIGITAL OUTPUT** | | | | | |
| Logic Family | | | CMOS | | |
| Logic Levels | Logic HI, $C_L$ = 10pF | $+V_S$ –0.5 | | $+V_S$ | V |
| | Logic LO, $C_L$ = 10pF | 0 | | +0.4 | V |
| **TRANSFER CHARACTERISTICS** | | | | | |
| Resolution | | 10 | | | Bit |
| Differential Non-Linearity | | | ±0.4 | | LSB |
| Integral Non-Linearity | | | ±2.0 | | LSB |
| No Missing Codes | | | Guaranteed | | |
| Signal Settling Time | Black to Full Scale Change to 1/4 LSB into ADS | | 110 | | ns |
| Conversion Rate | | 500kHz | | 18 | MHz |
| Data Latency | | | 5.5 | | Clocks |
| Signal-to-Noise Ratio[1] | Grounded Input Cap, VCA Gain Max | | 53 | | dB |
| Black Clamp Level | | | 32 | | LSB |
| **CDS** | | | | | |
| Data Settling Time to +0.1% for FS Change with $R_S$ = 40 | From Leading Edge of DATCK | | 11 | | ns |
| Input Capacitance | DATCK Low | | 20 | | pF |
| Input Time Constant | | | 300 | | ps |
| Data Full Scale Input | After AC Coupling Cap | | 500 | 600 | mV |
| **INPUT CLAMP** | | | | | |
| Clamp on Resistance | | | 3.0 | | kΩ |
| Clamp Level | | | 1 | | V |
| **VCA CHARACTERISTICS** | | | | | |
| Gain Control Voltage Range | | 0.3 | | 2.4 | V |
| Gain at Max Control Voltage | | | 34 | | dB |
| Gain Control Linearity | | | ±1.0 | | dB |
| Gain Control Settling Time | | | 10 | | µs |
| Transfer Function | | | 20.6 | | dB/V |
| **POWER SUPPLY** | | | | | |
| Rated Voltage | | +2.7 | +3.0 | +3.3 | V |
| Current, Quiescent | 3V Supply | | 63 | | mA |
| Power Dissipation | 3V Supply | | 190 | | mW |
| | 2.7V Supply | | 165 | | mW |
| Power Down Mode | | | 22 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified Range | Ambient | –25 | | +85 | °C |

NOTE: (1) SNR = 20log (Full Scale Voltage/rms Noise).



## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Analog Input | (0 –0.3V) to ($+V_S$ +0.3V) |
| Logic Input | (0 –0.3V) to ($+V_S$ +0.3V) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +150°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

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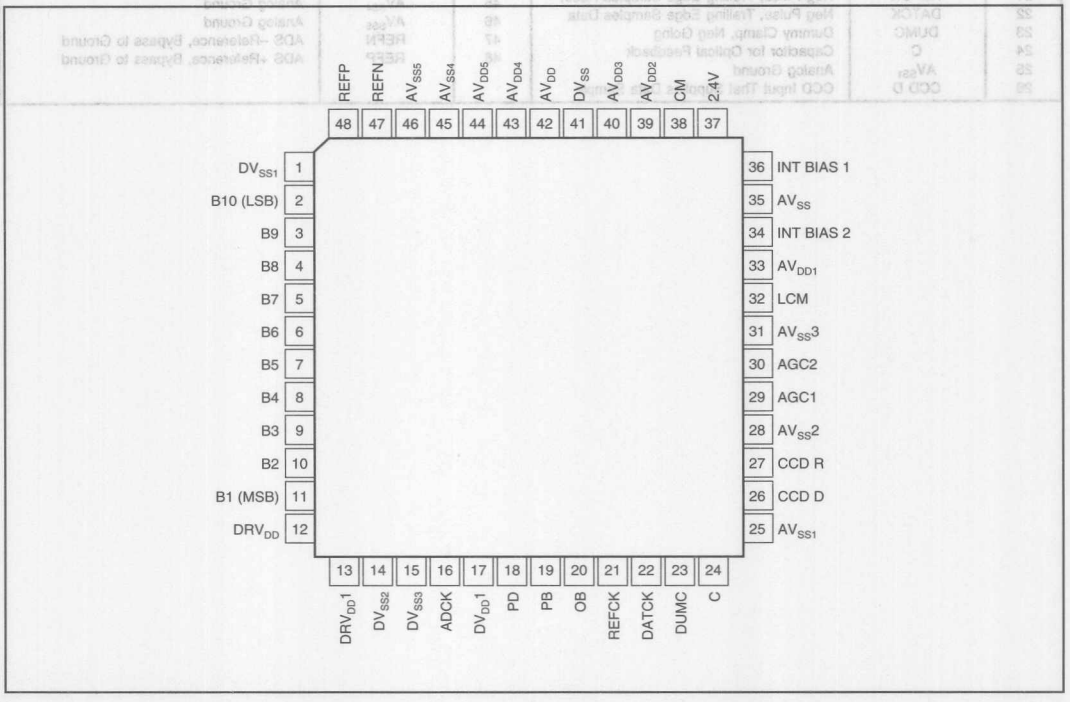
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| VSP2000 | 48-Pin LQFP | 340 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

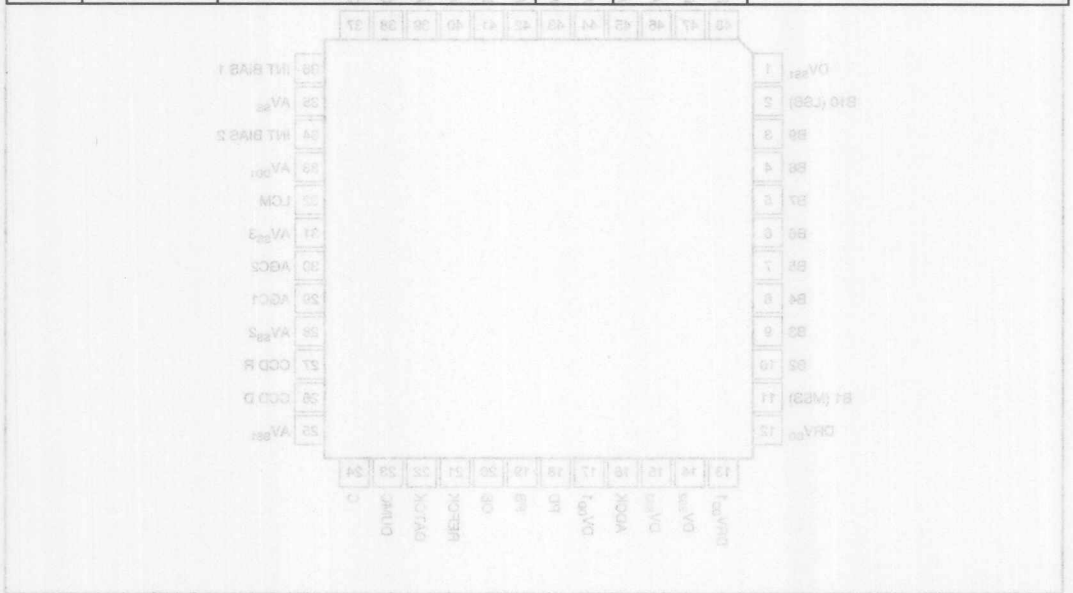
## PIN CONFIGURATION




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## PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION | PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|---|---|---|
| 1 | $DV_{SS1}$ | Digital Ground | 27 | CCD R | Capacitor for Dummy Feedback Loop |
| 2 | B10 (LSB) | LSB of ADS | 28 | $AV_{SS2}$ | Analog Ground |
| 3 | B9 | Bit 9 | 29 | AGC1 | Sets Gain of CCD Channel, 1kΩ Resistor |
| 4 | B8 | Bit 8 | 30 | AGC2 | Sets Gain of CCD Channel, 16kΩ Resistor |
| 5 | B7 | Bit 7 | 31 | $AV_{SS3}$ | Analog Ground |
| 6 | B6 | Bit 6 | 32 | LCM | Attenuator Common-Mode Bypass |
| 7 | B5 | Bit 5 | 33 | $AV_{DD1}$ | Analog +Supply |
| 8 | B4 | Bit 4 | 34 | INT BIAS2 | Internal Bias, should be connected to GND with 0.1µF Capacitor |
| 9 | B3 | Bit 3 | 35 | $AV_{SS}$ | Analog Ground |
| 10 | B2 | Bit 2 | 36 | INT BIAS1 | Internal Bias, should be connected to GND with 0.1µF Capacitor |
| 11 | B1 (MSB) | MSB of ADS | 37 | 2.4V | Attenuator Ladder Bypass |
| 12 | $DRV_{DD1}$ | Digital +Supply of ADS Output | 38 | CM | ADS Common-Mode Voltage |
| 13 | $DRV_{SS1}$ | Digital Ground for ADS Output | 39 | $AV_{DD2}$ | Analog +Supply |
| 14 | $DV_{SS2}$ | Analog Ground | 40 | $AV_{DD3}$ | Analog +Supply |
| 15 | $DV_{SS3}$ | Digital Ground | 41 | $DV_{SS}$ | Digital Ground |
| 16 | ADCK | ADS Clock, Converts on Positive Edge | 42 | $AV_{DD}$ | Analog +Supply |
| 17 | $DV_{DD1}$ | Digital +Supply | 43 | $AV_{DD4}$ | Analog +Supply |
| 18 | PD | L = Normal Operation, H = Reduced Power | 44 | $AV_{DD5}$ | Digital +Supply |
| 19 | PB | L = –FS + 32 LSB, H = Normal at CCD Mode | 45 | $AV_{SS4}$ | Analog Ground |
| 20 | OB | Optical Black Clamp Pulse, Neg Going | 46 | $AV_{SS5}$ | Analog Ground |
| 21 | REFCK | Neg Pulse, Trailing Edge Samples Reset | 47 | REFN | ADS –Reference, Bypass to Ground |
| 22 | DATCK | Neg Pulse, Trailing Edge Samples Data | 48 | REFP | ADS +Reference, Bypass to Ground |
| 23 | DUMC | Dummy Clamp, Neg Going | | | |
| 24 | C | Capacitor for Optical Feedback | | | |
| 25 | $AV_{SS1}$ | Analog Ground | | | |
| 26 | CCD D | CCD Input That Supplies Data Sample | | | |



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# VSP3000

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www.burr-brown.com/databook/VSP3000.html

## SpeedPLUS™ 12-BIT, 6MHz CCD/CIS SIGNAL PROCESSOR

## FEATURES

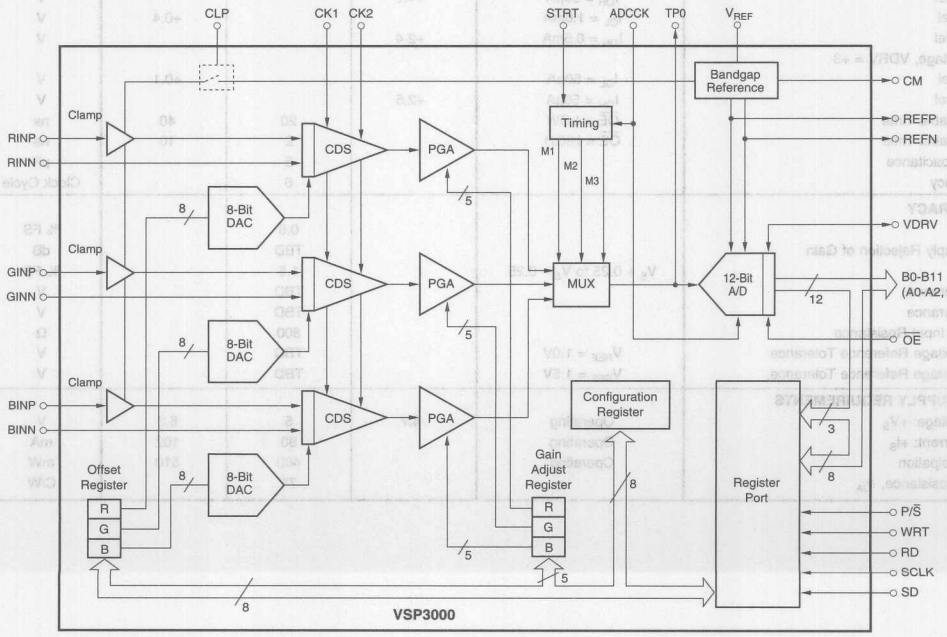
- INTEGTRATED TRIPLE-CORRELATED DOUBLE SAMPLER
- 3-CHANNEL, 6MHz COLOR MODE
- 0dB TO +13dB ANALOG PROGRAMMABLE GAIN AMPLIFIER
- INTERNAL VOLTAGE REFERENCE
- GUARANTEED NO MISSING CODES
- +3V/+5V DIGITAL I/O COMPATIBILITY
- LOW POWER: 400mW (typ)
- 48-LEAD LQFP SURFACE-MOUNT PACKAGE

## DESCRIPTION

The VSP3000 is a complete CCD/CIS image processor which operates from a single +5V supply. This complete image processor includes three Correlated Double Samplers (CDS) and Programmable Gain Amplifiers (PGA) to process CCD signal(s).

These three channel inputs also allow Contact Image Sensor (CIS) input(s).

The VSP3000 can be operated from 0°C to +85°C and is available in a 48-pin LQFP package.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

## SPECIFICATIONS—PRELIMINARY

At $T_A$ = full specified temperature range, $V_S$ = +5V, $f_{ADCCK}$ = 6MHz, $f_{CK1}$ = 2MHz, $f_{CK2}$ = 2MHz, and PGA gain = 1, unless otherwise specified.

| PARAMETER | CONDITIONS | VSP3000Y | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **RESOLUTION** | | | 12 | | Bits |
| **SPECIFIED TEMPERATURE RANGE** | | | 0 to +85 | | °C |
| **CONVERSION CHARACTERISTICS** | | | | | |
| 3-Channel CDS Mode | | | 6 | 10 | Msps |
| 3-Channel CIS Mode | | | 6 | 10 | Msps |
| **ANALOG INPUTS** | | | | | |
| Full-Scale Input Range | | 0.5 | | 3.5 | Vp-p |
| Input Capacitance | | | 10 | | pF |
| Input Limits | | GND – 0.4 | | $V_S$ – 0.3 | V |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Integral Non-Linearity (INL) | | | ±1 | ±2 | LSB |
| Differential Non-Linearity (DNL) | | | 0.3 | 0.75 | LSB |
| No Missing Codes | | | 12 | | Bits |
| Input-Referred Noise | | | 0.3 | | LSBs rms |
| **PSRR** | | | 0.04 | | % FSR |
| **DIGITAL INPUTS** | | | | | |
| Logic Family | | | TTL/HCT | | |
| Convert Command | Start Conversion | | Rising Edge of Convert Clock | | |
| High Level Input Current ($V_{IN}$ = $VD_{DD}$) | | | | 10 | µA |
| Low Level Input Current ($V_{IN}$ = 0V) | | | | 10 | µA |
| High Level Input Voltage | | 3.5 | | | V |
| Low Level Input Voltage | | | | 1 | V |
| Input Capacitance | | | 5 | | pF |
| **DIGITAL OUTPUTS** | | | | | |
| Logic Family | | | TTL/HCT | | |
| Convert Command | Start Conversion | | Straight Offset Binary | | |
| VDRV Supply Range | | +2.7 | | +5.3 | V |
| Output Voltage, VDRV = +5V | | | | | |
| Low Level | $I_{OL}$ = 50µA | | | +0.1 | V |
| High Level | $I_{OH}$ = 50µA | +4.6 | | | V |
| Low Level | $I_{OL}$ = 1.6mA | | | +0.4 | V |
| High Level | $I_{OH}$ = 0.5mA | +2.4 | | | V |
| Output Voltage, VDRV = +3 | | | | | |
| Low Level | $I_{OL}$ = 50µA | | | +0.1 | V |
| High Level | $I_{OH}$ = 50µA | +2.5 | | | V |
| 3-State Enable Time | $\overline{OE}$ = LOW | | 20 | 40 | ns |
| 3-State Enable Time | $\overline{OE}$ = HIGH | | 2 | 10 | ns |
| Output Capacitance | | | 5 | | pF |
| Data Latency | | | 6 | | Clock Cycle |
| **DC ACCURACY** | | | | | |
| Zero Error | | | 0.8 | | % FS |
| Power Supply Rejection of Gain | | | TBD | | dB |
| Gain Error | $V_S$ + 0.25 to $V_S$ – 0.25 | | 1.5 | | % FS |
| REFP Tolerance | | | TBD | | V |
| REFN Tolerance | | | TBD | | V |
| Reference Input Resistance | | | 800 | | Ω |
| Internal Voltage Reference Tolerance | $V_{REF}$ = 1.0V | | TBD | | V |
| Internal Voltage Reference Tolerance | $V_{REF}$ = 1.5V | | TBD | | V |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Supply Voltage: $+V_S$ | Operating | 4.7 | 5 | 5.3 | V |
| Supply Current: $+I_S$ | Operating | | 80 | 102 | mA |
| Power Dissipation | Operating | | 400 | 510 | mW |
| Thermal Resistance, $\theta_{JA}$ | | | 75 | | C/W |

| | |
|---|---|
| $+V_S$, VDRV | +6V |
| Analog Input | (–0.3V) to ($+V_S$ + 0.3V) |
| Logic Input | (–0.3V) to ($+V_S$ + 0.3V) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +150°C |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| VSP3000Y | 48-Lead LQFP | 340 | 0°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## DEMO BOARD ORDERING INFORMATION

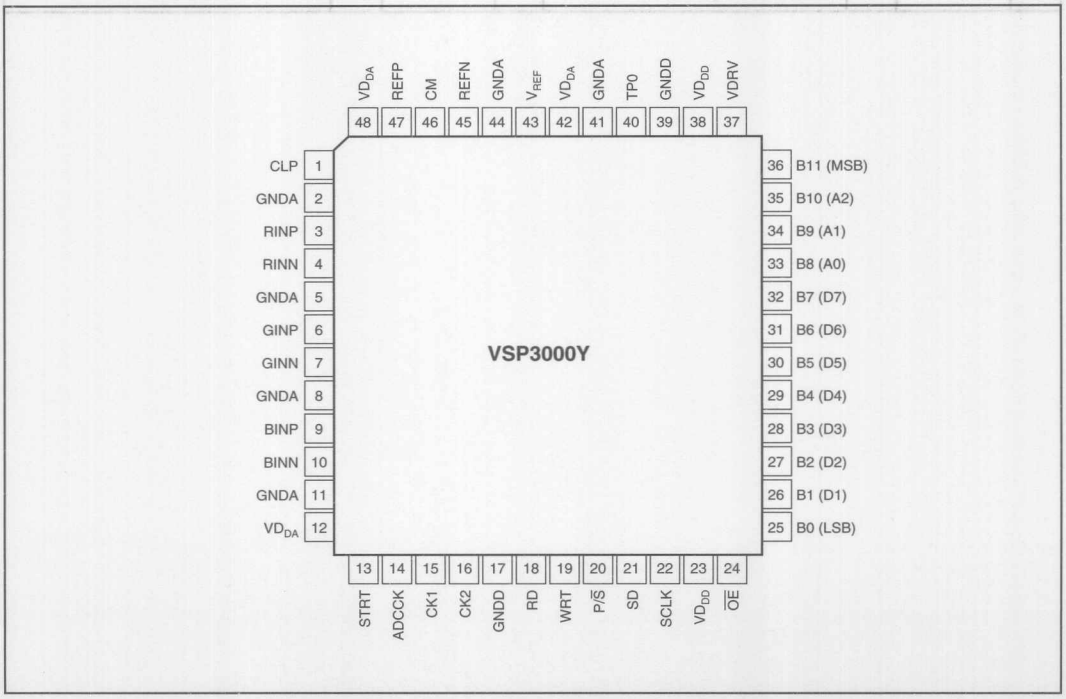
| PRODUCT | PACKAGE |
|---|---|
| VSP3000Y | DEM-VSP3000Y |

## DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN CONFIGURATION




The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN DESCRIPTIONS

| PIN | DESIGNATOR | TYPE | DESCRIPTION | PIN | DESIGNATOR | TYPE | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| 1 | CLP | DI | Clamp Enable | 25 | B0 (D0) LSB | DIO | A/D Output (Bit 0) and Register Data Port (Bit 0) |
| 2 | GNDA | P | Analog Ground | 26 | B1 (D1) | DIO | A/D Output (Bit 1) and Register Data Port (Bit 1) |
| 3 | RINP | AI | Red-Channel Analog Input | 27 | B2 (D2) | DIO | A/D Output (Bit 2) and Register Data Port (Bit 2) |
| 4 | RINN | AI | Red-Channel Reference Input | 28 | B3 (D3) | DIO | A/D Output (Bit 3) and Register Data Port (Bit 3) |
| 5 | GNDA | P | Analog Ground | 29 | B4 (D4) | DIO | A/D Output (Bit 4) and Register Data Port (Bit 4) |
| 6 | GINP | AI | Green-Channel Analog Input | 30 | B5 (D5) | DIO | A/D Output (Bit 5) and Register Data Port (Bit 5) |
| 7 | GINN | AI | Green-Channel Reference Input | 31 | B6 (D6) | DIO | A/D Output (Bit 6) and Register Data Port (Bit 6) |
| 8 | GNDA | P | Analog Ground | 32 | B7 (D7) | DIO | A/D Output (Bit 7) and Register Data Port (Bit 7) |
| 9 | BINP | AI | Blue-Channel Analog Input | 33 | B8 (A0) | DIO | A/D Output (Bit 8) and Register Address (Bit 0) |
| 10 | BINN | AI | Blue-Channel Reference Input | 34 | B9 (A1) | DIO | A/D Output (Bit 9) and Register Address (Bit 1) |
| 11 | GNDA | P | Analog Ground | 35 | B10 (A2) | DIO | A/D Output (Bit 10) and Register Address (Bit 2) |
| 12 | $VD_{DA}$ | P | Analog Power Supply, +5V | 36 | B11 MSB | DIO | A/D Output (Bit 11) |
| 13 | STRT | DI | Start Line Scanning | 37 | VDRV | P | Output Driver Voltage Supply |
| 14 | ADCCK | DI | A/D Converter Clock Input | 38 | $VD_{DD}$ | P | Digital Power Supply, +5V |
| 15 | CK1 | DI | Sample Reference Clock | 39 | GNDD | P | Digital Ground |
| 16 | CK2 | DI | Sample Data Clock | 40 | TP0 | AO | A/D Converter Input Monitor Pin |
| 17 | GNDD | P | Digital Ground | 41 | GNDA | P | Analog Ground |
| 18 | RD | DI | Read Signal for Registers | 42 | $VD_{DA}$ | P | Analog Power Supply, +5V |
| 19 | WRT | DI | Write Signal for Registers | 43 | VREF | AIO | Reference Input/Output |
| 20 | P/$\overline{S}$ | DI | Parallel/Serial Port Select. HIGH = Parallel, LOW = Serial | 44 | GNDA | P | Analog Ground |
| | | | | 45 | REFN | AO | Bottom Reference |
| 21 | SD | DI | Serial Data Input | 46 | CM | AO | Common-Mode Voltage |
| 22 | SCLK | DI | Serial Data Clock | 47 | REFP | AO | Top Reference |
| 23 | $VD_{DD}$ | P | Digital Power Supply, +5V | 48 | $VD_{DA}$ | P | Analog Power Supply, +5V |
| 24 | $\overline{OE}$ | DI | A/D Converter Output Enable | | | | |

# 3 Digital-to-Analog Converters

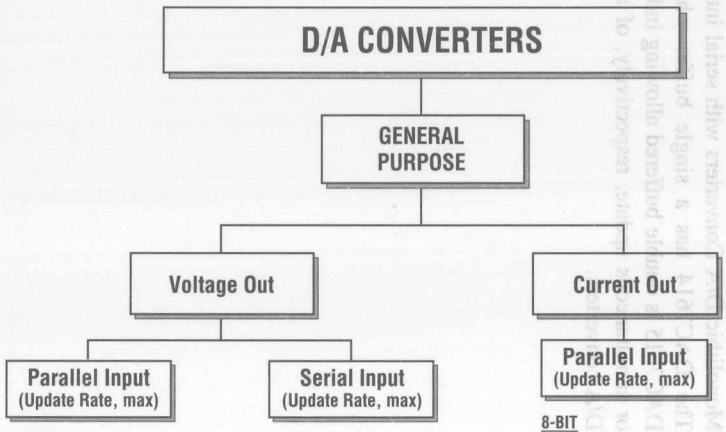
Burr-Brown offers a wide range of Digital-to-Analog (D/A) converters designed to meet critical requirements for industrial, audio and waveform-generation applications.

Industrial instrumentation D/As with 12-, 16-, and 18-bit resolutions are available in industry standard pinouts. There are also new smaller size, lower-power D/As specified over the extended industrial temperature range, –40°C to +85°C. Dual and Quad D/As are also available in the product line.

**DAC7624 and DAC7625** are new Quad, 12-Bit Monolithic D/A Converters with parallel interface. The DAC7624 resets to mid-scale ($800_H$). The DAC7625 resets to zero-scale ($000_H$).

**DAC7614 and DAC7615** are new Quad, 12-Bit Monolithic D/A Converters with serial interface. The DAC7614 has a single buffer while the DAC7615 is double buffered allowing individual or simultaneous update, respectively, of all four D/A converters.

# Digital-to-Analog Converters




**12-BIT**
DAC667 (250kHz)
DAC811 (250kHz)
DAC80 (250kHz)
DAC85 (250kHz)
DAC813 (166kHz)
DAC2813 (166kHz, Dual)
DAC4813 (166kHz, Quad)
DAC2815 (100kHz, Dual)
DAC4815 (100kHz, Quad)
**DAC7624 (100kHz, Quad MDAC)**
**DAC7625 (100kHz, Quad MDAC)**

**16-BIT**
DAC701 (125kHz)
DAC703 (125kHz)
DAC707 (125kHz)
DAC709 (125kHz)
DAC725 (125kHz)
DAC712 (100kHz)
DAC715 (100kHz)

**18-BIT**
DAC729 (125kHz)

**12-BIT**
DAC2814 (100kHz, MDAC, Dual)
DAC4814 (100kHz, MDAC, Quad)
***DAC7611 (100kHz, w/Reference)***
**DAC7614 (100kHz, Quad MDAC)**
**DAC7615 (100kHz, Quad MDAC)**

**16-BIT**
DAC56 (666kHz*)
DAC725 (125kHz)
DAC709 (125kHz)
DAC714 (100kHz)

**18-BIT**
DSP201 (500kHz)
DSP202 (500kHz, Dual)

**8-BIT**
DAC7528 (5MHz, MDAC)

**12-BIT**
DAC7800 (1.25MHz, MDAC)
DAC7801 (1.25MHz, MDAC)
DAC7802 (1.25MHz, MDAC)
DAC7541 (1MHz, MDAC)
DAC8043 (1MHz, MDAC)
DAC7545 (500kHz, MDAC)

**16-BIT**
DAC700 (1MHz)
DAC702 (1MHz)
DAC708 (1MHz)

* DENOTES TYPICAL
**BOLD DENOTES NEW PRODUCT**
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Some specifications have been estimated for comparisor purposes. Refer to data sheets for guaranteed specificati

## GENERAL PURP

| Product | Resolution (Bits) | Linearity Error (%FSR) | Settling Time (µs) | Output Range | Description |
|---|---|---|---|---|---|
| DAC56 | 16 | ±0.012 | 1.5* | ±3V | Serial Input, Flexible Bus Interface |
| DAC80 | 12 | ±0.012 | 0.3, 3* | ±1mA, –2mA; +5V, +10V, ±5V, ±10V | Industry Standard, General Purpose, Flexible Bus Interface |
| DAC667 | 12 | ±0.006 | 4 | ±2.5V, ±5V, ±10V, +5V, +10V | Industry Standard Pinout, Flexible Bus Interface |
| DAC700 | 16 | ±0.0015 | 1 | –2mA | General Purpose |
| DAC701 | 16 | ±0.0015 | 8 | +10V | General Purpose |
| DAC702 | 16 | ±0.0015 | 1 | ±1mA | General Purpose |
| DAC703 | 16 | ±0.0015 | 8 | ±10V | General Purpose |
| DAC707 | 16 | ±0.003 | 8 | ±10V | 16-Bit Parallel, Bus Interface |
| DAC708 | 16 | ±0.003 | 1 | ±1mA, –2mA | Serial/8-bit Parallel, Bus Interface |
| DAC709 | 16 | ±0.003 | 8 | ±5V, ±10V, +10V | Serial/8-bit Parallel, Bus Interface |
| DAC712 | 16 | ±0.003 | 12 | ±10V | 16-Bit Parallel, Bus Interface |
| DAC714 | 16 | ±0.003 | 10 | ±10V | Serial Interface, Bus Interface |
| DAC715 | 16 | ±0.003 | 10 | 0 to 10V | Parallel, Double Buffered |
| DAC729 | 18 | ±0.00075 | 5 | ±1mA, –2mA; +5V, +10V, ±5V, ±10V | Very High Resolution |
| DAC725 | 16 | ±0.003 | 8 | ±10V | Dual, Serial/8-bit Parallel, Bus Interface |
| DAC811 | 12 | ±0.006 | 4 | ±5V, ±10V, +10V | Flexible Bus Interface |
| DAC813 | 12 | ±0.006 | 4 | ±5V, ±10V, +10V | Small, Low Cost, Flexible Bus Interface |
| DAC1600 | 16 | ±0.003 | 8* | ±10V | Lowest Cost |
| DAC2813 | 12 | ±0.006 | 6 | ±10, 0 to 10 | Dual, 12-bit Port, Flexible Bus Interface |
| DAC2814 | 12 | ±0.012 | 10 | $+V_S$ –1.4V (max), $-V_S$ +1.4V (min) | Dual, Multiplying Serial Port, Flexible Bus Interface |
| DAC2815 | 12 | ±0.012 | 10 | $+V_S$ –1.4V (max), $-V_S$ +1.4V (min) | Dual Multiplying 8-bit Port, Flexible Bus Interface |
| DAC4813 | 12 | ±0.012 | 6 | ±10V | QUAD, 12-bit Port, Flexible Bus Interface |
| DAC4814 | 12 | ±0.012 | 10 | $+V_S$ –1.4V (max), $-V_S$ +1.4V (min) | QUAD, Multiplying Serial Port, Flexible Bus Interface |
| DAC4815 | 12 | ±0.012 | 10 | $+V_S$ –1.4V (max), $-V_S$ +1.4V (min) | QUAD, Multiplying 8-bit Port, Flexible Bus Interface |

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**BOLD DENOTES NEW PRODUCT**
***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPM***

Some specifications have been estimated for comparis
purposes. Refer to data sheets for guaranteed specific

## GENERAL PURPOSE (CONT)

| Product | Resolution (Bits) | Linearity Error (%FSR) | Settling Time (µs) | Output Range | Description |
|---|---|---|---|---|---|
| ***DAC7611*** | ***12*** | ***±0.012*** | ***10*** | ***0 to 4.096V*** | ***Serial, w/Reference, 8-pin Package*** |
| **DAC7614** | **12** | **±0.012** | **10** | **±2.5V** | **Quad, Multiplying Serial Port, Bipolar** |
| **DAC7615** | **12** | **±0.012** | **10** | **±2.5V** | **Quad, Multiplying Serial Port, Unipolar** |
| **DAC7624** | **12** | **±0.012** | **10** | **±2.5V** | **Quad, Multiplying Parallel Port, Bipolar** |
| **DAC7625** | **12** | **±0.012** | **10** | **±2.5V** | **Quad, Multiplying Parallel Port, Unipolar** |
| DAC7528 | 8 | ±0.012 | 0.18 | 0 to 1mA | Dual Multiplying DAC, Flexible Bus Interface |
| DAC7541A | 12 | ±0.012 | 1 | 0 to 1mA | Industry Standard, Bus Interface |
| DAC7545 | 12 | ±0.012 | 2 | 0 to 1mA | Industry Standard w/Latch, Bus Interface |
| DAC7800 | 12 | ±0.012 | 0.8 | 0 to 1mA | Octal, Serial Interface, with Bus Interface |
| DAC7801 | 12 | ±0.012 | 0.8 | 0 to 1mA | 8-bit Port Interface, with Bus Interface |
| DAC7802 | 12 | ±0.012 | 0.8 | 0 to 1mA | 12-bit Port Interface, with Bus Interface |
| DAC8043 | 12 | ±0.012 | 0.25* | 0 to 1mA | Single w/Bus, with Bus Interface |

## DIGITAL SIGNAL PROCESSING

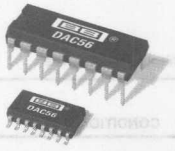
| Product | Resolution (Bits) | Linearity Error (%FSR) | Settling Time (µs) | Output Range (V) | Comments |
|---|---|---|---|---|---|
| DSP201 | 18 | ±0.006 | — | ±3 | DSP-Compatible Digital Interface, Single |
| DSP202 | 18 | ±0.006 | — | ±3 | DSP-Compatible Digital Interface, Dual |

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Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

For Immediate Assistance, Contact Your Local Salesperson

BURR-BROWN®



# DAC56

www.burr-brown.com/databook/DAC56.html

# Monolithic 16-Bit Resolution DIGITAL-TO-ANALOG CONVERTER



## FEATURES

- COMPLETE D/A CONVERTER:
  Internal Voltage Reference
  ±3V Output Operational Amplifier
  Pinout Allows $I_{OUT}$ (±1.0mA) Option
  No external components required
- 0.012% LINEARITY ERROR MAX
- 12-BIT MONOTONICITY GUARANTEED OVER 0°C TO +70°C
- ±5V TO ±12V POWER SUPPLY
- SETTLING TIME: $V_{OUT}$ = 1.5µs; $I_{OUT}$ = 350ns
- SERIAL DATA INPUT: Binary Two's Complement
- 16-PIN PLASTIC DIP AND SOIC

## APPLICATIONS

- PROCESS CONTROL
- ATE PIN ELECTRONICS LEVEL SETTING
- CLOSED-LOOP SERVO-CONTROL
- AUTO-CALIBRATION CIRCUIT FOR A/D BOARDS
- UP-GRADE REPLACEMENT FOR MULTIPLYING D/A
- X-Y PLOTTER
- DSP PROCESSOR BOARDS

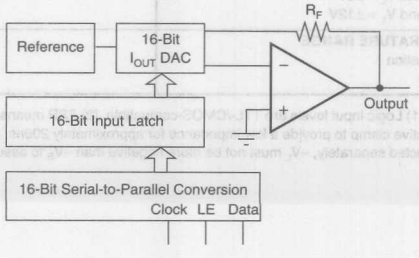
## DESCRIPTION

The DAC56 is a complete 16-bit monolithic D/A converter. Completely self-contained with a stable, low noise, internal zener voltage reference; high-speed current switches; a resistor ladder network; and a low noise output operational amplifier all on a single monolithic chip. The DAC56 operates over a wide power supply range from ±5V to ±12V.

Differential linearity error (DLE) is guaranteed to meet specifications without external adjustment. However, provisions for an externally adjustable circuit controlling the MSB error, the differential linearity error at bipolar zero, makes the DLE at BPZ essentially zero and provides for high system performance. The I/V amplifier stage includes an output current limiting circuit to protect both amplifier and load from excessive current. This assures the user of high system reliability.

A high-speed interface is capable of clocking in data at a rate of 10MHz max, and its interface logic contains a serial data clock (input), serial data (input) and latch-enable (input). Serial data is clocked MSB first into a 16-bit register and then latched into a 16-bit parallel register.

The DAC56 is packaged in a 16-pin plastic DIP and 16-pin SOIC.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
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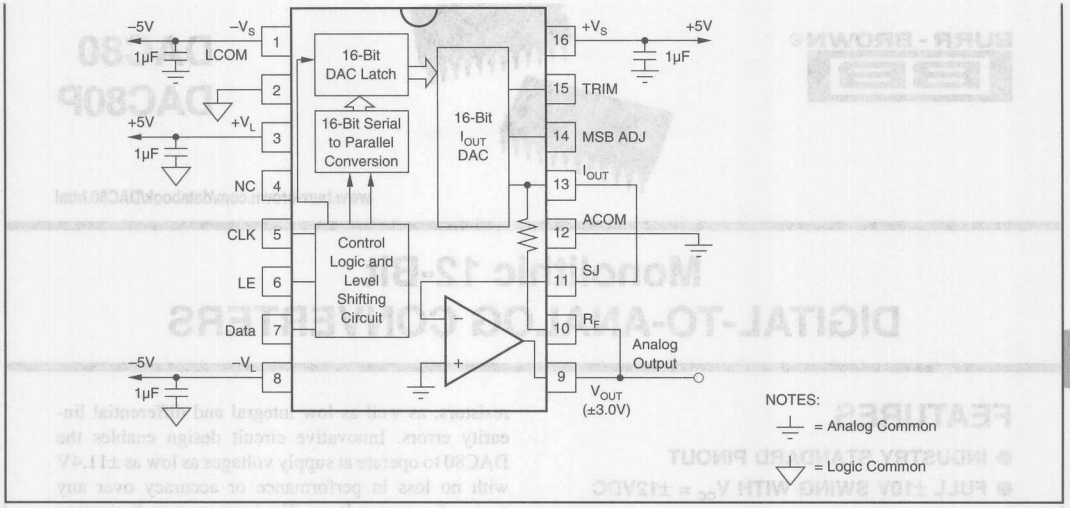
# SPECIFICATIONS

## ELECTRICAL

All specifications at +25°C, and power supply voltage of ±5V, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC56 MIN | DAC56 TYP | DAC56 MAX | UNITS |
|---|---|---|---|---|---|
| **DIGITAL INPUT** | | | | | |
| Resolution | | | 16 | | Bits |
| Digital Input Level: (1) $V_{IH}$ | | +2.4 | | $+V_L$ | V |
| $V_{IL}$ | | 0 | | +0.8 | V |
| $I_{IH} \bullet V_I = +2.7V$ | | | | +1 | µA |
| $I_{IL} \bullet V_I = +0.4V$ | | | | –50 | µA |
| Input Clock Frequency | | 10 | | | MHz |
| **ACCURACY** | | | | | |
| Integral Linearity Error | | | | ±0.012 | % of FSR(3) |
| Differential Linearity Error | | | | ±0.024 | % of FSR |
| Gain Error | | | | ±1.5 | % of FSR |
| Bipolar Zero Error | | | | ±0.5 | % of FSR |
| Monotonicity | 0°C to +70°C | | | 12 | Bits |
| **TEMPERATURE DRIFT** | 0°C to +70°C | | | | |
| Gain Drift | | | ±60 | | ppm of FSR/°C |
| Bipolar Zero Drift | | | ±20 | | ppm of FSR/°C |
| Linearity Drift | | | | ±0.012 | % of FSR |
| Differential Linearity Drift | | | | ±0.024 | % of FSR |
| **POWER SUPPLY SENSITIVITY** | $\pm V_S = \pm V_L = \pm 5VDC$ | | | | |
| Gain | | | ±0.0045 | | % of FSR/%V |
| Bipolar Zero | | | ±0.0015 | | % of FSR/%V |
| **SETTLING TIME** | to ±0.006% of FSR | | | | |
| Voltage Output | | | | | |
| 6V Step | | | 1.5 | | µs |
| 1LSB | | | 1 | | µs |
| Current Output | | | | | |
| 1mA Step | 10 to 100Ω Load | | 350 | | ns |
| | 1kΩ Load(3) | | 350 | | ns |
| Slew Rate | | | 12 | | V/µs |
| **ANALOG OUTPUT** | | | | | |
| Voltage Output Configuration | | | | | |
| Bipolar Range | | ±2.66 | ±3.0 | ±3.34 | V |
| Output Current | | ±8 | | | mA |
| Output Impedance | | | 0.1 | | Ω |
| Short Circuit Duration | | | Indefinite to Common | | |
| Current Output Configuration | | | | | |
| Bipolar Range | | | ±1 | | mA |
| Output Impedance | | | 1.2 | | kΩ |
| **WARMUP TIME** | | 1 | | | min |
| **POWER SUPPLY REQUIREMENTS(4)** | | | | | |
| Supply Voltage | | | | | |
| $+V_S$ and $+V_L$ | | +4.75 | +5.00 | +13.2 | V |
| $-V_S$ and $-V_L$ | | –4.75 | –5.00 | –13.2 | V |
| Supply Drain (No Load) | | | | | |
| +V ($+V_S$ and $+V_L$ = +5V) | | | +10 | +17 | mA |
| –V ($-V_S$ and $-V_L$ = –5V) | | | –25 | –35 | mA |
| +V ($+V_S$ and $+V_L$ = +12V) | | | +12 | | mA |
| –V ($-V_S$ and $-V_L$ = –12V) | | | –27 | | mA |
| Power Dissipation | | | | | |
| $V_S$ and $V_L$ = ±5V | | | 175 | 260 | mW |
| $V_S$ and $V_L$ = ±12V | | | 468 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | 0 | | 70 | °C |
| Storage | | –60 | | 100 | °C |

NOTES: (1) Logic input levels are TTL-/CMOS-compatible. (2) FSR means full-scale range and is equivalent to 6V (±3V) for DAC56 in the $V_{OUT}$ mode. (3) Measured with an active clamp to provide a low impedance for approximately 200ns. (4) All specifications assume $+V_S$ connected to $+V_L$ and $-V_S$ connected to $-V_L$. If supplies are connected separately, $-V_L$ must not be more negative than $-V_S$ to assure proper operation. No similar restriction applies to the value of $+V_L$ with respect to $+V_S$.




## PIN ASSIGNMENTS

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | $-V_S$ | Analog Negative Supply |
| 2 | LCOM | Logic Common |
| 3 | $+V_L$ | Logic Positive Supply |
| 4 | NC | No Connection |
| 5 | CLK | Clock Input |
| 6 | LE | Latch Enable Input |
| 7 | DATA | Serial Data Input |
| 8 | $-V_L$ | Logic Negative Supply |
| 9 | $V_{OUT}$ | Voltage Output |
| 10 | $R_F$ | Feedback Resistor |
| 11 | SJ | Summing Junction |
| 12 | ACOM | Analog Common |
| 13 | $I_{OUT}$ | Current Output |
| 14 | MSB ADJ | MSB Adjustment Terminal |
| 15 | TRIM | MSB Trim-pot Terminal |
| 16 | $+V_S$ | Analog Positive Supply |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| DAC56P | 16-Pin Plastic DIP | 180 |
| DAC56U | 16-Pin SOIC | 211 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

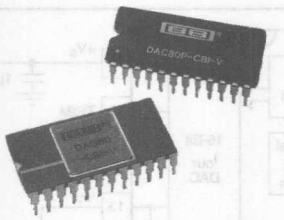
| | |
|---|---|
| DC Supply Voltage | ±15VDC |
| Input Logic Voltage | –1V to $+V_S/+V_L$ |
| Power Dissipation | 850mW |
| Operating Temperature | –25°C to +70°C |
| Storage Temperature | –80°C to +100°C |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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# DAC80
# DAC80P

www.burr-brown.com/databook/DAC80.html

# Monolithic 12-Bit DIGITAL-TO-ANALOG CONVERTERS

## FEATURES

- INDUSTRY STANDARD PINOUT
- FULL ±10V SWING WITH $V_{CC}$ = ±12VDC
- DIGITAL INPUTS ARE TTL- AND CMOS-COMPATIBLE
- GUARANTEED SPECIFICATIONS WITH ±12V AND ±15V SUPPLIES
- ±1/2LSB MAXIMUM NONLINEARITY: 0°C to +70°C
- SETTLING TIME: 4µs max to ±0.01% of Full Scale
- GUARANTEED MONOTONICITY: 0°C to +70°C
- TWO PACKAGE OPTIONS: Hermetic side-brazed ceramic and low-cost molded plastic

## DESCRIPTION

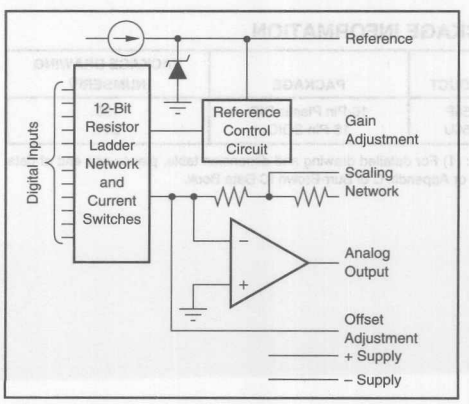
This monolithic digital-to-analog converter is pin-for-pin equivalent to the industry standard DAC80 first introduced by Burr-Brown. Its single-chip design includes the output amplifier and provides a highly stable reference capable of supplying up to 2.5mA to an external load without degradation of D/A performance.

This converter uses proven circuit techniques to provide accurate and reliable performance over temperature and power supply variations. The use of a buried zener diode as the basis for the internal reference contributes to the high stability and low noise of the device. Advanced methods of laser trimming result in precision output current and output amplifier feedback resistors, as well as low integral and differential linearity errors. Innovative circuit design enables the DAC80 to operate at supply voltages as low as ±11.4V with no loss in performance or accuracy over any range of output voltage. The lower power dissipation of this 118-mil by 121-mil chip results in higher reliability and greater long term stability.

Burr-Brown has further enhanced the reliability of the monolithic DAC80 by offering a hermetic, side-brazed, ceramic package. In addition, ease of use has been enhanced by eliminating the need for a +5V logic power supply.

For applications requiring both reliability and low cost, the DAC80P in a molded plastic package offers the same electrical performance over temperature as the ceramic model. The DAC80P is available with voltage output only.

For designs that require a wider temperature range, see Burr-Brown models DAC85H and DAC87H.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

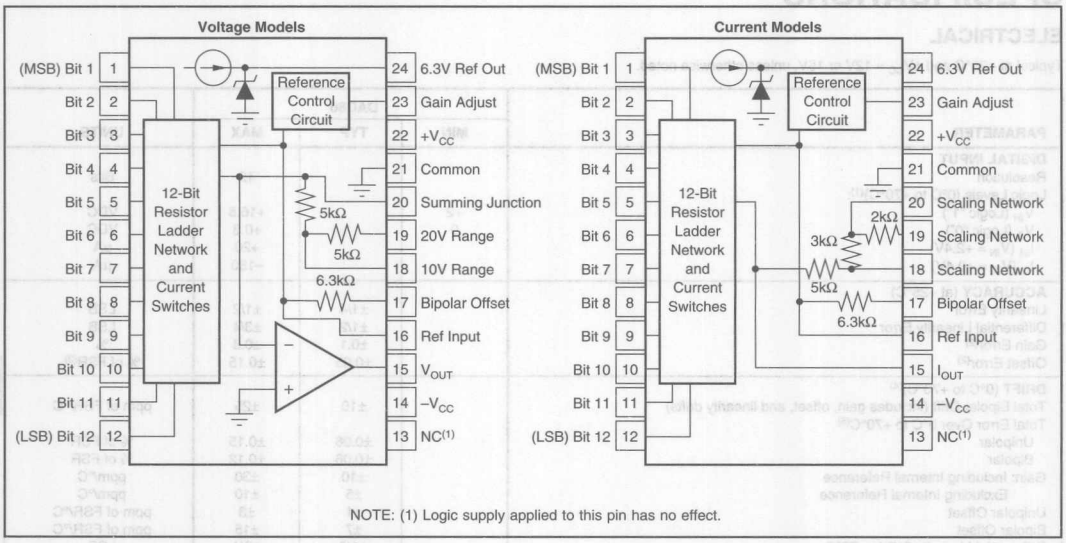
## ELECTRICAL

Typical at +25°C and $\pm V_{CC}$ = 12V or 15V, unless otherwise noted.

| PARAMETER | DAC80 MIN | DAC80 TYP | DAC80 MAX | UNITS |
|---|---|---|---|---|
| **DIGITAL INPUT** | | | | |
| Resolution | | | 12 | Bits |
| Logic Levels (0°C to +70°C)[1]: | | | | |
| $V_{IH}$ (Logic "1") | +2 | | +16.5 | VDC |
| $V_{IL}$ (Logic "0") | 0 | | +0.8 | VDC |
| $I_{IH}$ ($V_{IN}$ = +2.4V) | | | +20 | µA |
| $I_{IL}$ ($V_{IN}$ = +0.4V) | | | –180 | µA |
| **ACCURACY** (at +25°C) | | | | |
| Linearity Error | | ±1/4 | ±1/2 | LSB |
| Differential Linearity Error | | ±1/2 | ±3/4 | LSB |
| Gain Error[2] | | ±0.1 | ±0.3 | % |
| Offset Error[2] | | ±0.05 | ±0.15 | % of FSR[3] |
| **DRIFT** (0°C to +70°C)[4] | | | | |
| Total Bipolar Drift (includes gain, offset, and linearity drifts) | | ±10 | ±25 | ppm of FSR/°C |
| Total Error Over 0°C to +70°C[5] | | | | |
| Unipolar | | ±0.06 | ±0.15 | % of FSR |
| Bipolar | | ±0.06 | ±0.12 | % of FSR |
| Gain: Including Internal Reference | | ±10 | ±30 | ppm/°C |
| Excluding Internal Reference | | ±5 | ±10 | ppm/°C |
| Unipolar Offset | | ±1 | ±3 | ppm of FSR/°C |
| Bipolar Offset | | ±7 | ±15 | ppm of FSR/°C |
| Differential Linearity 0°C to +70°C | | ±1/2 | ±3/4 | LSB |
| Linearity Error 0°C to +70°C | | ±1/4 | ±1/2 | LSB |
| Monotonicity Guaranteed | 0 | | +70 | °C |
| **CONVERSION SPEED, $V_{OUT}$ Models** | | | | |
| Settling Time to ±0.01% of FSR | | | | |
| For FSR Change (2kΩ II 500pF Load) | | | | |
| with 10kΩ Feedback | | 3 | 4 | µs |
| with 5kΩ Feedback | | 2 | 3 | µs |
| For 1LSB Change | | 1 | | µs |
| Slew Rate | 10 | | | V/µs |
| **CONVERSION SPEED, $I_{OUT}$ Models** | | | | |
| Settling Time to ±0.01% of FSR | | | | |
| For FSR change: 10Ω to 100Ω Load | | 300 | | ns |
| 1kΩ Load | | 1 | | µs |
| **ANALOG OUTPUT, $V_{OUT}$ Models** | | | | |
| Ranges | | ±2.5, ±5, ±10, +5, +10 | | V |
| Output Current[6] | ±5 | | | mA |
| Output Impedance (DC) | | 0.05 | | Ω |
| Short Circuit to Common, Duration[7] | | Indefinite | | |
| **ANALOG OUTPUT, $I_{OUT}$ Models** | | | | |
| Ranges: Bipolar | ±0.96 | ±1.0 | ±1.04 | mA |
| Unipolar | –1.96 | –2.0 | –2.04 | mA |
| Output Impendance: Bipolar | 2.6 | 3.2 | 3.7 | kΩ |
| Unipolar | 4.6 | 6.6 | 8.6 | kΩ |
| Compliance | –2.5 | | +2.5 | V |
| **REFERENCE VOLTAGE OUTPUT** | +6.23 | +6.30 | +6.37 | V |
| External Current (constant load) | | | 2.5 | mA |
| Drift vs Temperature | | ±10 | ±20 | ppm/°C |
| Output Impedance | | 1 | | Ω |
| **POWER SUPPLY SENSITIVITY** | | | | |
| $V_{CC}$ = ±12VDC or ±15VDC | | ±0.002 | ±0.006 | % FSR/ % $V_{CC}$ |
| **POWER SUPPLY REQUIREMENTS** | | | | |
| $\pm V_{CC}$ | ±11.4 | | ±16.5 | VDC |
| Supply Drain (no load): $+V_{CC}$ | | 8 | 12 | mA |
| $-V_{CC}$ | | 15 | 20 | mA |
| Power Dissipation ($V_{CC}$ = ±15VDC) | | 345 | 480 | mW |
| **TEMPERATURE RANGE** | | | | |
| Specification | 0 | | +70 | °C |
| Operating | –25 | | +85 | °C |
| Storage: Plastic DIP | –60 | | +100 | °C |
| Ceramic DIP | –65 | | +150 | °C |

NOTES: (1) Refer to "Logic Input Compatibility" section. (2) Adjustable to zero with external trim potentiometer. (3) FSR means full scale range and is 20V for ±10V range, 10V for ±5V range for $V_{OUT}$ models; 2mA for $I_{OUT}$ models. (4) To maintain drift spec, internal feedback resistors must be used. (5) Includes the effects of gain, offset and linearity drift. Gain and offset errors externally adjusted to zero at +25°C. (6) For $\pm V_{CC}$ less than ±12VDC, limit output current load to ±2.5mA to maintain ±10V full scale output voltage swing. For output range of ±5V or less, the output current is ±5mA over entire $\pm V_{CC}$ range. (7) Short circuit current is 40mA, max.

## FUNCTIONAL DIAGRAM AND PIN ASSIGNMENTS




NOTE: (1) Logic supply applied to this pin has no effect.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_{CC}$ to Common | 0V to +18V |
| $-V_{CC}$ to Common | 0V to –18 |
| Digital Data Inputs to Common | –1V to +18V |
| Reference Output to Common | $\pm V_{CC}$ |
| Reference Input to Common | $\pm V_{CC}$ |
| Bipolar Offset to Common | $\pm V_{CC}$ |
| 10V Range R to Common | $\pm V_{CC}$ |
| 20V Range R to Common | $\pm V_{CC}$ |
| External Voltage to DAC Output | –5V to +5V |
| Lead Temperature (soldering, 10s) | +300°C |
| Max Junction Temperature | 165°C |
| Thermal Resistance, $\theta_{JA}$: Plastic DIP | 100°C/W |
| Ceramic DIP | 65°C/W |

**Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.**

## ORDERING INFORMATION

| PRODUCT | PACKAGE | OUTPUT |
|---|---|---|
| DAC80-CBI-I | Ceramic DIP | Current |
| DAC80Z-CBI-I | Ceramic DIP | Current |
| DAC80-CBI-V | Ceramic DIP | Voltage |
| DAC80Z-CBI-V | Ceramic DIP | Voltage |
| DAC80P-CBI-V | Plastic DIP | Voltage |

**BURN-IN SCREENING OPTION**

| PRODUCT | PACKAGE | BURN-IN TEMP. (160h)(1) |
|---|---|---|
| DAC80-CBI-V-BI | Ceramic DIP | +125°C |
| DAC80P-CBI-V-BI | Plastic DIP | +125°C |

NOTE: (1) Or equivalent combination. See text.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| DAC80P | 24-Pin Plastic DIP | 167 |
| DAC80 | 24-Pin Ceramic DIP | 125 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information table. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "–BI" to the base model number.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# DAC667

www.burr-brown.com/databook/DAC667.html

# Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER



## FEATURES

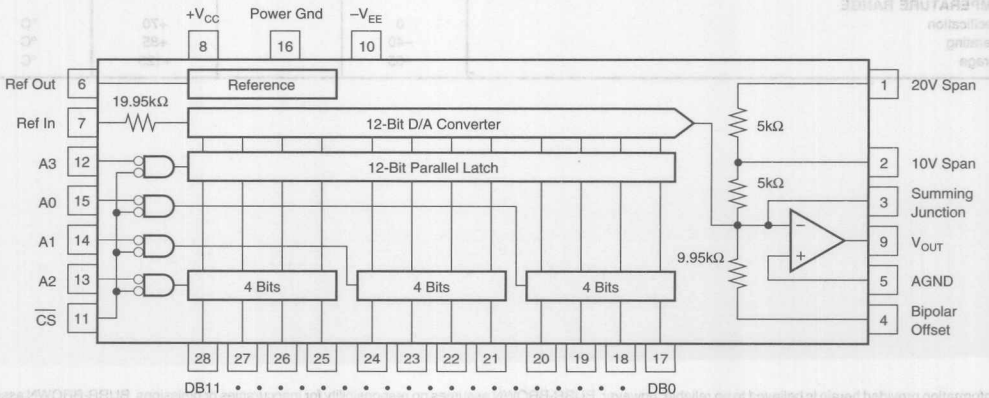
- ±3/4LSB MAX NONLINEARITY OVER TEMPERATURE
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- MICROCOMPUTER INTERFACE: Double-Buffered Latch
- VOLTAGE OUTPUT: ±10V, ±5V, +10V With ±12V to ±15V Supplies
- LOW POWER DISSIPATION: 345mW typ
- PIN COMPATIBLE WITH AD667

## DESCRIPTION

The DAC667 is a complete monolithic integrated circuit microprocessor-compatible 12-bit digital-to-analog converter. It includes a precision voltage reference, microcomputer interface logic, double-buffered latch, and a 12-bit D/A converter with a voltage output amplifier. Fast current switches and a laser-trimmed thin-film resistor network provide a highly accurate and fast D/A converter.

A double-buffered latch facilitates microcomputer interfacing to 4-, 8-, 12-, or 16-bit data buses. The input buffer latch holds the 12-bit data until it is transferred to an internal 12-bit D/A converter latch, giving precise timing control over an analog output change.

The DAC667 is specified to ±1/2LSB maximum linearity error at +25°C. The DAC667 is guaranteed monotonic over the specification temperature range. The DAC667 is available in 28-pin, 0.6" wide plastic DIP package.




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# SPECIFICATIONS

At $T_A$ = +25°C, ±12V. ±15V power supplies, unless otherwise noted.

| PARAMETER | DAC667JP MIN | DAC667JP TYP | DAC667JP MAX | UNITS |
|---|---|---|---|---|
| **DIGITAL INPUTS** | | | | |
| Resolution | | | 12 | Bits |
| Logic Levels (TTL Compatible, $T_{MIN}$ to $T_{MAX}$)[1] | | | | |
| $V_{IH}$ (Logic 1) | +2 | | +5.5 | V |
| $V_{IL}$ (Logic 0) | 0 | | +0.8 | V |
| $I_{IH}$ ($VI_H$ = 5.5V) | | 3 | 10 | µA |
| $I_{IL}$ ($V_{IL}$ = 0.8V) | | 1 | 5 | µA |
| **ACCURACY** | | | | |
| Linearity Error at +25°C | | ±1/4 | ±1/2 | LSB |
| $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | ±1/2 | ±3/4 | LSB |
| Differential Linearity Error at +25°C | | ±1/2 | ±3/4 | LSB |
| $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | Monotonicity Guaranteed | | LSB |
| Gain Error[2] | | ±0.1 | ±0.2 | % of FSR[3] |
| Unipolar Offset Error[2] | | ±1 | ±2 | LSB |
| Bipolar Zero[2] | | ±0.05 | ±0.1 | % of FSR |
| **DRIFT** | | | | |
| Differential Linearity | | ±2 | | ppm of FSR/°C |
| Gain (Full Scale), $T_A$ = +25°C to $T_{MIN}$ or $T_{MAX}$ | | ±5 | ±30 | ppm of FSR/°C |
| Unipolar Offset, $T_A$ = +25°C to $T_{MIN}$ or $T_{MAX}$ | | ±1 | ±3 | ppm of FSR/°C |
| Bipolar Zero, $T_A$ = +25°C to $T_{MIN}$ or $T_{MAX}$ | | ±5 | ±10 | ppm of FSR/°C |
| **CONVERSION SPEED** | | | | |
| Settling Time to ±0.01% of FSR for FSR Change (2kΩ II 500pF Load, $C_F$ = 0) | | | | |
| With 10kΩ Feedback | | 3 | 4 | µs |
| With 5kΩ Feedback | | 2 | 3 | µs |
| For LSB Change | | 2 | | µs |
| Slew Rate | 8 | | | V/µs |
| **ANALOG OUTPUT** | | | | |
| Ranges[4] | | ±2.5, ±5, ±10, +5, +10 | | V |
| Output Current | ±5 | | | mA |
| Output Impedance (DC) | | 0.05 | | Ω |
| Short Circuit Current | | | 40 | mA |
| **REFERENCE OUTPUT** | 9.9 | 10 | 10.1 | V |
| External Current | 0.1 | 1 | | mA |
| **POWER SUPPLY SENSITIVITY** | | | | |
| $V_{CC}$ = +11.4 to +16.5VDC | | 5 | 10 | ppm of FS/% |
| $V_{EE}$ = −11.4 to −16.5VDC | | 5 | 10 | ppm of FS/% |
| **POWER SUPPLY REQUIREMENTS** | | | | |
| Rated Voltages | | ±12, ±15 | | V |
| Range[4] | ±11.4 | | ±16.5 | V |
| Supply Current | | | | |
| +11.4 to +16.5VDC | | 14 | 17 | mA |
| −11.4 to −16.5VDC | | 9 | 12 | mA |
| **TEMPERATURE RANGE** | | | | |
| Specification | 0 | | +70 | °C |
| Operating | −40 | | +85 | °C |
| Storage | −65 | | +125 | °C |

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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $V_{CC}$ to Power Ground | 0V to +18V |
| $V_{EE}$ to Power Ground | 0V to –18V |
| Digital Inputs (Pins 11–15, 17–28) to Power Ground | –1V to +7V |
| Ref In to Reference Ground | ±12V |
| Bipolar Offset to Reference Ground | ±12V |
| 10V Span Resistor to Reference Ground | ±12V |
| 20V Span Resistor to Reference Ground | ±24V |
| Ref Out, $V_{OUT}$ (Pins 6, 9) | Indefinite Short to Power Ground, Momentary Short To $V_{CC}$ |
| Power Dissipation | 1000mW |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | TEMPERATURE RANGE | LINEARITY ERROR max at 25°C | GAIN TC, max (ppm/°C) | PACKAGE DRAWING NUMBER(1) |
|---|---|---|---|---|---|
| DAC667JP | 28-Pin Plastic DIP | 0°C to +70°C | ±1/2LSB | ±30 | 215 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## TIMING SPECIFICATIONS

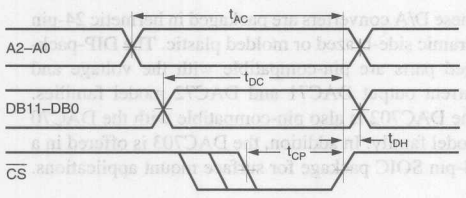
| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{DC}$ | Data Valid to End of $\overline{CS}$ | 50 | – | – | ns |
| $t_{AC}$ | Address Valid to End of $\overline{CS}$ | 100 | – | – | ns |
| $t_{CP}$ | $\overline{CS}$ Pulse Width | 100 | – | – | ns |
| $t_{DH}$ | Data Hold Time | 0 | – | – | ns |
| $t_{SETT}$ | Output Voltage Settling Time | – | 2 | 4 | µs |

All models, $T_A$ = +25°C, $V_{CC}$ = +12V or +15V, $V_{EE}$ = –12V or –15V.

## TIMING DIAGRAMS

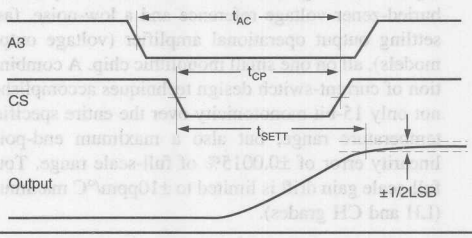
**Write Cycle #1**

Load first rank from Data Bus; A3 = 1.

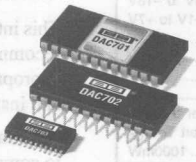



**Write Cycle #2**

Load second rank from first rank; A2, A1, A0 = 1.



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# DAC701
# DAC702
# DAC703

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# Monolithic 16-Bit DIGITAL-TO-ANALOG CONVERTERS

## FEATURES

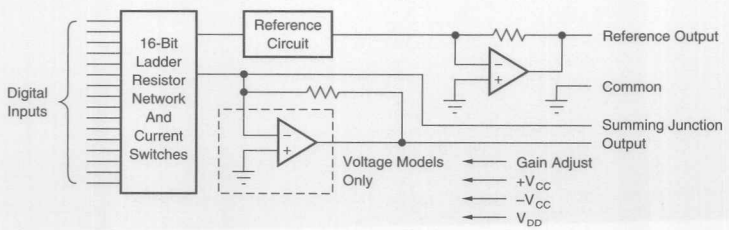
- $V_{OUT}$ AND $I_{OUT}$ MODELS
- HIGH ACCURACY:
  Linearity Error ±0.0015% of FSR max
  Differential Linearity Error ±0.003% of FSR max
- MONOTONIC (at 15 bits) OVER FULL SPECIFICATION TEMPERATURE RANGE
- PIN-COMPATIBLE WITH DAC70, DAC71, DAC72
- DUAL-IN-LINE PLASTIC AND HERMETIC CERAMIC AND SOIC

## DESCRIPTION

The DAC70X family comprise of complete 16-bit digital-to-analog converters that includes a precision buried-zener voltage reference and a low-noise, fast-settling output operational amplifier (voltage output models), all on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 15-bit monotonicity over the entire specified temperature range, but also a maximum end-point linearity error of ±0.0015% of full-scale range. Total full-scale gain drift is limited to ±10ppm/°C maximum (LH and CH grades).

Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C- and 54/74HC-compatible over the entire temperature range. Outputs of 0 to +10V, ±10V, 0 to –2mA, and ±1mA are available.

These D/A converters are packaged in hermetic 24-pin ceramic side-brazed or molded plastic. The DIP-packaged parts are pin-compatible with the voltage and current output DAC71 and DAC72 model families. The DAC702 is also pin-compatible with the DAC70 model family. In addition, the DAC703 is offered in a 24-pin SOIC package for surface mount applications.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At +25°C and rated power supplies, unless otherwise noted.

| PARAMETER | DAC702/703J | | | DAC701/702/703K | | | DAC701/702/703B, S | | | DAC701/702/703L, C | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT** | | | | | | | | | | | | | |
| **DIGITAL INPUT** | | | | | | | | | | | | | |
| Resolution | | | 16 | | | * | | | * | | | * | Bits |
| Digital Inputs [1] | | | | | | | | | | | | | |
| $V_{IH}$ | +2.4 | | +$V_{CC}$ | * | | * | * | | * | * | | * | V |
| $V_{IL}$ | –1.0 | | +0.8 | * | | * | * | | * | * | | * | V |
| $I_{IH}$, $V_I$ = +2.7V | | | +40 | | | * | | | * | | | * | µA |
| $I_{IL}$, $V_I$ = +0.4V | | –0.35 | –0.5 | | * | * | | * | * | | * | * | mA |
| **TRANSFER CHARACTERISTICS** | | | | | | | | | | | | | |
| **ACCURACY** [2] | | | | | | | | | | | | | |
| Linearity Error [4] | | ±0.0015 | ±0.006 | | * | ±0.003 | | * | * | | ±0.00075 | ±0.0015 | % of FSR [3] |
| Differential Linearity Error [4] | | ±0.003 | ±0.012 | | * | ±0.006 | | * | * | | ±0.0015 | ±0.003 | % of FSR |
| Differential Linearity Error at Bipolar Zero (DAC702/703) [4] | | | | | ±0.003 | ±0.006 | | ±0.0015 | ±0.003 | | * | * | % of FSR |
| Gain Error [5] | | ±0.07 | ±0.30 | | * | ±0.15 | | ±0.05 | ±0.10 | | * | * | % |
| Zero Error [5, 6] | | ±0.05 | ±0.10 | | * | * | | * | * | | * | * | % of FSR |
| Monotonicity Over Spec. Temp Range | 13 | | | 14 | | | * | | | 15 | | | Bits |
| **DRIFT** (over specification temperature range) | | | | | | | | | | | | | |
| Total Error Over Temperature Range (all models) [7] | | ±0.08 | | | * | ±0.15 | | ±0.05 | ±0.10 | | * | * | % of FSR |
| Total Full Scale Drift: | | | | | | | | | | | | | |
| DAC701 | | ±10 | | | * | ±30 | | ±8.5 | ±18 | | ±6 | ±13 | ppm of FSR/°C |
| DAC702/703 | | ±10 | | | * | ±25 | | ±7 | ±15 | | * | * | ppm of FSR/°C |
| Gain Drift (all models) | | ±10 | ±30 | | * | ±25 | | ±7 | ±15 | | ±5 | ±10 | ppm/°C |
| Zero Drift: | | | | | | | | | | | | | |
| DAC701 | | | | | ±2.5 | ±5 | | ±1.5 | ±3 | | * | * | ppm of FSR/°C |
| DAC702/703 | | ±5 | ±15 | | * | ±12 | | ±4 | ±10 | | ±2.5 | ±5 | ppm of FSR/°C |
| Differential Linearity Over Temp. [4] | | | ±0.012 | | | +0.009, –0.006 | | | * | | | +0.006, –0.003 | % of FSR |
| Linearity Error Over Temp. [4] | | | ±0.012 | | | ±0.006 | | | * | | | ±0.003 | % of FSR |
| **SETTLING TIME** (to ±0.003% of FSR) [8] | | | | | | | | | | | | | |
| DAC701/703 ($V_{OUT}$ Models) | | | | | | | | | | | | | |
| Full Scale Step, 2kΩ Load | | 4 | | | * | 8 | | * | * | | * | * | µs |
| 1LSB Step at Worst-Case Code [9] | | 2.5 | | | * | | | * | | | * | | µs |
| Slew Rate | | 10 | | | * | | | * | | | * | | V/µs |
| DAC702 ($I_{OUT}$ Models) | | | | | | | | | | | | | |
| Full Scale Step (2mA), 10 to 100Ω Load | | 350 | | | * | 1000 | | * | * | | * | * | ns |
| 1kΩ Load | | 1 | | | * | 3 | | * | * | | * | * | µs |
| **OUTPUT** | | | | | | | | | | | | | |
| **VOLTAGE OUTPUT MODELS** | | | | | | | | | | | | | |
| DAC701 (CSB Code) | | | | | 0 to +10 | | | * | | | | | V |
| DAC703 (COB Code) | | ±10 | | | * | | | * | | | * | | V |
| Output Current | ±5 | | | * | | | * | | | * | | | mA |
| Output Impedance | | 0.15 | | | * | | | * | | | * | | Ω |
| Short Circuit to Common Duration | | Indefinite | | | * | | | * | | | * | | |
| **CURRENT OUTPUT MODELS** | | | | | | | | | | | | | |
| DAC702 (COB Code) [10] | | ±1 | | | * | | | * | | | * | | mA |
| Output Impedance [10] | | 2.45 | | | * | | | * | | | * | | kΩ |
| Compliance Voltage | | ±2.5 | | | * | | | * | | | * | | V |

## SPECIFICATIONS (CONT)

At +25°C and rated power supplies, unless otherwise noted.

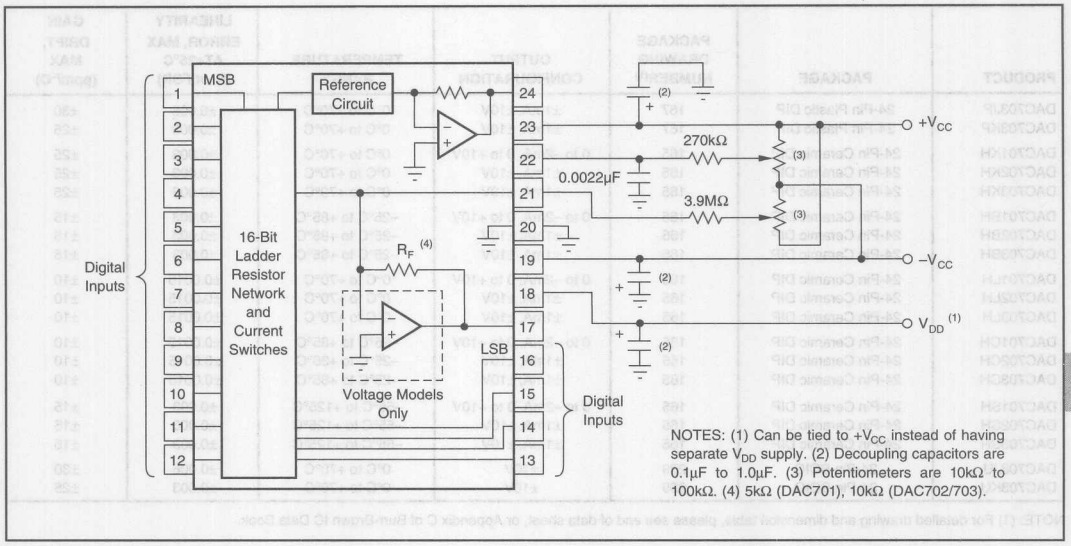
| PARAMETER | DAC702/703J | | | DAC701/702/703K | | | DAC701/702/703B, S | | | DAC701/702/703L, C | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **REFERENCE VOLTAGE** | | | | | | | | | | | | | |
| Voltage | | +6.3 | | +6.0 | +6.3 | +6.6 | +6.24 | +6.3 | +6.36 | * | * | * | V |
| Source Current Available for External Loads | | +2.5 | | +1.5 | * | | * | * | | * | * | | mA |
| Temperature Coefficient | | ±10 | | | * | ±25 | | * | ±15 | | * | * | ppm/°C |
| Short Circuit to Common Duration | | Indefinite | | | * | | | * | | | * | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | | | | | | |
| Voltage: $+V_{CC}$ | 13.5 | 15 | 16.5 | * | * | * | * | * | * | * | * | * | V |
| $-V_{CC}$ | 13.5 | 15 | 16.5 | * | * | * | * | * | * | * | * | * | V |
| $V_{DD}$ | +4.5 | +5 | +16.5 | * | * | * | * | * | * | * | * | * | V |
| Current (No Load): | | | | | | | | | | | | | |
| DAC702 | | | | | | | | | | | | | |
| ($I_{OUT}$ Models) | | | | | | | | | | | | | |
| $+V_{CC}$ | | +10 | +25 | | * | * | | * | * | | * | * | mA |
| $-V_{CC}$ | | −13 | −25 | | * | * | | * | * | | * | * | mA |
| $V_{DD}$ | | +4 | +8 | | * | * | | * | * | | * | * | mA |
| DAC701/703 | | | | | | | | | | | | | |
| ($V_{OUT}$ Models) | | | | | | | | | | | | | |
| $+V_{CC}$ | | +16 | +30 | | * | * | | * | * | | * | * | mA |
| $-V_{CC}$ | | −18 | −30 | | * | * | | * | * | | * | * | mA |
| $V_{DD}$ | | +4 | +8 | | * | * | | * | * | | * | * | mA |
| Power Dissipation: | | | | | | | | | | | | | |
| ($V_{DD}$ = +5.0V)(11) | | | | | | | | | | | | | |
| DAC702 | | 365 | | | * | 790 | | * | 630 | | * | * | mW |
| DAC701/703 | | 530 | | | * | 940 | | * | 780 | | * | * | mW |
| Power Supply Rejection: | | | | | | | | | | | | | |
| $+V_{CC}$ | | ±0.0015 | ±0.006 | | * | * | | * | ±0.003 | | * | * | % of FSR/%$V_{CC}$ |
| $-V_{CC}$ | | ±0.0015 | ±0.006 | | * | * | | * | ±0.003 | | * | * | % of FSR/%$V_{CC}$ |
| $V_{DD}$ | | ±0.0001 | ±0.001 | | * | * | | * | * | | * | * | % of FSR/%$V_{DD}$ |
| **TEMPERATURE RANGE** | | | | | | | | | | | | | |
| Specification: | | | | | | | | | | | | | |
| B, C Grades | | | | | | | −25 | | +85 | * | | * | °C |
| S Grades | | | | | | | −55 | | +125 | | | | °C |
| J, K, L Grades | 0 | | +70 | * | | * | | | | 0 | | +70 | °C |
| Storage: Ceramic | | | | −60 | | +150 | * | | * | * | | * | °C |
| Plastic, SOIC | −60 | | +100 | * | | * | | | | | | | °C |

* Specification same as model to the left.

NOTES: (1) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC, and 54/74HTC compatible over the operating voltage range of $V_{DD}$ = +5V to +15V and over the specified temperature range. The input switching threshold remains at the TTL threshold of 1.4V over the supply range of $V_{DD}$ = +5V to +15V. As logic "0" and logic "1" inputs vary over 0V to +0.8V and +2.4V to +10V respectively, the change in the D/A converter output voltage will not exceed ±0.0015% of FSR for the LH and CH grades, ±0.003% of FSR for the BH grade and ±0.006% of FSR for the KG grade. (2) DAC702 (current-output models) is specified and tested with an external output operational amplifier connected using the internal feedback resistor in all parameters except settling time. (3) FSR means full-scale range and is 20V for the ±10V range (DAC703), 10V for the 0 to +10V range (DAC701). FSR is 2mA for the ±1mA range (DAC702). (4) ±0.0015% of full-scale range is equivalent to 1LSB in 15-bit resolution. ±0.003% of full-scale range is equivalent to 1LSB in 14-bit resolution. ±0.006% of full-scale range is equivalent to 1LSB in 13-bit resolution. (5) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the zero point. (6) Error at input code $FFFF_H$ for DAC701, $7FFF_H$ for DAC702 and DAC703. (7) With gain and zero errors adjusted to zero at +25°C. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) At the major carry, $7FFF_H$ to $8000_H$ and $8000_H$ to $7FFF_H$. (10) Tolerance on output impedance and output current is ±30%. (11) Power dissipation is an additional 40mW when $V_{DD}$ is operated at +15V.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## CONNECTION DIAGRAMS




NOTES: (1) Can be tied to +$V_{CC}$ instead of having separate $V_{DD}$ supply. (2) Decoupling capacitors are 0.1µF to 1.0µF. (3) Potentiometers are 10kΩ to 100kΩ. (4) 5kΩ (DAC701), 10kΩ (DAC702/703).

## PIN ASSIGNMENTS

| PIN # | ALL PACKAGES | |
|---|---|---|
| | DAC702 | DAC701/703 |
| 1 | Bit 1 (MSB) | Bit 1 (MSB) |
| 2 | Bit 2 | Bit 2 |
| 3 | Bit 3 | Bit 3 |
| 4 | Bit 4 | Bit 4 |
| 5 | Bit 5 | Bit 5 |
| 6 | Bit 6 | Bit 6 |
| 7 | Bit 7 | Bit 7 |
| 8 | Bit 8 | Bit 8 |
| 9 | Bit 9 | Bit 9 |
| 10 | Bit 10 | Bit 10 |
| 11 | Bit 11 | Bit 11 |
| 12 | Bit 12 | Bit 12 |
| 13 | Bit 13 | Bit 13 |
| 14 | Bit 14 | Bit 14 |
| 15 | Bit 15 | Bit 15 |
| 16 | Bit 16 (LSB) | Bit 16 (LSB) |
| 17 | $R_{FEEDBACK}$ | $V_{OUT}$ |
| 18 | $V_{DD}$ | $V_{DD}$ |
| 19 | –$V_{CC}$ | –$V_{CC}$ |
| 20 | Common | Common |
| 21 | $I_{OUT}$ | Summing Junction (Zero Adjust) |
| 22 | Gain Adjust | Gain Adjust |
| 23 | +$V_{CC}$ | +$V_{CC}$ |
| 24 | +6.3V Reference Output | +6.3V Reference Output |

## ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|---|
| +$V_{CC}$ to Common | 0V, +18V |
| –$V_{CC}$ to Common | 0V, –18V |
| $V_{DD}$ to Common | 0V, +18V |
| Digital Data Inputs to Common | –1V, +18V |
| Reference Out to Common | Indefinite Short to Common |
| External Voltage Applied to $R_F$ (DAC702) | ±18V |
| External Voltage Applied to D/A Output (DAC701/703) | –5V to +5V |
| $V_{OUT}$ (DAC701/703) | Indefinite Short to Common |
| Power Dissipation | 1W |
| Storage Temperature | –60°C to +150°C |
| Lead Temperature (soldering, 10s) | 300°C |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

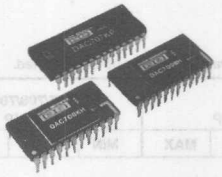
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | OUTPUT CONFIGURATION | TEMPERATURE RANGE | LINEARITY ERROR, MAX AT+25°C (% of FSR) | GAIN DRIFT, MAX (ppm/°C) |
|---|---|---|---|---|---|---|
| DAC703JP | 24-Pin Plastic DIP | 167 | ±1mA, ±10V | 0°C to +70°C | ±0.006 | ±30 |
| DAC703KP | 24-Pin Plastic DIP | 167 | ±1mA, ±10V | 0°C to +70°C | ±0.003 | ±25 |
| DAC701KH | 24-Pin Ceramic DIP | 165 | 0 to –2mA, 0 to +10V | 0°C to +70°C | ±0.003 | ±25 |
| DAC702KH | 24-Pin Ceramic DIP | 165 | ±1mA, ±10V | 0°C to +70°C | ±0.003 | ±25 |
| DAC703KH | 24-Pin Ceramic DIP | 165 | ±1mA, ±10V | 0°C to +70°C | ±0.003 | ±25 |
| DAC701BH | 24-Pin Ceramic DIP | 165 | 0 to –2mA, 0 to +10V | –25°C to +85°C | ±0.003 | ±15 |
| DAC702BH | 24-Pin Ceramic DIP | 165 | ±1mA, ±10V | –25°C to +85°C | ±0.003 | ±15 |
| DAC703BH | 24-Pin Ceramic DIP | 165 | ±1mA, ±10V | –25°C to +85°C | ±0.003 | ±15 |
| DAC701LH | 24-Pin Ceramic DIP | 165 | 0 to –2mA, 0 to +10V | 0°C to +70°C | ±0.0015 | ±10 |
| DAC702LH | 24-Pin Ceramic DIP | 165 | ±1mA, ±10V | 0°C to +70°C | ±0.0015 | ±10 |
| DAC703LH | 24-Pin Ceramic DIP | 165 | ±1mA, ±10V | 0°C to +70°C | ±0.0015 | ±10 |
| DAC701CH | 24-Pin Ceramic DIP | 165 | 0 to –2mA, 0 to +10V | –25°C to +85°C | ±0.0015 | ±10 |
| DAC702CH | 24-Pin Ceramic DIP | 165 | ±1mA, ±10V | –25°C to +85°C | ±0.0015 | ±10 |
| DAC703CH | 24-Pin Ceramic DIP | 165 | ±1mA, ±10V | –25°C to +85°C | ±0.0015 | ±10 |
| DAC701SH | 24-Pin Ceramic DIP | 165 | 0 to –2mA, 0 to +10V | –55°C to +125°C | ±0.003 | ±15 |
| DAC702SH | 24-Pin Ceramic DIP | 165 | ±1mA, ±10V | –55°C to +125°C | ±0.003 | ±15 |
| DAC703SH | 24-Pin Ceramic DIP | 165 | ±1mA, ±10V | –55°C to +125°C | ±0.003 | ±15 |
| DAC703JU | 24-Pin SOIC | 239 | ±10V | 0°C to +70°C | ±0.006 | ±30 |
| DAC703KU | 24-Pin SOIC | 239 | ±10V | 0°C to +70°C | ±0.003 | ±25 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR-BROWN®



# DAC707
# DAC708, 709

www.burr-brown.com/databook/DAC707.html

# Microprocessor-Compatible 16-BIT DIGITAL-TO-ANALOG CONVERTERS

## FEATURES

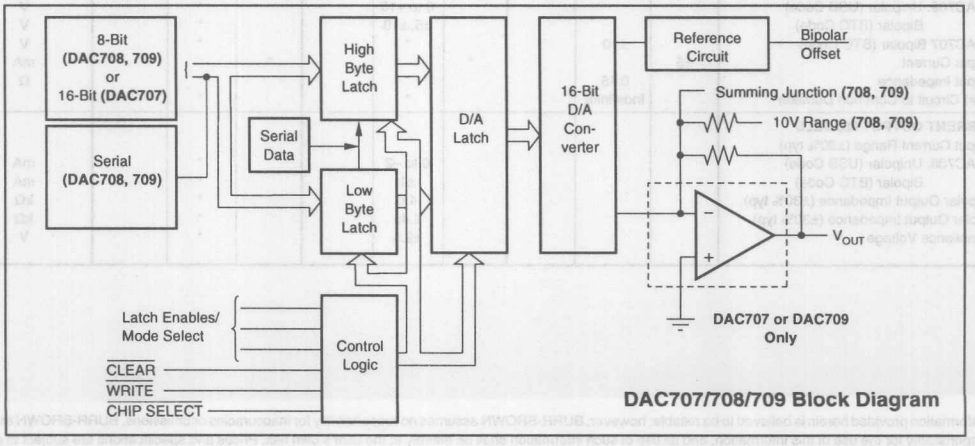
- TWO-CHIP CONSTRUCTION
- HIGH-SPEED 16-BIT PARALLEL, 8-BIT (BYTE) PARALLEL, AND SERIAL INPUT MODES
- DOUBLE-BUFFERED INPUT REGISTER CONFIGURATION
- $V_{OUT}$ AND $I_{OUT}$ MODELS
- HIGH ACCURACY: Linearity Error ±0.003% of FSR max Differential Linearity Error ±0.006% of FSR max
- MONOTONIC (TO 14 BITS) OVER SPECIFIED TEMPERATURE RANGE
- HERMETICALLY SEALED
- LOW COST PLASTIC VERSIONS AVAILABLE (DAC707JP/KP)

## DESCRIPTION

The DAC708 and DAC709 are 16-bit converters designed to interface to an 8-bit microprocessor bus. 16-bit data is loaded in two successive 8-bit bytes into parallel 8-bit latches before being transferred into the D/A latch. The DAC708 and DAC709 are current and voltage output models respectively and are in 24-pin hermetic DIPs. Input coding is Binary Two's Complement (bipolar) or Unipolar Straight Binary (unipolar, when an external logic inverter is used to invert the MSB). In addition, the DAC708/709 can be loaded serially (MSB first).

The DAC707 is designed to interface to a 16-bit bus. Data is written into a 16-bit latch and subsequently the D/A latch. The DAC707 has bipolar voltage output and input coding is Binary Two's Complement (BTC).

All models have Write and Clear control lines as well as input latch enable lines. In addition, DAC708 and DAC709 have Chip Select control lines. In the bipolar mode, the Clear input sets the D/A latch to give zero voltage or current output. They are all 14-bit accurate and are complete with reference, and for the DAC707, and DAC709, a voltage output amplifier. All models are available with an optional burn-in screening.




DAC707/708/709 Block Diagram

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $V_{CC}$ = ±15V, $V_{DD}$ = +5V, and after a 10-minute warm-up, unless otherwise noted.

| | DAC707JP | | | DAC707/708/709KH, DAC707KP | | | DAC707/708/709BH, SH | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **PRODUCT** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **INPUT** | | | | | | | | | | |
| **DIGITAL INPUT** | | | | | | | | | | |
| Resolution | | | 16 | | | * | | | * | Bits |
| Bipolar Input Code (all models) | | Binary Two's Complement | | | * | | | * | | |
| Unipolar Input Code[1] (DAC708/709 only) | | | | | Unipolar Straight Binary | | | * | | |
| Logic Levels[2]: $V_{IH}$ | +2.0 | | +5.5 | * | | * | * | | * | V |
| $V_{IL}$ | −1.0 | | +0.8 | * | | * | * | | * | V |
| $I_{IH}$ ($V_I$ = +2.7V) | | | 1 | | | * | | | * | µA |
| $I_{IL}$ ($V_I$ = +0.4V) | | | 1 | | | * | | | * | µA |
| **TRANSFER CHARACTERISTICS** | | | | | | | | | | |
| **ACCURACY[3]** | | | | | | | | | | |
| Linearity Error | | ±0.003 | ±0.006 | | ±0.0015 | ±0.003 | | * | * | % of FSR[4] |
| Differential Linearity Error[5] | | ±0.0045 | ±0.012 | | ±0.003 | ±0.006 | | * | * | % of FSR |
| at Bipolar Zero[5, 6] | | | | | ±0.003 | ±0.006 | | ±0.0015 | ±0.003 | % of FSR |
| Gain Error[7] | | ±0.07 | ±0.30 | | * | ±0.15 | | ±0.05 | ±0.10 | % |
| Zero Error[7] | | ±0.05 | ±0.1 | | * | * | | * | * | % of FSR |
| Monotonicity Over Spec Temp Range | 13 | | | 14 | | | 14 | | | Bits |
| Power Supply Sensitivity: $+V_{CC}$, $-V_{CC}$ | | ±0.0015 | ±0.006 | | * | * | | * | ±0.003 | % of FSR/%$V_{CC}$ |
| $V_{DD}$ | | ±0.0001 | ±0.001 | | * | * | | * | * | % of FSR/%$V_{DD}$ |
| **DRIFT** (Over Spec Temp Range[3]) | | | | | | | | | | |
| Total Error Over Temp Range[8] | | ±0.08 | | | * | ±0.15 | | * | ±0.10 | % of FSR |
| Total Full Scale Drift | | ±10 | | | * | ±25 | | * | ±15 | ppm of FSR/°C |
| Gain Drift | | ±10 | ±30 | | * | ±25 | | ±7 | ±15 | ppm/°C |
| Zero Drift: Unipolar (DAC708/709 only) | | | | | ±2.5 | ±5 | | ±1.5 | ±3 | ppm of FSR/°C |
| Bipolar (all models) | | ±5 | ±15 | | * | ±12 | | ±4 | ±10 | ppm of FSR/°C |
| Differential Linearity Over Temp[5] | | | ±0.012 | | | +0.009, −0.006 | | | * | % of FSR |
| Linearity Error Over Temp[5] | | | ±0.012 | | | ±0.006 | | | * | % of FSR |
| **SETTLING TIME** (to ±0.003% of FSR)[9] | | | | | | | | | | |
| Voltage Output Models | | | | | | | | | | |
| Full Scale Step (2kΩ load) | | 4 | | | * | 8 | | * | 8 | µs |
| 1LSB Step at Worst Case Code[10] | | 2.5 | | | * | 4 | | * | 4 | µs |
| Slew Rate | | 10 | | | * | | | * | | V/µs |
| Current Output Models | | | | | | | | | | |
| Full Scale Step (2mA): 10 to 100Ω Load | | | | | 350 | | | * | | ns |
| 1kΩ Load | | | | | 1 | | | * | | µs |
| **OUTPUT** | | | | | | | | | | |
| **VOLTAGE OUTPUT MODELS** | | | | | | | | | | |
| Output Voltage Range | | | | | | | | | | |
| DAC709: Unipolar (USB Code) | | | | | 0 to +10 | | | * | | V |
| Bipolar (BTC Code) | | | | | ±5, ±10 | | | * | | V |
| DAC707 Bipolar (BTC Code) | | ±10 | | | * | | | * | | V |
| Output Current | ±5 | | | * | | | * | | | mA |
| Output Impedance | | 0.15 | | | * | | | * | | Ω |
| Short Circuit to Common Duration | | Indefinite | | | * | | | * | | |
| **CURRENT OUTPUT MODELS** | | | | | | | | | | |
| Output Current Range (±30% typ) | | | | | | | | | | |
| DAC708: Unipolar (USB Code) | | | | | 0 to −2 | | | * | | mA |
| Bipolar (BTC Code) | | | | | ±1 | | | * | | mA |
| Unipolar Output Impedance (±30% typ) | | | | | 4.0 | | | * | | kΩ |
| Bipolar Output Impedance (±30% typ) | | | | | 2.45 | | | * | | kΩ |
| Compliance Voltage | | | | | ±2.5 | | | * | | V |

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## ELECTRICAL (CONT)

At $T_A$ = +25°C, $V_{CC}$ = ±15V, $V_{DD}$ = +5V, and after a 10-minute warm-up, unless otherwise noted.

| PRODUCT | DAC707JP | | | DAC707/708/709KH, DAC707KP | | | DAC707/708/709BH, SH | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | | | |
| Voltage (all models): $+V_{CC}$ | +13.5 | +15 | +16.5 | * | * | * | * | * | * | V |
| $-V_{CC}$ | −13.5 | −15 | −16.5 | * | * | * | * | * | * | V |
| $V_{DD}$ | +4.5 | +5 | +5.5 | * | * | * | * | * | * | V |
| Current (No Load, +15V Supplies) | | | | | | | | | | |
| Current Output Models: $+V_{CC}$ | | | | | +10 | +25 | | * | * | mA |
| $-V_{CC}$ | | | | | −13 | −25 | | * | * | mA |
| $V_{DD}$ | | | | | +5 | +10 | | * | * | mA |
| Voltage Output Models: $+V_{CC}$ | | +16 | +30 | | * | * | | * | * | mA |
| $-V_{CC}$ | | −18 | −30 | | * | * | | * | * | mA |
| $V_{DD}$ | | +5 | +10 | | * | * | | * | * | mA |
| Power Dissipation (±15V supplies) | | | | | | | | | | |
| Current Output Models | | | | | 370 | 800 | | * | * | mW |
| Voltage Output Models | | 535 | | | * | 950 | | * | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | | | |
| Specification: BH Grades | | | | | | | −25 | | +85 | °C |
| JP, KP, KH Grades | 0 | | +70 | * | | * | | | | °C |
| SH Grades | | | | | | | −55 | | +125 | °C |
| Storage: Ceramic | | | | −65 | | +150 | −65 | | +150 | °C |
| Plastic | −60 | | +100 | * | | * | | | | °C |

*Specification same as for models in column to the left.

NOTES: (1) MSB must be inverted externally prior to DAC708/709 input. (2) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC and 54/74HTC compatible over the specified temperature range. (3) DAC708 (current-output models) are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all tests. (4) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (5) ±0.0015% of Full Scale Range is equal to 1 LSB in 16-bit resolution, ±0.003% of Full Scale Range is equal to 1 LSB in 15-bit resolution. ±0.006% of Full Scale Range is equal to 1 LSB in 14-bit resolution. (6) Error at input code $0000_H$. (For unipolar connection on DAC708/709, the MSB must be inverted externally prior to D/A input.) (7) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point. (8) With gain and zero errors adjusted to zero at +25°C. (9) Maximum represents the 3σ limit. Not 100% tested for this parameter. (10) The bipolar worst-case code change is $FFFF_H$ to $0000_H$ and $0000_H$ to $FFFF_H$. For unipolar (DAC708/709 only) it is $7FFF_H$ to $8000_H$ and $8000_H$ to $7FFF_H$.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| DAC707JP | 28-Pin Plastic DBL Wide DIP | 215 |
| DAC707KP | 28-Pin Plastic DBL Wide DIP | 215 |
| DAC707BH | 28LD Side Brazed Hermetic Dip | 149 |
| DAC707KH | 28LD Side Brazed Hermetic DIP | 149 |
| DAC707SH | 28LD Side Brazed Hermetic DIP | 149 |
| DAC708BH | 24LD Side Brazed Hermetic DIP | 165 |
| DAC708KH | 24LD Side Brazed Hermetic DIP | 165 |
| DAC708SH | 24LD Side Brazed Hermetic DIP | 165 |
| DAC709BH | 24LD Side Brazed Hermetic DIP | 165 |
| DAC709KH | 24LD Side Brazed Hermetic DIP | 165 |
| DAC709SH | 24LD Side Brazed Hermetic DIP | 165 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $V_{DD}$ to COMMON | 0V, +15V |
| $+V_{CC}$ to COMMON | 0V, +18V |
| $-V_{CC}$ to COMMON | 0V, −18V |
| Digital Data Inputs to COMMON | −0.5V, $V_{DD}$ +0.5 |
| DC Current any input | ±10mA |
| Reference Out to COMMON | Indefinite Short to COMMON |
| $V_{OUT}$ (DAC707, DAC709) | Indefinite Short to COMMON |
| External Voltage Applied to $R_F$ (pin 13 or 14, DAC708) | ±18V |
| External Voltage Applied to D/A Output (pin 1, DAC707; pin 14, DAC709) | ±5V |
| Power Dissipation | 1000mW |
| Storage Temperature | −60°C to +150°C |
| Lead Temperature (soldering, 10s) | 300°C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

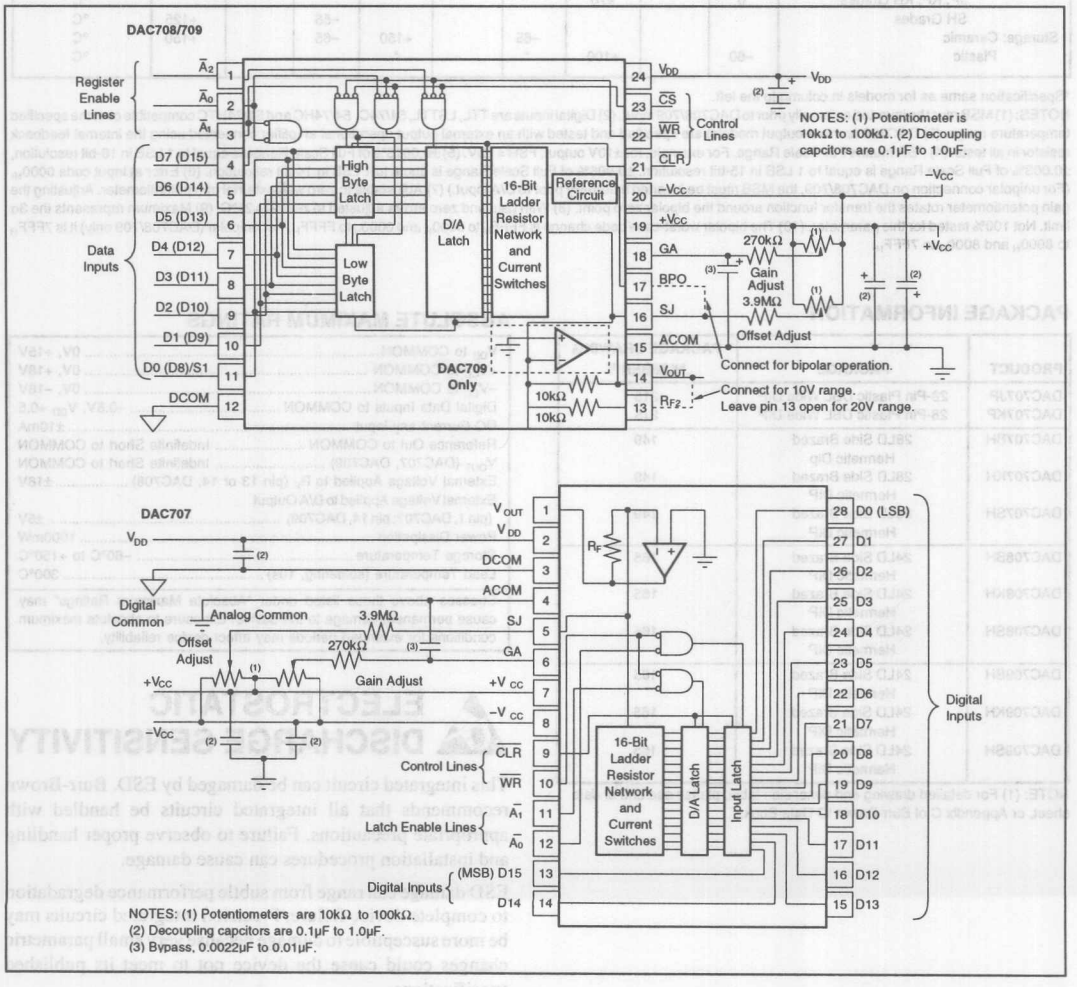
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

| PRODUCT | TEMPERATURE RANGE | INPUT CONFIGURATION | OUTPUT CONFIGURATION |
|---|---|---|---|
| DAC707JP | 0°C to +70°C | 16-bit port | ±10V output |
| DAC707JP-BI[1] | 0°C to +70°C | 16-bit port | ±10V output |
| DAC707KP | 0°C to +70°C | 16-bit port | ±10V output |
| DAC707KP-BI[1] | 0°C to +70°C | 16-bit port | ±10V output |
| DAC707KH | 0°C to +70°C | 16-bit port | ±10V output |
| DAC707KH-BI[1] | 0°C to +70°C | 16-bit port | ±10V output |
| DAC707BH | –25°C to +85°C | 16-bit port | ±10V output |
| DAC707BH-BI[1] | –25°C to +85°C | 16-bit port | ±10V output |
| DAC707SH | –55°C to +125°C | 16-bit port | ±10V output |
| DAC707SH-BI[1] | –55°C to +125°C | 16-bit port | ±10V output |
| DAC708KH | 0°C to +70°C | 8-bit port | ±1mA output |
| DAC708BH | –25°C to +85°C | 8-bit port | ±1mA output |
| DAC708SH | –55°C to +125°C | 8-bit port | ±1mA output |
| DAC709KH | 0°C to +70°C | 8-bit port | ±10V output |
| DAC709BH | –25°C to +85°C | 8-bit port | ±10V output |
| DAC709SH | –55°C to +125°C | 8-bit port | ±10V output |

NOTE: (1) 25 piece minimum order.

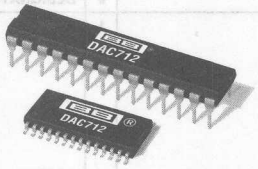
## CONNECTION DIAGRAMS



## DESCRIPTION OF PIN FUNCTIONS

| DAC707 | | Pin | DAC708/709 | |
|---|---|---|---|---|
| DESIGNATOR | DESCRIPTION | # | DESIGNATOR | DESCRIPTION |
| $V_{OUT}$ | Voltage output for DAC707 (±10V) | 1 | $A_2$ | Latch enable for D/A latch (Active low) |
| $V_{DD}$ | Logic supply (+5V) | 2 | $A_0$ | Latch enable for "low byte" input (Active low). When both $A_0$ and $A_1$ are logic "0", the serial input mode is selected and the serial input is enabled. |
| DCOM | Digital common | 3 | $A_1$ | Latch enable for "high byte" input (Active low). When both $A_0$ and $A_1$ are logic "0", the serial input mode is selected and the serial input is enabled. |
| ACOM | Analog common | 4 | D7 (D15) | Input for data bit 7 if enabling low byte (LB) latch or data bit 15 if enabling the high byte (HB) latch. |
| SJ | Summing junction of the internal output op amp for the DAC707. Offset adjust circuit is connected to the summing junction of the output amplifier. Refer to Block Diagram. | 5 | D6 (D14) | Input for data bit 6 if enabling LB latch or data bit 14 if enabling the HB latch. |
| GA | Gain adjust pin. Refer to Connection Diagram for gain adjust circuit. | 6 | D5 (D13) | Data bit 5 (LB) or data bit 13 (HB) |
| $+V_{CC}$ | Positive supply voltage (+15V) | 7 | D4 (D12) | Data bit 4 (LB) or data bit 12 (HB) |
| $-V_{CC}$ | Negative supply voltage (–15V) | 8 | D3 (D11) | Data bit 3 (LB) or data bit 11 (HB) |
| $\overline{CLR}$ | Clear line. Sets the input latch to zero and sets the D/A latch to the input code that gives bipolar zero on the D/A output (Active low) | 9 | D2 (D10) | Data bit 2 (LB) or data bit 10 (HB) |
| $\overline{WR}$ | Write control line (Active low) | 10 | D1 (D9) | Data bit 1 (LB) or data bit 9 (HB) |
| $\overline{A_1}$ | Enable for D/A converter latch (Active low) | 11 | D0 (D8)/SI | Data bit 0 (LB) or data bit 8 (HB). Serial input when serial mode is selected. |
| $\overline{A_0}$ | Enable for input latch (Active low) | 12 | DCOM | Digital common |
| D15 (MSB) | Data bit 15 (Most Significant Bit) | 13 | $R_{F2}$ | Feedback resistor for internal or external operational amplifier. Connect to pin 14 when a 10V output range is desired. Leave open for a 20V output range. |
| D14 | Data bit 14 | 14 | $V_{OUT}$ $R_{F1}$ (DAC708) | Voltage output for DAC709 or feedback resistor for use with an external output op amp for the DAC708. Refer to Connection Diagram for connection of external op amp to DAC708. |
| D13 | Data bit 13 | 15 | ACOM | Analog common |
| D12 | Data bit 12 | 16 | SJ (DAC709) $I_{OUT}$ (DAC708) | Summing junction of the internal output op amp for the DAC709, or the current output for the DAC708. Refer to Connection Diagram for connection of external op amp to DAC708. |
| D11 | Data bit 11 | 17 | BPO | Bipolar offset. Connect to pin 16 when operating in the bipolar mode. Leave open for unipolar mode. |
| D10 | Data bit 10 | 18 | GA | Gain adjust pin |
| D9 | Data bit 9 | 19 | $+V_{CC}$ | Positive supply voltage (+15V) |
| D8 | Data bit 8 | 20 | $-V_{CC}$ | Negative supply voltage (–15V) |
| D7 | Data bit 7 | 21 | $\overline{CLR}$ | Clear line. Sets the high and low byte input registers to zero and, for bipolar operation, sets the D/A register to the input code that gives bipolar zero on the D/A output. (In the unipolar mode, invert the MSB prior to the D/A.) |
| D6 | Data bit 6 | 22 | $\overline{WR}$ | Write control line |
| D5 | Data bit 5 | 23 | $\overline{CS}$ | Chip select control line |
| D4 | Data bit 4 | 24 | $V_{DD}$ | Logic supply (+5V) |
| D3 | Data bit 3 | 25 | No pin | |
| D2 | Data bit 2 | 26 | No pin | (The DAC708 and DAC709 are in 24-pin packages) |
| D1 | Data bit 1 | 27 | No pin | |
| D0 (LSB) | Data bit 0 (Least Significant Bit) | 28 | No pin | |

BURR - BROWN®




# DAC712

www.burr-brown.com/databook/DAC712.html

# 16-BIT DIGITAL-TO-ANALOG CONVERTER With 16-Bit Bus Interface

## FEATURES

- HIGH-SPEED 16-BIT PARALLEL DOUBLE-BUFFERED INTERFACE
- VOLTAGE OUTPUT: ±10V
- 13-, 14-, AND 15-BIT LINEARITY GRADES
- 16-BIT MONOTONIC OVER TEMPERATURE (L GRADE)
- POWER DISSIPATION: 600mW max
- GAIN AND OFFSET ADJUST: Convenient for Auto-Cal D/A Converters
- 28-LEAD DIP AND SOIC PACKAGES

## DESCRIPTION

DAC712 is a complete 16-bit resolution D/A converter with 16 bits of monotonicity over temperature.

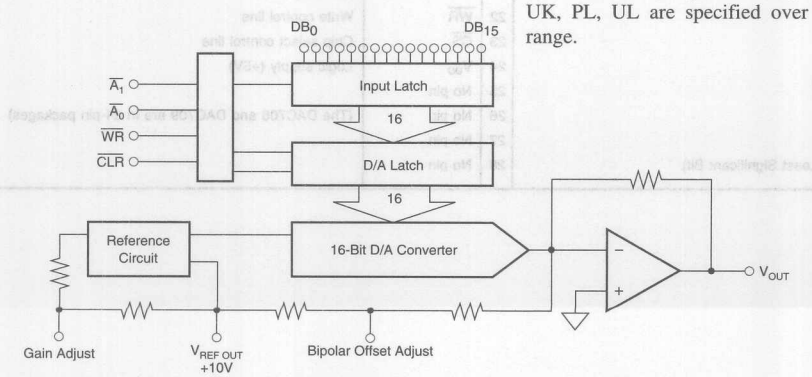
DAC712 has a precision +10V temperature compensated voltage reference, ±10V output amplifier and 16-bit port bus interface.

The digital interface is fast, 60ns minimum write pulse width, is double-buffered and has a CLEAR function that resets the analog output to bipolar zero.

GAIN and OFFSET adjustment inputs are arranged so that they can be easily trimmed by external D/A converters as well as by potentiometers.

DAC712 is available in two linearity error performance grades: ±4LSB and ±2LSB and three differential linearity grades: ±4LSB, ±2LSB, and ±1LSB. The DAC712 is specified at power supply voltages of ±12V and ±15V.

DAC712 is packaged in a 28-pin 0.3" wide plastic DIP and in a 28-lead wide-body plastic SOIC. The DAC712P, U, PB, UB, PC, UC are specified over the –40°C to +85°C temperature range and the DAC712PK, UK, PL, UL are specified over the 0°C to +70°C range.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132



PDS-1164E

BURR - BROWN®

# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = 25°C, $+V_{CC}$ = +12V and +15V, $-V_{CC}$ = −12V and −15V, unless otherwise noted.

| PARAMETER | DAC712P, U | | | DAC712PB, UB | | | DAC712PC, UC | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT** | | | | | | | | | | |
| **RESOLUTION** | | 16 | | | * | | | * | | Bits |
| **DIGITAL INPUTS** | | | | | | | | | | |
| Input Code | | Binary Two's Complement | | | * | | | * | | |
| Logic Levels[1] | | | | | | | | | | |
| $V_{IH}$ | +2.0 | | $+V_{CC}-1.4$ | * | | * | * | | * | V |
| $V_{IL}$ | 0 | | +0.8 | * | | * | * | | * | V |
| $I_{IH}$ ($V_I$ = +2.7V) | | | ±10 | | | * | | | * | µA |
| $I_{IL}$ ($V_I$ = +0.4V) | | | ±10 | | | * | | | * | µA |
| **TRANSFER CHARACTERISTICS** | | | | | | | | | | |
| **ACCURACY** | | | | | | | | | | |
| Linearity Error | | | ±4 | | | ±2 | | | ±2 | LSB |
| $T_{MIN}$ to $T_{MAX}$ | | | ±8 | | | ±4 | | | ±2 | LSB |
| Differential Linearity Error | | | ±4 | | | ±2 | | | ±1 | LSB |
| $T_{MIN}$ to $T_{MAX}$ | | | ±8 | | | ±4 | | | ±2 | LSB |
| Monotonicity Over Temp | 13 | | | 14 | | | 15 | | | Bits |
| Gain Error[3] | | | ±0.1 | | | ±0.1 | | | * | % |
| $T_{MIN}$ to $T_{MAX}$ | | | ±0.2 | | | ±0.15 | | | * | % |
| Bipolar Zero Error[3] | | | ±0.1 | | | * | | | * | % FSR[2] |
| | | | ±20 | | | * | | | * | mV |
| $T_{MIN}$ to $T_{MAX}$ | | | ±0.2 | | | ±0.15 | | | * | % FSR |
| | | | ±40 | | | ±30 | | | * | mV |
| Power Supply Sensitivity Of Full Scale: | | | ±0.003 | | | * | | | * | % FSR/% $V_{CC}$ |
| | | | ±30 | | | * | | | * | ppm FSR/% $V_{CC}$ |
| **DYNAMIC PERFORMANCE** | | | | | | | | | | |
| Settling Time (to ±0.003%FSR, 5kΩ ll 500pF Load)[4] | | | | | | | | | | |
| 20V Output Step | | 6 | | | * | 10 | | * | * | µs |
| 1 LSB Output Step[5] | | 4 | | | * | | | * | | µs |
| Output Slew Rate | | 10 | | | * | | | * | | V/µs |
| Total Harmonic Distortion + Noise | | | | | | | | | | |
| 0dB, 1001Hz, $f_S$ = 100kHz | | 0.005 | | | * | | | * | | % |
| −20dB, 1001Hz, $f_S$ = 100kHz | | 0.03 | | | * | | | * | | % |
| −60dB, 1001Hz, $f_S$ = 100kHz | | 3.0 | | | * | | | * | | % |
| SINAD | | | | | | | | | | |
| 1001Hz, $f_S$ = 100kHz | | 87 | | | * | | | * | | dB |
| Digital Feedthrough[5] | | 2 | | | * | | | * | | nV-s |
| Digital-to-Analog Glitch Impulse[5] | | 15 | | | * | | | * | | nV-s |
| Output Noise Voltage (Includes Reference) | | 120 | | | * | | | * | | nV/√Hz |
| **ANALOG OUTPUT** | | | | | | | | | | |
| Output Voltage Range | | | | | | | | | | |
| $+V_{CC}$, $-V_{CC}$ = ±11.4V | ±10 | | | * | | | * | | | V |
| Output Current | ±5 | | | * | | | * | | | mA |
| Output Impedance | | 0.1 | | | * | | | * | | Ω |
| Short Circuit to ACOM, Duration | | Indefinite | | | * | | | * | | |
| **REFERENCE VOLTAGE** | | | | | | | | | | |
| Voltage | +9.975 | +10.000 | +10.025 | * | * | * | * | * | * | V |
| $T_{MIN}$ to $T_{MAX}$ | +9.960 | | +10.040 | * | | * | * | | * | V |
| Output Resistance | | 1 | | | * | | | * | | Ω |
| Source Current | 2 | | | * | | | * | | | mA |
| Short Circuit to ACOM, Duration | | Indefinite | | | * | | | * | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | | | |
| Voltage: $+V_{CC}$ | +11.4 | +15 | +16.5 | * | * | * | * | * | * | V |
| $-V_{CC}$ | −11.4 | −15 | −16.5 | * | * | * | * | * | * | V |
| Current (No Load, ±15V Supplies) | | | | | | | | | | |
| $+V_{CC}$ | | 13 | 15 | | * | * | | * | * | mA |
| $-V_{CC}$ | | 22 | 25 | | * | * | | * | * | mA |
| Power Dissipation[6] | | 525 | 600 | | * | * | | * | * | mW |
| **TEMPERATURE RANGES** | | | | | | | | | | |
| Specification | | | | | | | | | | |
| All Grades | −40 | | +85 | * | | * | * | | * | °C |
| Storage | −60 | | +150 | * | | * | * | | * | °C |
| Thermal Coefficient $\theta_{JA}$ | | | | | | | | | | |
| DIP Package | | 75 | | | * | | | * | | °C/W |
| SOIC Package | | 75 | | | * | | | * | | °C/W |

* Specifications same as DAC712P, U.

NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for a ±10V output, FSR = 20V. (3) Errors externally adjustable to zero. (4) Maximum represents the 3σ limit. Not 100% tested for this parameter. (5) For the worst case code changes: $FFFF_{HEX}$ to $0000_{HEX}$ and $0000_{HEX}$ to $FFFF_{HEX}$. These are Binary Two's Complement (BTC) codes. (6) Typical supply voltages times maximum currents.

# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $+V_{CC}$ = +12V and +15V, $-V_{CC}$ = –12V and –15V, unless otherwise noted.

| PARAMETER | DAC712PK, UK MIN | DAC712PK, UK TYP | DAC712PK, UK MAX | DAC712PL, UL MIN | DAC712PL, UL TYP | DAC712PL, UL MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | |
| **RESOLUTION** | | 16 | | | * | | Bits |
| **DIGITAL INPUTS** | | | | | | | |
| Input Code | | Binary Two's Complement | | | * | | |
| Logic Levels[1] | | | | | | | |
| $V_{IH}$ | +2.0 | | $+V_{CC}$ – 1.4 | * | | * | V |
| $V_{IL}$ | 0 | | +0.8 | * | | * | V |
| $I_{IH}$ ($V_I$ = +2.7V) | | | ±10 | | | * | µA |
| $I_{IL}$ ($V_I$ = +0.4V) | | | ±10 | | | * | µA |
| **TRANSFER CHARACTERISTICS** | | | | | | | |
| **ACCURACY** | | | | | | | |
| Linearity Error | | | ±2 | | | ±2 | LSB |
| $T_{MIN}$ to $T_{MAX}$ | | | ±2 | | | ±2 | LSB |
| Differential Linearity Error | | | ±2 | | | ±1 | LSB |
| $T_{MIN}$ to $T_{MAX}$ | | | ±2 | | | ±1 | LSB |
| Monotonicity Over Temp | 15 | | | 16 | | | Bits |
| Gain Error[3] | | | ±0.1 | | | * | % |
| $T_{MIN}$ to $T_{MAX}$ | | | ±0.15 | | | ±0.02 | % |
| Bipolar Zero Error[3] | | | ±0.1 | | | * | % FSR[2] |
| | | | ±20 | | | ±0.15 | mV |
| $T_{MIN}$ to $T_{MAX}$ | | | ±0.15 | | | ±0.15 | % FSR |
| | | | ±30 | | | ±0.15 | mV |
| Power Supply Sensitivity of Full Scale | | | ±0.003 | | | * | %FSR/% $V_{CC}$ |
| | | | ±30 | | | * | ppm FSR/% $V_{CC}$ |
| **DYNAMIC PERFORMANCE** | | | | | | | |
| Settling Time (to ±0.003%FSR, 5kΩ II 500pF Load)[4] | | | | | | | |
| 20V Output Step | | 6 | 10 | | * | 10 | µs |
| 1LSB Output Step[5] | | 4 | | | * | | µs |
| Output Slew Rate | | 10 | | | * | | V/µs |
| Total Harmonic Distortion + Noise | | | | | | | |
| 0dB, 1001Hz, $f_S$ = 100kHz | | 0.005 | | | * | | % |
| –20dB, 1001Hz, $f_S$ = 100kHz | | 0.03 | | | * | | % |
| –60dB, 1001Hz, $f_S$ = 100kHz | | 3.0 | | | * | | % |
| SINAD | | | | | | | |
| 1001Hz, $f_S$ = 100kHz | | 87 | | | * | | dB |
| Digital Feedthrough[5] | | 2 | | | * | | nV–s |
| Digital-to-Analog Glitch Impulse[5] | | 15 | | | * | | nV–s |
| Output Noise Voltage (includes reference) | | 120 | | | * | | nV/√Hz |
| **ANALOG OUTPUT** | | | | | | | |
| Output Voltage Range | | | | | | | |
| $+V_{CC}$, $-V_{CC}$ = ±11.4V | ±10 | | | * | | | V |
| Output Current | ±5 | | | * | | | mA |
| Output Impedance | | 0.1 | | | * | | Ω |
| Short Circuit to ACOM, Duration | | Indefinite | | | * | | |
| **REFERENCE VOLTAGE** | | | | | | | |
| Voltage | +9.975 | +10.000 | +10.025 | * | * | * | V |
| $T_{MIN}$ to $T_{MAX}$ | +9.960 | | +10.040 | * | | * | V |
| Output Resistance | | 1 | | | * | | Ω |
| Source Current | 2 | | | * | | | mA |
| Short Circuit to ACOM, Duration | | Indefinite | | | * | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | |
| Voltage: $+V_{CC}$ | +11.4 | +15 | +16.5 | * | * | * | V |
| $-V_{CC}$ | –11.4 | –15 | –16.5 | * | * | * | V |
| Current (No Load, ±15V Supplies) | | | | | | | |
| $+V_{CC}$ | | 13 | 15 | | * | * | mA |
| $-V_{CC}$ | | 22 | 25 | | * | * | mA |
| Power Dissipation[6] | | 525 | 600 | | | * | mW |
| **TEMPERATURE RANGES** | | | | | | | |
| Specification | | | | | | | |
| All Grades | 0 | | +70 | * | | * | °C |
| Storage | –60 | | +150 | * | | * | °C |
| Thermal Coefficient, $\theta_{JA}$ | | | | | | | |
| DIP Package | | 75 | | | * | | °C/W |
| SOIC Package | | 75 | | | * | | °C/W |

* Specifications same as DAC712PK, UK.

NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for a ±10V output, FSR = 20V. (3) Errors externally adjustable to zero. (4) Maximum represents the 3σ limit. Not 100% tested for this parameter. (5) For the worst case code changes: $FFFF_{HEX}$ to $0000_{HEX}$ and $0000_{HEX}$ to $FFFF_{HEX}$. These are Binary Two's Complement (BTC) codes. (6) Typical supply voltages times maximum currents.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_{CC}$ to COMMON | 0V, +17V |
| $-V_{CC}$ to COMMON | 0V, –17V |
| $+V_{CC}$ to $-V_{CC}$ | 34V |
| Digital Inputs to COMMON | –1V to $+V_{CC}$ –0.7V |
| External Voltage Applied to BPO and Range Resistors | $\pm V_{CC}$ |
| $V_{REF\ OUT}$ | Indefinite Short to COMMON |
| $V_{OUT}$ | Indefinite Short to COMMON |
| Power Dissipation | 750mW |
| Storage Temperature | –60°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## PACKAGE INFORMATION

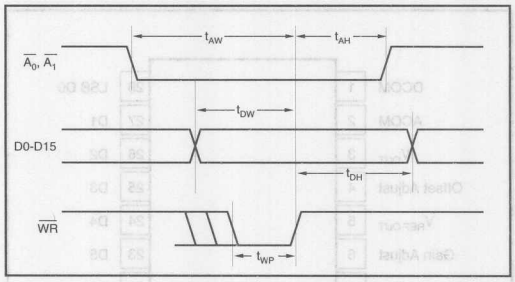
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| DAC712P | Plastic DIP | 246 |
| DAC712U | Plastic SOIC | 217 |
| DAC712PB | Plastic DIP | 246 |
| DAC712UB | Plastic SOIC | 217 |
| DAC712PK | Plastic DIP | 246 |
| DAC712UK | Plastic SOIC | 217 |
| DAC712PL | Plastic DIP | 246 |
| DAC712UL | Plastic SOIC | 217 |
| DAC712PC | Plastic DIP | 246 |
| DAC712UC | Plastic SOIC | 217 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

| PRODUCT | TEMPERATURE RANGE | LINEARITY ERROR MAX at +25°C | DIFFERENTIAL LINEARITY ERROR MAX at +25°C |
|---|---|---|---|
| DAC712P | –40°C to +85°C | ±4LSB | ±4LSB |
| DAC712U | –40°C to +85°C | ±4LSB | ±4LSB |
| DAC712PB | –40°C to +85°C | ±2LSB | ±2LSB |
| DAC712UB | –40°C to +85°C | ±2LSB | ±2LSB |
| DAC712PK | 0°C to +70°C | ±2LSB | ±2LSB |
| DAC712UK | 0°C to +70°C | ±2LSB | ±2LSB |
| DAC712PL | 0°C to +70°C | ±2LSB | ±1LSB |
| DAC712UL | 0°C to +70°C | ±2LSB | ±1LSB |
| DAC712PC | –40°C to +85°C | ±2LSB | ±1LSB |
| DAC712UC | –40°C to +85°C | ±2LSB | ±1LSB |

## TIMING DIAGRAM




## TIMING SPECIFICATIONS

$T_A$ = –40°C to +85°C, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = –12V or –15V.

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|---|---|---|---|---|
| $t_{DW}$ | Data Valid to End of $\overline{WR}$ | 50 | | ns |
| $t_{AW}$ | $\overline{A_0}$, $\overline{A_1}$ Valid to End of $\overline{WR}$ | 50 | | ns |
| $t_{AH}$ | $\overline{A_0}$, $\overline{A_1}$ Hold after End of $\overline{WR}$ | 10 | | ns |
| $t_{DH}$ | Data Hold after end of $\overline{WR}$ | 10 | | ns |
| $t_{WP}$(1) | Write Pulse Width | 50 | | ns |
| $t_{CP}$ | CLEAR Pulse Width | 200 | | ns |

NOTES: (1) For single-buffered operation, $t_{WP}$ is 80ns min. Refer to page 10.

## TRUTH TABLE

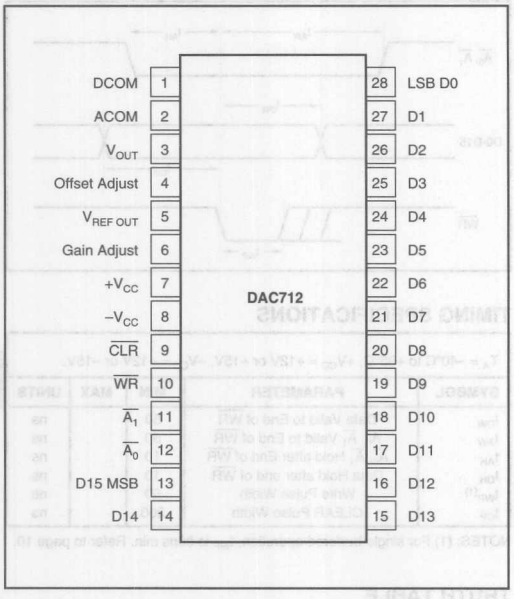
| $\overline{A_0}$ | $\overline{A_1}$ | $\overline{WR}$ | $\overline{CLR}$ | DESCRIPTION |
|---|---|---|---|---|
| 0 | 1 | 1 → 0 → 1 | 1 | Load Input Latch |
| 1 | 0 | 1 → 0 → 1 | 1 | Load D/A Latch |
| 1 | 1 | 1 → 0 → 1 | 1 | No Change |
| 0 | 0 | 0 | 1 | Latches Transparent |
| X | X | 1 | 1 | No Change |
| X | X | X | 0 | Reset D/A Latch |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION

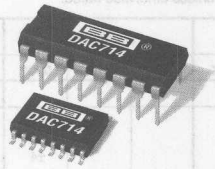



## PIN DESCRIPTIONS

| PIN | LABEL | DESCRIPTION |
|---|---|---|
| 1 | DCOM | Power Supply return for digital currents. |
| 2 | ACOM | Analog Supply Return. |
| 3 | $V_{OUT}$ | ±10V D/A Output. |
| 4 | Off Adj | Offset Adjust (Bipolar). |
| 5 | $V_{REF\ OUT}$ | Voltage Reference Output. |
| 6 | Gain Adj | Gain Adjust. |
| 7 | $+V_{CC}$ | +12V to +15V Supply. |
| 8 | $-V_{CC}$ | −12V to −15V Supply. |
| 9 | $\overline{CLR}$ | CLEAR. Sets D/A output to BIPOLAR ZERO (Active Low). |
| 10 | $\overline{WR}$ | Write (Active Low). |
| 11 | $\overline{A_1}$ | Enable for D/A latch (Active Low). |
| 12 | $\overline{A_0}$ | Enable for Input latch (Active Low). |
| 13 | D15 | Data Bit 15 (Most Significant Bit). |
| 14 | D14 | Data Bit 14. |
| 15 | D13 | Data Bit 13. |
| 16 | D12 | Data Bit 12. |
| 17 | D11 | Data Bit 11. |
| 18 | D10 | Data Bit 10. |
| 19 | D9 | Data Bit 9. |
| 20 | D8 | Data Bit 8. |
| 21 | D7 | Data Bit 7. |
| 22 | D6 | Data Bit 6. |
| 23 | D5 | Data Bit 5. |
| 24 | D4 | Data Bit 4. |
| 25 | D3 | Data Bit 3. |
| 26 | D2 | Data Bit 2. |
| 27 | D1 | Data Bit 1. |
| 28 | D0 | Data Bit 0 (Least Significant Bit). |

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# DAC714

www.burr-brown.com/databook/DAC714.html



# 16-Bit DIGITAL-TO-ANALOG CONVERTER With Serial Data Interface

## FEATURES:

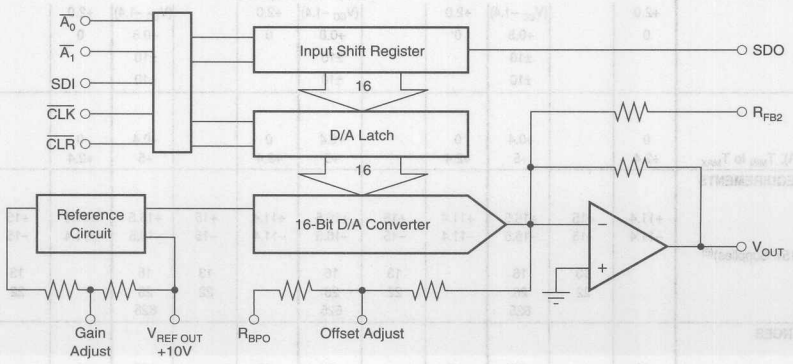
- SERIAL DIGITAL INTERFACE
- VOLTAGE OUTPUT: ±10V, ±5V, 0 to +10V
- ±1 LSB INTEGRAL LINEARITY
- 16-BIT MONOTONIC OVER TEMPERATURE
- PRECISION INTERNAL REFERENCE
- LOW NOISE: 120nV/√Hz Including Reference
- 16-LEAD PLASTIC AND CERAMIC SKINNY DIP AND PLASTIC SOIC PACKAGES

## DESCRIPTION

The DAC714 is a complete monolithic digital-to-analog converter including a +10V temperature compensated reference, current-to-voltage amplifier, a high-speed synchronous serial interface, a serial output which allows cascading multiple converters, and an asynchronous clear function which immediately sets the output voltage to midscale.

The output voltage range is ±10V, ±5V, or 0 to +10V while operating from ±12V or ±15V supplies. The gain and bipolar offset adjustments are designed so that they can be set via external potentiometers or external D/A converters. The output amplifier is protected against short circuit to ground.

The 16-pin DAC714 is available in a plastic 0.3" DIP, ceramic 0.3" CERDIP, and wide-body plastic SOIC package. The DAC714P, U, HB, and HC are specified over the –40°C to +85°C temperature range while the DAC714HL is specified over the 0°C to +70°C range.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

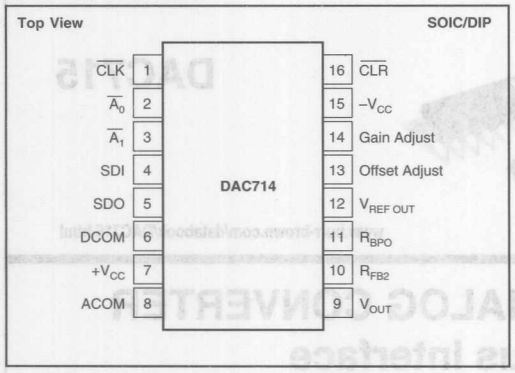
# SPECIFICATIONS

At $T_A$ = +25°C, $+V_{CC}$ = +12V and +15V, $-V_{CC}$ = −12V, and −15V, unless otherwise noted.

| PARAMETER | DAC714P, U | | | DAC714HB | | | DAC714HC | | | DAC714HL | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **TRANSFER CHARACTERISTICS** | | | | | | | | | | | | | |
| **ACCURACY** | | | | | | | | | | | | | |
| Linearity Error | | | ±4 | | | ±2 | | | ±1 | | | ±1 | LSB |
| $T_{MIN}$ to $T_{MAX}$ | | | ±8 | | | ±4 | | | ±2 | | | ±2 | LSB |
| Differential Linearity Error | | | ±4 | | | ±2 | | | ±1 | | | ±1 | LSB |
| $T_{MIN}$ to $T_{MAX}$ | | | ±8 | | | ±4 | | | ±2 | | | ±1 | LSB |
| Monotonicity | 14 | | | 15 | | | 16 | | | 16 | | | Bits |
| Monotonicity Over Spec Temp Range | 13 | | | 14 | | | 15 | | | 16 | | | Bits |
| Gain Error[3] | | | ±0.1 | | | ±0.1 | | | ±0.1 | | | ±0.1 | % |
| $T_{MIN}$ to $T_{MAX}$ | | | ±0.25 | | | ±0.25 | | | ±0.25 | | | ±0.25 | % |
| Unipolar/Bipolar Zero Error[3] | | | ±0.1 | | | ±0.1 | | | ±0.1 | | | ±0.1 | % of FSR[2] |
| $T_{MIN}$ to $T_{MAX}$ | | | ±0.2 | | | ±0.2 | | | ±0.2 | | | ±0.2 | % of FSR |
| Power Supply Sensitivity of Gain | | | ±0.003 | | | ±0.003 | | | ±0.003 | | | ±0.003 | %FSR/%$V_{CC}$ |
| | | | ±30 | | | ±30 | | | ±30 | | | ±30 | ppm FSR/%$V_{CC}$ |
| **DYNAMIC PERFORMANCE** | | | | | | | | | | | | | |
| Settling Time | | | | | | | | | | | | | |
| (to ±0.003%FSR, 5kΩ II 500pF Load)[4] | | | | | | | | | | | | | |
| 20V Output Step | | 6 | 10 | | 6 | 10 | | 6 | 10 | | 6 | 10 | µs |
| 1LSB Output Step[5] | | 4 | | | 4 | | | 4 | | | 4 | | µs |
| Output Slew Rate | | 10 | | | 10 | | | 10 | | | 10 | | V/µs |
| Total Harmonic Distortion | | | | | | | | | | | | | |
| 0dB, 1001Hz, $f_S$ = 100kHz | | 0.005 | | | 0.005 | | | 0.005 | | | 0.005 | | % |
| −20dB, 1001Hz, $f_S$ = 100kHz | | 0.03 | | | 0.03 | | | 0.03 | | | 0.03 | | % |
| −60dB, 1001Hz, $f_S$ = 100kHz | | 3.0 | | | 3.0 | | | 3.0 | | | 3.0 | | % |
| SINAD: 1001Hz, $f_S$ = 100kHz | | 87 | | | 87 | | | 87 | | | 87 | | dB |
| Digital Feedthrough[5] | | 2 | | | 2 | | | 2 | | | 2 | | nV–s |
| Digital-to-Analog Glitch Impulse[5] | | 15 | | | 15 | | | 15 | | | 15 | | nV–s |
| Output Noise Voltage (includes reference) | | 120 | | | 120 | | | 120 | | | 120 | | nV/√Hz |
| **ANALOG OUTPUT** | | | | | | | | | | | | | |
| Output Voltage Range | | | | | | | | | | | | | |
| $+V_{CC}$, $-V_{CC}$ = ±11.4V | ±10 | | | ±10 | | | ±10 | | | ±10 | | | V |
| Output Current | ±5 | | | ±5 | | | ±5 | | | ±5 | | | mA |
| Output Impedance | | 0.1 | | | 0.1 | | | 0.1 | | | 0.1 | | Ω |
| Short Circuit to ACOM Duration | | Indefinite | | | Indefinite | | | Indefinite | | | Indefinite | | |
| **REFERENCE VOLTAGE** | | | | | | | | | | | | | |
| Voltage | +9.975 | +10.000 | +10.025 | +9.975 | +10.000 | +10.025 | +9.975 | +10.000 | +10.025 | +9.975 | +10.000 | +10.025 | V |
| $T_{MIN}$ to $T_{MAX}$ | +9.960 | | +10.040 | +9.960 | | +10.040 | +9.960 | | +10.040 | +9.960 | | +10.040 | V |
| Output Resistance | | 1 | | | 1 | | | 1 | | | 1 | | Ω |
| Source Current | 2 | | | 2 | | | 2 | | | 2 | | | mA |
| Short Circuit to ACOM Duration | | Indefinite | | | Indefinite | | | Indefinite | | | Indefinite | | |
| **INTERFACE** | | | | | | | | | | | | | |
| **RESOLUTION** | | 16 | | | 16 | | | 16 | | | 16 | | Bits |
| **DIGITAL INPUTS** | | | | | | | | | | | | | |
| Serial Data Input Code | | | | | | | | | | | | | |
| Logic Levels[1] | | | | | | Binary Two's Complement | | | | | | | |
| $V_{IH}$ | +2.0 | | ($V_{CC}$ −1.4) | +2.0 | | ($V_{CC}$ −1.4) | +2.0 | | ($V_{CC}$ −1.4) | +2.0 | | ($V_{CC}$ −1.4) | V |
| $V_{IL}$ | 0 | | +0.8 | 0 | | +0.8 | 0 | | +0.8 | 0 | | +0.8 | V |
| $I_{IH}$ ($V_I$ = +2.7V) | | | ±10 | | | ±10 | | | ±10 | | | ±10 | µA |
| $I_{IL}$ ($V_I$ = +0.4V) | | | ±10 | | | ±10 | | | ±10 | | | ±10 | µA |
| **DIGITAL OUTPUT** | | | | | | | | | | | | | |
| Serial Data | | | | | | | | | | | | | |
| $V_{OL}$ ($I_{SINK}$ = 1.6mA) | 0 | | +0.4 | 0 | | +0.4 | 0 | | +0.4 | 0 | | +0.4 | V |
| $V_{OH}$ ($I_{SOURCE}$ = 500µA), $T_{MIN}$ to $T_{MAX}$ | +2.4 | | +5 | +2.4 | | +5 | +2.4 | | +5 | +2.4 | | +5 | V |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | | | | | | |
| Voltage | | | | | | | | | | | | | |
| $+V_{CC}$ | +11.4 | +15 | +16.5 | +11.4 | +15 | +16.5 | +11.4 | +15 | +16.5 | +11.4 | +15 | +16.5 | V |
| $-V_{CC}$ | −11.4 | −15 | −16.5 | −11.4 | −15 | −16.5 | −11.4 | −15 | −16.5 | −11.4 | −15 | −16.5 | V |
| Current (No Load, ±15V Supplies)[6] | | | | | | | | | | | | | |
| $+V_{CC}$ | | 13 | 16 | | 13 | 16 | | 13 | 16 | | 13 | 16 | mA |
| $-V_{CC}$ | | 22 | 26 | | 22 | 26 | | 22 | 26 | | 22 | 26 | mA |
| Power Dissipation[7] | | | 625 | | | 625 | | | 625 | | | 625 | mW |
| **TEMPERATURE RANGES** | | | | | | | | | | | | | |
| Specification | | | | | | | | | | | | | |
| All Grades | −40 | | +85 | −40 | | +85 | −40 | | +85 | 0 | | +70 | °C |
| Storage | −60 | | +150 | −60 | | +150 | −60 | | +150 | −60 | | +150 | °C |
| Thermal Coefficient, $\theta_{JA}$ | | 75 | | | 75 | | | 75 | | | 75 | | °C/W |

NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (3) Errors externally adjustable to zero. (4) Maximum represents the 3σ limit. Not 100% tested for this parameter. (5) For the worst-case Binary Two's Complement code changes: $FFFF_H$ to $0000_H$ and $0000_H$ to $FFFF_H$. (6) During power supply turn on, the transient supply current may approach 3x the maximum quiescent specification. (7) Typical (i.e. rated) supply voltages times maximum currents.

## PIN CONFIGURATION




## PIN DESCRIPTIONS

| PIN | LABEL | DESCRIPTION |
|---|---|---|
| 1 | $\overline{CLK}$ | Serial Data Clock |
| 2 | $\overline{A_0}$ | Enable for Input Register (Active Low) |
| 3 | $\overline{A_1}$ | Enable for D/A Latch (Active Low) |
| 4 | SDI | Serial Data Input |
| 5 | SDO | Serial Data Output |
| 6 | DCOM | Digital Ground |
| 7 | $+V_{CC}$ | Positive Power Supply |
| 8 | ACOM | Analog Ground |
| 9 | $V_{OUT}$ | D/A Output |
| 10 | $R_{FB2}$ | ±10V Range Feedback Output |
| 11 | $R_{BPO}$ | Bipolar Offset |
| 12 | $V_{REF\ OUT}$ | Voltage Reference Output |
| 13 | Offset Adjust | Offset Adjust |
| 14 | Gain Adjust | Gain Adjust |
| 15 | $-V_{CC}$ | Negative Power Supply |
| 16 | $\overline{CLR}$ | Clear |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| $+V_{CC}$ to Common | 0V to +17V |
| $-V_{CC}$ to Common | 0V to –17V |
| $+V_{CC}$ to $-V_{CC}$ | 34V |
| ACOM to DCOM | ±0.5V |
| Digital Inputs to Common | –1V to ($V_{CC}$ –0.7V) |
| External Voltage Applied to BPO and Range Resistors | $\pm V_{CC}$ |
| $V_{REF\ OUT}$ | Indefinite Short to Common |
| $V_{OUT}$ | Indefinite Short to Common |
| SDO | Indefinite Short to Common |
| Power Dissipation | 750mW |
| Storage Temperature | –60°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ORDERING INFORMATION

| PRODUCT | PACKAGE | LINEARITY ERROR max at +25°C | TEMPERATURE RANGE |
|---|---|---|---|
| DAC714P | Plastic DIP | ±4 LSB | –40°C to +85°C |
| DAC714U | Plastic SOIC | ±4 LSB | –40°C to +85°C |
| DAC714HB | Ceramic DIP | ±2 LSB | –40°C to +85°C |
| DAC714HC | Ceramic DIP | ±1 LSB | –40°C to +85°C |
| DAC714HL | Ceramic DIP | ±1 LSB | 0°C to +70°C |

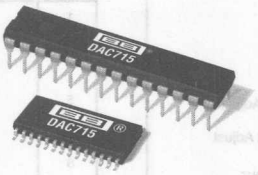
## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| DAC714P | Plastic DIP | 180 |
| DAC714U | Plastic SOIC | 211 |
| DAC714H | Ceramic DIP | 129 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# DAC715

www.burr-brown.com/databook/DAC715.html

# 16-BIT DIGITAL-TO-ANALOG CONVERTER with 16-Bit Bus Interface

## FEATURES

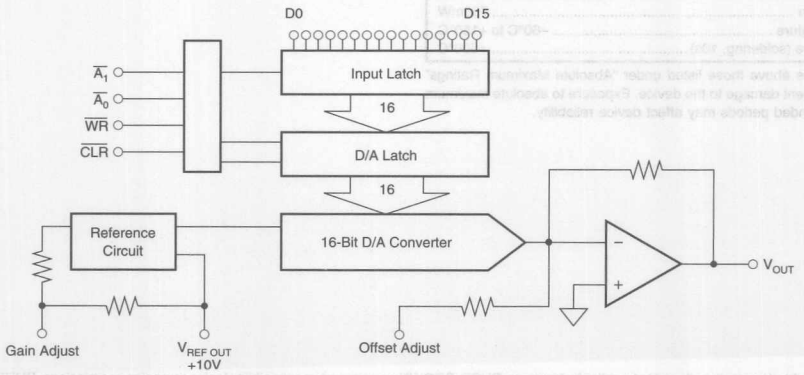
- HIGH-SPEED 16-BIT PARALLEL DOUBLE-BUFFERED INTERFACE
- VOLTAGE OUTPUT: 0 to +10V
- 13-, 14-, 15-BIT LINEARITY GRADES
- 16-BIT MONOTONIC OVER TEMPERATURE (L GRADE)
- POWER DISSIPATION: 600mW max
- GAIN AND OFFSET ADJUST: Convenient for Auto-Cal D/A Converters
- 28-LEAD DIP AND SOIC PACKAGES

## DESCRIPTION

The DAC715 is a complete monolithic digital-to-analog converter including a +10V temperature compensated reference, current-to-voltage amplifier, 16-bit parallel interface that is double buffered, and an asynchronous clear function which immediately sets the output voltage to one-half of full-scale.

The output voltage range is 0 to +10V while operating from ±12V or ±15V supplies. The gain and bipolar offset adjustments are designed so that they can be set via external potentiometers or external D/A converters. The output amplifier is protected against short circuit to ground.

The 28-pin DAC715 is available in a 0.3" plastic DIP and wide-body plastic SOIC package. The DAC715P, U, PB, and UB are specified over the –40°C to +85°C temperature range while the DAC715PK, UK, PL, and UL are specified over the 0°C to +70°C range.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $V_{CC}$ = ±15V, and after a 10-minute warm-up, unless otherwise noted.

| | DAC715P, U | | | DAC715PB, UB | | | DAC715PK, UK | | | DAC715PL, UL | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | UNITS |
| **INPUT** | | | | | | | | | | | | | |
| **RESOLUTION** | | | 16 | | | * | | | * | | | * | Bits |
| **DIGITAL INPUTS** | | | | | | | | | | | | | |
| Input Code | | Binary Two's Complement | | | * | | | * | | | * | | |
| Logic Levels[1]: $V_{IH}$ | +2.0 | | $+V_{CC}$ – 1.4 | * | | * | * | | * | * | | * | V |
| $V_{IL}$ | 0 | | +0.8 | * | | * | * | | * | * | | * | V |
| $I_{IH}$ ($V_I$ = +2.7V) | | | ±10 | | | * | | | * | | | * | µA |
| $I_{IL}$ ($V_I$ = +0.4V) | | | ±10 | | | * | | | * | | | * | µA |
| **TRANSFER CHARACTERISTICS** | | | | | | | | | | | | | |
| **ACCURACY** | | | | | | | | | | | | | |
| Linearity Error | | | ±4 | | | ±2 | | | ±2 | | | ±2 | LSB |
| $T_{MIN}$ to $T_{MAX}$ | | | ±8 | | | ±4 | | | ±2 | | | ±2 | LSB |
| Differential Linearity Error | | | ±4 | | | ±2 | | | ±2 | | | ±1 | LSB |
| $T_{MIN}$ to $T_{MAX}$ | | | ±8 | | | ±4 | | | ±2 | | | ±1 | LSB |
| Monotonicity Over Temp | 13 | | | 14 | | | 15 | | | 16 | | | Bits |
| Gain Error[3] | | | ±0.1 | | | ±0.1 | | | * | | | * | % |
| $T_{MIN}$ to $T_{MAX}$ | | | ±0.2 | | | ±0.15 | | | * | | | * | % |
| Offset Error[3] | | | ±0.1 | | | * | | | * | | | * | % FSR[2] |
| $T_{MIN}$ to $T_{MAX}$ | | | ±0.2 | | | * | | | * | | | * | % FSR |
| Power Supply Sensitivity Of Full Scale | | | ±0.003 | | | * | | | * | | | * | % FSR/%$V_{CC}$ |
| | | | ±30 | | | * | | | * | | | * | PPM FSR/%$V_{CC}$ |
| **DYNAMIC PERFORMANCE** | | | | | | | | | | | | | |
| Settling Time (to ±0.003%FSR, 5kΩ ll 500pF Load)[4] | | | | | | | | | | | | | |
| 10V Output Step | | 6 | 10 | | * | * | | * | * | | * | * | µs |
| 1 LSB Output Step[5] | | 4 | | | * | | | * | | | * | | µs |
| Output Slew Rate | | 10 | | | * | | | * | | | * | | V/µs |
| Total Harmonic Distortion + Noise | | | | | | | | | | | | | |
| 0dB, 1001Hz, $f_S$ = 100kHz | | 0.005 | | | * | | | * | | | * | | % |
| –20dB, 1001Hz, $f_S$ = 100kHz | | 0.03 | | | * | | | * | | | * | | % |
| –60dB, 1001Hz, $f_S$ = 100kHz | | 3.0 | | | * | | | * | | | * | | % |
| SINAD | | | | | | | | | | | | | |
| 1001Hz, $f_S$ = 100kHz | | 87 | | | * | | | * | | | * | | dB |
| Digital Feedthrough[5] | | 2 | | | * | | | * | | | * | | nV-s |
| Digital-to-Analog Glitch Impulse[5] | | 15 | | | * | | | * | | | * | | nV-s |
| Output Noise Voltage | | | | | | | | | | | | | |
| (includes Reference) | | 120 | | | * | | | * | | | * | | nV/√Hz |
| **ANALOG OUTPUT** | | | | | | | | | | | | | |
| Output Voltage Range | | | | | | | | | | | | | |
| $+V_{CC}$, $-V_{CC}$ = ±11.4V | 0 to +10 | | | * | | | * | | | * | | | V |
| Output Current | ±5 | | | * | | | * | | | * | | | mA |
| Output Impedance | | 0.1 | | | * | | | * | | | * | | Ω |
| Short Circuit to ACOM | | | | | | | | | | | | | |
| Duration | | Indefinite | | | * | | | * | | | * | | |
| **REFERENCE VOLTAGE** | | | | | | | | | | | | | |
| Voltage | +9.975 | +10.000 | +10.025 | * | * | * | * | * | * | * | * | * | V |
| $T_{MIN}$ to $T_{MAX}$ | +9.960 | | +10.040 | * | | * | * | | * | * | | * | V |
| Output Resistance | | 1 | | | * | | | * | | | * | | Ω |
| Source Current | 2 | | | * | | | * | | | * | | | mA |
| Short Circuit to ACOM, Duration | | Indefinite | | | * | | | * | | | * | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | | | | | | |
| Voltage: $+V_{CC}$ | +11.4 | +15 | +16.5 | * | * | * | * | * | * | * | * | * | V |
| $-V_{CC}$ | –16.5 | –15 | –11.4 | * | * | * | * | * | * | * | * | * | V |
| Current (no load, ±15V Supplies) | | | | | | | | | | | | | |
| $+V_{CC}$ | | 13 | 15 | | * | * | | * | * | | * | * | mA |
| $-V_{CC}$ | | 22 | 25 | | * | * | | * | * | | * | * | mA |
| Power Dissipation | | 525 | 600 | | * | * | | * | * | | * | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | | | | | | |
| Specification All Grades | –40 | | +85 | * | | * | 0 | | +70 | * | | * | °C |
| Storage | –60 | | +150 | * | | * | * | | * | * | | * | °C |
| Thermal Resistance $\theta_{JA}$ | | | | | | | | | | | | | |
| DIP Package | | 75 | | | * | | | * | | | * | | °C/W |
| SOIC Package | | 75 | | | * | | | * | | | * | | °C/W |

* Specifications same as DAC715P, U.

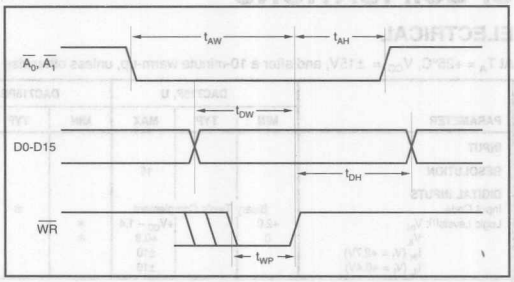
NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for a 0 to +10V output, FSR = 10V. (3) Errors externally adjustable to zero. (4) Maximum represents greater than the 3σ limit. Not 100% tested for this parameter. (5) For the worst case code changes: $FFFF_H$ to $0000_H$ and $0000_H$ to $FFFF_H$. These are Binary Two's Complement (BTC) codes. (6) Typical supply voltages times maximum currents.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| $+V_{CC}$ to COMMON | 0V, +17V |
| $-V_{CC}$ to COMMON | 0V, –17V |
| $+V_{CC}$ to $-V_{CC}$ | 34V |
| Digital Inputs to COMMON | –1V to $+V_{CC}$ |
| External Voltage Applied to BPO and Range Resistors | $\pm V_{CC}$ |
| $V_{REF\ OUT}$ | Indefinite Short to COMMON |
| $V_{OUT}$ | Indefinite Short to COMMON |
| Power Dissipation | 750mW |
| Storage Temperature | –60°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## TIMING DIAGRAM




## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| DAC715P | Plastic DIP | 246 |
| DAC715U | Plastic SOIC | 217 |
| DAC715PB | Plastic DIP | 246 |
| DAC715UB | Plastic SOIC | 217 |
| DAC715PK | Plastic DIP | 246 |
| DAC715UK | Plastic SOIC | 217 |
| DAC715PL | Plastic DIP | 246 |
| DAC715UL | Plastic SOIC | 217 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## TIMING SPECIFICATIONS

$T_A$ = –40°C to +85°C, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = –12V or –15V.

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|---|---|---|---|---|
| $t_{DW}$ | Data Valid to End of $\overline{WR}$ | 50 | | ns |
| $t_{AW}$ | $\overline{A_0}$, $\overline{A_1}$ Valid to End of $\overline{WR}$ | 50 | | ns |
| $t_{AH}$ | $\overline{A_0}$, $\overline{A_1}$ Hold after End of $\overline{WR}$ | 10 | | ns |
| $t_{DH}$ | Data Hold after end of $\overline{WR}$ | 10 | | ns |
| $t_{WP}$[1] | Write Pulse Width | 50 | | ns |
| $t_{CP}$ | CLEAR Pulse Width | 200 | | ns |

NOTES: (1) For single-buffered operation, $t_{WP}$ is 80ns min. Refer to page 10.

## ORDERING INFORMATION

| PRODUCT | PACKAGE | TEMPERATURE RANGE | DIFFERENTIAL LINEARITY ERROR MAX at +25°C |
|---|---|---|---|
| DAC715P | Plastic DIP | –40°C to +85°C | ±4LSB |
| DAC715U | Plastic SOIC | –40°C to +85°C | ±4LSB |
| DAC715PB | Plastic DIP | –40°C to +85°C | ±2LSB |
| DAC715UB | Plastic SOIC | –40°C to +85°C | ±2LSB |
| DAC715PK | Plastic DIP | 0°C to 70°C | ±2LSB |
| DAC715UK | Plastic SOIC | 0°C to 70°C | ±2LSB |
| DAC715PL | Plastic DIP | 0°C to 70°C | ±1LSB |
| DAC715UL | Plastic SOIC | 0°C to 70°C | ±1LSB |

## TRUTH TABLE

| $\overline{A_0}$ | $\overline{A_1}$ | $\overline{WR}$ | $\overline{CLR}$ | DESCRIPTION |
|---|---|---|---|---|
| 0 | 1 | 1 → 0 → 1 | 1 | Load Input Latch |
| 1 | 0 | 1 → 0 → 1 | 1 | Load D/A Latch |
| 1 | 1 | 1 → 0 → 1 | 1 | No Change |
| 0 | 0 | 0 | 1 | Latches Transparent |
| X | X | 1 | 1 | No Change |
| X | X | X | 0 | Reset D/A Latch |

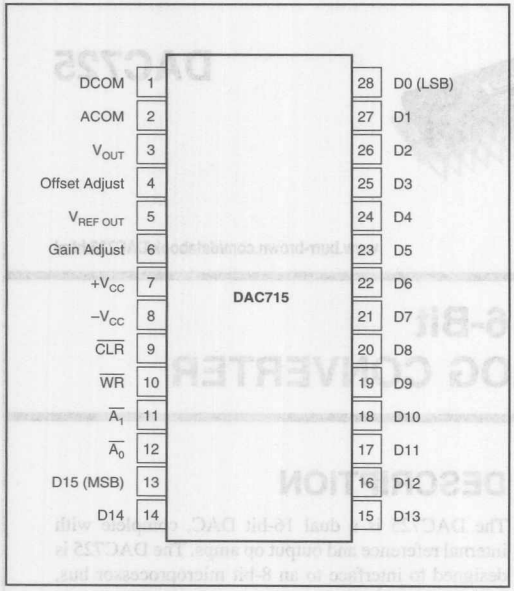
## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

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## PIN CONFIGURATION




## PIN DESCRIPTIONS

| PIN | LABEL | DESCRIPTION |
|---|---|---|
| 1 | DCOM | Digital Ground |
| 2 | ACOM | Analog Ground |
| 3 | $V_{OUT}$ | 0 to +10V D/A Output |
| 4 | Offset Adjust | Offset Adjust |
| 5 | $V_{REF\ OUT}$ | Voltage Reference Output |
| 6 | Gain Adjust | Gain Adjust |
| 7 | $+V_{CC}$ | +12V to +15V Supply |
| 8 | $-V_{CC}$ | –12V to –15V Supply |
| 9 | $\overline{CLR}$ | CLEAR. Sets D/A output to Half Scale (Active Low) |
| 10 | $\overline{WR}$ | Write (Active Low) |
| 11 | $\overline{A_1}$ | Enable for D/A latch (Active Low) |
| 12 | $\overline{A_0}$ | Enable for Input latch (Active Low) |
| 13 | D15 | Data Bit 15 (Most Significant Bit) |
| 14 | D14 | Data Bit 14 |
| 15 | D13 | Data Bit 13 |
| 16 | D12 | Data Bit 12 |
| 17 | D11 | Data Bit 11 |
| 18 | D10 | Data Bit 10 |
| 19 | D9 | Data Bit 9 |
| 20 | D8 | Data Bit 8 |
| 21 | D7 | Data Bit 7 |
| 22 | D6 | Data Bit 6 |
| 23 | D5 | Data Bit 5 |
| 24 | D4 | Data Bit 4 |
| 25 | D3 | Data Bit 3 |
| 26 | D2 | Data Bit 2 |
| 27 | D1 | Data Bit 1 |
| 28 | D0 | Data Bit 0 (Least Significant Bit) |

BURR-BROWN®




# DAC725

www.burr-brown.com/databook/DAC725.html

# Dual 16-Bit DIGITAL-TO-ANALOG CONVERTER

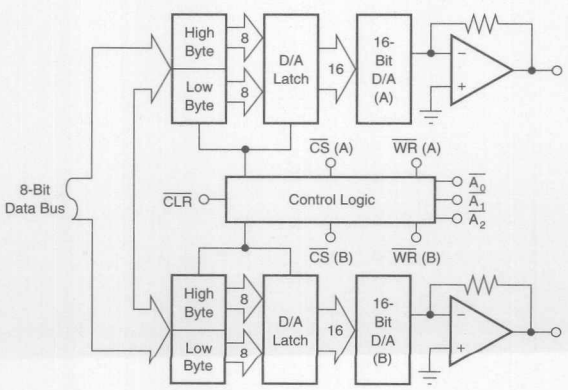
## FEATURES

- COMPLETE DUAL $V_{OUT}$ DAC
- DOUBLE-BUFFERED INPUT REGISTER
- HIGH-SPEED DATA INPUT: Serial or Parallel
- HIGH ACCURACY: ±0.003% Linearity Error
- 14-BIT MONOTONICITY OVER TEMPERATURE
- PLASTIC PACKAGE
- CLEAR INPUT TO SET ZERO OUTPUT

## DESCRIPTION

The DAC725 is a dual 16-bit DAC, complete with internal reference and output op amps. The DAC725 is designed to interface to an 8-bit microprocessor bus, but can also be interfaced to wider buses. The hybrid construction minimizes the digital feedthrough typically associated with products that combine the digital bus interface circuitry with high-accuracy analog circuitry.

The 16-bit data word is loaded into either of the DACs in two 8-bit bytes per 16-bit word. The versatility of the control lines allows the data word to be directed to either DAC, in any order. The voltage-out DACs are dedicated to a bipolar output voltage of ±10V. The output is immediately set to 0V when the Clear command is given. This feature, combined with the bus interfacing and complete DAC circuitry, makes the DAC725 ideal for automatic test equipment, power control, servo systems, and robotics applications.




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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $V_{CC}$ = ±15V, and after a 10-minute warm-up, unless otherwise noted.

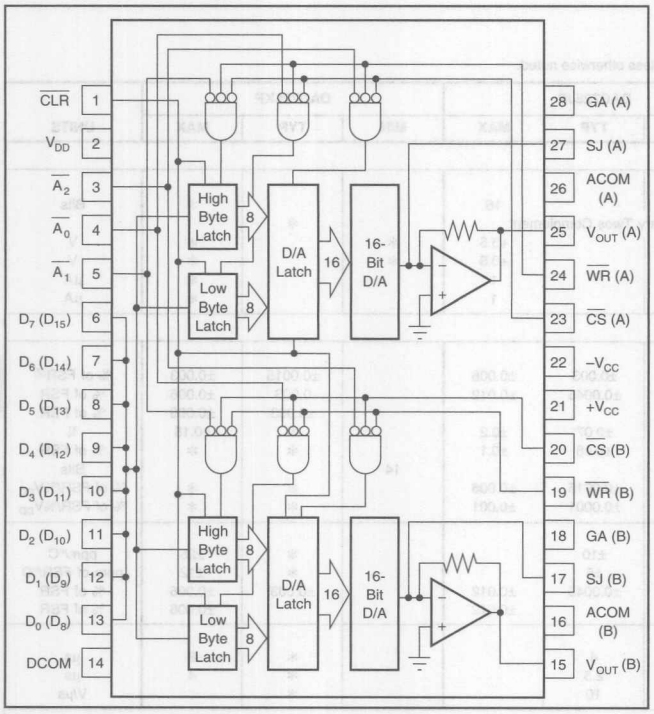
| PARAMETER | DAC725JP MIN | DAC725JP TYP | DAC725JP MAX | DAC725KP MIN | DAC725KP TYP | DAC725KP MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | |
| **DIGITAL INPUT** | | | | | | | |
| Resolution | | | 16 | | | * | Bits |
| Bipolar Input Code | | Binary Twos Complement | | | * | | |
| Logic Levels[1]: $V_{IH}$ | +2 | | +5.5 | * | | * | V |
| $V_{IL}$ | –1 | | +0.8 | * | | * | V |
| $I_{IH}$ ($V_I$ = +2.7V) | | | 1 | | | * | µA |
| $I_{IL}$ ($V_I$ = +0.4V) | | | 1 | | | * | µA |
| **TRANSFER CHARACTERISTICS** | | | | | | | |
| **ACCURACY** | | | | | | | |
| Linearity Error | | ±0.003 | ±0.006 | | ±0.0015 | ±0.003 | % of FSR[2] |
| Differential Linearity Error[3] | | ±0.0045 | ±0.012 | | 0.003 | ±0.006 | % of FSR |
| At Bipolar Zero: KP[3, 4] | | | | | ±0.003 | ±0.006 | % of FSR |
| Gain Error[5] | | ±0.07 | ±0.2 | | * | ±0.15 | % |
| Bipolar Zero Error[5] | | ±0.05 | ±0.1 | | * | * | % of FSR |
| Montonicity Over Specified Temp. Range | 13 | | | 14 | | | Bits |
| Power Supply Sensitivity: $+V_{CC}$, $-V_{CC}$ | | ±0.0015 | ±0.006 | | * | * | % of FSR/%$V_{CC}$ |
| $V_{DD}$ | | ±0.0001 | ±0.001 | | * | * | % of FSR/%$V_{DD}$ |
| **DRIFT** (Over Specified Temperature Range) | | | | | | | |
| Gain Drift | | ±10 | | | * | ±25 | ppm/°C |
| Bipolar Zero Drift | | ±5 | | | * | ±12 | ppm of FSR/°C |
| Differential Linearity Over Temperature[3] | | ±0.0045 | ±0.012 | | ±0.003 | ±0.006 | % of FSR |
| Linearity Error Over Temperature[3] | | | ±0.012 | | | ±0.006 | % of FSR |
| **SETTLING TIME** (to ±0.003% of FSR)[6] | | | | | | | |
| 20V Step (2kΩ load) | | 4 | | | * | 8 | µs |
| 1LSB Step at Worst-Case Code[7] | | 2.5 | | | * | 4 | µs |
| Slew Rate | | 10 | | | * | | V/µs |
| **OUTPUT** | | | | | | | |
| Output Voltage Range[8] | ±10 | | | * | | | V |
| Output Current | ±5 | | | * | | | mA |
| Output Impedance | | 0.15 | | | * | | Ω |
| Short Circuit to Common Duration | | Indefinite | | | * | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | |
| Voltage: $+V_{CC}$ | +11.4 | +15 | +16.5 | * | * | * | V |
| $-V_{CC}$ | –11.4 | –15 | –16.5 | * | * | * | V |
| $V_{DD}$ | +4.5 | +5 | +5.5 | * | * | * | V |
| Current (No load, ±15V supplies): $+V_{CC}$ | | +29 | +35 | | * | * | mA |
| $-V_{CC}$ | | –35 | –40 | | * | * | mA |
| $V_{DD}$ | | +6 | +10 | | * | * | mA |
| Power Dissipation (±15V supplies) | | 920 | 1175 | | * | * | mW |
| **TEMPERATURE RANGE** | | | | | | | |
| Specification | 0 | | +70 | * | | * | °C |
| Storage | –60 | | +150 | * | | * | °C |

* Specification same as DAC725JP.

NOTES: (1) Digital inputs are TTL, LSTTL, 54/74HC and 54/74HTC compatible over the specification temperature range. (2) FSR means Full-Scale Range. For example, for ±10V output, FSR = 20V. (3) ±0.0015% of FSR is equal to 1LSB in 16-bit resolution. ±0.003% of FSR is equal to 1LSB in 15-bit resolution. ±0.006% of FSR is equal to 1LSB in 14-bit resolution. (4) Error at input code $0000_H$ (BTC). (5) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point. (6) Maximum represents the 3σ limit. Not tested for this parameter. (7) The bipolar worst-case code change is $FFFF_H$ to $0000_H$ (BTC). (8) Minimum supply voltage for ±10V output swing is approximately ±13V. Output swing for ±12V supplies is at least ±9V.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## CONNECTION DIAGRAM




## PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | CLR | Clear line. Sets the D/A register to $0000_{HEX}$, which gives bipolar zero on the D/A output. |
| 2 | $V_{DD}$ | Logic supply (+5V). |
| 3 | $\overline{A_2}$ | Latch enable for D/A latch (active low). |
| 4 | $\overline{A_0}$ | Latch enable for "low byte" input (active low). |
| 5 | $\overline{A_1}$ | Latch enable for "high byte" input (active low). |
| 6 | $D_7$ ($D_{15}$) (MSB) | Input for data bit 7 if enabling low byte (LB) latch, or data bit 15 if enabling the high byte (HB) latch. |
| 7 | $D_6$ ($D_{14}$) | Input for data bit 6 if enabling LB latch, or data bit 14 if enabling HB latch. |
| 8 | $D_5$ ($D_{13}$) | Data bit 5 (LB) or data bit 13 (HB). |
| 9 | $D_4$ ($D_{12}$) | Data bit 4 (LB) or data bit 12 (HB). |
| 10 | $D_3$ ($D_{11}$) | Data bit 3 (LB) or data bit 11 (HB). |
| 11 | $D_2$ ($D_{10}$) | Data bit 2 (LB) or data bit 10 (HB). |
| 12 | $D_1$ ($D_9$) | Data bit 1 (LB) or data bit 9 (HB). |
| 13 | $D_0$ ($D_8$) | Data bit 0 (LB) or data bit 8 (HB). |
| 14 | DCOM | Digital common. |
| 15 | $V_{OUT}$ (B) | Voltage output for DAC B. |
| 16 | ACOM (B) | Analog common for DAC B. |
| 17 | SJ (B) | Summing junction of the internal op amp for DAC B. |
| 18 | GA (B) | Gain adjust pin for DAC B. |
| 19 | $\overline{WR}$ (B) | Write control line for DAC B. |
| 20 | $\overline{CS}$ (B) | Chip select control line for DAC B. |
| 21 | $+V_{CC}$ | Positive supply voltage (+15V). |
| 22 | $-V_{CC}$ | Negative supply voltage (–15V). |
| 23 | $\overline{CS}$ (A) | Chip select control line for DAC A. |
| 24 | $\overline{WR}$ (A) | Write control line for DAC A. |
| 25 | $V_{OUT}$ (A) | Voltage output for DAC A. |
| 26 | ACOM (A) | Analog common for DAC A. |
| 27 | SJ (A) | Summing junction of the internal op amp for DAC A. |
| 28 | GA (A) | Gain adjust pin for DAC A. |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $V_{DD}$ to COMMON | 0V, +15V |
| $+V_{CC}$ to COMMON | 0V, +18V |
| $-V_{CC}$ to COMMON | 0V, –18V |
| Digital Data Inputs to COMMON | –0.5V, $V_{DD}$ + 0.5 |
| DC Current any Input | ±10mA |
| Reference Out to COMMON | Indefinite Short to COMMON |
| $V_{OUT}$ | Indefinite Short to COMMON |
| External Voltage Applied to $R_F$ | ±18V |
| External Voltage Applied to D/A Output | ±5V |
| Power Dissipation | 2000mW |
| Storage Temperature | –60°C to +150°C |
| Lead Temperature (soldering, 10s) | 300°C |

NOTE: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

| PRODUCT | LINEARITY ERROR max (% of FSR) | TEMPERATURE RANGE |
|---|---|---|
| DAC725JP | ±0.012 | 0°C to +70°C |
| DAC725KP | ±0.006 | 0°C to +70°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| DAC725JP | 28-Pin Plastic DIP | 215 |
| DAC725KP | 28-Pin Plastic DIP | 215 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR-BROWN®



# DAC729

www.burr-brown.com/databook/DAC729.html



# Ultra-High Resolution 18-BIT DIGITAL-TO-ANALOG CONVERTER

## FEATURES

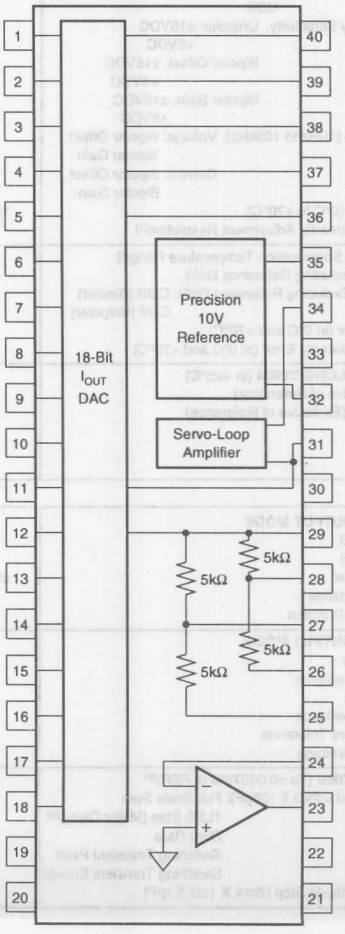
- 16-BIT LINEARITY GUARANTEED (K Grade)
- USER ADJUSTABLE TO 18-BIT LINEARITY
- PRECISION INTERNAL REFERENCE
- FAST SETTLING, LOW NOISE INTERNAL OP AMP
- LOW DRIFT
- HERMETIC 40-PIN CERAMIC PACKAGE
- $I_{OUT}$ OR $V_{OUT}$ OPERATION

## DESCRIPTION

The DAC729 sets the standard in very high accuracy digital-to-analog conversion. It is supplied from the factory at a guaranteed linearity of 16 bits, and is user-adjustable to 18-bit linearity (1LSB = FSR/262144).

To attain this high level of accuracy, the design takes advantage of Burr-Brown's thin-film monolithic DAC process, dielectric op amp process, hybrid capabilities, and advanced test and laser-trim techniques.

The DAC729 hybrid layout is specifically partitioned to minimize the effects of external load-current-induced thermal errors. The op amp design consists of a fast settling precision op amp with a current buffer within the feedback loop. This buffer isolates the load from the precision op amp, which results in a fast settling (8µs to 16 bits) output. The standard 40-pin package offers full hermeticity, contributing to the excellent reliability of the DAC729.




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## ELECTRICAL

At $T_A$ = +25°C, $V_{CC}$ = ±15V, $V_{DD}$ = +5V, using internal reference op amp, unless otherwise noted. COB = ±10V FSR, CSB = 0V to +10V FSR.

| PARAMETER | DAC729JH MIN | DAC729JH TYP | DAC729JH MAX | DAC729KH MIN | DAC729KH TYP | DAC729KH MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DIGITAL INPUT** | | | | | | | |
| Resolution | | 18 | | | * | | Bits |
| Digital Inputs[1]: $V_{IH}$ | +2.4 | | $+V_L$ | * | | * | V |
| $V_{IL}$ | 0 | | +0.8 | * | | * | V |
| $I_{IH}$, $V_{IN}$ = +2.7V | | | +5 | | | * | µA |
| $I_{IL}$, $V_{IN}$ = +0.4V | | | –300 | | | * | µA |
| **TRANSFER CHARACTERISTICS[2]** | | | | | | | |
| **ACCURACY** | | | | | | | |
| Linearity Error[3] | | | ±0.0015 | | | ±0.00076 | % of FSR[4] |
| Differential Linearity Error | | | ±0.003 | | | ±0.0015 | % of FSR |
| Gain Error[5] | | ±0.05 | ±0.10 | | * | * | % |
| Offset Error:[5]Voltage, COB[6] | | ±5 | ±10 | | * | * | mV |
| CSB[6] | | ±3 | ±5 | | * | * | mV |
| Current, COB | | | ±5 | | | * | µA |
| CSB | | | ±1 | | | * | µA |
| Power Supply Sensitivity, Unipolar: ±15VDC | | ±0.0001 | ±0.0005 | | * | * | % of FSR/%$V_S$ |
| +5VDC | | ±0.0001 | ±0.0005 | | * | * | % of FSR/%$V_S$ |
| Bipolar Offset: ±15VDC | | ±0.0004 | ±0.0015 | | * | * | % of FSR/%$V_S$ |
| +5VDC | | ±0.0001 | ±0.0005 | | * | * | % of FSR/%$V_S$ |
| Bipolar Gain: ±15VDC | | ±0.0005 | ±0.0015 | | * | * | % of FSR/%$V_S$ |
| +5VDC | | ±0.0001 | ±0.0005 | | * | * | % of FSR/%$V_S$ |
| Output Noise (10Hz to 100kHz), Voltage: Bipolar Offset | | 29 | | | * | | µVrms |
| Bipolar Gain | | 37 | | | * | | µVrms |
| Current: Bipolar Offset | | 2.9 | | | * | | nArms |
| Bipolar Gain | | 3 | | | * | | nArms |
| Monotonicity (0°C to +70°C) | 15 | 16 | | 16 | 17 | | Bits |
| Differential Linearity Adjustment Resolution[7] | | 18 | | | * | | Bits |
| **DRIFT** (Over Specification Temperature Range) | | | | | | | |
| Gain Drift (Excluding Reference Drift) | | ±3 | ±5 | | * | * | ppm/°C |
| Offset Drift (Excluding Reference Drift): COB (Bipolar) | | ±2 | ±5 | | * | * | ppm of FSR/°C |
| CSB (Unipolar) | | ±2 | ±3 | | * | * | ppm of FSR/°C |
| Linearity Error (at 0°C and +70°C) | | ±0.3 | ±1 | | ±0.3 | ±0.5 | ppm of FSR/°C |
| Differential Linearity Error (at 0°C and +70°C) | | ±0.5 | ±2 | | ±0.5 | ±1 | ppm of FSR/°C |
| **STABILITY, LONG TERM** (at +25°C) | | | | | | | |
| Gain (Exclusive of Reference) | | ±5 | | | ±5 | | ppm/1000hr |
| Offset: COB (Exclusive of Reference) | | ±5 | | | ±5 | | ppm of FSR/1000hr |
| CSB | | ±5 | | | ±5 | | ppm of FSR/1000hr |
| Linearity | | ±2 | | | ±2 | | ppm of FSR/1000hr |
| Reference | | ±5 | | | ±5 | | ppm/1000hr |
| **OUTPUT** | | | | | | | |
| **VOLTAGE OUTPUT MODE** | | | | | | | |
| Ranges: COB | | ±2.5, ±5, ±10 | | | * | | V |
| CSB | | 0 to +10, 0 to +5 | | | * | | V |
| Output Current | ±5 | | | * | | | mA |
| Output Impedance | | 0.15 | | | * | | Ω |
| Short Circuit Duration | | Indefinite to Common | | | Indefinite to Common | | |
| **CURRENT OUTPUT MODE** | | | | | | | |
| COB Ranges | | ±1 | | | * | | mA |
| Output Impedance | | 2.86 | | | * | | kΩ |
| CSB Ranges | | 0 to –2 | | | * | | mA |
| Output Impedance | | 4.0 | | | * | | kΩ |
| Output Current Tolerance | | | ±0.1 | | | * | % of FSR |
| Compliance Voltage | | –1 to +5 | | | * | | V |
| **SETTLING TIME** (To ±0.00076% of FSR)[8] | | | | | | | |
| Voltage (Load = 2kΩ ll 100pF): Full-Scale Step | | 5 | 8 | | * | * | µs |
| 1LSB Step (Major Carry)[9] | | 4 | 7 | | * | * | µs |
| Slew Rate | | 20 | | | * | | V/µs |
| Switching Transient Peak | | 500 | | | * | | mV |
| Switching Transient Energy | | 0.45 | | | * | | V-µs |
| Current Full-Scale Step (2mA X 10Ω ll 1pF) | | 300 | | | * | | ns |

# SPECIFICATIONS (CONT)

## ELECTRICAL

At $T_A$ = +25°C, $V_{CC}$ = ±15V, $V_{DD}$ = +5V, using internal reference op amp, unless otherwise noted. COB = ±10V FSR, CSB = 0V to +10V FSR.

| PARAMETER | DAC729JH MIN | DAC729JH TYP | DAC729JH MAX | DAC729KH MIN | DAC729KH TYP | DAC729KH MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **REFERENCE** | | | | | | | |
| Output (pin 32) : Voltage | +9.990 | +10.000 | +10.010 | * | * | * | V |
| Source Current[10] | | | +4 | | | * | mA |
| Temperature Coefficient | | ±2 | ±4 | | * | * | ppm/°C |
| Short-Circuit Duration | | Indefinite to Common | | | Indefinite to Common | | |
| Power Supply Sensitivity | | 0.00025 | 0.003 | | * | * | %/V |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | |
| Voltage: $+V_{CC}$ | +13.5 | +15 | +16.5 | * | * | * | V |
| $-V_{CC}$ | −16.5 | −15 | −13.5 | * | * | * | V |
| $V_{DD}$ | +4.75 | +5 | +5.25 | * | * | * | V |
| Current: $+V_{CC}$ | | +30 | +40 | | * | * | mA |
| $-V_{CC}$ | | −45 | −60 | | * | * | mA |
| $V_{DD}$ | | +18 | +25 | | * | * | mA |
| Power Dissipation (Rated Supplies) | | 1.22 | 1.63 | | * | * | W |
| **ENVIRONMENTAL SPECIFICATIONS** | | | | | | | |
| Temperature Range: Specification | 0 | | +70 | * | | * | °C |
| Storage | −60 | | +150 | * | | * | °C |

* Specifications same as DAC729JH.

NOTES: (1) TTL- and CMOS-compatible. (2) Specified for $V_{OUT}$ mode using the internal op amp. (3) ±0.00076% of full-scale range is 1/2LSB for 16-bit resolution. (4) FSR means full-scale range, 20V for ±10V range, etc. (5) Adjustable to zero error with an external potentiometer. (6) COB is complementary offset binary (bipolar); CSB is complementary straight binary (unipolar). (7) Using the MSB adjustment circuit, the user may improve the DAC linearity to 1/2LSB of this specification with gain and offset errors adjusted to zero at 25°C. (8) Maximum represents 3σ limit, not 100% production tested. (9) At the major carry; 20000 to $1FFFF_{HEX}$ and from 1FFFF to $20000_{HEX}$. (10) Maximum with no degradation in specifications. External loads must be constant.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| $V_{DD}$ to Common | 0V to +7V |
| $+V_{CC}$ to Common | 0V to +18V |
| $-V_{CC}$ to Common | 0V to −18V |
| Digital Data Inputs (pins 1-18) to Common | −0.5V to $V_{DD}$ |
| Reference Voltage In (pin 31) | +9V to +11V |
| Reference Out (pin 32) to Common | Indefinite Short to Common |
| External Voltage Applied to D/A Output (pin 29) | −5V to +5V |
| External Voltage Applied to Feedback Resistors (pins 25, 26, 27, 28) | −15V to +15V |
| $V_{OUT}$ (pin 23) | Indefinite Short to Common |
| Power Dissipation | 3000mW |
| Storage Temperature | −60°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## PACKAGE/ORDERING INFORMATION

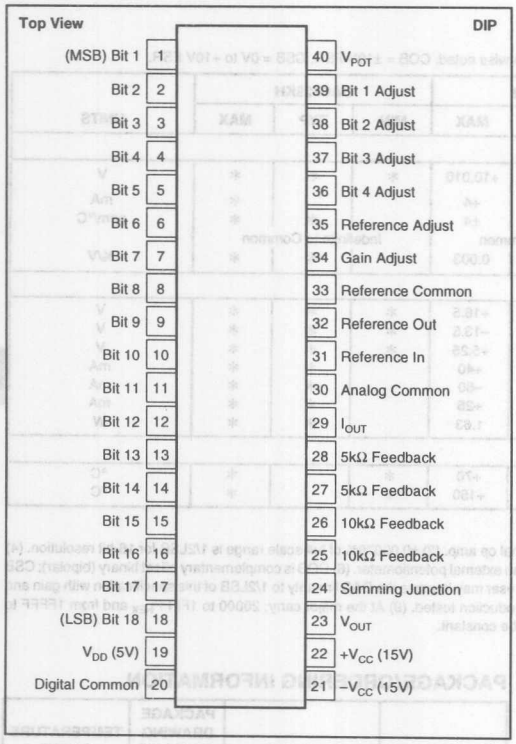
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| DAC729JH | 40-Pin Hermetic DIP | 214 | 0°C to +70°C |
| DAC729KH | 40-Pin Hermetic DIP | 214 | 0°C to +70°C |
| DAC729KH-BI | 40-Pin Hermetic DIP | 214 | 0°C to +70°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



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## PIN CONNECTIONS

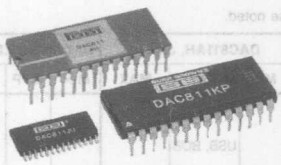



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®




# DAC811

www.burr-brown.com/databook/DAC811.html



# Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER

## FEATURES

- SINGLE INTEGRATED CIRCUIT CHIP
- MICROCOMPUTER INTERFACE: DOUBLE-BUFFERED LATCH
- VOLTAGE OUTPUT: ±10V, ±5V, +10V
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- ±1/2LSB MAXIMUM NONLINEARITY OVER TEMPERATURE
- GUARANTEED SPECIFICATIONS AT ±12V AND ±15V SUPPLIES
- TTL/5V CMOS-COMPATIBLE LOGIC INPUTS

## DESCRIPTION

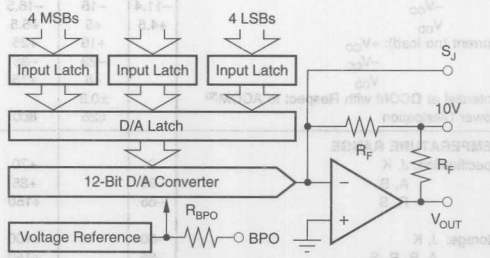
The DAC811 is a complete, single-chip integrated-circuit, microprocessor-compatible, 12-bit digital-to-analog converter. The chip combines a precision voltage reference, microcomputer interface logic, and double-buffered latch, in a 12-bit D/A converter with a voltage output amplifier. Fast current switches and a laser-trimmed thin-film resistor network provide a highly accurate and fast D/A converter.

Microcomputer interfacing is facilitated by a double-buffered latch. The input latch is divided into three 4-bit nibbles to permit interfacing to 4-, 8-, 12-, or 16-bit buses and to handle right-or left-justified data. The 12-bit data in the input latches is transferred to the D/A latch to hold the output value.

Input gating logic is designed so that loading the last nibble or byte of data can be accomplished simultaneously with the transfer of data (previously stored in adjacent latches) from adjacent input latches to the D/A latch. This feature avoids spurious analog output values while using an interface technique that saves computer instructions.

The DAC811 is laser trimmed at the wafer level and is specified to ±1/4LSB maximum linearity error (B, K, and S grades) at 25°C and ±1/2LSB maximum over the temperature range. All grades are guaranteed monotonic over the specification temperature range.

The DAC811 is available in six performance grades and three package types. DAC811J and K are specified over the temperature ranges of 0°C to +70°C; DAC811A and B are specified over –25°C to +85°C; DAC811R and S are specified over –55°C to +125°C. DAC811J and K are packaged in a reliable 28-pin plastic DIP or plastic SOIC package, while DAC811A, B, R and S are available in a 28-pin 0.6" wide dual-inline hermetically sealed ceramic side-brazed package (H package).




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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C. $\pm V_{CC}$ = 12V or 15V, unless otherwise noted.

| PARAMETER | DAC811AH, JP, JU | | | DAC811BH, KP, KU | | | DAC811RH | | | DAC811SH | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **DIGITAL INPUT** | | | | | | | | | | | | | |
| Resolution | | | 12 | | | * | | | * | | | * | Bits |
| Codes[1] | | USB, BOB | | | * | | | * | | | * | | |
| Digital Inputs Over Temperature Range[2] | | | | | | | | | | | | | |
| $V_{IH}$ | +2 | | +15 | * | | * | * | | * | * | | * | VDC |
| $V_{IL}$ | 0 | | +0.8 | * | | * | * | | * | * | | * | VDC |
| $I_{IH}$, $V_I$ = +2.7V | | | +10 | | | * | | | * | | | * | µA |
| $I_{IL}$, $V_I$ = +0.4V | | | ±20 | | | * | | | * | | | * | µA |
| Digital Interface Timing Over Temperature Range | | | | | | | | | | | | | |
| $t_{WP}$, $\overline{WR}$ Pulse Width | 50 | | | * | | | * | | | * | | | ns |
| $t_{AW}$1, $N_X$ and $\overline{LDAC}$ Valid to End of $\overline{WR}$ | 50 | | | * | | | * | | | * | | | ns |
| $t_{DW}$, Data Valid to End of $\overline{WR}$ | 80 | | | * | | | * | | | * | | | ns |
| $t_{DH}$, Data Valid Hold Time | 0 | | | * | | | +10 | | | * | | | ns |
| **ACCURACY** | | | | | | | | | | | | | |
| Linearity Error | | ±1/4 | ±1/2 | | ±1/8 | ±1/4 | | ±1/4 | ±1/2 | | ±1/8 | ±1/4 | LSB |
| Differential Linearity Error | | ±1/2 | ±3/4 | | ±1/4 | ±1/2 | | ±1/2 | ±3/4 | | ±1/4 | ±1/2 | LSB |
| Gain Error[3] | | ±0.1 | ±0.2 | | * | * | | * | * | | * | * | % |
| Offset Error[3, 4] | | ±0.05 | ±0.15 | | * | * | | * | * | | * | * | % of FSR[5] |
| Monotonicity | | Guaranteed | | | * | | | * | | | * | | |
| Power Supply Sensitivity: $+V_{CC}$ | | ±0.001 | ±0.003 | | * | * | | * | * | | * | * | % of FSR/%$V_{CC}$ |
| $-V_{CC}$ | | ±0.002 | ±0.006 | | * | * | | * | * | | * | * | % of FSR/%$V_{CC}$ |
| $V_{DD}$ | | ±0.0005 | ±0.0015 | | * | * | | * | * | | * | * | % of FSR/%$V_{DD}$ |
| **DRIFT** (Over Specification Temperature Range) | | | | | | | | | | | | | |
| Gain | | ±10 | ±30 | | ±10 | ±20 | | ±15 | ±30 | | ±15 | ±30 | ppm/°C |
| Unipolar Offset | | ±5 | ±10 | | ±5 | ±7 | | ±5 | ±10 | | ±5 | ±7 | ppm of FSR/°C |
| Bipolar Zero | | ±5 | ±10 | | ±5 | ±7 | | ±5 | ±10 | | ±5 | ±7 | ppm of FSR/°C |
| Linearity Error Over Temperature Range | | ±1/2 | ±3/4 | | ±1/4 | ±1/2 | | ±1/2 | ±3/4 | | ±1/4 | ±1/2 | LSB |
| Monotonicity Over Temperature Range | | Guaranteed | | | * | | | * | | | * | | |
| **SETTLING TIME**[6] (to within ±0.01% of FSR of Final Value; 2kΩ load) | | | | | | | | | | | | | |
| For Full Scale Range Change, 20V Range | | 3 | 4 | | * | * | | * | * | | * | * | µs |
| 10V Range | | 3 | 4 | | * | * | | * | * | | * | * | µs |
| For 1LSB Change at Major Carry[7] | | 1 | | | * | | | * | | | * | | µs |
| Slew Rate[6] | 8 | 12 | | * | * | | * | * | | * | * | | V/µs |
| **ANALOG OUTPUT** | | | | | | | | | | | | | |
| Voltage Range ($\pm V_{CC}$ = 15V)[8]: Unipolar | | 0 to +10 | | | * | | | * | | | * | | V |
| Bipolar | | ±5, ±10 | | | * | | | * | | | * | | V |
| Output Current | ±5 | | | * | | | * | | | * | | | mA |
| Output Impedance (at DC) | | 0.2 | | | * | | | * | | | * | | Ω |
| Short Circuit to Common Duration | | Indefinite | | | * | | | * | | | * | | |
| **REFERENCE VOLTAGE** | | | | | | | | | | | | | |
| Voltage | +6.2 | +6.3 | +6.4 | * | * | * | * | * | * | * | * | * | V |
| Source Current Available for External Loads | +2 | | | * | | | * | | | * | | | mA |
| Temperature Coefficient | | ±10 | ±30 | | ±10 | ±20 | | ±10 | ±30 | | ±10 | ±20 | ppm/°C |
| Short Circuit to Common Duration | | Indefinite | | | * | | | * | | | * | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | | | | | | |
| Voltage: $+V_{CC}$ | +11.4 | +15 | +16.5 | * | * | * | * | * | * | * | * | * | VDC |
| $-V_{CC}$ | −11.4 | −15 | −16.5 | * | * | * | * | * | * | * | * | * | VDC |
| $V_{DD}$ | +4.5 | +5 | +5.5 | * | * | * | * | * | * | * | * | * | VDC |
| Current (no load): $+V_{CC}$ | | +16 | +25 | | * | * | | * | * | | * | * | mA |
| $-V_{CC}$ | | −23 | −35 | | * | * | | * | * | | * | * | mA |
| $V_{DD}$ | | +8 | +15 | | * | * | | * | * | | * | * | mA |
| Potential at DCOM with Respect to ACOM[9] | | ±0.5 | | | * | | | * | | | * | | V |
| Power Dissipation | | 625 | 800 | | * | * | | * | * | | * | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | | | | | | |
| Specification: J, K | 0 | | +70 | * | | * | * | | * | * | | * | °C |
| A, B | −25 | | +85 | * | | * | * | | * | * | | * | °C |
| R, S | −65 | | +150 | * | | * | * | | * | * | | * | °C |
| | | | | | | | −55 | | +125 | * | | * | °C |
| Storage: J, K | −60 | | +100 | * | | * | * | | * | * | | * | °C |
| A, B, R, S | −65 | | +150 | * | | * | * | | * | * | | * | °C |

* Specification same as model to immediate left.

NOTES: (1) USB = unipolar straight binary; BOB = bipolar offset binary. (2) TTL, LSTTL and 54/74 HC compatible. (3) Adjustable to zero with external trim potentiometer. (4) Error at input code $000_{16}$ for both unipolar and bipolar ranges. (5) FSR means full scale range and is 20V for the ±10V range. (6) Maximum represents the 3σ limit. Not 100% tested for this parameter. (7) At the major carry, $7FF_{16}$ to $800_{16}$ and $800_{16}$ to $7FF_{16}$. (8) Minimum supply voltage required for ±10V output swing is ±13.5V. Output swing for ±11.4V supplies is at least −8V to +8V. (9) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

## PIN DESCRIPTIONS

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | $+V_{DD}$ | Logic supply, +5V. |
| 2 | $\overline{WR}$ | Write, command signal to load latches. Logic low loads latches. |
| 3 | $\overline{LDAC}$ | Load D/A converter, enables $\overline{WR}$ to load the D/A latch. Logic low enables. |
| 4 | $\overline{N_A}$ | Nibble A, enables $\overline{WR}$ to load input latch A (the most significant nibble). Logic low enables. |
| 5 | $\overline{N_B}$ | Nibble B, enables $\overline{WR}$ to load input latch B. Logic low enables. |
| 6 | $\overline{N_C}$ | Nibble C, enables $\overline{WR}$ to load input latch C (the least significant nibble). Logic low enables. |
| 7 | $D_{11}$ | Data bit 12, MSB, positive true. |
| 8 | $D_{10}$ | Data bit 11. |
| 9 | $D_9$ | Data bit 10. |
| 10 | $D_8$ | Data bit 9. |
| 11 | $D_7$ | Data bit 8. |
| 12 | $D_6$ | Data bit 7. |
| 13 | $D_5$ | Data bit 6. |
| 14 | $D_4$ | Data bit 5. |
| 15 | DCOM | Digital common, $V_{DD}$ supply return. |
| 16 | $D_0$ | Data bit 1, LSB. |
| 17 | $D_1$ | Data bit 2. |
| 18 | $D_2$ | Data bit 3. |
| 19 | D3 | Data bit 4. |
| 20 | $+V_{CC}$ | Analog supply input, +15V or +12V. |
| 21 | $-V_{CC}$ | Analog supply input, –15V or –12V. |
| 22 | Gain Adj | To externally adjust gain. |
| 23 | ACOM | Analog common, $\pm V_{cc}$ supply return. |
| 24 | $V_{OUT}$ | D/A converter voltage output. |
| 25 | 10V Range | Connect to pin 24 for 10V range. |
| 26 | SJ | Summing junction of output amplifier. |
| 27 | BPO | Bipolar offset. Connect to pin 26 for bipolar operation. |
| 28 | Ref Out | 6.3V reference output. |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_{CC}$ | 0 to +18V |
| $-V_{CC}$ to ACOM | 0 to –18V |
| $V_{DD}$ to DCOM | 0 to +7V |
| $V_{DD}$ to ACOM | ±7V |
| ACOM to DCOM | ±7V |
| Digital Inputs (Pins 2–14, 16–19) to DCOM | –0.4V to +18V |
| External Voltage Applied to 10V Range Resistor | ±12V |
| Ref Out | Indefinite Short to ACOM |
| External Voltage Applied to DAC Output | –5V to +5V |
| Power Dissipation | 1000mW |
| Lead Temperature (soldering, 10s) | +300°C |
| Max Junction Temperature | +165°C |
| Thermal Resistance, $\theta_{J-A}$: Plastic DIP and SOIC | 100°C/W |
| Ceramic DIP | 65°C/W |

NOTE: Stresses above those listed above may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

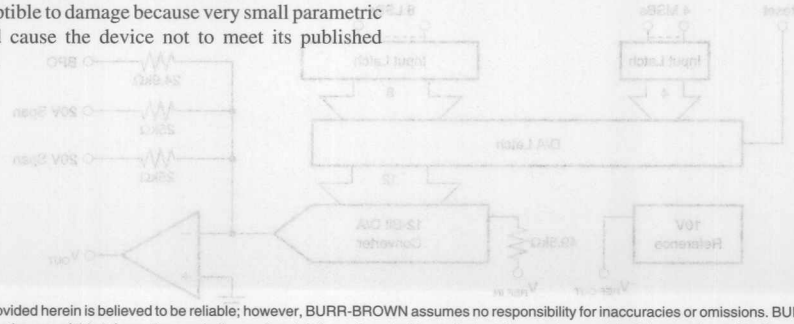
## ORDERING INFORMATION

| PRODUCT | PACKAGE | TEMPERATURE RANGE (°C) | LINEARITY ERROR, MAX AT +25°C | GAIN DRIFT (ppm/°C) |
|---|---|---|---|---|
| DAC811JP | Plastic DIP | 0 to +70 | ±1/2LSB | 30 |
| DAC811JU | Plastic SOIC | 0 to +70 | ±1/2LSB | 30 |
| DAC811KP | Plastic DIP | 0 to +70 | ±1/4LSB | 15 |
| DAC811KU | Plastic SOIC | 0 to +70 | ±1/4LSB | 15 |
| DAC811AH | Ceramic DIP | –25 to +85 | ±1/2LSB | 30 |
| DAC811BH | Ceramic DIP | –25 to +85 | ±1/4LSB | 15 |
| DAC811RH | Ceramic DIP | –55 to +125 | ±1/2LSB | 30 |
| DAC811SH | Ceramic DIP | –55 to +125 | ±1/4LSB | 20 |

## PACKAGE INFORMATION

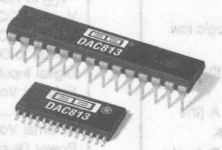
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| DAC811AH | 28-Pin Side-Brazed DIP | 149 |
| DAC811BH | 28-Pin Side-Brazed DIP | 149 |
| DAC811RH | 28-Pin Side-Brazed DIP | 149 |
| DAC811SH | 28-Pin Side-Brazed DIP | 149 |
| DAC811JP | 28-Pin Plastic DIP | 215 |
| DAC811KP | 28-Pin Plastic DIP | 215 |
| DAC811JU | 28-Pin SOIC | 217 |
| DAC811KU | 28-Pin SOIC | 217 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



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# DAC813

www.burr-brown.com/databook/DAC813.html

# Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER

## FEATURES

- ±1/2LSB NONLINEARITY OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- LOW POWER: 270mW typ
- DIGITAL INTERFACE DOUBLE BUFFERED: 12 AND 8 + 4 BITS
- SPECIFIED AT ±12V AND ±15V POWER SUPPLIES
- RESET FUNCTION TO BIPOLAR ZERO
- 0.3" WIDE DIP AND SO PACKAGES

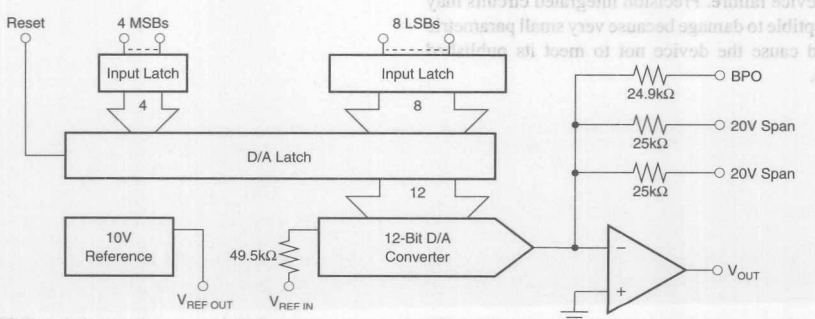
## DESCRIPTION

The DAC813 is a complete monolithic 12-bit digital-to-analog converter with a flexible digital interface. It includes a precision +10V reference, interface control logic, double-buffered latch and a 12-bit D/A converter with voltage output operational amplifier. Fast current switches and laser-trimmed thin-film resistors provide a highly accurate, fast D/A converter.

Digital interfacing is facilitated by a double buffered latch. The input latch consists of one 8-bit byte and one 4-bit nibble to allow interfacing to 8-bit (right justified format) or 16-bit data buses. Input gating logic is designed so that the last nibble or byte to be loaded can be loaded simultaneously with the transfer of data to the D/A latch saving computer instructions.

A reset control allows the DAC813 D/A latch to asynchronously reset the D/A output to bipolar zero, a feature useful for power-up reset, recalibration, or for system re-initialization upon system failure.

The DAC813 is specified to ±1/2LSB maximum linearity error (J, A grades) and ±1/4LSB (K grade). It is packaged in 28-pin 0.3" wide plastic DIP and 28-lead plastic SOIC




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# SPECIFICATIONS

At $T_A$ = +25°C, $\pm V_{CC}$ = ±12V or ±15V and load on $V_{OUT}$ = 5kΩ II 500pF to common, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC813JP, JU, AU | | | DAC813KP, KU | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **DIGITAL INPUTS** | | | | | | | | |
| Resolution | | | | 12 | | * | | Bits |
| Codes(1) | | | USB, BOB | | | * | | |
| Digital Inputs Over Temperature Range(2) | | | | | | | | |
| $V_{IH}$(3) | | +2 | | +5.5 | * | | * | VDC |
| $V_{IL}$ | | 0 | | +0.8 | * | | * | VDC |
| DATA Bits, $\overline{WR}$, $\overline{Reset}$, $\overline{LDAC}$, $\overline{LMSB}$, $\overline{LLSB}$ | | | | ±10 | | | * | µA |
| $I_{IH}$ | $V_{IN}$ = +2.7V | | | ±10 | | | * | µA |
| $I_{IL}$ | $V_{IN}$ = +0.4V | | | | | | | |
| **ACCURACY** | | | | | | | | |
| Linearity Error | | | ±1/4 | ±1/2 | | ±1/8 | ±1/4 | LSB |
| Differential Linearity Error | | | ±1/2 | ±3/4 | | ±1/4 | ±1/2 | LSB |
| Gain Error(4) | | | ±0.05 | ±0.2 | | * | * | % |
| Unipolar Offset Error(5) | | | ±0.01 | ±0.02 | | * | * | % of FSR(7) |
| Bipolar Zero Error(6) | | | ±0.02 | ±0.2 | | * | * | % of FSR |
| Monotonicity | | | Guaranteed | | | * | | |
| Power Supply Sensitivity: $+V_{CC}$ | 20V Range | | 5 | 10 | | * | * | ppm of FSR/% |
| $-V_{CC}$ | | | 1 | 10 | | * | * | ppm of FSR/% |
| **DRIFT** | Over Specification | | | | | | | |
| Gain | Temperature Range | | ±5 | ±30 | | * | ±15 | ppm/°C |
| Unipolar Offset | | | ±1 | ±3 | | * | ±3 | ppm of FSR/°C |
| Bipolar Zero | | | ±3 | ±10 | | * | ±5 | ppm of FSR/°C |
| Linearity Error Over Temperature Range | | | ±1/2 | ±3/4 | | ±1/4 | ±1/2 | LSB |
| Monotonicity Over Temperature Range | | | Guaranteed | | | * | | |
| **SETTLING TIME**(8) (To Within ±0.01% of FSR of Final Value; 5kΩ II 500pF load) | | | | | | | | |
| For Full Scale Range Change | 20V Range | | 4.5 | 6 | | * | * | µs |
| | 10V Range | | 3.3 | 5 | | * | * | µs |
| For 1LSB Change at Major Carry(9) | | | 2 | | | * | | µs |
| Slew Rate | | | 10 | | | * | | V/µs |
| **ANALOG OUTPUT** | | | | | | | | |
| Voltage Range: Unipolar | $\pm V_{CC}$ > ±11.4V | | 0 to +10 | | | * | | V |
| Bipolar | $\pm V_{CC}$ > ±11.4V | | ±5, ±10 | | | * | | V |
| Output Current | | ±5 | | | * | | | mA |
| Output Impedance | At DC | | 0.2 | | | * | | Ω |
| Short Circuit to Common Duration | | | Indefinite | | | * | | |
| **REFERENCE VOLTAGE** | | | | | | | | |
| Voltage | | +9.95 | +10 | +10.05 | * | * | * | V |
| Source Current Available for External Loads | | 5 | | | * | | | mA |
| Impedance | | | 2 | | | * | | Ω |
| Temperature Coefficient | | | ±5 | ±25 | | * | * | ppm/°C |
| Short Circuit to Common Duration | | | Indefinite | | | * | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | |
| Voltage: $+V_{CC}$ | | +11.4 | +15 | +16.5 | * | * | * | VDC |
| $-V_{CC}$ | | −11.4 | −15 | −16.5 | * | * | * | VDC |
| Current: $+V_{CC}$ + $V_L$ | No Load | | 13 | 15 | | * | * | mA |
| $-V_{CC}$ | No Load | | −5 | −7 | | * | * | mA |
| Potential at DCOM with Respect to ACOM(10) | | −3 | | +3 | * | | * | V |
| Power Dissipation | | | 270 | 330 | | * | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: J, K | | 0 | | +70 | * | | * | °C |
| A | | −40 | | +85 | * | | * | °C |
| Operating: J, K | | −40 | | +85 | * | | * | °C |
| A | | −55 | | +125 | * | | * | °C |
| Storage: J, K | | −60 | | +100 | * | | * | °C |
| A | | −65 | | +150 | * | | * | °C |

* Same as specification for DAC813AU, JP, JU.

NOTES: (1) USB = Unipolar Straight Binary; BOB = Bipolar Offset Binary. (2) TTL and 5V CMOS compatible. (3) Open DATA input lines will be pulled above +5.5V. See discussion under LOGIC INPUT COMPATIBILITY in the OPERATION section. (4) Specified with 500Ω Pin 6 to 7. Adjustable to zero with external trim potentiometer. (5) Error at input code $000_{HEX}$ for unipolar mode, FSR = 10V. (6) Error at input code $800_{HEX}$ for bipolar range. Specified with 100Ω Pin 6 to 4 and with 500Ω pin 6 to 7. See page 9 for zero adjustment procedure. (7) FSR means Full Scale Range and is 20V for the ±10V range. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) At the major carry, $7FF_{HEX}$ to $800_{HEX}$ and $800_{HEX}$ to $7FF_{HEX}$. (10) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

## PIN DESCRIPTIONS

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | $+V_L$ | Positive supply pin for logic circuits. Connect to $+V_{CC}$. |
| 2, 3 | 20V Range | Connect Pin 2 or Pin 3 to Pin 9 ($V_{OUT}$) for a 20V FSR. Connect both to Pin 9 for a 10V FSR. |
| 4 | BPO | Bipolar offset. Connect to Pin 6 ($V_{REF\ OUT}$) through 100Ω resistor or 200Ω potentiometer for bipolar operation. |
| 5 | ACOM | Analog common, $\pm V_{CC}$ supply return. |
| 6 | $V_{REF\ OUT}$ | +10V reference output referred to ACOM. |
| 7 | $V_{REF\ IN}$ | Connected to $V_{REF\ OUT}$ through a 1kΩ gain adjustment potentiometer or a 500Ω resistor. |
| 8 | $+V_{CC}$ | Analog supply input, nominally +12V to +15V referred to ACOM. |
| 9 | $V_{OUT}$ | D/A converter voltage output. |
| 10 | $-V_{CC}$ | Analog supply input, nominally –12V or –15V referred to ACOM. |
| 11 | $\overline{WR}$ | Master enable for $\overline{LDAC}$, $\overline{LLSB}$, and $\overline{LMSB}$. Must be low for data transfer to any latch. |
| 12 | $\overline{LDAC}$ | Load DAC. Must be low with $\overline{WR}$ for data transfer to the D/A latch and simultaneous update of the D/A converter. |
| 13 | $\overline{Reset}$ | When low, resets the D/A latch such that a Bipolar Zero output is produced. This control overrides all other data input operations. |
| 14 | $\overline{LMSB}$ | Enable for 4-bit input latch of $D_8$-$D_{11}$ data inputs. NOTE: This logic path is slower than the $\overline{WR}$ path. |
| 15 | $\overline{LLSB}$ | Enable for 8-bit input latch of $D_0$-$D_7$ data inputs. NOTE: This logic path is slower than the $\overline{WR}$ path. |
| 16 | DCOM | Digital common. |
| 17 | D0 | Data Bit 1, LSB. |
| 18 | D1 | Data Bit 2. |
| 19 | D2 | Data Bit 3. |
| 20 | D3 | Data Bit 4. |
| 21 | D4 | Data Bit 5. |
| 22 | D5 | Data Bit 6. |
| 23 | D6 | Data Bit 7. |
| 24 | D7 | Data Bit 8. |
| 25 | D8 | Data Bit 9. |
| 26 | D9 | Data Bit 10. |
| 27 | D10 | Data Bit 11. |
| 28 | D11 | Data Bit 12, MSB, positive true. |

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| $+V_{CC}$ to ACOM | 0 to +18V |
| $-V_{CC}$ to ACOM | 0 to –18V |
| $+V_{CC}$ to $-V_{CC}$ | 0 to +36V |
| DCOM with respect to ACOM | ±4V |
| Digital Inputs (Pins 11–15, 17–28) to DCOM | –0.5V to $+V_{CC}$ |
| External Voltage Applied to BPO Span Resistor | $\pm V_{CC}$ |
| $V_{REF\ OUT}$ | Indefinite Short to ACOM |
| $V_{OUT}$ | Indefinite Short to ACOM |
| Power Dissipation | 750mW |
| Lead Temperature (soldering, 10s) | +300°C |
| Max Junction Temperature | +165°C |
| Thermal Resistance, $\theta_{J\text{-}A}$: Plastic DIP and SOIC | 130°C/W |
| Ceramic DIP | 85°C/W |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE | LINEARITY ERROR, MAX AT +25°C (LSB) | GAIN DRIFT (ppm/°C) |
|---|---|---|---|---|---|
| DAC813JP | 28-Pin Plastic DIP | 246 | 0°C to +70°C | ±1/2 | ±30 |
| DAC813JU | 28-Lead Plastic SOIC | 217 | 0°C to +70°C | ±1/2 | ±30 |
| DAC813KP | 28-Pin Plastic DIP | 246 | 0°C to +70°C | ±1/4 | ±15 |
| DAC813KU | 28-Lead Plastic SOIC | 217 | 0°C to +70°C | ±1/4 | ±15 |
| DAC813AU | 28-Lead Plastic SOIC | 217 | –40°C to +85°C | ±1/2 | ±30 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# DAC1220

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www.burr-brown.com/databook/DAC1220.html

# 20-Bit Low Power DIGITAL-TO-ANALOG CONVERTER



## FEATURES

- 20-BIT MONOTONICITY GUARANTEED OVER –40°C to +85°C
- LOW POWER: 1mW
- VOLTAGE OUTPUT
- SETTLING TIME: 2ms to 0.012%
- MAX LINEARITY ERROR: ±0.0015% of FSR
- ON-CHIP CALIBRATION

## APPLICATIONS

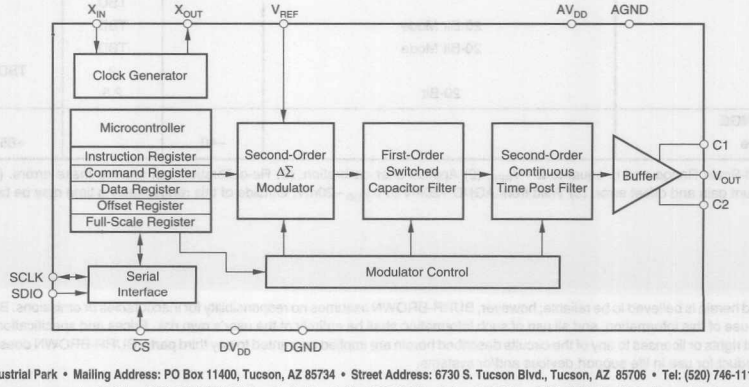
- PROCESS CONTROL
- ATE PIN ELECTRONICS
- CLOSED-LOOP SERVO-CONTROL
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTS

## DESCRIPTION

The DAC1220 is a 20-bit digital-to-analog (D/A) converter offering 20-bit monotonic performance over the specified temperature range. It utilizes delta-sigma technology to achieve 20-bit performance in a small package at very low power. The resolution of the device can be programmed to 20 bits for full-scale settling to 0.003% within 10ms or 16 bits for full-scale settling to 0.012% within 2ms. The output range is 0V to two times the external reference voltage and on-chip calibration circuitry provides extremely low offset and gain error.

The DAC1220 features a synchronous serial interface that is SPI and Microwire compatible. In single converter applications, the serial interface can be accomplished with just two wires, allowing low cost isolation. For multiple converters, a third $\overline{CS}$ signal allows for selection of the appropriate D/A converter.

The DAC1220 has been designed for closed-loop control applications in the industrial process control market and high resolution applications in the test and measurement market. It is also ideal for remote applications, battery powered instruments and isolated systems. The DAC1220 is available in a 16-pin plastic DIP and 16-lead SSOP package and is guaranteed over the –40°C to +85°C temperature range.




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# SPECIFICATION

All specifications $T_{MIN}$ to $T_{MAX}$, $AV_{DD} = DV_{DD} = +5V$, $f_{XIN} = 2.5MHz$, $V_{REF} = +2.5V$, and 16-bit mode, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC1220 MIN | DAC1220 TYP | DAC1220 MAX | UNITS |
|---|---|---|---|---|---|
| **ACCURACY** | | | | | |
| Monotonicity | | 16 | | | Bits |
| Monotonicity | 20-Bit Mode | 20 | | | Bits |
| Linearity Error | | | | ±0.0015 | %FSR(1) |
| Unipolar Offset Error(2) | | | | TBD | %FSR |
| Unipolar Offset Error Drift(3) | | | 5 | TBD | ppm/°C |
| Gain Error(2) | | | | TBD | %FSR |
| Gain Error Drift(3) | | | 5 | TBD | ppm/°C |
| Power Supply Rejection Ratio | | | | TBD | ppm/V |
| **ANALOG OUTPUT** | | | | | |
| Output Voltage(4) | | 0 | | $2 \cdot V_{REF}$ | V |
| Output Current | | | | TBD | mA |
| Capacitive Load | | | 500 | | pF |
| Short-Circuit Current | | | 10 | | mA |
| Short-Circuit Duration | GND or $V_{DD}$ | | Indefinite | | |
| **DYNAMIC PERFORMANCE** | | | | | |
| Settling Time(5) | To ±0.012% | | | 2 | ms |
| | 20-Bit Mode, to ±0.003% | | | 10 | ms |
| Output Noise Voltage | 0.1Hz to 10Hz | | 1 | | µVrms |
| Output Noise Voltage | 20-Bit Mode | | 40 | | $nV/\sqrt{Hz}$ |
| **REFERENCE INPUT** | | | | | |
| Input Voltage | | 2.0 | | 3.0 | V |
| Input Impedance | | | TBD | | kΩ |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic Family | | | TTL-Compatible CMOS | | |
| Logic Levels (all except $X_{IN}$) | | | | | |
| $V_{IH}$ | $I_{IH} = ±10µA$ | 2.0 | | $DV_{DD}$ +0.3 | V |
| $V_{IL}$ | $I_{IL} = ±10µA$ | –0.3 | | 0.8 | V |
| $V_{OH}$ | $I_{OH} = –0.8mA$ | 3.6 | | | V |
| $V_{OL}$ | $I_{OL} = 1.6mA$ | | | 0.4 | V |
| $X_{IN}$ Input Levels | | | | | |
| $V_{IN}$ | | TBD | | $DV_{DD}$ +0.3 | V |
| $V_{IL}$ | | –0.3 | | TBD | V |
| $X_{IN}$ Frequency Range ($f_{XIN}$) | | 0.5 | | 2.5 | MHz |
| Data Format | User Programmable | | Two's Complement or Offset Binary | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Power Supply Voltage | | 4.75 | | 5.25 | V |
| Supply Current | | | | | |
| Analog Current | | | TBD | | µA |
| Digital Current | | | TBD | | µA |
| Analog Current | 20-Bit Mode | | TBD | | µA |
| Digital Current | 20-Bit Mode | | TBD | | µA |
| Power Dissipation | | | 2 | TBD | mW |
| | 20-Bit | | 2.5 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified Performance | | –40 | | +85 | °C |

NOTES: (1) FSR is Full-Scale Range and is equal to $2 \cdot V_{REF}$. (2) Applies after calibration. (3) Re-calibration can remove these errors. (4) Ideal output voltage, does not take into account gain and offset error. (5) Valid from AGND +20mV to $AV_{DD}$ –20mV. Outside of this range, settling time may be twice the value indicated.

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## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| $AV_{DD}$ to $DV_{DD}$ | –0.3V to 6V |
| $AV_{DD}$ to AGND | –0.3V to 6V |
| $DV_{DD}$ to DGND | –0.3V to 6V |
| AGND to DGND | ±0.3V |
| $V_{REF}$ Voltage to AGND | –0.3V to $AV_{DD}$ + 0.3V |
| Digital Input Voltage to DGND | –0.3V to $DV_{DD}$ + 0.3V |
| Digital Output Voltage to DGND | –0.3V to $DV_{DD}$ + 0.3V |
| Package Power Dissipation | $(T_{JMAX} - T_A)/\theta_{JA}$ |
| Maximum Junction Temperature ($T_{JMAX}$) | +150°C |
| Thermal Resistance, $\theta_{JA}$ | |
| 16-Lead SSOP | 200°C/W |
| 16-Pin Plastic DIP | 100°C/W |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

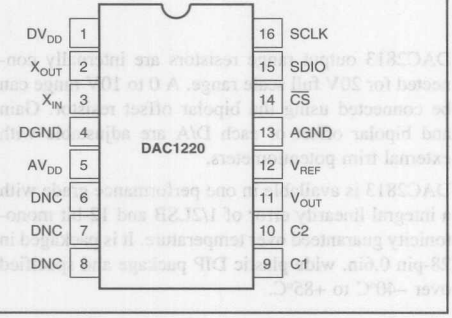
## PACKAGE/ORDERING INFORMATION

| PRODUCT | MAXIMUM LINEARITY ERROR (% FSR) | SPECIFICATION TEMPERATURE RANGE | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|---|---|
| DAC1220E | ±0.0015 | –40°C to +85°C | 16-Lead SSOP | 322 |
| DAC1220P | ±0.0015 | –40°C to +85°C | 16-Pin Plastic DIP | 180 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

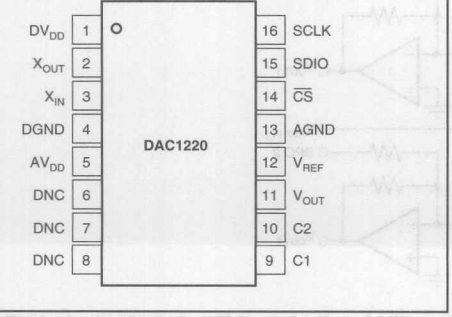
## PIN CONFIGURATION

Top View DIP




## PIN CONFIGURATION

Top View SSOP




## PIN DESCRIPTIONS

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | $DV_{DD}$ | Digital Supply, +5V nominal. |
| 2 | $X_{OUT}$ | System Clock Output (for Crystal). |
| 3 | $X_{IN}$ | System Clock Input. |
| 4 | DGND | Digital Ground. |
| 5 | $AV_{DD}$ | Analog Supply, +5V nominal. |
| 6 | DNC | Do Not Connect. |
| 7 | DNC | Do Not Connect. |
| 8 | DNC | Do Not Connect. |
| 9 | C1 | Filter Capacitor, see text. |
| 10 | C2 | Filter Capacitor, see text. |
| 11 | $V_{OUT}$ | Analog Output Voltage. |
| 12 | $V_{REF}$ | Reference Input. |
| 13 | AGND | Analog Ground. |
| 14 | $\overline{CS}$ | Chip Select Input. |
| 15 | SDIO | Serial Data Input/Output. |
| 16 | SCLK | Clock Input for serial data transfer. |

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# DAC2813

www.burr-brown.com/databook/DAC2813.html

# DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTER (12-bit port interface)

## FEATURES

- COMPLETE WITH REFERENCE AND OUTPUT AMPLIFIERS
- 12-BIT PORT INTERFACE
- ANALOG OUTPUT RANGE: ±10V
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- INTEGRAL LINEARITY ERROR: ±1/2LSB max
- ±12V to ±15V SUPPLIES
- 28-PIN PLASTIC DIP PACKAGE

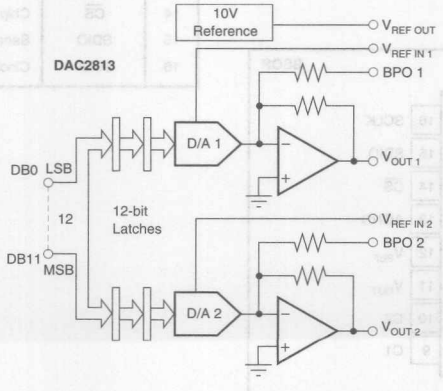
## DESCRIPTION

DAC2813 is a complete dual 12-bit digital-to-analog converter with bus interface logic. Each package includes a precision +10V voltage reference, double-buffered bus interface including a RESET function and 12-bit D/A converters with voltage-output operational amplifiers.

The double-buffered interface consists of a 12-bit input latch and a D/A latch for each D/A converter. A RESET control allows the D/A outputs to be asynchronously reset to bipolar zero, a feature useful for power-up reset, system initialization and recalibration.

DAC2813 output range resistors are internally connected for 20V full scale range. A 0 to 10V range can be connected using the bipolar offset resistor. Gain and bipolar offset of each D/A are adjustable with external trim potentiometers.

DAC2813 is available in one performance grade with a integral linearity error of 1/2LSB and 12-bit monotonicity guaranteed over temperature. It is packaged in 28-pin 0.6in. wide plastic DIP package and specified over –40°C to +85°C.




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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = −12V or −15V, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC2813AP MIN | DAC2813AP TYP | DAC2813AP MAX | UNITS |
|---|---|---|---|---|---|
| **INPUTS** | | | | | |
| **DIGITAL INPUTS** | Over Temperature Range | | | | |
| Input Code (1) | | | Bipolar Offset Binary | | |
| Logic Levels (2) | | | | | |
| $V_{IH}$ | | +2 | | +5.5(3) | V |
| $V_{IL}$ | | 0 | | +0.8 | V |
| Logic Input Currents | | | | | |
| DB0-DB11, $\overline{WR}$, $\overline{LDAC}$, $\overline{RESET}$,$\overline{EN}_X$ | | | | | |
| $I_{IH}$ | $V_I$ = +2.7V | | | ±20 | µA |
| $I_{IL}$ | $V_I$ = +0.4V | | | ±20 | µA |
| **TRANSFER CHARACTERISTICS** | | | | | |
| **ACCURACY** | | | | | |
| Linearity Error | | | ±1/4 | ±1/2 | LSB |
| Differential Linearity Error | | | ±1/2 | ±1 | LSB |
| Gain Error (5,6) | | | ±0.05 | ±0.2 | % |
| Bipolar Zero Error (5,7) | | | ±0.05 | ±0.2 | %FSR(4) |
| Power Supply Sensitivity | | | | | |
| Of Full Scale $+V_{CC}$ | | | ±5 | ±20 | ppmFSR/%+$V_{CC}$ |
| $-V_{CC}$ | | | ±1 | ±10 | ppmFSR/%−$V_{CC}$ |
| **DRIFT** | Over Specification Temperature Range | | | | |
| Gain | | | ±5 | ±30 | ppm/°C |
| Bipolar Zero Drift | | | ±5 | ±15 | ppmFSR/°C |
| Linearity Error over Temperature | | | ±1/2 | ±3/4 | LSB |
| Monotonicity | | | Guaranteed | | |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| **SETTLING TIME** (8) | To within ±0.012%FSR of Final Value 5kΩ II 500pF Load | | | | |
| Full Scale Range Change | 20V Range | | 4.5 | 6 | µs |
| 1LSB Output Step (9) At Major Carry | | | 2 | | µs |
| Slew Rate | | | 10 | | V/µs |
| Crosstalk (10) | 5kΩ Loads | | 0.1 | | LSB |
| **OUTPUT** | | | | | |
| Output Voltage Range | $\pm V_{CC} \geq \pm 11.4V$ | | | ±10 | V |
| Output Current | | ±5 | | | mA |
| Output Impedance | | | 0.2 | | Ω |
| Short Circuit to ACOM Duration | | | Indefinite | | |
| **REFERENCE VOLTAGE** | | | | | |
| Voltage | | +9.95 | +10.00 | +10.05 | V |
| Source Current Available for External Loads | | 2 | | | mA |
| Impedance | | | 0.2 | | Ω |
| Temperature Coefficient | | | ±5 | ±25 | ppm/°C |
| Short Circuit to Common Duration | | | Indefinite | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage:$+V_{CC}$ | | +11.4 | +15 | +16.5 | V |
| $-V_{CC}$ | | −11.4 | −15 | −16.5 | V |
| Current: | No Load $\pm V_{CC} = \pm 15V$ | | | | |
| $+V_{CC}$ | | | 24 | 30 | mA |
| $-V_{CC}$ | | | 12 | 14 | mA |
| Power Dissipation | | | 540 | 660 | mW |
| Potential at DCOM with Respect to ACOM (11) | | −3 | | +3 | V |
| **TEMPERATURE RANGES** | | | | | |
| Specification | | −40 | | +85 | °C |
| Storage | | −60 | | +100 | °C |
| Thermal Resistance, $\theta_{JA}$,Plastic DIP | | | 30 | | °C/W |

NOTES: (1) For Two's Complement Input Coding invert the MSB with an external logic inverter. (2) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (3) Open DATA input lines will be pulled above +5.5V. See discussion under LOGIC INPUT COMPATIBILITY section. (4) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (5) Adjustable to zero with external trim potentiometer. (6) Specified with 500Ω connected between $V_{REF\ OUT}$ and $V_{REF\ IN}$. (7) Error at input code $800_{HEX}$. DAC2813 specified with 100Ω connected between$V_{REF\ OUT}$ and $V_{REF\ IN}$; and with 500Ω connected between $V_{REF\ OUT}$ and BPO. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) For the worst-case code change: $7FF_{HEX}$ to $800_{HEX}$ and $800_{HEX}$ to $7FF_{HEX}$. (10) Crosstalk is defined as the change in any output as a result of any other output being driven from −10V to +10V at rated output current. (11) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| $+V_{CC}$ to ACOM | 0 to +18V |
| $-V_{CC}$ to ACOM | 0 to −18V |
| $+V_{CC}$ to $-V_{CC}$ | 0 to +36V |
| ACOM to DCOM | ±4V |
| Digital Inputs to DCOM | −1V to $+V_{CC}$ |
| External Voltage applied to BPO Resistor | ±18V |
| $V_{REF\ OUT}$ | Indefinite short to ACOM |
| $V_{OUT}$ | Momentary to ±18V |
| Lead Temperature, soldering 10s | +300°C |
| Max Junction Temperature | 165°C |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTROSTATIC DISCHARGE SENSITIVITY

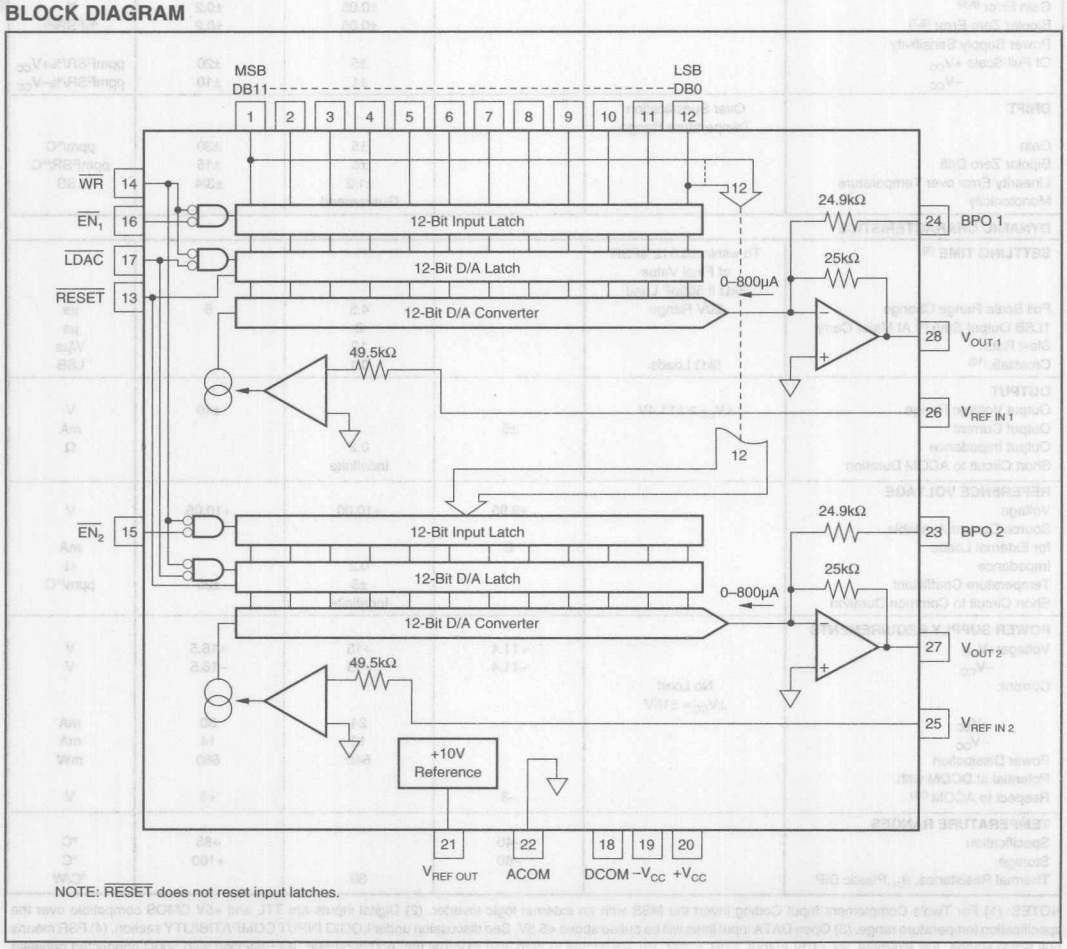
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| DAC2813AP | 28-Pin DBL Wide DIP | 215 | −40°C to +85°C |

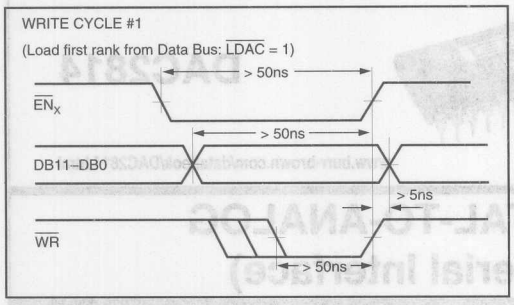
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

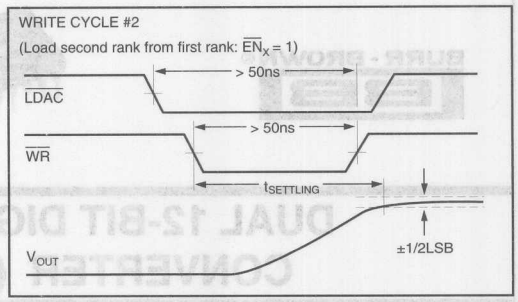
## BLOCK DIAGRAM




NOTE: $\overline{RESET}$ does not reset input latches.

## TIMING DIAGRAMS

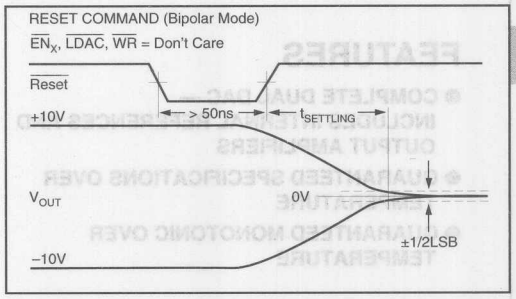



## TRUTH TABLE

| WR | EN1 | EN2 | LDAC | RESET | OPERATION |
|---|---|---|---|---|---|
| X | X | X | X | 0 | Reset both D/A Latches. Does not reset input latches. |
| 1 | X | X | X | 1 | No Operation |
| X | 1 | 1 | 1 | 1 | No Operation |
| 0 | 1 | 0 | 1 | 1 | Load Data into First Rank for D/A 2 |
| 0 | 0 | 1 | 1 | 1 | Load Data into First Rank for D/A 1 |
| 0 | 1 | 1 | 0 | 1 | Load Second Rank from First Rank, both D/As |
| 0 | 0 | 0 | 0 | 1 | All Latches Transparent |

"X" = Don't Care




## PIN DESCRIPTIONS

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | DB11 | DATA, MSB, positive true. |
| 2 | DB10 | DATA |
| 3 | DB9 | DATA |
| 4 | DB8 | DATA |
| 5 | DB7 | DATA |
| 6 | DB6 | DATA |
| 7 | DB5 | DATA |
| 8 | DB4 | DATA |
| 9 | DB3 | DATA |
| 10 | DB2 | DATA |
| 11 | DB1 | DATA |
| 12 | DB0 | DATA, LSB. |
| 13 | RESET | Resets output of all D/As to bipolar-zero. The D/A remains in this state until overwritten an LDAC-WR command. RESET does not reset the input latch. After power–up and reset, input latches will be in an indeterminant state. |
| 14 | WR | Write strobe. Must be low for data transfer to any latch (except RESET). |
| 15 | EN2 | Enable for 12-bit input data latch of D/A 2. NOTE: This logic path is slower than the WR\ path. |
| 16 | EN1 | Enable for 12-bit input data latch of D/A 1. NOTE: This logic path is slower than the WR\ path. |
| 17 | LDAC | Load DAC enable. Must be low with WR for data transfer to the D/A latch and simultaneous update of both D/A converters. |
| 18 | DCOM | Digital common, logic currents return. |
| 19 | $-V_{CC}$ | Analog supply input, nominally –12V or –15V referred to ACOM. |
| 20 | $+V_{CC}$ | Analog supply input, nominally +12V or +15V referred to ACOM. |
| 21 | $V_{REF\ OUT}$ | +10V reference output. |
| 22 | ACOM | Analog common, $+V_{CC}$, $-V_{CC}$ supply return. |
| 23 | BPO2 | Bipolar offset. Connect to pin 21 ($V_{REF\ OUT}$) through a 100Ω resistor or through a 200 potentiometer for Bipolar Offset Adjust for D/A 2. |
| 24 | BPO1 | Bipolar offset. Connect to pin 21 ($V_{REF\ OUT}$) through a 100Ω resistor or through a 200 potentiometer for Bipolar Offset Adjust or D/A 1. |
| 25 | $V_{REF\ IN\ 2}$ | Connect to $V_{REF\ OUT}$ through 500Ω fixed resistor or through a 1kΩ gain adjustment potentiometer for D/A 2. |
| 26 | $V_{REF\ IN\ 1}$ | Connect to $V_{REF\ OUT}$ through 500Ω fixed resistor or through a 1kΩ gain adjustment potentiometer for D/A 1. |
| 27 | $V_{OUT\ 2}$ | D/A 2 analog output. |
| 28 | $V_{OUT\ 1}$ | D/A 1 analog output. |

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# DAC2814

www.burr-brown.com/databook/DAC2814.html

# DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTER (Serial Interface)

## FEATURES

- COMPLETE DUAL DAC — INCLUDES INTERNAL REFERENCES AND OUTPUT AMPLIFIERS
- GUARANTEED SPECIFICATIONS OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- HIGH-SPEED SERIAL INTERFACE (10MHz CLOCK)
- LOW POWER: 300mW (150mW/DAC)
- LOW GAIN DRIFT: 5ppm/°C
- LOW NONLINEARITY: ±1/2 LSB max
- UNIPOLAR OR BIPOLAR OUTPUT
- CLEAR/RESET TO UNIPOLAR OR BIPOLAR ZERO

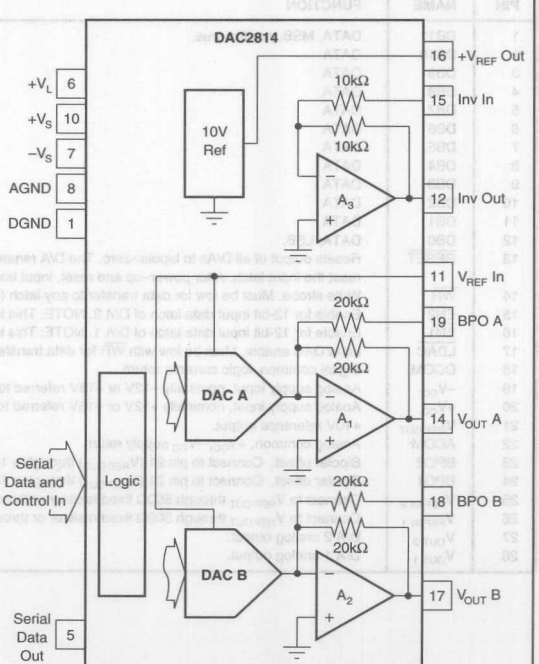
## DESCRIPTION

The DAC2814 is one in a family of dual and quad 12-bit digital-to-analog converters. Serial, 8-bit, 12-bit interfaces are available.

The DAC2814 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for either unipolar 0 to 10V, 0 to –10V, or bipolar ±10V output ranges.

The DAC2814 has a high-speed serial interface capable of being clocked at 10MHz. Serial data are clocked DAC B MSB first into a 24-bit shift register, then strobed into each DAC separately or simultaneously as required. The DAC has an asynchronous clear control for reset to unipolar or bipolar zero depending on the mode selected. This feature is useful for power-on reset or system calibration. The DAC2814 is packaged in a 24-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.




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# SPECIFICATIONS, Guaranteed over $T_A$ = –40°C to +85°C unless otherwise specified.

## ELECTRICAL

Specifications as shown for $V_S$ = ±12V or ±15V, $V_L$ = +5V, and $R_L$ = 2kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC2814AP | | | DAC2814BP | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **DIGITAL INPUTS** | | | | | | | | |
| Resolution | | 12 | | | * | | | Bits |
| $V_{IH}$ (Input High Voltage) | | +2 | | +5 | * | | * | V |
| $V_{IL}$ (Input Low Voltage) | | 0 | | +0.8 | * | | * | V |
| $I_{IN}$ ( Input Current) | $T_A$ = 25°C | | | ±1 | | | * | µA |
| | $T_A$ = –40°C to +85°C | | | ±10 | | | * | µA |
| $C_{IN}$ (Input Capacitance) | | | 0.8 | | | * | | pF |
| **DIGITAL OUTPUT** | | | | | | | | |
| Data Out $V_{OL}$ | $I_{SINK}$ = 1.6mA | 0 | | +0.4 | * | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +2.4 | | +5 | * | | * | V |
| **ACCURACY** | | | | | | | | |
| Integral, Relative Linearity[1] | | | | ±1 | | | ±1/2 | LSB |
| Differential Nonlinearity[2] | $T_A$ = 25°C | | | ±1 | | | * | LSB |
| | $T_A$ = –40°C to +85°C | | +1.5/–1 | | | | ±1 | LSB |
| Unipolar Offset Error | $T_A$ = +25°C | | | ±1 | | | ±0.5 | mV |
| | $T_A$ = –40°C TO +85°C | | | ±3 | | | * | mV |
| Bipolar Zero Error | | | | ±20 | | | ±10 | mV |
| Gain Error Unipolar, Bipolar | With Internal or External 10.0V Ref | | | ±0.2 | | | ±0.15 | % |
| Power Supply Sensitivity[3] | $V_S$ = ±11.4V to ±18V | | | 30 | | | * | ppmFSR/V |
| | $V_L$ = +4.5V to +5.5V | | | | | | | |
| **TEMPERATURE DRIFT** | | | | | | | | |
| Gain Drift Unipolar, Bipolar | | | ±5 | ±30 | | * | ±20 | ppm/°C |
| Unipolar Offset Drift | | | ±0.1 | ±5 | | * | * | ppmFSR/°C |
| Bipolar Zero Drift | | | ±5 | ±15 | | * | ±8 | ppmFSR/°C |
| **REFERENCE OUTPUT** | | | | | | | | |
| Output Voltage | | +9.980 | +10 | +10.020 | +9.985 | * | +10.015 | V |
| Reference Drift | | | ±2 | ±30 | | * | ±20 | ppm/°C |
| Output Current | $T_A$ = 25°C | +10/–5 | | | * | | | mA |
| | $T_A$ = –40°C to +85°C | +6.5/–5 | | | * | | | mA |
| Max Load Capacitance (For Stability) | | | 500 | | | * | | pF |
| Short Circuit Current | | | ±20 | | | * | | mA |
| Load Regulation ($\Delta V_{OUT}$ vs $\Delta I_{LOAD}$) | | | | 40 | | | * | ppm/mA |
| Supply Regulation ($\Delta V_{OUT}$ vs $\Delta V_S$) | | | | ±5 | | | * | ppm/V |
| **INVERTER** | | | | | | | | |
| –10V Reference[4], Inverter Output | | –10.020 | –10 | –9.980 | –10.015 | * | –9.985 | V |
| –10V Reference Drift | | | | ±30 | | | ±20 | ppm/°C |
| DC Output Impedance | | | 0.1 | | | * | | Ω |
| Output Current | | ±7 | | | * | | | mA |
| Max Load Capacitance (For Stability) | | | 200 | | | * | | pF |
| Short Circuit Current | | | ±30 | | | * | | mA |
| **REFERENCE INPUT** | | | | | | | | |
| Reference Input Resistance | | 3.5 | 5 | | * | * | | kΩ |
| Inverter Input Resistance | | 7 | 10 | | * | * | | kΩ |
| BPO Input Resistance | | 14 | 20 | | * | * | | kΩ |
| Reference Input Range | | | | ±10 | | | * | V |
| **ANALOG SIGNAL OUTPUTS** | | | | | | | | |
| Voltage Range | | $–V_S$ + 1.4 | | $+V_S$ – 1.4 | * | | * | V |
| DC Output Impedance | | | 0.1 | | | * | | Ω |
| Output Current | | ±5 | | | * | | | mA |
| Max Load Capacitance (For Stability) | $V_{OUT}$ | | 500 | | | * | | pF |
| Short Circuit Current | | | ±30 | | | * | | mA |
| **DYNAMIC PERFORMANCE[5]** | $C_L$ = 100pF | | | | | | | |
| Unipolar Mode Settling Time | To 1/2 LSB of Full Scale | | 2.5 | 10 | | * | * | µs |
| Bipolar Mode Settling Time | To 1/2 LSB of Full Scale | | 3.5 | 10 | | * | * | µs |
| Slew Rate | | | 10 | | | * | | V/µs |
| Small-Signal Bandwidth | | | 3 | | | * | | MHz |
| **ANALOG GROUND CURRENT** (Code Dependent) | | | ±2 | | | * | | mA |
| **DIGITAL CROSSTALK** | Full Scale Transition $C_L$= 100pF | | 3 | | | * | | nV-s |
| **D/A GLITCH IMPULSE** | | | 30 | | | * | | nV-s |

## SPECIFICATIONS (CONT), Guaranteed over $T_A$ = –40°C to +85°C unless otherwise specified.

### ELECTRICAL

Specifications as shown for $V_S$ = ±12V or ±15V, $V_L$ = +5V, and $R_L$ = 2kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC2814AP | | | DAC2814BP | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **POWER SUPPLY** | | | | | | | | |
| $+V_S$ and $-V_S$ | | ±11.4 | ±15 | ±18 | * | * | * | V |
| $+V_L$ | | 4.5 | 5 | 5.5 | * | * | * | V |
| $+I_S$ | | | +10 | +13.5 | | * | * | mA |
| $-I_S$ | | | –10 | –13.5 | | * | * | mA |
| $+I_L$ | Digital Inputs = 0V or $+V_L$ | | 0.2 | 1 | | * | * | mA |
| $+I_L$ | Digital Inputs = $V_{IL}$ or $V_{IH}$ | | | 5 | | | * | mA |
| Total Power, All DACs | | | 300 | 410 | | * | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified | | –40 | | +85 | * | | * | °C |
| Operating | | –40 | | +85 | * | | * | °C |
| Thermal Resistance $\theta_{JA}$ | | | 75 | | | * | | °C/W |

* Specifications same as DAC2814AP.

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes voltage output DAC, voltage reference, and reference inverter. (4) Inverter output with inverter input connected to $+V_{REF}$. (5) Guaranteed but not tested.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_L$ to AGND | 0V, +7V |
| $+V_L$ to DGND | 0V, +7V |
| $+V_S$ to AGND | 0V, +18V |
| $-V_S$ to AGND | 0V, –18V |
| AGND to DGND | ±0.3V |
| Any digital input to DGND | –0.3V, $+V_L$ +0.3V |
| Ref In to AGND | ±25V |
| Ref In to DGND | ±25V |
| Storage Temperature Range | –55°C to +125°C |
| Operating Temperature Range | –40°C to +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Junction Temperature | +155°C |
| Output Short Circuit | Continuous to common or $\pm V_S$ |
| Reference Short Circuit | Continuous to common or $+V_S$ |

### PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| DAC2814AP | 24-Pin Plastic DIP | 167 |
| DAC2814BP | 24-Pin Plastic DIP | 167 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

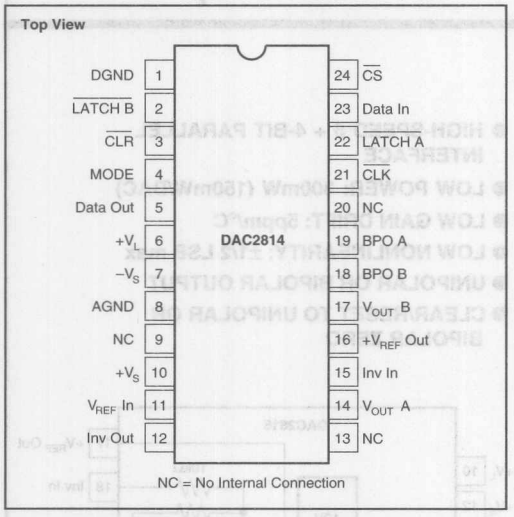
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## PIN DESIGNATIONS

| PIN | DESCRIPTOR | FUNCTION | PIN | DESCRIPTOR | FUNCTION |
|---|---|---|---|---|---|
| 1 | DGND | Digital common | 24 | $\overline{CS}$ | Chip select enable, DAC A and DAC B |
| 2 | $\overline{LATCH\ B}$ | Latch data update, logic input, DAC B | 23 | Data In | Serial data input |
| 3 | $\overline{CLR}$ | Asychronous input reset to zero | 22 | $\overline{LATCH\ A}$ | Latch data update, logic input, DAC A |
| 4 | MODE | Selection input for unipolar or bipolar reset to zero | 21 | $\overline{CLK}$ | Clock input |
| 5 | Data Out | Serial data output | 20 | NC | No internal connection |
| 6 | $+V_L$ | Positive logic power supply, +5V input | 19 | BPO A | Bipolar offset input, DAC A |
| 7 | $-V_S$ | Negative analog power supply , –15V input | 18 | BPO B | Bipolar offset input, DAC B |
| 8 | AGND | Analog common | 17 | $V_{OUT}$ B | Analog output voltage, DAC B |
| 9 | NC | No internal connection | 16 | $+V_{REF}$ Out | Reference voltage, +10V output |
| 10 | $+V_S$ | Positive analog power supply, +15V input | 15 | Inv In | Inverter (A3) input |
| 11 | $V_{REF}$ In | ± Reference voltage input | 14 | $V_{OUT}$ A | Analog output voltage, DAC A |
| 12 | Inv Out | Inverter (A3) output | 13 | NC | No internal connection |

## PIN CONFIGURATIONS

Top View




NC = No Internal Connection

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# DAC2815

www.burr-brown.com/databook/DAC2815.html

# DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTER (8-Bit Port Interface)

## FEATURES

- COMPLETE DUAL DAC — INCLUDES INTERNAL REFERENCES AND OUTPUT AMPLIFIERS
- GUARANTEED SPECIFICATIONS OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- HIGH-SPEED 8 + 4-BIT PARALLEL INTERFACE
- LOW POWER: 300mW (150mW/DAC)
- LOW GAIN DRIFT: 5ppm/°C
- LOW NONLINEARITY: ±1/2 LSB max
- UNIPOLAR OR BIPOLAR OUTPUT
- CLEAR/RESET TO UNIPOLAR OR BIPOLAR ZERO

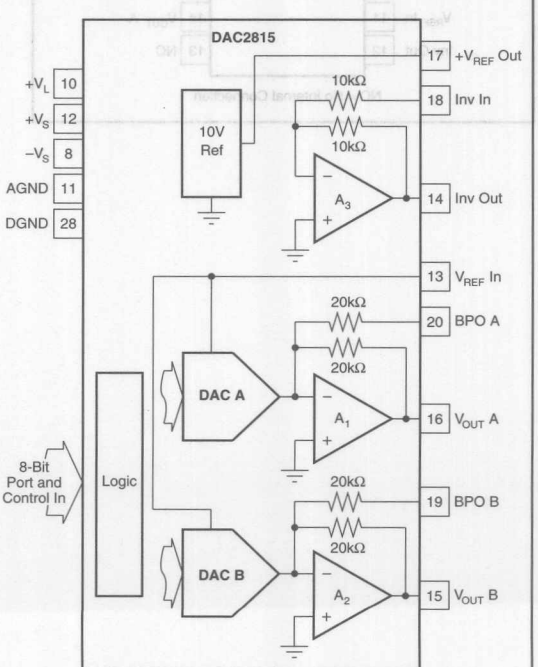
## DESCRIPTION

The DAC2815 is one in a family of dual and quad 12-bit digital-to-analog converters (DACs). Serial, 8-bit, 12-bit interfaces are available.

The DAC2815 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for either unipolar 0 to 10V, 0 to –10V, or bipolar ±10V output ranges.

The DAC2815 has a 2-byte (8 + 4) double-buffered interface. Data is first loaded (level transferred) into the input registers in two steps for each DAC. Then both DACs are updated simultaneously. The DAC has an asynchronous clear control for reset to unipolar or bipolar zero depending on the mode selected. This feature is useful for power-on reset or system calibration. The DAC2815 is packaged in a 28-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

## SPECIFICATIONS, Guaranteed over $T_A$ = –40°C to +85°C unless otherwise specified.

### ELECTRICAL

Specifications as shown for $V_S$ = ±12V or ±15V, $V_L$ = +5V, and $R_L$ = 2kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC2815AP MIN | DAC2815AP TYP | DAC2815AP MAX | DAC2815BP MIN | DAC2815BP TYP | DAC2815BP MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **DIGITAL INPUTS** | | | | | | | | |
| Resolution | | 12 | | | * | | | Bits |
| $V_{IH}$ (Input High Voltage) | | 2 | | 5 | * | | * | V |
| $V_{IL}$ (Input Low Voltage) | | 0 | | 0.8 | * | | * | V |
| $I_{IN}$ ( Input Current) | $T_A$ = 25°C | | | ±1 | | | * | µA |
| | $T_A$ = –40°C to +85°C | | | ±10 | | | * | µA |
| $C_{IN}$ (Input Capacitance) | | | 0.8 | | | * | | pF |
| **ACCURACY** | | | | | | | | |
| Integral, Relative Linearity[1] | | | | ±1 | | | ±1/2 | LSB |
| Differential Nonlinearity[2] | $T_A$ = 25°C | | | ±1 | | | * | LSB |
| | $T_A$ = –40°C to +85°C | | +1.5/–1 | | | | ±1 | LSB |
| Unipolar Offset Error | $T_A$ = +25°C | | | ±1 | | | ±0.5 | mV |
| | $T_A$ = –40°C TO +85°C | | | ±3 | | | * | mV |
| Bipolar Zero Error | | | | ±20 | | | ±10 | mV |
| Gain Error Unipolar, Bipolar | With Internal or External 10.0V Ref | | | ±0.2 | | | ±0.15 | % |
| Power Supply Sensitivity[3] | $V_S$ = ±11.4V to ±18V, $V_L$ = +4.5V to +5.5V | | | 30 | | | * | ppmFSR/V |
| **TEMPERATURE DRIFT** | | | | | | | | |
| Gain Drift Unipolar, Bipolar | | | ±5 | ±30 | | * | ±20 | ppm/°C |
| Unipolar Offset Drift | | | ±0.1 | ±5 | | * | * | ppmFSR/°C |
| Bipolar Zero Drift | | | ±5 | ±15 | | * | ±8 | ppmFSR/°C |
| **REFERENCE OUTPUT** | | | | | | | | |
| Output Voltage | | +9.980 | +10 | +10.020 | +9.985 | * | +10.015 | V |
| Reference Drift | | | ±2 | ±30 | | * | ±20 | ppm/°C |
| Output Current | $T_A$ = 25°C | +10/–5 | | | * | | | mA |
| | $T_A$ = –40°C to +85°C | +6.5/–5 | | | * | | | mA |
| Max Load Capacitance (For Stability) | | | 500 | | | * | | pF |
| Short Circuit Current | | | ±20 | | | * | | mA |
| Load Regulation ($\Delta V_{OUT}$ vs $\Delta I_{LOAD}$) | | | | 40 | | | * | ppm/mA |
| Supply Regulation ($\Delta V_{OUT}$ vs $\Delta V_S$) | | | | ±5 | | | * | ppm/V |
| **INVERTER** | | | | | | | | |
| –10V Reference[4], Inverter Output | | –10.020 | –10 | –9.980 | –10.015 | * | –9.985 | V |
| –10V Reference Drift | | | | ±30 | | | ±20 | ppm/°C |
| DC Output Impedance | | | 0.1 | | | * | | Ω |
| Output Current | | ±7 | | | * | | | mA |
| Max Load Capacitance (For Stability) | | | 200 | | | * | | pF |
| Short Circuit Current | | | ±30 | | | * | | mA |
| **REFERENCE INPUT** | | | | | | | | |
| Reference Input Resistance | | 3.5 | 5 | | * | * | | kΩ |
| Inverter Input Resistance | | 7 | 10 | | * | * | | kΩ |
| BPO Input Resistance | | 14 | 20 | | * | * | | kΩ |
| Reference Input Range | | | | ±10 | | | * | V |
| **ANALOG SIGNAL OUTPUTS** | | | | | | | | |
| Voltage Range | | $–V_S$ + 1.4 | | $+V_S$ – 1.4 | * | | * | V |
| DC Output Impedance | | | 0.1 | | | * | | Ω |
| Output Current | | ±5 | | | * | | | mA |
| Max Load Capacitance (For Stability) | $V_{OUT}$ | | 500 | | | * | | pF |
| Short Circuit Current | | | ±30 | | | * | | mA |
| **DYNAMIC PERFORMANCE[5]** | $C_L$ = 100pF | | | | | | | |
| Unipolar Mode Settling Time | To 1/2 LSB of Full Scale | | 2.5 | 10 | | * | * | µs |
| Bipolar Mode Settling Time | To 1/2 LSB of Full Scale | | 3.5 | 10 | | * | * | µs |
| Slew Rate | | | 10 | | | * | | V/µs |
| Small-Signal Bandwidth | | | 3 | | | * | | MHz |
| **ANALOG GROUND CURRENT** (Code Dependent) | | | ±2 | | | * | | mA |
| **DIGITAL CROSSTALK** | Full Scale Transition $C_L$= 100pF | | 3 | | | * | | nV-s |
| **D/A GLITCH IMPULSE** | | | 30 | | | * | | nV-s |

Specifications as shown for $V_S$ = ±12V or ±15V, $V_L$ = +5V, and $R_L$ = 2kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC2815AP | | | DAC2815BP | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **POWER SUPPLY** | | | | | | | | |
| $+V_S$ and $-V_S$ | | ±11.4 | ±15 | ±18 | * | * | * | V |
| $+V_L$ | | 4.5 | 5 | 5.5 | * | * | * | V |
| $+I_S$ | | | +10 | +13.5 | | * | * | mA |
| $-I_S$ | | | −10 | −13.5 | | * | * | mA |
| $+I_L$ | Digital Inputs = 0V or $+V_L$ | | 0.2 | 1 | | * | * | mA |
| $+I_L$ | Digital Inputs = $V_{IL}$ or $V_{IH}$ | | | 5 | | | * | mA |
| Total Power, All DACs | | | 300 | 410 | | * | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified | | −40 | | +85 | * | | * | °C |
| Operating | | −40 | | +85 | * | | * | °C |
| Thermal Resistance, $\theta_{JA}$ | | | 75 | | | * | | °C/W |

* Specifications same as DAC2815AP.

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes voltage output DAC, voltage reference, and reference inverter. (4) Inverter output with inverter input connected to $+V_{REF}$. (5) Guaranteed but not tested.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_L$ to AGND | 0V, +7V |
| $+V_L$ to DGND | 0V, +7V |
| $+V_S$ to AGND | 0V, +18V |
| $-V_S$ to AGND | 0V, −18V |
| AGND to DGND | ±0.3V |
| Any digital input to DGND | −0.3V, $+V_L$ +0.3V |
| Ref In to AGND | ±25V |
| Ref In to DGND | ±25V |
| Storage Temperature Range | −55°C to +125°C |
| Operating Temperature Range | −40°C to +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Junction Temperature | +155°C |
| Output Short Circuit | Continuous to common or $\pm V_S$ |
| Reference Short Circuit | Continuous to common or $+V_S$ |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| DAC2815AP | 28-Pin Plastic DIP | 215 |
| DAC2815BP | 28-Pin Plastic DIP | 215 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

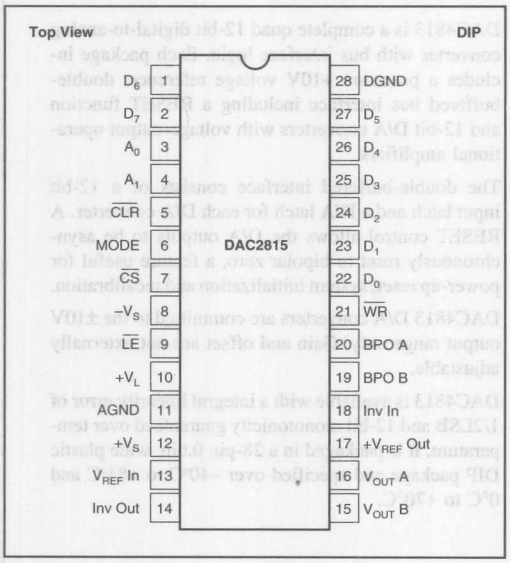
| PRODUCT | LINEARITY ERROR (LSB) |
|---|---|
| DAC2815AP | ±1 |
| DAC2815BP | ±1/2 |

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## PIN DESIGNATIONS

| PIN | DESCRIPTOR | FUNCTION | PIN | DESCRIPTOR | FUNCTION |
|---|---|---|---|---|---|
| 1 | $D_6$ | Data bit 6 input | 28 | DGND | Digital common |
| 2 | $D_7$ | Data bit 7 input | 27 | $D_5$ | Data bit 5 input |
| 3 | $A_0$ | Address 0 input | 26 | $D_4$ | Data bit 4 input |
| 4 | $A_1$ | Address 1 input | 25 | $D_3$ | Data bit 3 input |
| 5 | $\overline{CLR}$ | Asychronous input reset to zero | 24 | $D_2$ | Data bit 2 input |
| 6 | MODE | Selection input for unipolar or bipolar reset to zero | 23 | $D_1$ | Data bit 1 input |
| 7 | $\overline{CS}$ | Chip select enable, DAC A and DAC B | 22 | $D_0$ | Data bit 0 input |
| 8 | $-V_S$ | Negative analog power supply, –15V input | 21 | $\overline{WR}$ | Write input, DAC A and DAC B |
| 9 | $\overline{LE}$ | Latch data enable, DAC A and DAC B | 20 | BPO A | Bipolar offset input, DAC A |
| 10 | $+V_L$ | Positive logic power supply, +5V input | 19 | BPO B | Bipolar offset input, DAC B |
| 11 | AGND | Analog common | 18 | Inv In | Inverter (A3) input |
| 12 | $+V_S$ | Positive analog power supply, +15V input | 17 | $+V_{REF}$ Out | Reference voltage, +10V output |
| 13 | $V_{REF}$ In | ± Reference voltage input | 16 | $V_{OUT}$ A | Analog output voltage, DAC A |
| 14 | Inv Out | Inverter ($A_3$) output | 15 | $V_{OUT}$ B | Analog output voltage, DAC B |

## PIN CONFIGURATION



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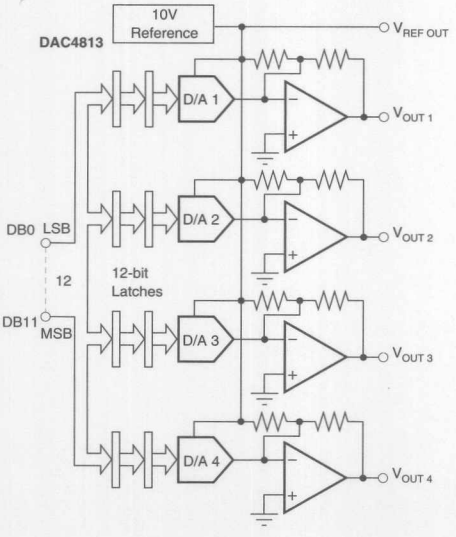

# DAC4813

www.burr-brown.com/databook/DAC4813.html

# QUAD 12-BIT DIGITAL-TO-ANALOG CONVERTER (12-bit port interface)

## FEATURES

- COMPLETE WITH REFERENCE AND OUTPUT AMPLIFIERS
- 12-BIT PORT INTERFACE
- ANALOG OUTPUT RANGE: ±10V
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- INTEGRAL LINEARITY ERROR: ±1/2LSB max
- ±12V to ±15V SUPPLIES
- 28-PIN PLASTIC DIP PACKAGE




## DESCRIPTION

DAC4813 is a complete quad 12-bit digital-to-analog converter with bus interface logic. Each package includes a precision +10V voltage reference, double-buffered bus interface including a RESET function and 12-bit D/A converters with voltage-output operational amplifiers.

The double-buffered interface consists of a 12-bit input latch and a D/A latch for each D/A converter. A RESET control allows the D/A outputs to be asynchronously reset to bipolar zero, a feature useful for power-up reset, system initialization and recalibration.

DAC4813 D/A converters are committed to the ±10V output range only. Gain and offset are not externally adjustable.

DAC4813 is available with a integral linearity error of 1/2LSB and 12-bit monotonicity guaranteed over temperature. It is packaged in a 28-pin 0.6in. wide plastic DIP package and specified over –40°C to +85°C and 0°C to +70°C.

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# SPECIFICATIONS

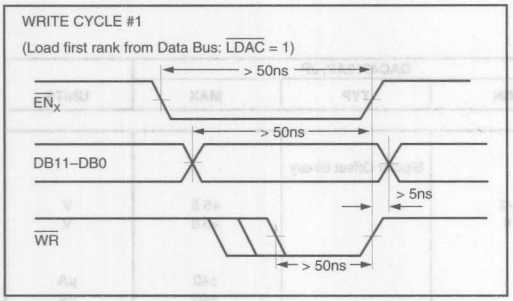
## ELECTRICAL

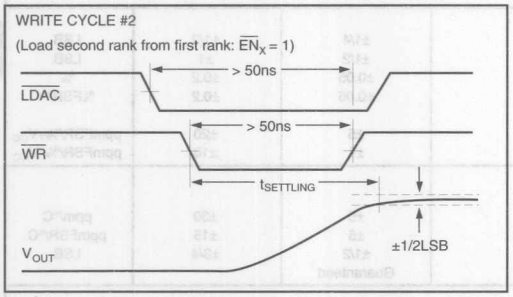
$T_A$ = +25°C, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = −12V or −15V, unless otherwise noted.

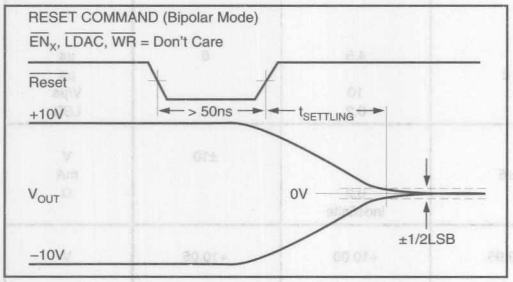
| PARAMETER | CONDITIONS | DAC4813AP, JP MIN | DAC4813AP, JP TYP | DAC4813AP, JP MAX | UNITS |
|---|---|---|---|---|---|
| **INPUTS** | | | | | |
| **DIGITAL INPUTS** | Over Temperature | | | | |
| Input Code [1] | Range | | Bipolar Offset Binary | | |
| Logic Levels [2] | | | | | |
| $V_{IH}$ [3] | | +2 | | +5.5 | V |
| $V_{IL}$ | | 0 | | +0.8 | V |
| Logic Input Currents | | | | | |
| DB0-DB11, $\overline{WR}$, $\overline{LDAC}$, $\overline{RESET}$,$\overline{EN_X}$ | | | | | |
| $I_{IH}$ | $V_I$ = +2.7V | | | ±40 | µA |
| $I_{IL}$ | $V_I$ = +0.4V | | | ±40 | µA |
| **TRANSFER CHARACTERISTICS** | | | | | |
| **ACCURACY** | | | | | |
| Linearity Error | | | ±1/4 | ±1/2 | LSB |
| Differential Linearity Error | | | ±1/2 | ±1 | LSB |
| Gain Error | | | ±0.05 | ±0.2 | % |
| Bipolar Zero Error [5] | | | ±0.05 | ±0.2 | %FSR[4] |
| Power Supply Sensitivity | | | | | |
| Of Full Scale $+V_{CC}$ | | | ±5 | ±20 | ppmFSR/%+$V_{CC}$ |
| $-V_{CC}$ | | | ±1 | ±10 | ppmFSR/%−$V_{CC}$ |
| **DRIFT** | Over Specification Temperature Range | | | | |
| Gain | | | ±5 | ±30 | ppm/°C |
| Bipolar Zero Drift | | | ±5 | ±15 | ppmFSR/°C |
| Linearity Error over Temperature | | | ±1/2 | ±3/4 | LSB |
| Monotonicity | | | Guaranteed | | |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| **SETTLING TIME** [6] | To within ±0.012%FSR of Final Value 5kΩ II 500pF Load | | | | |
| Full Scale Range Change | 20V Range | | 4.5 | 6 | µs |
| 1LSB Output Step [7] At Major Carry | | 2 | | | µs |
| Slew Rate | | | 10 | | V/µs |
| Crosstalk [8] | 5kΩ Loads | | 0.2 | | LSB |
| **OUTPUT** | | | | | |
| Output Voltage Range | $\pm V_{CC} \geq \pm 11.4V$ | | | ±10 | V |
| Output Current | | ±5 | | | mA |
| Output Impedance | | | 0.2 | | Ω |
| Short Circuit to ACOM Duration | at DC | | Indefinite | | |
| **REFERENCE VOLTAGE** | | | | | |
| Voltage | | +9.95 | +10.00 | +10.05 | V |
| Source Current Available for External Loads | | 2 | | | mA |
| Impedance | | | 0.2 | | Ω |
| Temperature Coefficient | | | ±5 | ±25 | ppm/°C |
| Short Circuit to Common Duration | at DC | | Indefinite | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage: $+V_{CC}$ | | +11.4 | +15 | +16.5 | V |
| $-V_{CC}$ | | −11.4 | −15 | −16.5 | V |
| Current: | No Load $\pm V_{CC}$ = ±15V | | | | |
| $+V_{CC}$ | | | 48 | 60 | mA |
| $-V_{CC}$ | | | 24 | 28 | mA |
| Power Dissipation | | | 1080 | 1320 | mW |
| Potential at DCOM with Respect to ACOM [9] | | −3 | | +3 | V |
| **TEMPERATURE RANGES** | | | | | |
| Specification: AP | | −40 | | +85 | °C |
| JP | | 0 | | +70 | °C |
| Storage | | −60 | | +100 | °C |
| Thermal Resistance, $\theta_{JA}$,Plastic DIP | | | | 30 | °C/W |

NOTES: (1) For Two's Complement Input Coding invert the MSB with an external logic inverter. (2) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (3) Open DATA input lines will be pulled above +5.5V. See discussion under LOGIC INPUT COMPATIBILITY in the OPERATION section. (4) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (5) Error at input code $800_{HEX}$. (6) Maximum represents the 3σ limit. Not 100% tested for this parameter. (7) For the worst-case code change: $7FF_{HEX}$ to $800_{HEX}$ and $800_{HEX}$ to $7FF_{HEX}$. (8) Crosstalk is defined as the change in any output as a result of any other output being driven from −10V to +10V at rated output current. (9) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

## TIMING DIAGRAMS




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_{CC}$ to ACOM | 0 to +18V |
| $-V_{CC}$ to ACOM | 0 to –18V |
| $+V_{CC}$ to $-V_{CC}$ | 0 to +36V |
| ACOM to DCOM | ±4V |
| Digital Inputs to DCOM | –1V to $+V_{CC}$ |
| External Voltage applied to BPO Resistor | ±18V |
| $V_{REF\ OUT}$ | Indefinite short to ACOM |
| $V_{OUT}$ | Momentary to ±18V |
| Lead Temperature, soldering 10s | +300°C |
| Max Junction Temperature | 165°C |

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| DAC4813AP | 28-Pin Plastic DBL Wide DIP | 215 | –40°C to +85°C |
| DAC4813JP | 28-Pin Plastic DBL Wide DIP | 215 | 0°C to +70°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

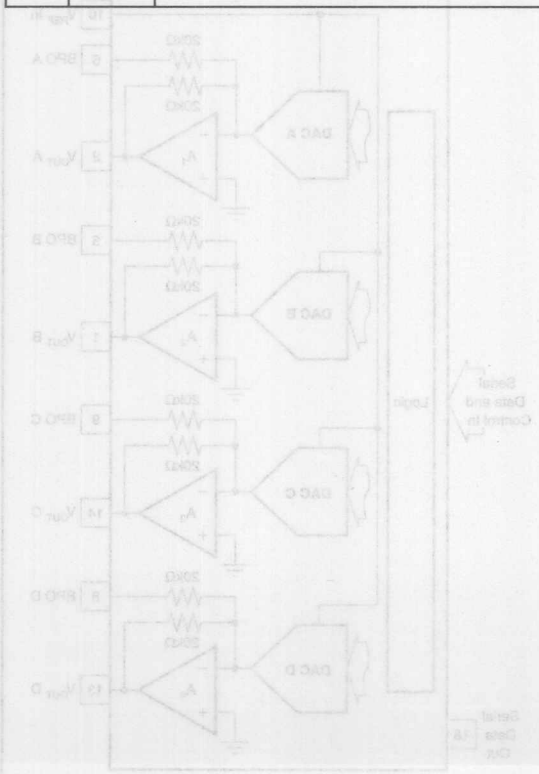
## TRUTH TABLE

| $\overline{WR}$ | $\overline{EN1}$ | $\overline{EN2}$ | $\overline{EN3}$ | $\overline{EN4}$ | $\overline{LDAC}$ | $\overline{RESET}$ | OPERATION |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | 0 | Reset all D/A Latches |
| 1 | X | X | X | X | X | 1 | No Operation |
| X | 1 | 1 | 1 | 1 | 1 | 1 | No Operation |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | Load Data into First Rank for D/A 4 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | Load Data into First Rank for D/A 3 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | Load Data into First Rank for D/A 2 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | Load Data into First Rank for D/A 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | Load Second Rank from First Rank, All D/As |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | All Latches Transparent |

"X" = Don't Care

## PIN DESCRIPTIONS

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | DB11 | DATA, MSB, positive true. |
| 2 | DB10 | DATA |
| 3 | DB9 | DATA |
| 4 | DB8 | DATA |
| 5 | DB7 | DATA |
| 6 | DB6 | DATA |
| 7 | DB5 | DATA |
| 8 | DB4 | DATA |
| 9 | DB3 | DATA |
| 10 | DB2 | DATA |
| 11 | DB1 | DATA |
| 12 | DB0 | DATA, LSB. |
| 13 | $\overline{\text{RESET}}$ | Resets output of all D/As to bipolar-zero. The D/A remains in this state until overwritten by a $\overline{\text{LDAC}}$-$\overline{\text{WR}}$ command. RESET does not reset the input latch. After power–up and reset, input latches will be in an indeterminant state. |
| 14 | $\overline{\text{WR}}$ | Write strobe. Must be low for data transfer to any latch (except RESET). |
| 15 | $\overline{\text{EN1}}$ | Enable for 12-bit input data latch of D/A1. NOTE: This logic path is slower than the $\overline{\text{WR}}$/ path. |
| 16 | $\overline{\text{EN2}}$ | Enable for 12-bit input data latch of D/A2. NOTE: This logic path is slower than the $\overline{\text{WR}}$/ path. |
| 17 | $\overline{\text{EN3}}$ | Enable for 12-bit input data latch of D/A3. NOTE: This logic path is slower than the $\overline{\text{WR}}$ /path. |
| 18 | $\overline{\text{EN4}}$ | Enable for 12-bit input data latch of D/A4. NOTE: This logic path is slower than the $\overline{\text{WR}}$/ path. |
| 19 | $\overline{\text{LDAC}}$ | Load DAC enable. Must be low with $\overline{\text{WR}}$ for data transfer to the D/A latch and simultaneous update of all D/A converters. |
| 20 | DCOM | Digital common, logic currents return. |
| 21 | $-V_{CC}$ | Analog supply input, nominally –12V or –15V referred to ACOM. |
| 22 | ACOM | Analog common, $+V_{CC}$, $-V_{CC}$ supply return. |
| 23 | $+V_{CC}$ | Analog supply input, nominally +12V or +15V referred to ACOM. |
| 24 | $V_{OUT\ 4}$ | D/A 4 analog output. |
| 25 | $V_{OUT\ 3}$ | D/A 3 analog output. |
| 26 | $V_{OUT\ 2}$ | D/A 2 analog output. |
| 27 | $V_{OUT\ 1}$ | D/A 1 analog output. |
| 28 | $V_{REF\ OUT}$ | +10V reference output. |



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# DAC4814

www.burr-brown.com/databook/DAC4814.html

# Quad 12-Bit Digital-to-Analog Converter (Serial Interface)

## FEATURES

- COMPLETE QUAD DAC — INCLUDES INTERNAL REFERENCES AND OUTPUT AMPLIFIERS
- GUARANTEED SPECIFICATIONS OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- HIGH-SPEED SERIAL INTERFACE (10MHz CLOCK)
- LOW POWER: 600mW (150mW/DAC)
- LOW GAIN DRIFT: 5ppm/°C
- LOW NONLINEARITY: ±1/2 LSB max
- UNIPOLAR OR BIPOLAR OUTPUT
- CLEAR/RESET TO UNIPOLAR OR BIPOLAR ZERO

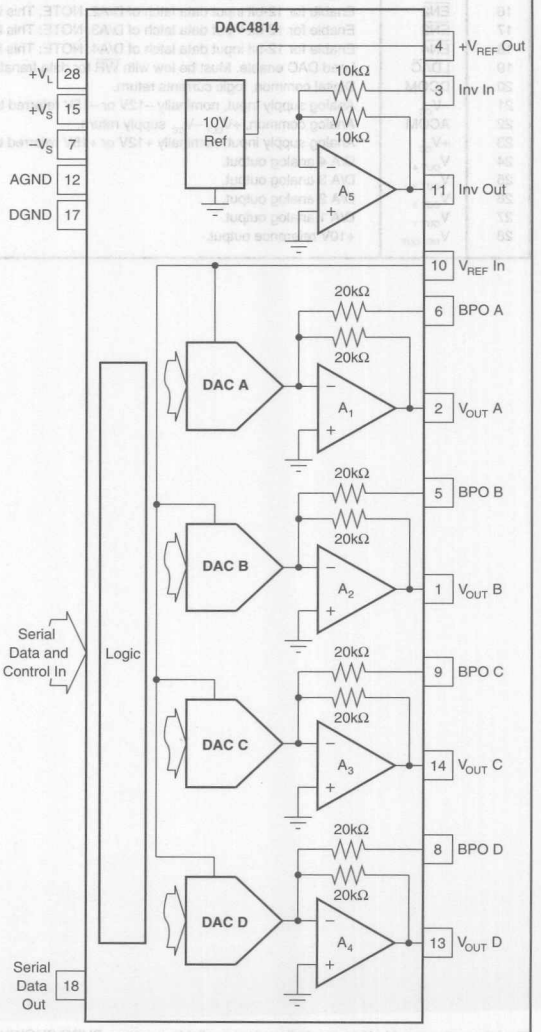
## DESCRIPTION

The DAC4814 is one in a family of dual and quad 12-bit digital-to-analog converters. Serial, 8-bit, 12-bit interfaces are available.

The DAC4814 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for either unipolar 0 to 10V, 0 to –10V, or bipolar ±10V output ranges.

The DAC4814 has a high-speed serial interface capable of being clocked at 10MHz. Serial data are clocked DAC D MSB first into a 48-bit shift register, then strobed into each DAC separately or simultaneously as required. The DAC has an asynchronous clear control for reset to unipolar or bipolar zero depending on the mode selected. This feature is useful for power-on reset or system calibration. The DAC4814 is packaged in a 28-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

## SPECIFICATIONS, Guaranteed over $T_A$ = –40°C to +85°C unless otherwise specified.

### ELECTRICAL

Specifications as shown for $V_S$ = ±12V or ±15V, $V_L$ = +5V, and $R_L$ = 2kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC4814AP MIN | DAC4814AP TYP | DAC4814AP MAX | DAC4814BP MIN | DAC4814BP TYP | DAC4814BP MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **DIGITAL INPUTS** | | | | | | | | |
| Resolution | | 12 | | | * | | | Bits |
| $V_{IH}$ (Input High Voltage) | | +2 | | +5 | * | | * | V |
| $V_{IL}$ (Input Low Voltage) | | 0 | | +0.8 | * | | * | V |
| $I_{IN}$ ( Input Current) | $T_A$ = 25°C | | | ±1 | | | * | µA |
| | $T_A$ = –40°C to +85°C | | | ±10 | | | * | µA |
| $C_{IN}$ (Input Capacitance) | | | 0.8 | | | * | | pF |
| **DIGITAL OUTPUT** | | | | | | | | |
| Data Out $V_{OL}$ | $I_{SINK}$ = 1.6mA | 0 | | +0.4 | * | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +2.4 | | +5 | * | | * | V |
| **ACCURACY** | | | | | | | | |
| Integral, Relative Linearity[1] | | | | ±1 | | | ±1/2 | LSB |
| Differential Nonlinearity[2] | $T_A$ = 25°C | | | ±1 | | | * | LSB |
| | $T_A$ = –40°C to +85°C | | +1.5/–1 | | | | ±1 | LSB |
| Unipolar Offset Error | $T_A$ = +25°C | | | ±1 | | | ±0.5 | mV |
| | $T_A$ = –40°C to +85°C | | | ±3 | | | * | mV |
| Bipolar Zero Error | | | | ±20 | | | ±10 | mV |
| Gain Error Unipolar, Bipolar | With Internal or External 10.0V Ref | | | ±0.2 | | | ±0.15 | % |
| Power Supply Sensitivity[3] | $V_S$ = ±11.4V to ±18V | | | 30 | | | * | ppmFSR/V |
| | $V_L$ = +4.5V to +5.5V | | | | | | | |
| **TEMPERATURE DRIFT** | | | | | | | | |
| Gain Drift Unipolar, Bipolar | | | ±5 | ±30 | | * | ±20 | ppm/°C |
| Unipolar Offset Drift | | | ±0.1 | ±5 | | * | * | ppmFSR/°C |
| Bipolar Zero Drift | | | ±5 | ±15 | | * | ±8 | ppmFSR/°C |
| **REFERENCE OUTPUT** | | | | | | | | |
| Output Voltage | | +9.980 | +10 | +10.020 | +9.985 | * | +10.015 | V |
| Reference Drift | | | ±2 | ±30 | | * | ±20 | ppm/°C |
| Output Current | $T_A$ = 25°C | +10/–5 | | | * | | | mA |
| | $T_A$ = –40°C to +85°C | +6.5/–5 | | | * | | | mA |
| Max Load Capacitance (For Stability) | | | 500 | | | * | | pF |
| Short Circuit Current | | | ±20 | | | * | | mA |
| Load Regulation ($\Delta V_{OUT}$ vs $\Delta I_{LOAD}$) | | | | 40 | | | * | ppm/mA |
| Supply Regulation ($\Delta V_{OUT}$ vs $\Delta V_S$) | | | | ±5 | | | * | ppm/V |
| **INVERTER** | | | | | | | | |
| –10V Reference[4], Inverter Output | | –10.020 | –10 | –9.980 | –10.015 | * | –9.985 | V |
| –10V Reference Drift | | | | ±30 | | | ±20 | ppm/°C |
| DC Output Impedance | | | 0.1 | | | * | | Ω |
| Output Current | | ±7 | | | * | | | mA |
| Max Load Capacitance (For Stability) | | | 200 | | | * | | pF |
| Short Circuit Current | | | ±30 | | | * | | mA |
| **REFERENCE INPUT** | | | | | | | | |
| Reference Input Resistance | | 1.75 | 2.5 | | * | * | | kΩ |
| Inverter Input Resistance | | 7 | 10 | | * | * | | kΩ |
| BPO Input Resistance | | 14 | 20 | | * | * | | kΩ |
| Reference Input Range | | | | ±10 | | | * | V |
| **ANALOG SIGNAL OUTPUTS** | | | | | | | | |
| Voltage Range | | $–V_S$ + 1.4 | | $+V_S$ – 1.4 | * | | * | V |
| DC Output Impedance | | | 0.1 | | | * | | Ω |
| Output Current | | ±5 | | | * | | | mA |
| Max Load Capacitance (For Stability) | $V_{OUT}$ | | 500 | | | * | | pF |
| Short Circuit Current | | | ±30 | | | * | | mA |
| **DYNAMIC PERFORMANCE[5]** | $C_L$ = 100pF | | | | | | | |
| Unipolar Mode Settling Time | To 1/2 LSB of Full Scale | | 2.5 | 10 | | * | * | µs |
| Bipolar Mode Settling Time | To 1/2 LSB of Full Scale | | 3.5 | 10 | | * | * | µs |
| Slew Rate | | | 10 | | | * | | V/µs |
| Small-Signal Bandwidth | | | 3 | | | * | | MHz |
| **ANALOG GROUND CURRENT** (Code Dependent) | | | ±4 | | | * | | mA |
| **DIGITAL CROSSTALK** | Full Scale Transition $C_L$= 100pF | | 3 | | | * | | nV-s |
| **D/A GLITCH IMPULSE** | | | 30 | | | * | | nV-s |

## ELECTRICAL

Specifications as shown for $V_S$ = ±12V or ±15V, $V_L$ = +5V, and $R_L$ = 2kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC4814AP | | | DAC4814BP | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **POWER SUPPLY** | | | | | | | | |
| $+V_S$ and $-V_S$ | | ±11.4 | ±15 | ±18 | * | * | * | V |
| $+V_L$ | | 4.5 | 5 | 5.5 | * | * | * | V |
| $+I_S$ | | | +20 | +24 | | * | * | mA |
| $-I_S$ | | | –20 | –25.5 | | * | * | mA |
| $+I_L$ | Digital Inputs = 0V or $+V_L$ | | 0.4 | 2 | | * | * | mA |
| $+I_L$ | Digital Inputs = $V_{IL}$ or $V_{IH}$ | | | 10 | | | * | mA |
| Total Power, All DACs | | | 600 | 753 | | * | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified | | –40 | | +85 | * | | * | °C |
| Operating | | –40 | | +85 | * | | * | °C |
| Thermal Resistance, $\theta_{JA}$ | | | 75 | | | * | | °C/W |

* Specifications same as DAC4814AP.

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes voltage output DAC, voltage reference, and reference inverter. (4) Inverter output with inverter input connected to $+V_{REF}$. (5) Guaranteed to but not tested.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_L$ to AGND | 0V, +7V |
| $+V_L$ to DGND | 0V, +7V |
| $+V_S$ to AGND | 0V, +18V |
| $-V_S$ to AGND | 0V, –18V |
| AGND to DGND | ±0.3V |
| Any digital input to DGND | –0.3V, $+V_L$ +0.3V |
| Ref In to AGND | ±25V |
| Ref In to DGND | ±25V |
| Storage Temperature Range | –55°C to +125°C |
| Operating Temperature Range | –40°C to +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Junction Temperature | +155°C |
| Output Short Circuit | Continuous to common or $\pm V_S$ |
| Reference Short Circuit | Continuous to common or $+V_S$ |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| DAC4814AP | 28-Pin Plastic DBL Wide DIP | 215 |
| DAC4814BP | 28-Pin Plastic DBL Wide DIP | 215 |

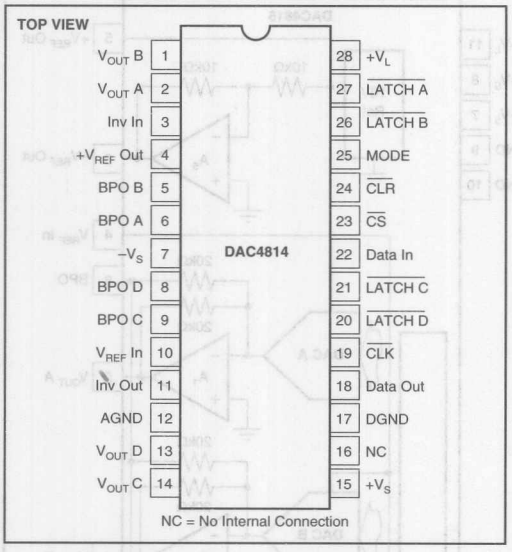
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN DESIGNATIONS

| PIN | DESCRIPTOR | FUNCTION | PIN | DESCRIPTOR | FUNCTION |
|---|---|---|---|---|---|
| 1 | $V_{OUT}$ B | Analog output voltage, DAC B | 28 | $+V_L$ | Positive logic power supply, +5V input |
| 2 | $V_{OUT}$ A | Analog output voltage, DAC A | 27 | $\overline{\text{LATCH A}}$ | Latch data update, logic input, DAC A |
| 3 | Inv In | Inverter ($A_S$) input | 26 | $\overline{\text{LATCH B}}$ | Latch data update, logic input, DAC B |
| 4 | $+V_{REF}$ Out | Positive reference voltage output (+10V output) | 25 | MODE | Selection input for unipolar or bipolar reset to zero |
| 5 | BPO B | Biplolar offset input, DAC B | 24 | $\overline{\text{CLR}}$ | Asynchronous input reset to zero |
| 6 | BPO A | Bipolar offset input, DAC A | 23 | $\overline{\text{CS}}$ | Chip select enable, DAC A, B, C, and D |
| 7 | $-V_S$ | Negative analog power supply , –15V input | 22 | Data In | Serial data input |
| 8 | BPO D | Bipolar offset input, DAC D | 21 | $\overline{\text{LATCH C}}$ | Latch data update, logic input, DAC C |
| 9 | BPO C | Bipolar offset input, DAC C | 20 | $\overline{\text{LATCH D}}$ | Latch data update, logic input, DAC D |
| 10 | $V_{REF}$ In | ± Reference voltage input | 19 | $\overline{\text{CLK}}$ | Clock input |
| 11 | Inv Out | Inverter ($A_S$) output | 18 | Data Out | Serial data output |
| 12 | AGND | Analog common | 17 | DGND | Digital common |
| 13 | $V_{OUT}$ D | Analog output voltage, DAC D | 16 | NC | No internal connection |
| 14 | $V_{OUT}$ C | Analog output voltage, DAC C | 15 | $+V_S$ | Positive analog power supply, +15V input |

## PIN CONFIGURATION



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# DAC4815

www.burr-brown.com/databook/DAC4815.html

# Quad 12-Bit Digital-to-Analog Converter (8-Bit Port Interface)

## FEATURES

- COMPLETE QUAD DAC — INCLUDES INTERNAL REFERENCES AND OUTPUT AMPLIFIERS
- GUARANTEED SPECIFICATIONS OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- HIGH-SPEED 8 + 4-BIT PARALLEL INTERFACE
- LOW POWER, 600mW (150mW/DAC)
- LOW GAIN DRIFT, 5ppm/°C
- LOW NONLINEARITY: ±1/2 LSB max
- BIPOLAR OUTPUT
- CLEAR/RESET TO BIPOLAR ZERO

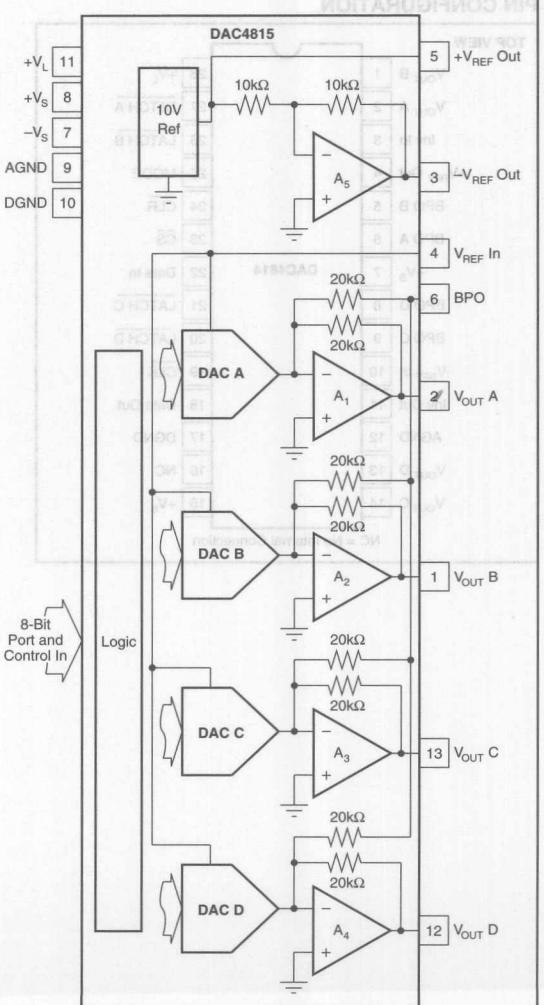
## DESCRIPTION

The DAC4815 is one in a family of dual and quad 12-bit digital-to-analog converters (DACs). Serial, 8-bit, 12-bit interfaces are available.

The DAC4815 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for bipolar ±10V output range.

The DAC4815 has a 2-byte (8 + 4) double-buffered interface. Data is first loaded (level transferred) into the input registers in two steps for each DAC. Then both DACs are updated simultaneously. The DAC has an asynchronous clear control for reset to bipolar zero. This feature is useful for power-on reset or system calibration. The DAC4815 is packaged in a 28-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.




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# SPECIFICATIONS, Guaranteed over $T_A$ = –40°C to +85°C unless otherwise specified.

## ELECTRICAL

Specifications as shown for $V_S$ = ±12V or ±15V, $V_L$ = +5V, and $R_L$ = 2kΩ, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC4815AP MIN | DAC4815AP TYP | DAC4815AP MAX | DAC4815BP MIN | DAC4815BP TYP | DAC4815BP MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **DIGITAL INPUTS** | | | | | | | | |
| Resolution | | 12 | | | * | | | Bits |
| $V_{IH}$ (Input High Voltage) | | 2 | | 5 | * | | * | V |
| $V_{IL}$ (Input Low Voltage) | | 0 | | 0.8 | * | | * | V |
| $I_{IN}$ ( Input Current) | $T_A$ = 25°C | | | ±1 | | | * | µA |
| | $T_A$ = –40°C to +85°C | | | ±10 | | | * | µA |
| $C_{IN}$ (Input Capacitance) | | | 0.8 | | | * | | pF |
| **ACCURACY** | | | | | | | | |
| Integral, Relative Linearity[1] | | | | ±1 | | | ±1/2 | LSB |
| Differential Nonlinearity[2] | $T_A$ = 25°C | | | ±1 | | | * | LSB |
| | $T_A$ = –40°C to +85°C | | ±1.5/–1 | | | | ±1 | LSB |
| Bipolar Zero Error | | | ±20 | | | ±10 | mV | |
| Gain Error | With Internal or External 10.0V Ref | | | ±0.2 | | | ±0.15 | % |
| Power Supply Sensitivity[3] | $V_S$ = ±11.4V to ±18V<br>$V_L$ = +4.5V to +5.5V | | | 30 | | | * | ppmFSR/V |
| **TEMPERATURE DRIFT** | | | | | | | | |
| Gain Drift | | | ±5 | ±30 | | * | ±20 | ppm/°C |
| Bipolar Zero Drift | | | ±5 | ±15 | | * | ±8 | ppmFSR/°C |
| **REFERENCE OUTPUT** | | | | | | | | |
| Output Voltage | | +9.980 | +10 | +10.020 | +9.985 | * | +10.015 | V |
| Reference Drift | | | ±2 | ±30 | | * | ±20 | ppm/°C |
| Output Current | $T_A$ = 25°C | +10/–5 | | | * | | | mA |
| | $T_A$ = –40°C to +85°C | +5/–5 | | | * | | | mA |
| Max Load Capacitance (For Stability) | | | 500 | | | * | | pF |
| Short Circuit Current | | | ±20 | | | * | | mA |
| Load Regulation ($\Delta V_{OUT}$ vs $\Delta I_{LOAD}$) | | | | 40 | | | * | ppm/mA |
| Supply Regulation ($\Delta V_{OUT}$ vs $\Delta V_S$) | | | | ±5 | | | * | ppm/V |
| **–REFERENCE OUTPUT,** Inverter | | | | | | | | |
| –10V Reference | | –10.020 | –10 | –9.980 | –10.015 | * | –9.985 | V |
| –10V Reference Drift | | | | ±30 | | | ±20 | ppm/°C |
| DC Output Impedance | | | 0.1 | | | * | | Ω |
| Output Current | | ±7 | | | * | | | mA |
| Max Load Capacitance (For Stability) | | | 200 | | | * | | pF |
| Short Circuit Current | | | 30 | | | * | | mA |
| **REFERENCE INPUT** | | | | | | | | |
| Reference Input Resistance | | 1.75 | 2.5 | | * | * | | kΩ |
| Inverter Input Resistance | | 7 | 10 | | * | * | | kΩ |
| BPO Input Resistance | | 3.5 | 5 | | * | * | | kΩ |
| Reference Input Range | | | | ±10 | | | * | V |
| **ANALOG SIGNAL OUTPUTS** | | | | | | | | |
| Voltage Range | | $–V_S$ + 1.4 | | $+V_S$ – 1.4 | * | | * | V |
| DC Output Impedance | | | 0.1 | | | * | | Ω |
| Output Current | | ±5 | | | * | | | mA |
| Max Load Capacitance (For Stability) | $V_{OUT}$ | | 500 | | | * | | pF |
| Short Circuit Current | | | ±30 | | | * | | mA |
| **DYNAMIC PERFORMANCE[4]** | $C_L$ = 100pF | | | | | | | |
| Settling Time | To 1/2 LSB of Full Scale | | 3.5 | 10 | | * | * | µs |
| Slew Rate | | | 10 | | | * | | V/µs |
| Small-Signal Bandwidth | | | 3 | | | * | | MHz |
| **ANALOG GROUND CURRENT** (Code Dependent) | | | ±4 | | | * | | mA |
| **DIGITAL CROSSTALK** | Full Scale Transition<br>$C_L$ = 100pF | | 3 | | | * | | nV-s |
| **DIGITAL-TO-ANALOG GLITCH IMPULSE** | | | 30 | | | * | | nV-s |
| **POWER SUPPLY** | | | | | | | | |
| $+V_S$ and $–V_S$ | | ±11.4 | ±15 | ±18 | * | * | * | V |
| $+V_L$ | | 4.5 | 5 | 5.5 | * | * | * | V |
| $+I_S$ | | | +20 | +24 | | * | * | mA |
| $–I_S$ | | | –20 | –25.5 | | * | * | mA |
| $+I_L$ | Digital Inputs = 0V or $+V_L$ | | 0.4 | 2 | | * | * | mA |
| $+I_L$ | Digital Inputs = $V_{IL}$ or $V_{IH}$ | | | 10 | | | * | mA |
| Total Power, All DACs | | | 600 | 753 | | * | * | mW |

## SPECIFICATIONS (CONT), Guaranteed over $T_A$ = –40°C to +85°C unless otherwise specified.

### ELECTRICAL

Specifications as shown for $V_S$ = ±12V or ±15V, $V_L$ = +5V, and $R_L$ = 2kΩ unless otherwise noted.

| PARAMETER | CONDITIONS | DAC4815AP | | | DAC4815BP | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified | | –40 | | +85 | * | | * | °C |
| Operating | | –40 | | +85 | * | | * | °C |
| Thermal Resistance, $\theta_{JA}$ | | | 75 | | | * | | °C/W |

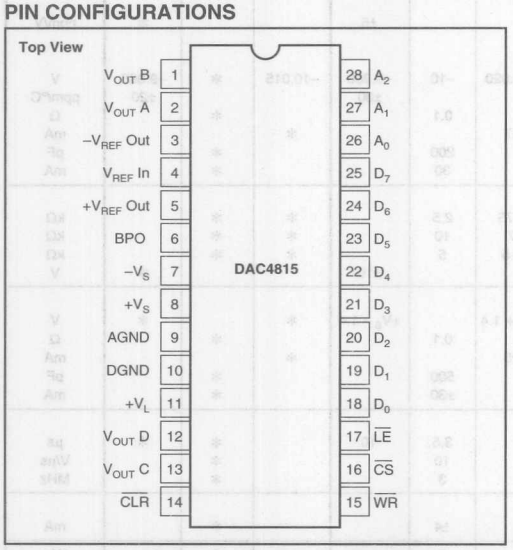
* Specifications same as DAC4815AP.

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes effect of voltage output DAC, voltage references. (4) Guaranteed but not tested.

### PIN DESIGNATIONS

| PIN | DESCRIPTOR | FUNCTION | PIN | DESCRIPTOR | FUNCTION |
|---|---|---|---|---|---|
| 1 | $V_{OUT}$ B | Analog output voltage, DAC B | 28 | $A_2$ | Address line 2 input |
| 2 | $V_{OUT}$ A | Analog output voltage, DAC A | 27 | $A_1$ | Address line 1 input |
| 3 | $-V_{REF}$ Out | Negative reference voltage output (–10V output) | 26 | $A_0$ | Address line 0 input |
| 4 | $V_{REF}$ In | ± Reference voltage input | 25 | $D_7$ | Data bit 7 input |
| 5 | $+V_{REF}$ Out | Positive reference voltage output (+10V output) | 24 | $D_6$ | Data bit 6 input |
| 6 | BPO | Bipolar offset input, DAC A, B, C, and D | 23 | $D_5$ | Data bit 5 input |
| 7 | $-V_S$ | Negative analog power supply, –15V input | 22 | $D_4$ | Data bit 4 input |
| 8 | $+V_S$ | Positive analog power supply, +15V input | 21 | $D_3$ | Data bit 3 input |
| 9 | AGND | Analog common | 20 | $D_2$ | Data bit 2 input |
| 10 | DGND | Digital common | 19 | $D_1$ | Data bit 1 input |
| 11 | $+V_L$ | Positive logic power supply, +5V input | 18 | $D_0$ | Data bit 0 input |
| 12 | $V_{OUT}$ D | Analog output voltage, DAC D | 17 | $\overline{LE}$ | Latch data enable, DAC A, B, C, and D |
| 13 | $V_{OUT}$ C | Analog output voltage, DAC C | 16 | $\overline{CS}$ | Chip select enable, DAC A, B, C, and D |
| 14 | $\overline{CLR}$ | Asynchronous input reset to zero | 15 | $\overline{WR}$ | Write input, DAC A, B, C, and D |

### PIN CONFIGURATIONS




### PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | LINEARITY ERROR (LSB) |
|---|---|---|---|
| DAC4815AP | 28-Pin Plastic DIP | 215 | ±1 |
| DAC4815BP | 28-Pin Plastic DIP | 215 | ±1/2 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_L$ to AGND | 0V, +7V |
| $+V_L$ to DGND | 0V, +7V |
| $+V_S$ to AGND | 0V, +18V |
| $-V_S$ to AGND | 0V, –18V |
| AGND to DGND | ±0.3V |
| Any digital input to GND | –0.3V, $+V_L$ +0.3V |
| Ref In to AGND | ±25V |
| Ref In to DGND | ±25V |
| Storage Temperature Range | –55°C to +125°C |
| Operating Temperature Range | –40°C to +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Junction Temperature | +155°C |
| Output Short Circuit | Continuous to common or $\pm V_S$ |
| Reference Short Circuit | Continuous to common or $+V_S$ |

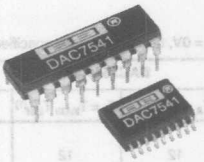
### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# DAC7541

www.burr-brown.com/databook/DAC7541.html



# Low Cost 12-Bit CMOS Four-Quadrant Multiplying DIGITAL-TO-ANALOG CONVERTER

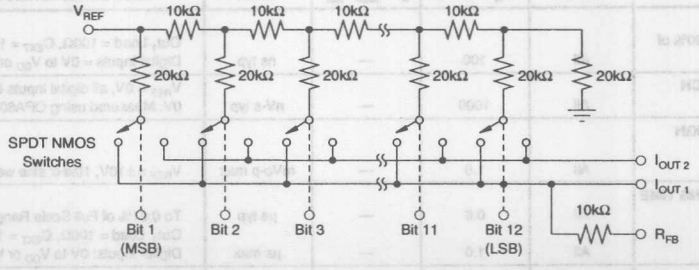
## FEATURES

- FULL FOUR-QUADRANT MULTIPLICATION
- 12-BIT END-POINT LINEARITY
- DIFFERENTIAL LINEARITY ±1/2LSB MAX OVER TEMPERATURE
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- TTL-/CMOS-COMPATIBLE
- SINGLE +5V TO +15V SUPPLY
- LATCH-UP RESISTANT
- 7521/7541/7541A REPLACEMENT
- PACKAGES: Plastic DIP, Plastic SOIC
- LOW COST

## DESCRIPTION

The Burr-Brown DAC7541A is a low cost 12-bit, four-quadrant multiplying digital-to-analog converter. Laser-trimmed thin-film resistors on a monolithic CMOS circuit provide true 12-bit integral and differential linearity over the full specified temperature range.

DAC7541A is a direct, improved pin-for-pin replacement for 7521, 7541, and 7541A industry standard parts. In addition to a standard 18-pin plastic package, the DAC7541A is also available in a surface-mount plastic 18-pin SOIC.




Digital Inputs (DTL-/TTL-/CMOS-compatible)
Logic: A switch is closed to $I_{OUT\ 1}$ for its digital input in a "HIGH" state.

Switches shown for digital inputs "HIGH".

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

## ELECTRICAL

At +25°C, $+V_{DD}$ = +12V or +15V, $V_{REF}$ = +10V, $V_{PIN\ 1} = V_{PIN\ 2}$ = 0V, unless otherwise specified.

| PARAMETER | DAC7541A GRADE | $T_A$ = +25°C | $T_A = T_{MAX}, T_{MIN}$[1] | UNITS | TEST CONDITIONS/COMMENTS |
|---|---|---|---|---|---|
| **ACCURACY** | | | | | |
| Resolution | All | 12 | 12 | Bits | |
| Relative Accuracy | J | ±1 | ±1 | LSB max | ±1LSB = ±0.024% of FSR. |
| | K | ±1/2 | ±1/2 | LSB max | ±1/2LSB = ±0.012% of FSR. |
| Differential Non-linearity | J | ±1 | ±1 | LSB max | All grades guaranteed monotonic to 12 bits, |
| | K | ±1/2 | ±1/2 | LSB max | $T_{MIN}$ to $T_{MAX}$. |
| Gain Error | J | ±6 | ±8 | LSB max | Measured using internal $R_{FB}$ and includes effect |
| | K | ±1 | ±3 | LSB max | of leakage current and gain T.C. |
| | | | | | Gain error can be trimmed to zero. |
| Gain Temperature Coefficient | | | | | |
| (ΔGain/ΔTemperature) | ALL | | 5 | ppm/°C max | Typical value is 2ppm/°C. |
| Output Leakage Current: $Out_1$ (Pin 1) | J, K | ±5 | ±10 | nA max | All digital inputs = 0V. |
| $Out_2$ (Pin 2) | J, K | ±5 | ±10 | nA max | All digital inputs = $V_{DD}$. |
| **REFERENCE INPUT** | | | | | |
| Voltage (Pin 17 to GND) | All | −10/+10 | −10/+10 | V min/max | |
| Input Resistance (Pin 17 to GND) | All | 7-18 | 7-18 | kΩ min/max | |
| | | | | | Typical input resistance = 11kΩ. |
| | | | | | Typical input resistance temperature coefficient is |
| | | | | | −50ppm/°C. |
| **DIGITAL INPUTS** | | | | | |
| $V_{IN}$ (Input HIGH Voltage) | All | 2.4 | 2.4 | V min | |
| $V_{IL}$ (Input LOW Voltage) | All | 0.8 | 0.8 | V max | |
| $I_{IN}$ (Input Current) | All | ±1 | ±1 | µA max | Logic inputs are MOS gates. |
| | | | | | $I_{IN}$ typ (25°C) = 1nA |
| $C_{IN}$ (Input Capacitance)[2] | All | 8 | 8 | pF max | $V_{IN}$ = 0V |
| **POWER SUPPLY REJECTION** | | | | | |
| ΔGain/$\Delta V_{DD}$ | All | ±0.01 | ±0.02 | % per % max | $V_{DD}$ = +11.4V to +16V |
| **POWER SUPPLY** | | | | | |
| $V_{DD}$ Range | All | +5 to +16 | +5 to +16 | V min to V max | Accuracy is not guaranteed over this range. |
| $I_{DD}$ | All | 2 | 2 | mA max | All digital inputs $V_{IL}$ or $V_{IN}$. |
| | All | 100 | 500 | µA max | All digital inputs 0V or $V_{DD}$. |

NOTES: (1) Temperature ranges are: = 0°C to + 70°C for JP, KP, JU and KU versions. (2) Guaranteed by design but not production tested.

## AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not production tested.
$V_{DD}$ = +15V, $V_{REF}$ = +10V except where stated, $V_{PIN\ 1} = V_{PIN\ 2}$ = 0V, output amp is OPA606 except where stated.

| PARAMETER | DAC7541A GRADE | $T_A$ = +25°C | $T_A = T_{MAX}, T_{MIN}$[1] | UNITS | TEST CONDITIONS/COMMENTS |
|---|---|---|---|---|---|
| **PROPAGATION DELAY** | | | | | |
| (from Digital Input change to 90% of | | | | | $Out_1$ Load = 100Ω, $C_{EXT}$ = 13pF. |
| final Analog Output) | All | 100 | — | ns typ | Digital Inputs = 0V to $V_{DD}$ or $V_{DD}$ to 0V. |
| **DIGITAL-TO-ANALOG GLITCH IMPULSE** | All | 1000 | — | nV-s typ | $V_{REF}$ = 0V, all digital inputs 0V to $V_{DD}$ or $V_{DD}$ to 0V. Measured using OPA606 as output amplifier. |
| **MULTIPLYING FEEDTHROUGH ERROR** | | | | | |
| ($V_{REF}$ to $Out_1$) | All | 1.0 | — | mVp-p max | $V_{REF}$ = ±10V, 10kHz sine wave. |
| **OUTPUT CURRENT SETTLING TIME** | All | 0.6 | — | µs typ | To 0.01% of Full Scale Range. |
| | | | | | $Out_1$ Load = 100Ω, $C_{EXT}$ = 13pF. |
| | All | 1.0 | — | µs max | Digital Inputs: 0V to $V_{DD}$ or $V_{DD}$ to 0V. |
| **OUTPUT CAPACITANCE** | | | | | |
| $C_{OUT\ 1}$ (Pin 1) | All | 100 | 100 | pF max | Digital Inputs = $V_{IH}$ |
| $C_{OUT\ 2}$ (Pin 2) | All | 60 | 60 | pF max | Digital Inputs = $V_{IH}$ |
| $C_{OUT\ 1}$ (Pin 1) | All | 70 | 70 | pF max | Digital Inputs = $V_{IL}$ |
| $C_{OUT\ 2}$ (Pin 2) | All | 100 | 100 | pF max | Digital Inputs = $V_{IL}$ |

NOTE: (1) Temperature ranges are: = 0°C to + 70°C for JP, KP, JU and KU versions.

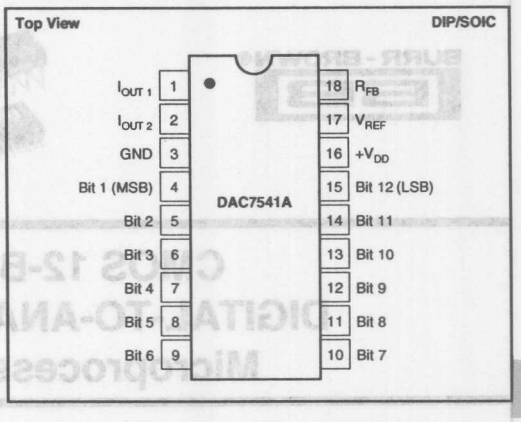
## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| $V_{DD}$ (Pin 16) to Ground | +17V |
| $V_{REF}$ (Pin 17) to Ground | +25V |
| $V_{RFB}$ (Pin 18) to Ground | ±25V |
| Digital Input Voltage (pins 4-15) to Ground | –0.4V, $V_{DD}$ |
| $V_{PIN\ 1}$, $V_{PIN\ 2}$ to Ground | –0.4V, $V_{DD}$ |
| Power Dissipation (any Package): | |
| To +75°C | 450mW |
| Derates above +75°C | –6mW/°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Storage Temperature: Plastic Package | +125°C |

NOTE: (1) Stresses above those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## PIN CONNECTIONS

Top View DIP/SOIC




## ELECTROSTATIC DISCHARGE SENSITIVITY

The DAC7541A is an ESD (electrostatic discharge) sensitive device. The digital control inputs have a special FET structure, which turns on when the input exceeds the supply by 18V, to minimize ESD damage. However, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

## BURN-IN SCREENING

Burn-in screening is an option available for the models in the Ordering Information table. Burn-in duration is 160 hours at the indicated temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| DAC7541JP | Plastic DIP | 218 |
| DAC7541KP | Plastic DIP | 218 |
| DAC7541JU | Plastic SOIC | 219 |
| DAC7541KU | Plastic SOIC | 219 |
| DAC7541JP-BI | Plastic DIP | 218 |
| DAC7541KP-BI | Plastic DIP | 218 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

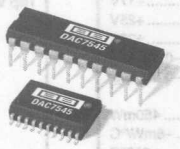
| PRODUCT | PACKAGE | TEMPERATURE RANGE | RELATIVE ACCURACY (LSB) | GAIN ERROR (LSB) |
|---|---|---|---|---|
| DAC7541AJP | Plastic DIP | 0°C to +70°C | ±1 | ±6 |
| DAC7541AKP | Plastic DIP | 0°C to +70°C | ±1/2 | ±1 |
| DAC7541AJU | Plastic SOIC | 0°C to +70°C | ±1 | ±6 |
| DAC7541AKU | Plastic SOIC | 0°C to +70°C | ±1/2 | ±1 |

**BURN-IN SCREENING OPTION**
See text for details.

| PRODUCT | PACKAGE | TEMPERATURE RANGE | RELATIVE ACCURACY (LSB) | BURN-IN TEMP. (160 Hours)[1] |
|---|---|---|---|---|
| DAC7541AJP-BI | Plastic DIP | 0°C to +70°C | ±1 | +85°C |
| DAC7541AKP-BI | Plastic DIP | 0°C to +70°C | ±1/2 | +85°C |

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# DAC7545

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# CMOS 12-Bit Multiplying DIGITAL-TO-ANALOG CONVERTER Microprocessor Compatible

## FEATURES

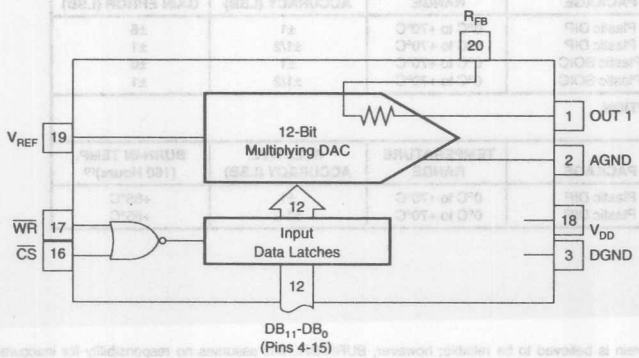
- FOUR-QUADRANT MULTIPLICATION
- LOW GAIN TC: 2ppm/°C typ
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- SINGLE 5V TO 15V SUPPLY
- TTL/CMOS LOGIC COMPATIBLE
- LOW OUTPUT LEAKAGE: 10nA max
- LOW OUTPUT CAPACITANCE: 70pF max
- DIRECT REPLACEMENT FOR AD7545, PM-7545

## DESCRIPTION

The DAC7545 is a low-cost CMOS, 12-bit four-quadrant multiplying, digital-to-analog converter with input data latches. The input data is loaded into the DAC as a 12-bit data word. The data flows through to the DAC when both the chip select ($\overline{CS}$) and the write ($\overline{WR}$) pins are at a logic low.

Laser-trimmed thin-film resistors and excellent CMOS voltage switches provide true 12-bit integral and differential linearity. The device operates on a single +5V to +15V supply and is available in 20-pin plastic DIP or 20-lead plastic SOIC packages. Devices are specified over the commercial.

The DAC7545 is well suited for battery or other low power applications because the power dissipation is less than 0.5mW when used with CMOS logic inputs and $V_{DD}$ = +5V.




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# SPECIFICATIONS

## ELECTRICAL

$V_{REF}$ = +10V, $V_{OUT\,1}$ = 0V, ACOM = DCOM, unless otherwise specified.

| PARAMETER | GRADE | DAC7545 $V_{DD}$ = +5V $T_A$ = +25°C | DAC7545 $V_{DD}$ = +5V $T_{MAX}$-$T_{MIN}$[1] | DAC7545 $V_{DD}$ = +15V $T_A$ = +25°C | DAC7545 $V_{DD}$ = +15V $T_{MAX}$-$T_{MIN}$[1] | UNITS | TEST CONDITIONS/COMMENTS |
|---|---|---|---|---|---|---|---|
| **STATIC PERFORMANCE** | | | | | | | |
| Resolution | All | 12 | 12 | 12 | 12 | Bits | |
| Accuracy | J | ±2 | ±2 | ±2 | ±2 | LSB | |
| | K | ±1 | ±1 | ±1 | ±1 | LSB | |
| | L | ±1/2 | ±1/2 | ±1/2 | ±1/2 | LSB | |
| | GL | ±1/2 | ±1/2 | ±1/2 | ±1/2 | LSB | |
| Differential Nonlinearity | J | ±4 | ±4 | ±4 | ±4 | LSB | 10-Bit Monotonic, $T_{MIN}$ to $T_{MAX}$ |
| | K | ±1 | ±1 | ±1 | ±1 | LSB | 10-Bit Monotonic, $T_{MIN}$ to $T_{MAX}$ |
| | L | ±1 | ±1 | ±1 | ±1 | LSB | 12-Bit Monotonic, $T_{MIN}$ to $T_{MAX}$ |
| | GL | ±1 | ±1 | ±1 | ±1 | LSB | 12-Bit Monotonic, $T_{MIN}$ to $T_{MAX}$ |
| Gain Error (with internal $R_{FB}$)[2] | J | ±20 | ±20 | ±25 | ±25 | LSB | D/A register loaded with $FFF_H$. Gain error is adjustable using the circuits in Figures 2 and 3. |
| | K | ±10 | ±10 | ±15 | ±15 | LSB | |
| | L | ±5 | ±6 | ±10 | ±10 | LSB | |
| | GL | ±2 | ±3 | ±6 | ±7 | LSB | |
| Gain Temperature Coefficient[3] (ΔGain/ΔTemperature) | All | ±5 | ±5 | ±10 | ±10 | ppm/°C for $V_{DD}$ = +5 | Typical value is 2ppm/°C |
| DC Supply Rejection[3] (ΔGain/Δ$V_{DD}$) | All | 0.015 | 0.03 | 0.01 | 0.02 | %/% | Δ$V_{DD}$ ±5% |
| Output Leakage Current at Out 1 | J, K, L, GL | 10 | 50 | 10 | 50 | nA | $DB_0$-$DB_{11}$ = 0V; $\overline{WR}$, $\overline{CS}$ = 0V |
| **DYNAMIC PERFORMANCE** | | | | | | | |
| Current Settling Time[3] | All | 2 | 2 | 2 | 2 | µs | To 1/2LSB. $Out_1$ Load = 100Ω |
| Propagation Delay[3] (from digital input change to 90% of final analog output) | All | 300 | | 250 | | ns | DAC output measured from falling edge of $\overline{WR}$. $\overline{CS}$ = 0V. $Out_1$ Load = 100Ω. $C_{EXT}$ = 13pF[4] |
| Glitch Energy | All | 400 | | 250 | | nV-s[5] | $V_{REF}$ = ACOM |
| AC Feedback at $I_{OUT}$ 1 | All | 5 | 5 | 5 | 5 | mVp-p[5] | $V_{REF}$ = ±10V, 10kHz Sine Wave |
| **REFERENCE INPUT** | | | | | | | |
| Input Resistance (pin 19 to AGND) | All | 7<br>25 | 7<br>25 | 7<br>25 | 7<br>25 | kΩ[6]<br>kΩ | Input resistance TC = 300ppm/°C[5] |
| **AC OUTPUTS** | | | | | | | |
| Output Capacitance[3]: $C_{OUT\,1}$ | All | 70 | 70 | 70 | 70 | pF | $DB_0$-$DB_{11}$ = 0V; $\overline{WR}$, $\overline{CS}$ = 0V |
| $C_{OUT\,2}$ | All | 200 | 200 | 200 | 200 | pF | $DB_0$-$DB_{11}$ = $V_{DD}$; $\overline{WR}$, $\overline{CS}$ = 0V |
| **DIGITAL INPUTS** | | | | | | | |
| $V_{IH}$ (Input HIGH Voltage) | All | 2.4 | 2.4 | 13.5 | 13.5 | V[6] | |
| $V_{IL}$ (Input LOW Voltage) | All | 0.8 | 0.8 | 1.5 | 1.5 | V | |
| $I_{IN}$ (Input Current)[7] | All | ±1 | ±10 | ±1 | ±10 | µA | $V_{IN}$ = 0 or $V_{DD}$ |
| Input Capacitance[3]: $DB_0$-$DB_{11}$ | All | 5 | 5 | 5 | 5 | pF | $V_{IN}$ = 0V |
| $\overline{WR}$, $\overline{CS}$ | All | 20 | 20 | 20 | 20 | pF | $V_{IN}$ = 0V |
| **SWITCHING CHARACTERISTICS[8]** | | | | | | | |
| Chip Select to Write Setup Time, $t_{CS}$ | All | 280 | 380 | 180 | 200 | ns[6] | See Timing Diagram |
| | | 200 | 270 | 120 | 150 | ns[5] | |
| Chip Select to Write Hold Time, $t_{CH}$ | All | 0 | 0 | 0 | 0 | ns[6] | |
| Write Pulse Width, $t_{WR}$ | All | 250 | 400 | 160 | 240 | ns[6] | $t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$ |
| | | 175 | 280 | 100 | 170 | ns[5] | |
| Data Setup Time, $t_{DS}$ | All | 140 | 210 | 90 | 120 | ns[6] | |
| | | 100 | 150 | 60 | 80 | ns[5] | |
| Data Hold Time, $t_{DH}$ | All | 10 | 10 | 10 | 10 | ns[6] | |
| **POWER SUPPLY, $I_{DD}$** | | | | | | | |
| | All | 2 | 2 | 2 | 2 | mA | All Digital Inputs $V_{IL}$ or $V_{IH}$ |
| | All | 100 | 500 | 100 | 500 | µA | All Digital Inputs 0V or $V_{DD}$ |
| | All | 10 | 10 | 10 | 10 | µA[5] | All Digital Inputs 0V or $V_{DD}$ |

NOTES: (1) Temperature ranges—J, K, L, GL: –40°C to +85°C. (2) This includes the effect of 5ppm max, gain TC. (3) Guaranteed but not tested. (4) $DB_0$-$DB_{11}$ = 0V to $V_{DD}$ or $V_{DD}$ to 0V. (5) Typical. (6) Minimum. (7) Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA. (8) Sample tested at +25°C to ensure compliance.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

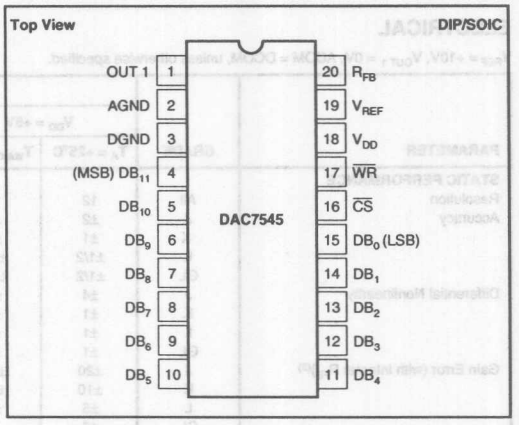
## ABSOLUTE MAXIMUM RATINGS[1]

$T_A$ = +25°C, unless otherwise noted.

| | |
|---|---|
| $V_{DD}$ to DGND | –0.3V, +17 |
| Digital Input to DGND | –0.3V, $V_{DD}$ |
| $V_{RFB}$, $V_{REF}$, to DGND | ±25V |
| $V_{PIN\ 1}$ to DGND | –0.3V, $V_{DD}$ |
| AGND to DGND | –0.3V, $V_{DD}$ |
| Power Dissipation: Any Package to +75°C | 450mW |
| Derates above +75°C by | 6mW/°C |
| Operating Temperature: | |
| Commercial J, K, L, GL | –40°C to +85°C |
| Storage Temperature | –65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## PIN CONNECTIONS




## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | TEMPERATURE RANGE | RELATIVE ACCURACY (LSB) | GAIN ERROR (LSB) $V_{DD}$ = +5V | PACKAGE DRAWING NUMBER[1] |
|---|---|---|---|---|---|
| DAC7545JP | 20-Pin Plastic PDIP | –40°C to +85°C | ±2 | ±20 | 222 |
| DAC7545KP | 20-Pin Plastic PDIP | –40°C to +85°C | ±1 | ±10 | 222 |
| DAC7545LP | 20-Pin Plastic PDIP | –40°C to +85°C | ±1/2 | ±5 | 222 |
| DAC7545GLP | 20-Pin Plastic PDIP | –40°C to +85°C | ±1/2 | ±2 | 222 |
| DAC7545JU | 20-Pin Plastic SOIC | –40°C to +85°C | ±2 | ±20 | 221 |
| DAC7545KU | 20-Pin Plastic SOIC | –40°C to +85°C | ±1 | ±10 | 221 |
| DAC7545LU | 20-Pin Plastic SOIC | –40°C to +85°C | ±1/2 | ±5 | 221 |
| DAC7545GLU | 20-Pin Plastic SOIC | –40°C to +85°C | ±1/2 | ±2 | 221 |

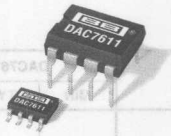
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integral circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

BURR-BROWN®



# DAC7611

www.burr-brown.com/databook/DAC7611.html

# 12-Bit Serial Input DIGITAL-TO-ANALOG CONVERTER



## FEATURES

- LOW POWER: 2.5mW
- 1mV LSB WITH 4.095V FULL-SCALE RANGE
- COMPLETE WITH REFERENCE
- 12-BIT LINEARITY AND MONOTONICITY OVER INDUSTRIAL TEMP RANGE
- ASYNCHRONOUS RESET TO 0V
- 3-WIRE INTERFACE: Up to 20MHz Clock

## APPLICATIONS

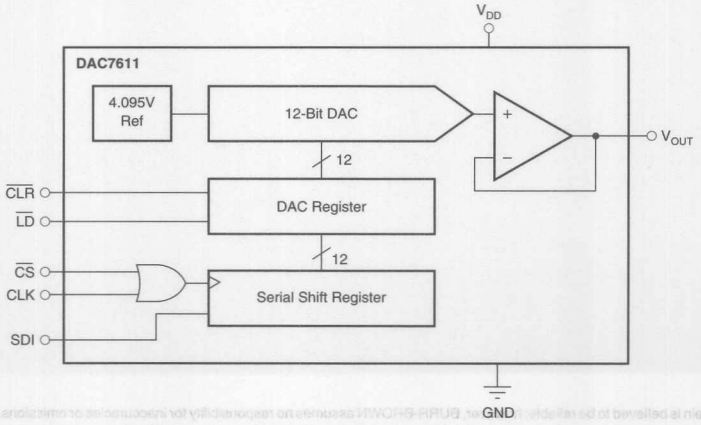
- PROCESS CONTROL
- DATA ACQUISITION SYSTEMS
- CLOSED-LOOP SERVO-CONTROL
- PC PERIPHERALS
- PORTABLE INSTRUMENTATION

## DESCRIPTION

The DAC7611 is a 12-bit digital-to-analog converter (DAC) with guaranteed 12-bit monotonicity performance over the industrial temperature range. It requires a single +5V supply and contains an input shift register, latch, 4.095V reference, DAC, and high speed rail-to-rail output amplifier. For a full-scale step, the output will settle to 0.012% within 10µs. The device consumes 2.5mW (0.5mA at 5V).

The synchronous serial interface is compatible with a wide variety of DSPs and microcontrollers. Clock (CLK), serial data in (SDI), and load strobe ($\overline{LD}$) comprise the serial interface. In addition, two control pins provide a chip select ($\overline{CS}$) function and an asynchronous clear ($\overline{CLR}$) input. The $\overline{CLR}$ input can be used to ensure that the DAC7611 output is 0V on power-up or as required by the application.

The DAC7611 is available in an 8-lead SOIC or 8-pin plastic DIP package and is fully specified over the industrial temperature range of –40°C to +85°C.




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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = –40°C to +85°C, and $V_{DD}$ = +5V, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC7611P, U | | | DAC7611PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ACCURACY** | | | | | | | | |
| Resolution | | 12 | | | * | | | Bits |
| Relative Accuracy[1] | | –1 | ±1/4 | +1 | –0.5 | ±1/8 | +0.5 | LSB |
| Differential Nonlinearity | No Missing Codes | –1 | ±1/2 | +1 | –0.5 | ±1/4 | +0.5 | LSB |
| Zero-Scale Error | Code $000_H$ | –1 | +1 | +3 | * | * | * | LSB |
| Full Scale Voltage | Code $FFF_H$ | 4.079 | 4.095 | 4.111 | 4.087 | 4.095 | 4.103 | V |
| **ANALOG OUTPUT** | | | | | | | | |
| Output Current | Code $800_H$ | ±5 | ±7 | | * | * | | mA |
| Load Regulation | $R_{LOAD} \geq 402\Omega$, Code $800_H$ | | 1 | 3 | | * | * | LSB |
| Capacitive Load | No Oscillation | | 500 | | | * | | pF |
| Short Circuit Current | | | ±10 | | | * | | mA |
| Short Circuit Duration | GND or $V_{DD}$ | | Indefinite | | | * | | |
| **DIGITAL INPUT** | | | | | | | | |
| Data Format | | | Serial | | | * | | |
| Data Coding | | | Straight Binary | | | * | | |
| Logic Family | | | TTL | | | * | | |
| Logic Levels | | | | | | | | |
| $V_{DD}$ | | 2.4 | | | * | | | V |
| $V_{IL}$ | | | | 0.8 | | | * | V |
| $I_{IH}$ | | | | ±10 | | | * | µA |
| $I_{IL}$ | | | | ±10 | | | * | µA |
| **DYNAMIC PERFORMANCE** | | | | | | | | |
| Settling Time[2] | To ±1 LSB of Final Value | | 10 | | | * | | µs |
| DAC Glitch | | | TBD | | | * | | nV-s |
| Digital Feedthrough | | | 2 | | | * | | nV-s |
| Output Noise Voltage | 10Hz to 100kHz | | 120 | | | * | | $nV\sqrt{Hz}$ |
| **POWER SUPPLY** | | | | | | | | |
| $V_{DD}$ | | +4.75 | +5.0 | +5.25 | * | * | * | V |
| $I_{DD}$ | $V_{IH}$ = 5V, $V_{IL}$ = 0V, No Load | | 0.5 | 1 | | * | * | mA |
| Power Dissipation | $V_{IH}$ = 5V, $V_{IL}$ = 0V, No Load | | 2.5 | 5 | | * | * | mW |
| Power Supply Sensitivity | $\Delta V_{DD}$ = ±5% | | 0.001 | 0.004 | | * | * | %/% |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | °C |

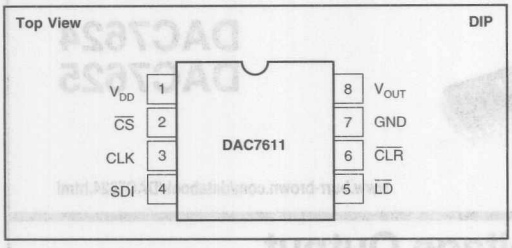
* Same specification as for DAC7611P, U.

NOTES: (1) This term is sometimes referred to as Linearity Error or Integral Nonlinearity (INL). (2) Specification does not apply to negative-going transitions where the final output voltage will be within 6 LSBs of ground. In this region, settling time may be double the value indicated.

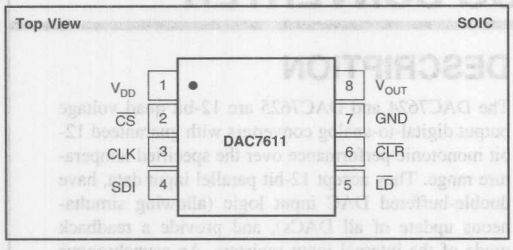


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## PIN CONFIGURATION




## PIN CONFIGURATION




## PIN DESCRIPTION

| PIN | LABEL | DESCRIPTION |
|---|---|---|
| 1 | $V_{DD}$ | Power Supply |
| 2 | $\overline{CS}$ | Chip Select (active LOW). Can be used instead of CLK for the Serial Data Input (with CLK tied LOW). |
| 3 | CLK | Synchronous Clock for the Serial Data Input. This pin can be tied LOW and $\overline{CS}$ used to provide the clock function. |
| 4 | SDI | Serial Data Input. Data is clocked into the internal serial register on the rising edge of CLK or $\overline{CS}$. |
| 5 | $\overline{LD}$ | Loads the Internal DAC Register. NOTE: The DAC register is a transparent latch and is transparent when $\overline{LD}$ is LOW (regardless of the state of $\overline{CS}$ or CLK). |
| 6 | $\overline{CLR}$ | Asynchronous Input to Clear the DAC Register. When $\overline{CLR}$ is strobbed LOW, the DAC register is set to $000_H$ and the output voltage to 0V. |
| 7 | GND | Ground |
| 8 | $V_{OUT}$ | Voltage Output. Fixed output voltage range of approximately 0V to 4.095V (1mV/LSB). The internal reference maintains this output range over time, temperature, and power supply variations (within the values defined in the specifications section). |

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| $V_{DD}$ to GND | –0.3V to 6V |
| Digital Inputs to GND | –0.3V to $V_{DD}$ + 0.3V |
| $V_{OUT}$ to GND | –0.3V to $V_{DD}$ + 0.3V |
| Power Dissipation | 325mW |
| Thermal Resistance, $\theta_{JA}$ | 150°C/W |
| Maximum Junction Temperature | +150°C |
| Operating Temperature Range | –40°C to +85°C |
| Storage Temperature Range | –65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

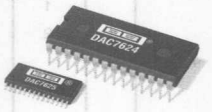
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | MINIMUM RELATIVE ACCURACY (LSB) | DIFFERENTIAL NONLINEARITY (LSB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|---|---|---|
| DAC7611P | ±1 | ±1 | –40°C to +85°C | 8-Pin DIP | 006 |
| DAC7611U | ±1 | ±1 | –40°C to +85°C | 8-Lead SOIC | 182 |
| DAC7611PB | ±0.5 | ±0.5 | –40°C to +85°C | 8-Pin DIP | 006 |
| DAC7611UB | ±0.5 | ±0.5 | –40°C to +85°C | 8-Lead SOIC | 182 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# DAC7624
# DAC7625

www.burr-brown.com/databook/DAC7624.html

# 12-Bit Quad Voltage Output DIGITAL-TO-ANALOG CONVERTER

## FEATURES

- LOW POWER: 20mW
- UNIPOLAR OR BIPOLAR OPERATION
- SETTLING TIME: 10μs to 0.012%
- 12-BIT LINEARITY AND MONOTONICITY: –40°C to +85°C
- RESET TO MID-SCALE (DAC7624) OR ZERO-SCALE (DAC7625)
- DATA READBACK
- DOUBLE-BUFFERED DATA INPUTS

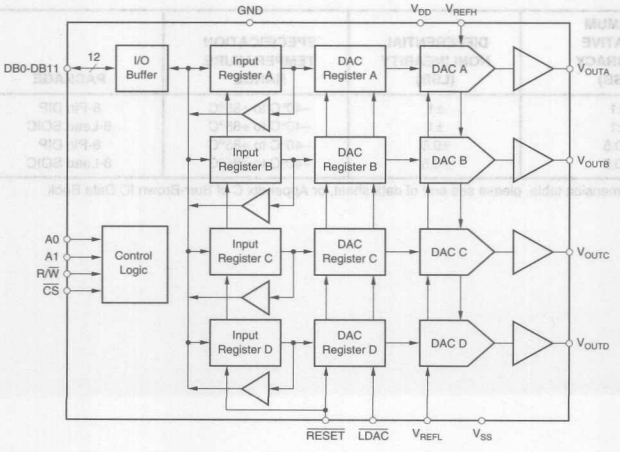
## APPLICATIONS

- PROCESS CONTROL
- ATE PIN ELECTRONICS
- CLOSED-LOOP SERVO-CONTROL
- MOTOR CONTROL
- DATA ACQUISITION SYSTEMS
- DAC-PER-PIN PROGRAMMERS

## DESCRIPTION

The DAC7624 and DAC7625 are 12-bit quad voltage output digital-to-analog converters with guaranteed 12-bit monotonic performance over the specified temperature range. They accept 12-bit parallel input data, have double-buffered DAC input logic (allowing simultaneous update of all DACs), and provide a readback mode of the internal input registers. An asynchronous reset clears all registers to a mid-scale code of $800_H$ (DAC7624) or to a zero-scale of $000_H$ (DAC7625). The DAC7624 and DAC7625 can operate from a single +5V supply or from +5V and –5V supplies.

Low power and small size per DAC make the DAC7624 and DAC7625 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The DAC7624 and DAC7625 are available in a 28-pin plastic double-wide or a 28-lead SOIC package, and offer guaranteed specifications over the –40°C to +85°C temperature range.




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# SPECIFICATION

At $T_A$ = –40°C to +85°C, $V_{DD}$ = +5V, $V_{SS}$ = –5V, $V_{REFH}$ = +2.5V, $V_{REFL}$ = –2.5V, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC7624P, U DAC7625P, U MIN | DAC7624P, U DAC7625P, U TYP | DAC7624P, U DAC7625P, U MAX | DAC7624PB, UB DAC7625PB, UB MIN | DAC7624PB, UB DAC7625PB, UB TYP | DAC7624PB, UB DAC7625PB, UB MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **ACCURACY** | | | | | | | | |
| Linearity Error(1) | $V_{SS}$ = 0V or –5V | | | ±2 | | | ±1 | LSB(2) |
| Linearity Matching(3) | $V_{SS}$ = 0V or –5V | | | ±2 | | | ±1 | LSB |
| Differential Linearity Error | $V_{SS}$ = 0V or –5V | | | ±1 | | | ±1 | LSB |
| Monotonicity | $T_{MIN}$ to $T_{MAX}$ | 12 | | | * | | | Bits |
| Zero-Scale Error | Code = $000_H$ | | | ±4 | | | * | LSB |
| Zero-Scale Drift | | | 2 | 5 | | * | * | ppm/°C |
| Zero-Scale Matching(3) | | | | ±2 | | | ±1 | LSB |
| Full-Scale Error | Code = $FFF_H$ | | | ±4 | | | * | LS |
| Full-Scale Matching(3) | | | | ±2 | | | ±1 | LSB |
| Zero-Scale Error | Code = $00A_H$, $V_{SS}$ = 0V | | | ±8 | | | * | LSB |
| Zero-Scale Drift | $V_{SS}$ = 0V | | 5 | 10 | | * | * | ppm/°C |
| Zero-Scale Matching(3) | $V_{SS}$ = 0V | | | ±4 | | | ±2 | LSB |
| Full-Scale Error | Code = $FFF_H$, $V_{SS}$ = 0V | | | ±8 | | | * | LSB |
| Full-Scale Matching(3) | $V_{SS}$ = 0V | | | ±4 | | | ±2 | LSB |
| Power Supply Rejection | | | 30 | | | * | | ppm/V |
| **ANALOG OUTPUT** | | | | | | | | |
| Voltage Output(4) | $V_{REFL}$ = 0V, $V_{SS}$ = 0V | 0 | | $V_{REFH}$ | * | | * | V |
| | $V_{SS}$ = –5V | $V_{REFL}$ | | $V_{REFH}$ | * | | * | V |
| Output Current | | –1.25 | | +1.25 | * | | * | mA |
| Load Capacitance | No Oscillation | | 100 | | | * | | pF |
| Short-Circuit Current | | | +5, –120 | | | * | | mA |
| Short-Circuit Duration | | | Momentary | | | * | | |
| **REFERENCE INPUT** | | | | | | | | |
| $V_{REFH}$ Input Range | $V_{SS}$ = 0V or –5V | $V_{REFL}$ +1.25 | | +2.5 | * | | * | V |
| $V_{REFL}$ Input Range | $V_{SS}$ = 0V | 0 | | $V_{REFH}$ –1.25 | * | | * | V |
| $V_{REFL}$ Input Range | $V_{SS}$ = –5V | –2.5 | | $V_{REFH}$ –1.25 | * | | * | V |
| **DYNAMIC PERFORMANCE** | | | | | | | | |
| Settling Time(5) | To ±0.012% | | 5 | 10 | | * | * | µs |
| Channel-to-Channel Crosstalk | Full-Scale Step On any other DAC | | 0.25 | | | * | | LSB |
| Output Noise Voltage | 0Hz to 1MHz | | 40 | | | * | | nV/√Hz |
| **DIGITAL INPUT/OUTPUT** | | | | | | | | |
| Logic Family | | | TTL-Compatible CMOS | | | * | | |
| Logic Levels | | | | | | | | |
| $V_{IH}$ | $I_{IH} \leq \pm 10\mu A$ | 2.4 | | $V_{DD}$ +0.3 | * | | * | V |
| $V_{IL}$ | $I_{IL} \leq \pm 10\mu A$ | –0.3 | | 0.8 | * | | * | V |
| $V_{OH}$ | $I_{OH}$ = –0.8mA | 3.6 | | $V_{DD}$ | * | | * | V |
| $V_{OL}$ | $I_{OL}$ = 1.6mA | 0.0 | | 0.4 | * | | * | V |
| Data Format | | | Straight Binary | | | * | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | |
| $V_{DD}$ | | 4.75 | | 5.25 | * | | * | V |
| $V_{SS}$ | If $V_{SS} \neq$ 0V | –5.25 | | –4.75 | * | | * | V |
| $I_{DD}$ | | | 1.5 | 1.9 | | * | * | mA |
| $I_{SS}$ | | –2.1 | –1.6 | | * | * | | mA |
| Power Dissipation | $V_{SS}$ = –5V | | 15 | 20 | | * | * | mW |
| | $V_{SS}$ = 0V | | 7.5 | 10 | | * | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | DAC7624P, U, PB, UB DAC7625P, U, PB, UB | –40 | | +85 | * | | * | °C |

NOTES: (1) If $V_{SS}$ = 0V, specification applies at code $00A_H$ and above. (2) LSB means Least Significant Bit, when $V_{REFH}$ equals +2.5V and $V_{REFL}$ equals –2.5V, then one LSB equals 1.22mV. (3) All DAC outputs will match within the specified error band. (4) Ideal output voltage, does not take into account zero or full-scale error. (5) If $V_{SS}$ = –5V, full-scale 5V step. If $V_{SS}$ = 0V, full-scale positive 2.5V step and negative step from code $FFF_H$ to $00A_H$.

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## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| $V_{DD}$ to $V_{SS}$ | –0.3V to 11V |
| $V_{DD}$ to GND | –0.3V to 5.5V |
| $V_{REFL}$ to $V_{SS}$ | –0.3V to ($V_{DD}$ – $V_{SS}$) |
| $V_{DD}$ to $V_{REFH}$ | –0.3V to ($V_{DD}$ – $V_{SS}$) |
| $V_{REFH}$ to $V_{REFL}$ | –0.3V to ($V_{DD}$ – $V_{SS}$) |
| Digital Input Voltage to GND | –0.3V to $V_{DD}$ + 0.3V |
| Digital Output Voltage to GND | –0.3V to $V_{DD}$ + 0.3V |
| Maximum Junction Temperature | +150°C |
| Operating Temperature Range | –40°C to +85°C |
| Storage Temperature Range | –65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

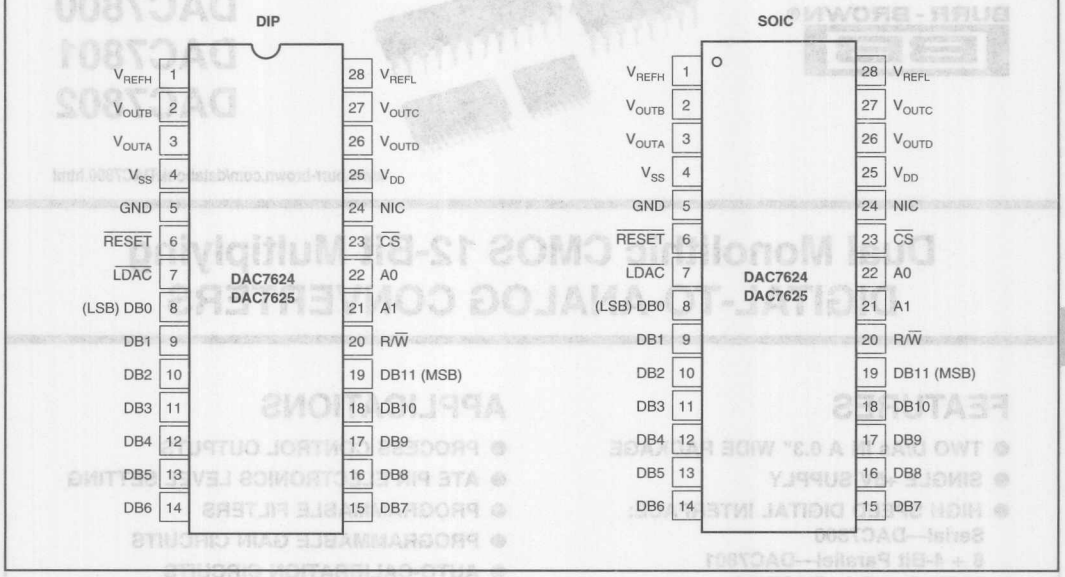
## PACKAGE/ORDERING INFORMATION

| PRODUCT | MAXIMUM LINEARITY ERROR (LSB) | MAXIMUM DIFFERENTIAL LINEARITY ERROR (LSB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|---|---|---|
| DAC7624P | ±2 | ±1 | –40°C to +85°C | 28-Pin Plastic DIP | 215 |
| DAC7624U | ±2 | ±1 | –40°C to +85°C | 28-Lead SOIC | 217 |
| DAC7624PB | ±1 | ±1 | –40°C to +85°C | 28-Pin Plastic DIP | 215 |
| DAC7624UB | ±1 | ±1 | –40°C to +85°C | 28-Lead SOIC | 217 |
| DAC7625P | ±2 | ±1 | –40°C to +85°C | 28-Pin Plastic DIP | 215 |
| DAC7625U | ±2 | ±1 | –40°C to +85°C | 28-Lead SOIC | 217 |
| DAC7625PB | ±1 | ±1 | –40°C to +85°C | 28-Pin Plastic DIP | 215 |
| DAC7625UB | ±1 | ±1 | –40°C to +85°C | 28-Lead SOIC | 217 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN CONFIGURATIONS

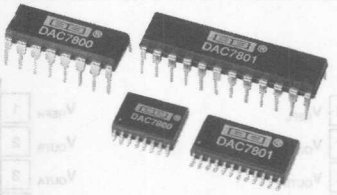
Top View




## PIN DESCRIPTIONS

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_{REFH}$ | Reference Input Voltage High. Sets maximum output voltage for all DACs. |
| 2 | $V_{OUTB}$ | DAC B Voltage Output. |
| 3 | $V_{OUTA}$ | DAC A Voltage Output. |
| 4 | $V_{SS}$ | Negative Analog Supply Voltage, 0V or –5V. |
| 5 | GND | Ground. |
| 6 | $\overline{RESET}$ | Asynchronous Reset Input. Sets DAC and input registers to either mid-scale ($800_H$, DAC7624) or zero-scale ($000_H$, DAC7625) when LOW. |
| 7 | $\overline{LDAC}$ | Load DAC Input. All DAC Registers are transparent when LOW. |
| 8 | DB0 | Data Bit 0. Least significant bit of 12-bit word. |
| 9 | DB1 | Data Bit 1 |
| 10 | DB2 | Data Bit 2 |
| 11 | DB3 | Data Bit 3 |
| 12 | DB4 | Data Bit 4 |
| 13 | DB5 | Data Bit 5 |
| 14 | DB6 | Data Bit 6 |
| 15 | DB7 | Data Bit 7 |
| 16 | DB8 | Data Bit 8 |
| 17 | DB9 | Data Bit 9 |
| 18 | DB10 | Data Bit 10 |
| 19 | DB11 | Data Bit 11. Most significant bit of 12-bit word. |
| 20 | R/$\overline{W}$ | Read/Write Control Input (read = HIGH, write = LOW). |
| 21 | A1 | Register/DAC Select (C or D = HIGH, A or B = LOW). |
| 22 | A0 | Register/DAC Select (B or D = HIGH, A or C = LOW). |
| 23 | $\overline{CS}$ | Chip Select Input. |
| 24 | NIC | Not Internally Connected. Pin has no internal connection to the device. |
| 25 | $V_{DD}$ | Positive Analog Supply Voltage, +5V nominal. |
| 26 | $V_{OUTD}$ | DAC D Voltage Output. |
| 27 | $V_{OUTC}$ | DAC C Voltage Output. |
| 28 | $V_{REFL}$ | Reference Input Voltage Low. Sets minimum output voltage for all DACs. |

BURR - BROWN®



# DAC7800
# DAC7801
# DAC7802

www.burr-brown.com/databook/DAC7800.html

# Dual Monolithic CMOS 12-Bit Multiplying DIGITAL-TO-ANALOG CONVERTERS

## FEATURES

- TWO D/As IN A 0.3" WIDE PACKAGE
- SINGLE +5V SUPPLY
- HIGH SPEED DIGITAL INTERFACE:
  Serial—DAC7800
  8 + 4-Bit Parallel—DAC7801
  12-Bit Parallel—DAC7802
- MONOTONIC OVER TEMPERATURE
- LOW CROSSTALK: –94dB min
- FULLY SPECIFIED OVER –40°C TO +85°C

## APPLICATIONS

- PROCESS CONTROL OUTPUTS
- ATE PIN ELECTRONICS LEVEL SETTING
- PROGRAMMABLE FILTERS
- PROGRAMMABLE GAIN CIRCUITS
- AUTO-CALIBRATION CIRCUITS

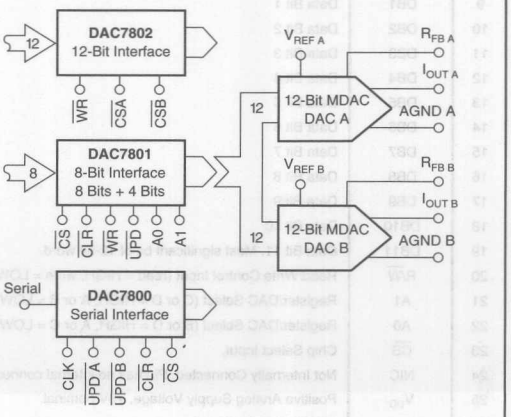
## DESCRIPTION

The DAC7800, DAC7801 and DAC7802 are members of a new family of monolithic dual 12-bit CMOS multiplying digital-to-analog converters. The digital interface speed and the AC multiplying performance are achieved by using an advanced CMOS process optimized for data conversion circuits. High stability on-chip resistors provide true 12-bit integral and differential linearity over the wide industrial temperature range of –40°C to +85°C.

DAC7800 features a serial interface capable of clocking-in data at a rate of at least 10MHz. Serial data is clocked (edge triggered) MSB first into a 24-bit shift register and then latched into each D/A separately or simultaneously as required by the application. An asynchronous CLEAR control is provided for power-on reset or system calibration functions. It is packaged in a 16-pin 0.3" wide plastic DIP.

DAC7801 has a 2-byte (8 + 4) double-buffered interface. Data is first loaded (level transferred) into the input registers in two steps for each D/A. Then both D/As are updated simultaneously. DAC7801 features an asynchronous CLEAR control. DAC7801 is packaged in a 24-pin 0.3" wide plastic DIP.

DAC7802 has a single-buffered 12-bit data word interface. Parallel data is loaded (edge triggered) into the single D/A register for each D/A. DAC7802 is packaged in a 24-pin 0.3" wide plastic DIP.




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# SPECIFICATIONS

## ELECTRICAL

At $V_{DD}$ = +5VDC, $V_{REF\ A}$ = $V_{REF\ B}$ = +10V, $T_A$ = –40°C to +85°C, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC7800, 7801, 7802K | | | DAC7800, 7801, 7802L | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ACCURACY** | | | | | | | | |
| Resolution | | 12 | | | * | | | Bits |
| Relative Accuracy | | | | ±1 | | | ±1/2 | LSB |
| Differential Nonlinearity | | | | ±1 | | | * | LSB |
| Gain Error | Measured Using $R_{FB\ A}$ and $R_{FB\ B}$. All Registers Loaded with All 1s. | | | ±3 | | | ±1 | LSB |
| Gain Temperature Coefficient[1] | | | 2 | 5 | | * | * | ppm/°C |
| Output Leakage Current | $T_A$ = +25°C | | 0.005 | 10 | | * | * | nA |
| | $T_A$ = –40°C to +85°C | | 3 | 150 | | * | * | nA |
| **REFERENCE INPUT** | | | | | | | | |
| Input Resistance | | 6 | 10 | 14 | * | * | * | kΩ |
| Input Resistance Match | | | 0.5 | 3 | | * | 2 | % |
| **DIGITAL INPUTS** | | | | | | | | |
| $V_{IH}$ (Input High Voltage) | | 2 | | | * | | | V |
| $V_{IL}$ (Input Low Voltage) | | | | 0.8 | | | * | V |
| $I_{IN}$ (Input Current) | $T_A$ = +25°C | | | ±1 | | | * | µA |
| | $T_A$ = –40°C to +85°C | | | ±10 | | | * | µA |
| $C_{IN}$ (Input Capacitance) | | | 0.8 | 10 | | * | * | pF |
| **POWER SUPPLY** | | | | | | | | |
| $V_{DD}$ | | 4.5 | | 5.5 | * | | * | V |
| $I_{DD}$ | | | 0.2 | 2 | | * | * | mA |
| Power Supply Rejection | $V_{DD}$ from 4.5V to 5.5V | | | 0.002 | | | * | %/% |

* Same specification as for DAC7800, 7801, 7802K.

## AC PERFORMANCE

**OUTPUT OP AMP IS OPA602.**

At $V_{DD}$ = +5VDC, $V_{REF\ A}$ = $V_{REF\ B}$ = +10V, $T_A$ = +25°C, unless otherwise noted. These specifications are fully characterized but not subject to test.

| PARAMETER | CONDITIONS | DAC7800, 7801, 7802K | | | DAC7800, 7801, 7802L | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OUTPUT CURRENT SETTLING TIME** | To 0.01% of Full Scale $R_L$ = 100Ω, $C_L$ = 13pF | | 0.4 | 0.8 | | * | * | µs |
| **DIGITAL-TO-ANALOG GLITCH IMPULSE** | $V_{REF\ A}$ = $V_{REF\ B}$ = 0V $R_L$ = 100Ω, $C_L$ = 13pF | | 0.9 | | | * | | nV-s |
| **AC FEEDTHROUGH** | $f_{VREF}$ = 10kHz | | –75 | –72 | | * | * | dB |
| **OUTPUT CAPACITANCE** | DAC Loaded with All 0s | | 30 | 50 | | * | * | pF |
| | DAC Loaded with All 1s | | 70 | 100 | | * | * | pF |
| **CHANNEL-TO-CHANNEL ISOLATION** | | | | | | | | |
| $V_{REF\ A}$ to $I_{OUT\ B}$ | $f_{VREF\ A}$ = 10kHz $V_{REF\ B}$ = 0V, Both DACs Loaded with 1s | –90 | –94 | | * | * | | dB |
| $V_{REF\ B}$ to $I_{OUT\ A}$ | $f_{VREF\ B}$ = 10kHz $V_{REF\ A}$ = 0V, Both DACs Loaded with 1s | –90 | –101 | | * | * | | dB |
| **DIGITAL CROSSTALK** | Full Scale Transition $R_L$ = 100Ω, $C_L$ = 13pF | | 0.9 | | | * | | nV-s |

* Same specification as for DAC7800, 7801, 7802K.

NOTE: (1) Guaranteed but not tested.

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| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | RELATIVE ACCURACY | GAIN ERROR |
|---|---|---|---|---|
| DAC7800KP | 16-Pin PDIP | 180 | ±1LSB | ±3LSB |
| DAC7800LP | 16-Pin PDIP | 180 | ±1/2LSB | ±1LSB |
| DAC7800KU | 16-Lead SOIC | 211 | | |
| DAC7800LU | 16-Lead SOIC | 211 | | |
| DAC7801KP | 24-Pin DIP | 243 | ±1LSB | ±3LSB |
| DAC7801LP | 24-Pin DIP | 243 | ±1/2LSB | ±1LSB |
| DAC7801KU | 24-Lead SOIC | 239 | | |
| DAC7801LU | 24-Lead SOIC | 239 | | |
| DAC7802KP | 24-Pin DIP | 243-3 | ±1LSB | ±3LSB |
| DAC7802LP | 24-Pin DIP | 243-3 | ±1/2LSB | ±1LSB |
| DAC7802KU | 24-Lead SOIC | 239 | | |
| DAC7802LU | 24- Lead SOIC | 239 | | |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

At $T_A$ = +25°C, unless otherwise noted.

| | |
|---|---|
| $V_{DD}$ to AGND | 0V, +7V |
| $V_{DD}$ to DGND | 0V, +7V |
| AGND to DGND | –0.3, $V_{DD}$ |
| Digital Input to DGND | –0.3, $V_{DD}$ + 0.3 |
| $V_{REF\ A}$, $V_{REF\ B}$ to AGND | ±20V |
| $V_{REF\ A}$, $V_{REF\ B}$ to DGND | ±20V |
| $I_{OUT\ A}$, $I_{OUT\ B}$ to AGND | –0.3, $V_{DD}$ |
| Storage Temperature Range | –55°C to +125°C |
| Operating Temperature Range | –40°C to +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Junction Temperature | +175°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

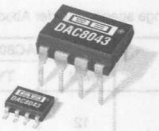
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure.

Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

*Digital Inputs*: All digital inputs of the DAC780X family incorporate on-chip ESD protection circuitry. This protection is designed and has been tested to withstand five 2500V positive and negative discharges (100pF in series with 1500Ω) applied to each digital input.

*Analog Pins*: Each analog pin has been tested to Burr-Brown's analog ESD test consisting of five 1000V positive and negative discharges (100pF in series with 1500Ω) applied to each pin. AGND, $I_{OUT}$, and $R_{FB}$ show some sensitivity. Failure to observe ESD handling procedures could result in catastrophic device failure.

BURR-BROWN®



# DAC8043

www.burr-brown.com/databook/DAC8043.html



# CMOS 12-Bit Serial Input Multiplying DIGITAL-TO-ANALOG CONVERTER

## FEATURES

- 12-BIT ACCURACY IN 8-PIN MINI-DIP AND 8-PIN SOIC
- FAST 3-WIRE SERIAL INTERFACE
- LOW INL AND DNL: ±1/2 LSB max
- GAIN ACCURACY TO ±1LSB max
- LOW GAIN TEMPCO: 5ppm/°C max
- OPERATES WITH +5V SUPPLY
- TTL/CMOS COMPATIBLE
- ESD PROTECTED

## APPLICATIONS

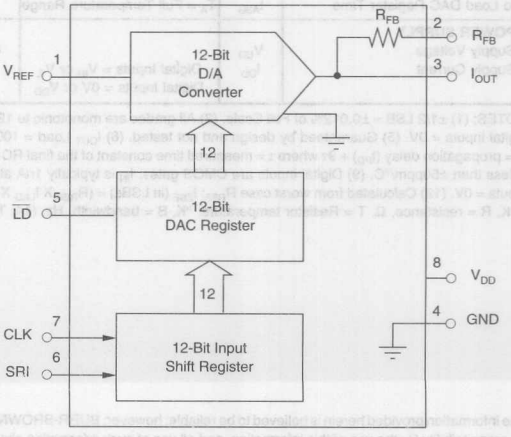
- AUTOMATIC CALIBRATION
- MOTION CONTROL
- MICROPROCESSOR CONTROL SYSTEMS
- PROGRAMMABLE AMPLIFIER/ ATTENUATORS
- DIGITALLY CONTROLLED FILTERS

## DESCRIPTION

The DAC8043 is a 12-bit current output multiplying digital-to-analog converter (DAC) that is packaged in a space saving surface mount 8-pin SOIC and an 8-pin Mini-DIP. Its 3-wire serial interface saves additional circuit board space which results in low power dissipation. When used with microprocessors having a serial port, the DAC8043 minimizes the digital noise feedthrough from its input to output. The serial port can be used as a dedicated analog bus and kept inactive while the DAC8043 is in use. Serial interfacing reduces the complexity of opto or transformer isolation applications.

The DAC8043 contains a 12-bit serial-in, parallel-out shift register, a 12-bit DAC register, a 12-bit CMOS DAC, and control logic. Serial input (SRI) data is clocked into the input register on the rising edge of the clock (CLK) pulse. When the new data word had been clocked in, it is loaded into the DAC register by taking the $\overline{LD}$ input low. Data in the DAC register is converted to an output current by the D/A converter.

The DAC8043 operates from a single +5V power supply which makes the DAC8043 an ideal low power, small size, high performance solution for several applications.




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# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

At $V_{DD}$ = +5V; $V_{REF}$ = +10V; $I_{OUT}$ = GND = 0V; $T_A$ = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | DAC8043P, U | | | DAC8043PC, UC | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **STATIC PERFORMANCE** | | | | | | | | | |
| Resolution | N | | 12 | | | 12 | | | Bits |
| Nonlinearity[1] | INL | | | | ±1 | | | ±1/2 | LSB |
| Differential Nonlinearity[2] | DNL | | | | ±1 | | | ±1/2 | LSB |
| Gain Error[3] | FSE | $T_A$ = +25°C | | | ±2 | | | ±1 | LSB |
| | | $T_A$ = Full Temp Range | | | ±2 | | | ±2 | LSB |
| Gain Tempco[5] | $TC_{FSE}$ | | | | ±5 | | | ±5 | ppm/°C |
| Power Supply Rejection Ratio | PSRR | $\Delta V_{DD}$ = ±5% | | ±0.0006 | ±0.002 | | ±0.0006 | ±0.002 | %/% |
| Output Leakage Current[4] | $I_{LKG}$ | $T_A$ = +25°C | | | ±5 | | | ±5 | nA |
| | | $T_A$ = Full Temp Range | | | ±100 | | | ±25 | nA |
| Zero Scale Error[7, 12] | $I_{ZSE}$ | $T_A$ = +25°C | | | 0.03 | | | 0.03 | LSB |
| | | $T_A$ = Full Temp Range | | | 0.60 | | | 0.15 | LSB |
| Input Resistance[8] | $R_{IN}$ | | 7 | 11 | 15 | 7 | 11 | 15 | kΩ |
| **AC PERFORMANCE** | | | | | | | | | |
| Output Current Settling Time[5, 6] | $t_S$ | $T_A$ = +25°C | | 0.25 | 1 | | 0.25 | 1 | µs |
| Digital-to-Analog Glitch | | $V_{REF}$ = 0V | | 2 | 20 | | 2 | 20 | nVs |
| Energy[5, 10] | Q | $I_{OUT}$ = Load = 100Ω<br>$C_{EXT}$ = 13pF<br>DAC Register Loaded Alternately with all 0s and all 1s | | | | | | | |
| Feedthrough Error[5, 11] ($V_{REF}$ to $I_{OUT}$) | FT | $V_{REF}$ = 20Vp-p at f = 10kHz<br>Digital Input = 0000 0000 0000 | | 0.7 | 1 | | 0.7 | 1 | mVp-p |
| Total Harmonic Distortion[5] | THD | $T_A$ = +25°C<br>$V_{REF}$ = $6V_{RMS}$ at 1kHz<br>DAC Register Loaded with all 1s | | –85 | | | –85 | | dB |
| Output Noise Voltage Density[5, 13] | $e_N$ | 10Hz to 100kHz<br>Between $R_{FB}$ and $I_{OUT}$ | | | 17 | | | 17 | $nV/\sqrt{Hz}$ |
| **DIGITAL INPUTS** | | | | | | | | | |
| Digital Input High | $V_{IH}$ | | 2.4 | | | 2.4 | | | V |
| Digital Input Low | $V_{IL}$ | | | | 0.8 | | | 0.8 | V |
| Input Leakage Current[9] | $I_{IL}$ | $V_{IN}$ = 0V to +5V | | | ±1 | | | ±1 | µA |
| Input Capacitance[5, 11] | $C_{IN}$ | $V_{IN}$ = 0V | | | 8 | | | 8 | pF |
| **ANALOG OUTPUTS** | | | | | | | | | |
| Output Capacitance[5] | $C_{OUT}$ | Digital Inputs = $V_{IH}$ | | | 110 | | | 110 | pF |
| | | Digital Inputs = $V_{IL}$ | | | 80 | | | 80 | pF |
| **TIMING CHARACTERISTICS[5, 14]** | | | | | | | | | |
| Data Setup Time | $t_{DS}$ | $T_A$ = Full Temperature Range | 40 | | | 40 | | | ns |
| Data Hold Time | $t_{DH}$ | $T_A$ = Full Temperature Range | 80 | | | 80 | | | ns |
| Clock Pulse Width High | $t_{CH}$ | $T_A$ = Full Temperature Range | 90 | | | 90 | | | ns |
| Clock Pulse Width Low | $t_{CL}$ | $T_A$ = Full Temperature Range | 120 | | | 120 | | | ns |
| Load Pulse Width | $t_{LD}$ | $T_A$ = Full Temperature Range | 120 | | | 120 | | | ns |
| LSB Clock into Input Register to Load DAC Register Time | $t_{ASB}$ | $T_A$ = Full Temperature Range | 0 | | | 0 | | | ns |
| **POWER SUPPLY** | | | | | | | | | |
| Supply Voltage | $V_{DD}$ | | 4.75 | 5 | 5.25 | 4.75 | 5 | 5.25 | V |
| Supply Current | $I_{DD}$ | Digital Inputs = $V_{IH}$ or $V_{IL}$ | | | 500 | | | 500 | µA |
| | | Digital Inputs = 0V or $V_{DD}$ | | | 100 | | | 100 | µA |

NOTES: (1) ±1/2 LSB = ±0.012% of Full Scale. (2) All grades are monotonic to 12-bits over temperature. (3) Using internal feedback resistor. (4) Applies to $I_{OUT}$; All digital inputs = 0V. (5) Guaranteed by design and not tested. (6) $I_{OUT}$ Load = 100Ω, $C_{EXT}$ = 13pF, digital input = 0V to $V_{DD}$ or $V_{DD}$ to 0V. Extrapolated to 1/2 LSB: $t_S$ = propagation delay ($t_{PD}$) + 9τ where τ = measured time constant of the final RC decay. (7) $V_{REF}$ = +10V, all digital inputs = 0V. (8) Absolute temperature coefficient is less than ±50ppm/°C. (9) Digital inputs are CMOS gates: $I_{IN}$ is typically 1nA at +25°C. (10) $V_{REF}$ = 0V, all digital inputs = 0V to $V_{DD}$ or $V_{DD}$ to 0V. (11) All digital inputs = 0V. (12) Calculated from worst case $R_{REF}$: $I_{ZSE}$ (in LSBs) = ($R_{REF}$ X $I_{LKG}$ X 4096)/$V_{REF}$. (13) Calculations from en = $\sqrt{4K\,TRB}$ where: K = Boltzmann constant, J/°K, R = resistance, Ω. T = Resistor temperature, °K, B = bandwidth, Hz. (14) Tested at $V_{IN}$ = 0V or $V_{DD}$.

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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $V_{DD}$ to GND | 0V, +7V |
| $V_{REF}$ to GND | ±25V |
| $V_{RFB}$ to GND | ±25V |
| Digital Input Voltage Range | –0.3V to $V_{DD}$ |
| Output Voltage (Pin 3) | –0.3 V to $V_{DD}$ |
| Operating Temperature Range | |
| AD | 0°C to +70°C |
| P, PC, U, UC | –40°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature | –65°C to + 150°C |
| Lead Temperature (soldering, 10s) | +300° C |
| $\theta_{JA}$(1) | |
| U Package | +100°C/W |
| P Package | +96°C/W |
| $\theta_{JC}$ | |
| U Package | +42°C/W |
| P Package | +37°C/W |

NOTE: (1) $\theta_{JA}$ is specified for worst case mounting conditions, i.e., $\theta_{JA}$ is specified for device in socket for PDIP packages.

**CAUTION:** 1. Do not apply voltages higher than $V_{DD}$ or less than GND potential on any terminal except $V_{REF}$ (Pin 1) and $R_{FB}$ (Pin 2). 2. The digital control inputs are ESD protected: however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. 3. Use proper anti-static handling procedures. 4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

## ORDERING INFORMATION

| PRODUCT | INL | TEMPERATURE RANGE | PACKAGE |
|---|---|---|---|
| DAC8043P | 1LSB | –40°C to +85°C | 8-pin Plastic DIP |
| DAC8043PC | 1/2LSB | –40°C to +85°C | 8-pin Plastic DIP |
| DAC8043U | 1LSB | –40°C to +85°C | 8-pin SOIC |
| DAC8043UC | 1/2LSB | –40°C to +85°C | 8-pin SOIC |

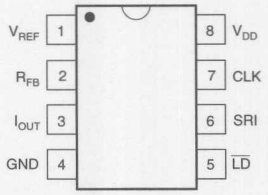
## PACKAGING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| DAC8043P | 8-Pin PDIP | 006 |
| DAC8043PC | 8-Pin PDIP | 006 |
| DAC8043U | 8-Pin SOIC | 182 |
| DAC8043UC | 8-Pin SOIC | 182 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN CONFIGURATION

Top View — 8-Pin Plastic DIP, 8-Pin SOIC




## ELECTROSTATIC DISCHARGE SENSITIVITY

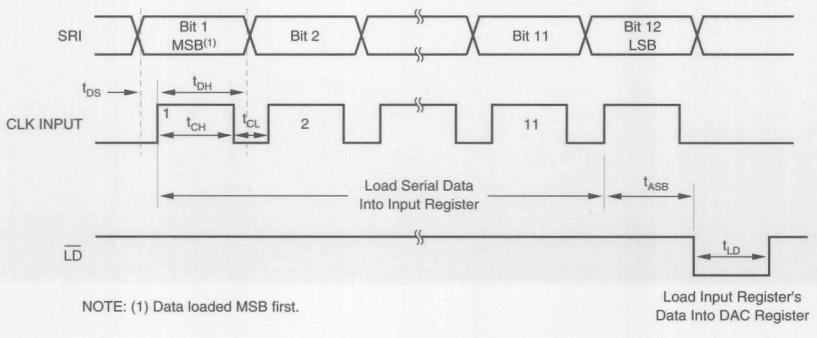
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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

*Digital Inputs:* All digital inputs of the DAC8043 incorporate on-chip ESD protection circuitry. This protection is designed and has been tested to withstand five 2500V positive and negative discharges (100pF in series with 1500Ω) applied to each digital input.

*Analog Pins:* Each analog pin has been tested to Burr-Brown's analog ESD test consisting of five 1000V positive and negative discharges (100pF in series with 1500Ω) applied to each pin. $V_{REF}$ and $R_{FB}$ show some sensitivity.

## WRITE CYCLE TIMING DIAGRAM



## PIN CONFIGURATION




## ELECTROSTATIC DISCHARGE SENSITIVITY

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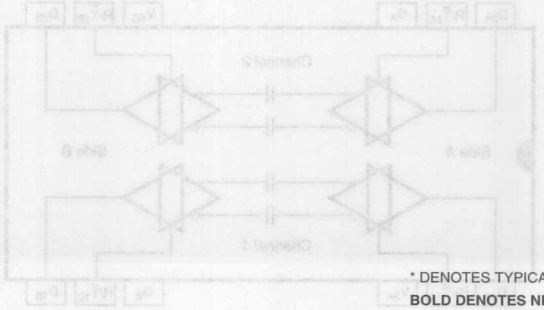
# 4 Digital Interface Products

## DIGITAL COUPLER

| Product | Isolation Voltage Cont Peak (Vrms) | Isolation Voltage Pulse Test Peak (V) | Leakage Current 240VAC 60Hz (μA) | Data Rate (MBd)* | Power Consumption Per Channel max (mW) | Ext Power Req | Temp[1] | Pkg | Description |
|---|---|---|---|---|---|---|---|---|---|
| ISO150 | 1500 | 2400[2] | 0.6 | 80 | 25 | Yes | XInd | DIP, SOIC | Dual Isolated Transceiver |
| ISO485 | 1500 | NS | NS | 20 | 180 at 5MBit/s | Yes | XInd | DIP | RS-485 Transceiver |

NOTES: (1) XInd = –40°C to +85°C. (2) Partial discharge test voltage, ac Vrms.

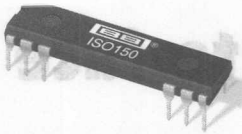




* DENOTES TYPICAL
**BOLD DENOTES NEW PRODUCT**
***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

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# ISO150

www.burr-brown.com/databook/ISO150.html

# Dual, Isolated, Bi-Directional DIGITAL COUPLER

## FEATURES

- REPLACES HIGH-PERFORMANCE OPTOCOUPLERS
- DATA RATE: 80M Baud, typ
- LOW POWER CONSUMPTION: 25mW Per Channel, max
- TWO CHANNELS, EACH BI-DIRECTIONAL, PROGRAMMABLE BY USER
- PARTIAL DISCHARGE TESTED: 2400Vrms
- CREEPAGE DISTANCE OF 16.5mm (DIP)
- LOW COST PER CHANNEL
- PLASTIC DIP AND SOIC PACKAGES

## APPLICATIONS

- DIGITAL ISOLATION FOR A/D, D/A CONVERSION
- ISOLATED UART INTERFACE
- MULTIPLEXED DATA TRANSMISSION
- ISOLATED PARALLEL TO SERIAL INTERFACE
- TEST EQUIPMENT
- MICROPROCESSOR SYSTEM INTERFACE
- ISOLATED LINE RECEIVER
- GROUND LOOP ELIMINATION

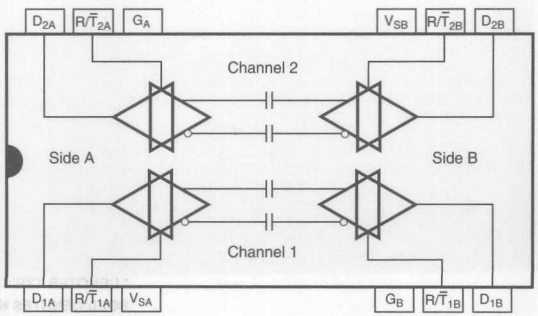
## DESCRIPTION

The ISO150 is a two-channel, galvanically isolated data coupler capable of data rates of 80MBaud, typical. Each channel can be individually programmed to transmit data in either direction.

Data is transmitted across the isolation barrier by coupling complementary pulses through high voltage 0.4pF capacitors. Receiver circuitry restores the pulses to standard logic levels. Differential signal transmission rejects isolation-mode voltage transients up to 1.6kV/µs.

ISO150 avoids the problems commonly associated with optocouplers. Optically isolated couplers require high current pulses and allowance must be made for LED aging. The ISO150's Bi-CMOS circuitry operates at 25mW per channel.

ISO150 is available in a 24-pin DIP package and in a 28-lead SOIC. Both are specified for operation from –40°C to 85°C.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = +25°C and $V_S$ = +5V, unless otherwise noted.

| PARAMETER | CONDITION | ISO150AP, AU MIN | ISO150AP, AU TYP | ISO150AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **ISOLATION PARAMETERS** | | | | | |
| Rated Voltage, Continuous | 60Hz | 1500 | | | Vrms |
| Partial Discharge, 100% Test[1] | 1s, 5pC | 2400 | | | Vrms |
| Creepage Distance (External) | | | | | |
| DIP—"P" Package | | | 16 | | mm |
| SOIC—"U" Package | | | 7.2 | | mm |
| Internal Isolation Distance | | | 0.10 | | mm |
| Isolation Voltage Transient Immunity[2] | | | 1.6 | | kV/µs |
| Barrier Impedance | | | $>10^{14}$ \|\| 7 | | Ω \|\| pF |
| Leakage Current | 240Vrms, 60Hz | | 0.6 | | µArms |
| **DC PARAMETERS** | | | | | |
| Logic Output Voltage, High, $V_{OH}$ | $I_{OH}$ = 6mA | $V_S$–1 | | $V_S$ | V |
| Low, $V_{OL}$ | $I_{OL}$ = 6mA | 0 | | 0.4 | V |
| Logic Output Short-Circuit Current | Source or Sink | | 30 | | mA |
| Logic Input Voltage, High[3] | | 2 | | $V_S$ | V |
| Low[3] | | 0 | | 0.8 | V |
| Logic Input Capacitance | | | 5 | | pF |
| Logic Input Current | | | <1 | | nA |
| Power Supply Voltage Range[3] | | 3 | 5 | 5.5 | V |
| Power Supply Current[4] | | | | | |
| Transmit Mode | DC | | 0.001 | 100 | µA |
| | 50MBaud | | 14 | | mA |
| Receive Mode | DC | | 7.2 | 10 | mA |
| | 50MBaud | | 16 | | mA |
| **AC PARAMETERS** | | | | | |
| Data Rate, Maximum[5] | $C_L$ = 50pF | 50 | 80 | | MBaud |
| Data Rate, Minimum | | DC | | | |
| Propagation Time[6] | $C_L$ = 50pF | | 27 | 40 | ns |
| Propagation Delay Skew[7] | $C_L$ = 50pF | | 0.5 | 2 | ns |
| Pulse Width Distortion[8] | $C_L$ = 50pF | | 1.5 | 6 | ns |
| Output Rise/Fall Time, 10% to 90% | $C_L$ = 50pF | | 9 | 14 | ns |
| Mode Switching Time | | | | | |
| Receive-to-Transmit | | | 13 | | ns |
| Transmit-to-Receive | | | 75 | | ns |
| **TEMPERATURE RANGE** | | | | | |
| Operating Range | | –40 | | 85 | °C |
| Storage | | –40 | | 125 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | 75 | | °C/W |

NOTES: (1) All devices receive a 1s test. Failure criterion is ≥5 pulses of ≥5pC. (2) The voltage rate-of-change across the isolation barrier that can be sustained without data errors. (3) Logic inputs are HCT-type and thresholds are a function of power supply voltage with approximately 0.4V hysteresis—see text. (4) Supply current measured with both transceivers set for the indicated mode. Supply current varies with data rate—see typical curves. (5) Calculated from the maximum Pulse Width Distortion (PWD), where Data Rate = 0.3/PWD. (6) Propagation time measured from $V_{IN}$ = 1.5V to $V_O$ = 2.5V. (7) The difference in propagation time of channel A and channel B in any combination of transmission directions. (8) The difference between propagation time of a rising edge and a falling edge.



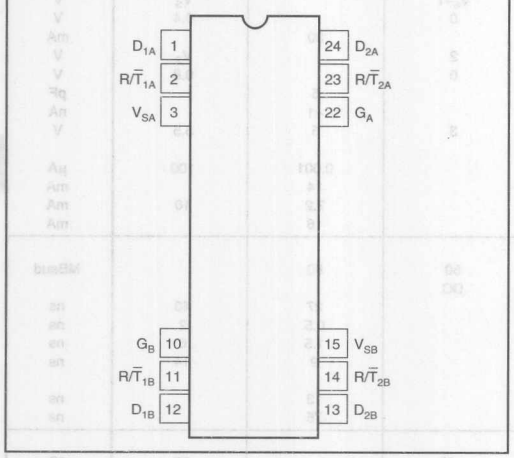
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## ABSOLUTE MAXIMUM RATINGS

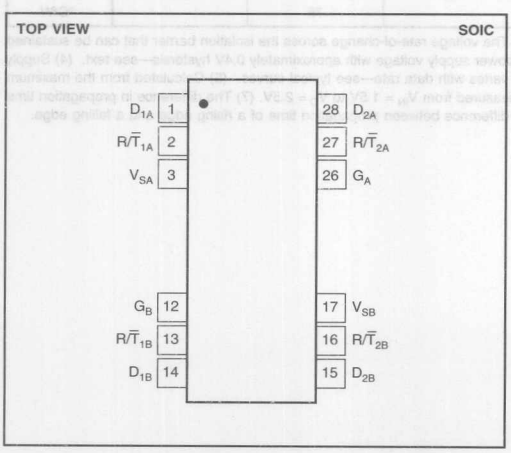
| | |
|---|---|
| Storage Temperature | –40°C to +125°C |
| Supply Voltages, $V_S$ | –0.5 to 6V |
| Transmitter Input Voltage, $V_I$ | –0.5 to $V_S$ + 0.5V |
| Receiver Output Voltage, $V_O$ | –0.5 to $V_S$ + 0.5V |
| $R/\overline{T}_X$ Inputs | –0.5 to $V_S$ + 0.5V |
| Isolation Voltage dV/dt, $V_{ISO}$ | 500kV/µs |
| $D_X$ Short to Ground | Continuous |
| Junction Temperature, $T_J$ | 175°C |
| Lead Temperature (soldering, 10s) | 260°C |
| 1.6mm below seating plane (DIP package) | 300°C |

## PIN CONFIGURATION

TOP VIEW — DIP




TOP VIEW — SOIC




## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| ISO150AP | 24-Pin Single-Wide DIP | 243-1 |
| ISO150AU | 28-Lead SOIC | 217-2 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN DESCRIPTIONS

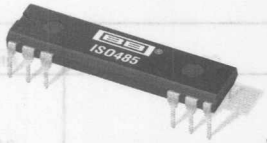
| NAME | FUNCTION |
|---|---|
| $D_{1A}$ | Data in or data out for transceiver 1A. $R/\overline{T}_{1A}$ held low makes $D_{1A}$ an input pin. |
| $R/\overline{T}_{1A}$ | Receive/Transmit switch controlling transceiver 1A. |
| $V_{SA}$ | +5V supply pin for side A which powers transceivers 1A and 2A. |
| $G_B$ | Ground pin for transceivers 1B and 2B. |
| $R/\overline{T}_{1B}$ | Receive/Transmit switch controlling transceiver 1B. |
| $D_{1B}$ | Data in or data out for transceiver 1B. $R/\overline{T}_{1B}$ held low makes $D_{1B}$ an input pin. |
| $D_{2B}$ | Data in or data out for transceiver 2B. $R/\overline{T}_{2B}$ held low makes $D_{2B}$ an input pin. |
| $R/\overline{T}_{2B}$ | Receive/Transmit switch controlling $D_{2B}$. |
| $V_{SB}$ | +5V supply pin for side B which powers transceivers 1B and 2B. |
| $G_A$ | Ground pin for transceivers 1A and 2A. |
| $R/\overline{T}_{2A}$ | Receive/Transmit switch controlling transceiver 2A. |
| $D_{2A}$ | Data in or data out for transceiver 2A. $R/\overline{T}_{2A}$ held low makes $D_{2A}$ in input pin. |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR - BROWN®




# ISO485

www.burr-brown.com/databook/ISO485.html

# Isolated RS-485 DIFFERENTIAL BUS TRANSCEIVER

## FEATURES

- RS-485 AND RS-422 COMPATIBLE
- 100% TESTED FOR HIGH-VOLTAGE BREAKDOWN
- RATED 1500Vrms
- SINGLE-WIDE 24-PIN PLASTIC DIP
- EASY TO USE
- LOW POWER: 180mW typ at 5Mbit/s

## APPLICATIONS

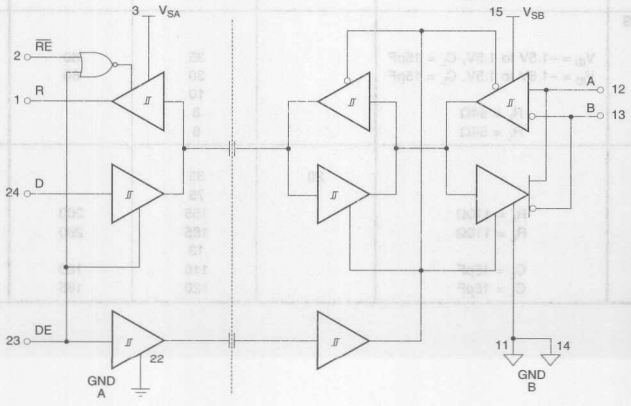
- MULTIPOINT DATA TRANSMISSION ON LONG BUS LINES IN NOISY ENVIRONMENTS

## DESCRIPTION

The ISO485 differential, isolated bus transceiver uses Burr-Brown's capacitively coupled isolation technology to provide high-speed, low cost bus isolation. The ISO485 is designed for bi-directional data communication on multipoint bus transmission lines and meets EIA Standard RS-485 as well as EIA Standard RS-422A requirements.

The ISO485 uses high voltage 0.4pF capacitors instead of the LED and photodetector which are used in equivalent optocoupler solutions. As a consequence the part count of the isolated RS-485 channel is reduced from multiple optocoupler channels, an RS-485 transceiver chip and supporting circuitry to one ISO485. The capacitors in the ISO485 provide a high voltage barrier, 1500Vrms and greatly reduce current spikes on the power line.

The ISO485 combines a 3-state differential line driver and a differential-input line receiver both of which operate from a single 5V power supply. The driver differential outputs and the receiver differential input/output bus ports are designed to offer minimum loading to the bus whenever the driver is disabled or $V_S$ = 0V.




**TRUTH TABLE**

| DE | $\overline{RE}$ | RS-485 BUS |
|---|---|---|
| 0 | 0 | $R_X$ |
| 0 | 1 | HIGH Z |
| 1 | 0 | HIGH Z |
| 1 | 1 | $T_X$ |

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# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = 5V, unless otherwise specified.

| PARAMETER | CONDITION | ISO485P MIN | ISO485P TYP | ISO485P MAX | UNITS |
|---|---|---|---|---|---|
| **DRIVER DC CHARACTERISTICS** | | | | | |
| Input Voltage | | | | | |
| High MIN | | | | 2 | V |
| Low MAX | | 0.8 | | | V |
| Input Current | | | | | |
| High-Level | $V_{IN}$ = 2.4V | | | ±1 | µA |
| Low-Level | $V_{IN}$ = 0.4V | | | ±1 | µA |
| Output Voltage | $I_{OUT}$ = 0 | 0 | | 5 | V |
| Differential Output Voltage | $I_{OA} - I_{OB}$ = 0 | 1.5 | | 5 | V |
| | $R_{LOAD}$ = 100Ω | 2 | 2.5 | 5 | V |
| | $R_{LOAD}$ = 54Ω | 1.5 | 2.5 | 5 | V |
| Change In Magnitude of Differential Output Voltage | $R_{LOAD}$ = 54Ω or 100Ω | | | ±0.5 | V |
| Common-Mode Output Voltage | $R_{LOAD}$ = 54Ω or 100Ω | | | 3 | V |
| Change in Magnitude of Common-Mode Output Voltage | $R_{LOAD}$ = 54Ω or 100Ω | | | ±0.2 | V |
| Output Current | $V_{OUT}$ = 7V, output disabled | | | 1 | mA |
| | $V_{OUT}$ = –7V, output disabled | | | –0.8 | mA |
| Short-Circuit Output Current (1 sec max) | $V_{OUT}$ = –7V | | –250 | | mA |
| | $V_{OUT}$ = 0V | | –150 | | mA |
| | $V_{OUT}$ = $V_S$ | | 250 | | mA |
| | $V_{OUT}$ = 12V | | 250 | | mA |
| **DRIVER SWITCHING CHARACTERISTICS** | | | | | |
| Propagation Delay Time, Low-to-High Level Output | $R_{LOAD}$ = 54Ω | | | 60 | ns |
| Propagation Delay Time, High-to-Low Level Output | $R_{LOAD}$ = 54Ω | | | 60 | ns |
| Input to Output Propagation Delay Skew | $R_{LOAD}$ = 54Ω | | 10 | | ns |
| Output Rise Time | $R_{LOAD}$ = 54Ω | | 10 | | ns |
| Output Fall Time | $R_{LOAD}$ = 54Ω | | 10 | | ns |
| **RECEIVER DC CHARACTERISTICS** | | | | | |
| Differential-Input-Threshold Voltage | | | | | |
| High | $V_{OUT}$ = 2.7V, $I_{OUT}$ = –0.4mA | | | 0.2 | V |
| Low | $V_{OUT}$ = 0.5V, $I_{OUT}$ = 8mA | –0.2 | | | V |
| Hysteresis | | | 70 | | mV |
| High-Level Output Voltage | $V_{ID}$ = 200mV, $I_{OH}$ = 400µA | 2.4 | | | V |
| Low-Level Output Voltage | $V_{ID}$ = 200mV, $I_{OL}$ = 8mA | | | 0.4 | V |
| High-Impedance-State Output Current | $V_{OUT}$ = 1.4V | | | ±1 | µA |
| Line Input Current | $V_{IN}$ = 12V, other output = 0V | | 0.7 | | mA |
| | $V_{IN}$ = –7V, other output = 0V | | –0.6 | | mA |
| Enable-Input Current | | | | | |
| High | $V_{IH}$ = 2.7V | | | 1 | µA |
| Low | $V_{IL}$ = 0.4V | | | 1 | µA |
| Input Resistance | | 12 | | | kΩ |
| Short-Circuit Output Current | 1 sec max | | 40 | | mA |
| **RECEIVER SWITCHING CHARACTERISTICS** | | | | | |
| Propagation Delay Time, Low-to-High Level Output | $V_{ID}$ = –1.5V to 1.5V, $C_L$ = 15pF | | 35 | 60 | ns |
| Propagation Delay Time, High-to-Low Level Output | $V_{ID}$ = –1.5V to 1.5V, $C_L$ = 15pF | | 30 | 60 | ns |
| Input to Output Propagation Delay Skew | | | 10 | | ns |
| Output Rise Time | $R_L$ = 54Ω | | 8 | | ns |
| Output Fall Time | $R_L$ = 54Ω | | 8 | | ns |
| **TRANSCEIVER SPECIFICATIONS** | | | | | |
| Maximum Data Rate | | 20 | 35 | | Mbits/s |
| Propagation Delay Driver to Receiver | | | 75 | | ns |
| Driver Output Enable Time | $R_L$ = 110Ω | | 155 | 200 | ns |
| Driver Output Disable Time | $R_L$ = 110Ω | | 185 | 280 | ns |
| Propagation Delay Receiver to Driver | | | 13 | | ns |
| Receiver Output Enable Time | $C_L$ = 15pF | | 110 | 180 | ns |
| Receiver Output Disable Time | $C_L$ = 15pF | | 120 | 185 | ns |

## SPECIFICATIONS (CONT)

At $T_A$ = +25°C, $V_S$ = 5V, unless otherwise specified.

| PARAMETER | CONDITION | ISO485P MIN | ISO485P TYP | ISO485P MAX | UNITS |
|---|---|---|---|---|---|
| **TRANSCEIVER SPECIFICATIONS (CONT)** | | | | | |
| Supply Voltage | | | | | |
| $V_S$A | | 3 | 5 | 5.5 | V |
| $V_S$B | | 4.75 | 5 | 5.25 | V |
| Supply Current | DE RE RS-485 BUS | | | | |
| $V_S$A | 0 0 Rx | | | 5 | mA |
| $V_S$A | 0 1 HIGH Z | | | 0.4 | mA |
| $V_S$A | 1 0 HIGH Z | | | 0.4 | mA |
| $V_S$A | 1 1 Tx | | | 0.4 | mA |
| $V_S$B | 0 0 Rx | | | 55 | mA |
| $V_S$B | 0 1 HIGH Z | | | 55 | mA |
| $V_S$B | 1 0 HIGH Z | | | 51 | mA |
| $V_S$B | 1 1 Tx | | | 51 | mA |
| **RECOMMENDED OPERATING CONDITIONS** | | | | | |
| Voltage at Any Bus Terminal | (separately or common-mode) | –7 | | 12 | V |
| High-Level Driver Input Voltage | | 2 | | | V |
| Low-Level Driver Input Voltage | | | | 0.8 | V |
| Differential Receiver Input Voltage | | | | ±12 | V |
| Output Current High-Level | | | | | |
| | Driver | | | –60 | mA |
| | Receiver | | | –400 | µA |
| Output Current Low-Level | | | | | |
| | Driver | | | 60 | mA |
| | Receiver | | | 8 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –40 | | 85 | °C |
| Storage | | –40 | | 125 | °C |
| **ISOLATION PARAMETERS** | | | | | |
| Rated Voltage, Continuous | 50Hz | 1500 | | | Vrms |
| Partial Discharge, 100% Test(1) | 1s, 5pC | 2400 | | | Vrms |
| Creepage Distance (External) DIP = "P" Package | | | 16 | | mm |
| Internal Isolation Distance | | | 0.10 | | mm |
| Isolation Voltage Transient Immunity(2) | | | 1.6 | | kV/µs |
| Barrier Impedance | | | > $10^{14}$ ‖ 7 | | Ω ‖ pF |
| Leakage Current | 240Vrms, 60Hz | | 0.6 | | µArms |

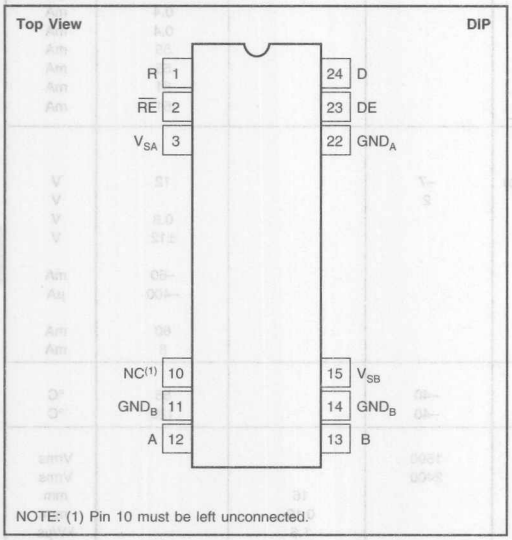
NOTES: (1) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pC. (2) The voltage rate-of-change across the isolation barrier that can be sustained without data errors.



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| | |
|---|---|
| Voltage at any bus terminal | –10 to 15V |
| Enable Input Voltage | 0 to $V_{CC}$ + 0.5V |
| Continuous total dissipation at 25°C free-air temp. | 750mW |
| Lead solder temperature, 260°C for 10s, 1.6mm below seating plane | 300°C |
| Junction Temperature | 150°C |
| Package thermal transfer, $\theta_{JA}$ | 75°C/W |

## PIN CONFIGURATION




NOTE: (1) Pin 10 must be left unconnected.

| PRODUCT | PACKAGE | NUMBER(1) |
|---|---|---|
| ISO485P | 24-Pin Single-Wide DIP | 243-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN ASSIGNMENTS

| PIN # | NAME | DESCRIPTION |
|---|---|---|
| 1 | R | Data Received From Transmission Line |
| 2 | $\overline{RE}$ | Receive Switch Controlling Receiving Of Data |
| 3 | $V_{SA}$ | +5V Supply Pin For Side A |
| 10 | NC | This Pin MUST Be Left Unconnected |
| 11 | $GND_B$ | Ground Pin For Side B. Also Connected To Pin 14 |
| 12 | A | Data, Driver Out/Receiver In |
| 13 | B | Data, Driver Out/Receiver In |
| 14 | $GND_B$ | Ground Pin For Side B. Also Connected To Pin 11 |
| 15 | $V_{SB}$ | +5V Supply Pin For Side B |
| 22 | $GND_A$ | Ground Pin For Side A |
| 23 | DE | Driver Switch Controlling Output Of Data |
| 24 | D | Data To Be Transmitted |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# 5 Multiplexers

Burr-Brown analog multiplexers provide one of the most cost effective methods of achieving multiple-channel signal distribution. Single-ended and differential channel versions are available in both ceramic and plastic packages.

These high speed multiplexers are input protected and can withstand voltages of 70Vp-p without damaging the device. Full ±15V input range is provided on all devices.

| | | |
|---|---|---|
| MPC506 | 16 to 1 mux | single-ended |
| MPC507 | 8 to 1 mux | differential |
| MPC508 | 8 to 1 mux | single-ended |
| MPC509 | 4 to 1 mux | differential |

## ANALOG MULTIPLEXER (Input, Settling Time, max)

**16-CHANNEL**
MPC506 (Single, 3.5µs)
MPC800 (Single, 800ns)

**8-CHANNEL**
MPC507 (Diff, 3.5µs)
MPC508 (Single, 3.5µs)

**4-CHANNEL**
MPC509 (Diff, 3.5µs)
MPC100 (Single, 450MHz)

**2-CHANNEL**
MPC104 (Single, 590MHz)
MPC102 (Single, 370MHz, Dual)

*For Immediate Assistance, Contact Your Local Salesperson*

**BOLD DENOTES NEW PRODUCT**
***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

# ANALOG MULTIPLEXERS

| Product | Channels | Input Range (V) | On Resistance max (Ω) | Small Signal Bandwidth | Settling Time (to 0.01%) | Temp Range[1] | Pkg[2] | Description |
|---|---|---|---|---|---|---|---|---|
| MPC100AP | 4-channel, single ended | ±4.2 | 0.88M | 450MHz | — | Ext | 14-p PDIP | Buffered 4 x 1 |
| MPC100AU | 4-channel, single ended | ±4.2 | 0.88M | 450MHz | — | Ext | 14-p SOIC | Buffered 4 x 1 |
| MPC102AP | dual 2-channel, single ended | ±3.6 | 0.88M | 370MHz | — | Ext | 14-p PDIP | Buffered Dual 2 x 1 |
| MPC102AU | dual 2-channel, single ended | ±3.6 | 0.88M | 370MHz | — | Ext | 14-p SOIC | Buffered Dual 2 x 1 |
| MPC104AP | 2-channel, single ended | ±3.6 | 0.88M | 590MHz | — | Ext | 8-p PDIP | Buffered 2 x 1 |
| MPC104AU | 2-channel, single ended | ±3.6 | 0.88M | 590MHz | — | Ext | 8-p SOIC | Buffered 2 x 1 |
| MPC506AP | 16-channel, single ended | ±15 | 1.8k | — | 3.5µs | Ext | 28-p PDIP | Protected Inputs, CMOS |
| MPC506AG | 16-channel, single ended | ±15 | 1.8k | — | 3.5µs | Ext | 28-p CDIP | Protected Inputs, CMOS |
| MPC506AU | 16-channel, single ended | ±15 | 1.8k | — | 3.5µs | Ext | 29-p SOIC | Protected Inputs, CMOS |
| MPC507AP | 8-channel, differential | ±15 | 1.8k | — | 3.5µs | Ext | 28-p PDIP | Protected Inputs, CMOS |
| MPC507AG | 8-channel, differential | ±15 | 1.8k | — | 3.5µs | Ext | 28-p CDIP | Protected Inputs, CMOS |
| MPC507AU | 8-channel, differential | ±15 | 1.8k | — | 3.5µs | Ext | 28-p SOIC | Protected Inputs, CMOS |
| MPC508AP | 8-channel, single ended | ±15 | 1.8k | — | 3.5µs | Ext | 16-p PDIP | Protected Inputs, CMOS |
| MPC508AG | 8-channel, single ended | ±15 | 1.8k | — | 3.5µs | Ext | 16-p CDIP | Protected Inputs, CMOS |
| MPC508AU | 8-channel, single ended | ±15 | 1.8k | — | 3.5µs | Ext | 16-p SOIC | Protected Inputs, CMOS |
| MPC509AP | 4-channel, differential | ±15 | 1.8k | — | 3.5µs | Ext | 16-p PDIP | Protected Inputs, CMOS |
| MPC509AG | 4-channel, differential | ±15 | 1.8k | — | 3.5µs | Ext | 16-p CDIP | Protected Inputs, CMOS |
| MPC509AU | 4-channel, differential | ±15 | 1.8k | — | 3.5µs | Ext | 16-p SOIC | Protected Inputs, CMOS |
| MPC800KG | 16 single or 8 differential | ±15 | 750 | — | 800ns | Com | CDIP | High Speed, CMOS |
| MPC801KG | 8 single or 4 differential | ±15 | 750 | — | 800ns | Com | CDIP | High Speed, CMOS |

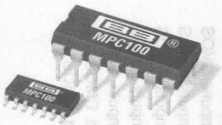
NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ext = –40°C to +85°C, Mil = –55°C to +125°C. (2) CDIP = Ceramic DIP, PDIP = Plastic DIP.

**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

BURR - BROWN®



# MPC100

www.burr-brown.com/databook/MPC100.html

# Wide Bandwidth 4 x 1 VIDEO MULTIPLEXER

## FEATURES

- BANDWIDTH: 250MHz (1.4Vp-p)
- LOW INTERCHANNEL CROSSTALK: ≤60dB (30MHz, DIP); ≤70dB (30MHz, SO)
- LOW SWITCHING TRANSIENTS: +2.5/–1.2mV
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.05%, 0.01°
- LOW QUIESCENT CURRENT: One Channel Selected: ±4.6mA No Channel Selected: ±230µA

## APPLICATIONS

- VIDEO ROUTING AND MULTIPLEXING (CROSSPOINTS)
- RADAR SYSTEMS
- DATA ACQUISITION
- INFORMATION TERMINALS
- SATELLITE OR RADIO LINK IF ROUTING

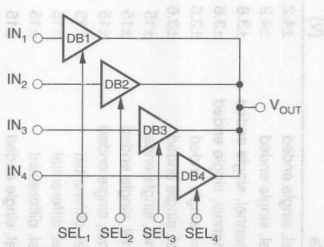
## DESCRIPTION

The MPC100 is a very wide bandwidth 4-to-1 channel video signal multiplexer which can be used in a wide variety of applications.

MPC100 is designed for wide-bandwidth systems, including high-definition television and broadcast equipment. Although it is primarily used to route video signals, the harmonic and dynamic attributes of the MPC100 make it appropriate for other analog signal routing applications such as radar, communications, computer graphics, and data acquisition systems.

The MPC100 consists of four identical monolithic integrated open-loop buffer amplifiers, which are connected internally at the output. The unidirectional transmission path consists of bipolar complementary buffers, which offer extremely high output-to-input isolation. The MPC100 multiplexer enables one of the four input channels to connect to the output. The output of the multiplexer is in a high-impedance state when no channel is selected. When one channel is selected with a digital "1" at the corresponding SEL-input, the component acts as a buffer with high input impedance and low output impedance.

The wide bandwidth of over 250MHz at 1.4Vp-p signal level, high linearity and low distortion, and low input voltage noise of $4nV/\sqrt{Hz}$ make this crosspoint switch suitable for RF and video applications. All performance is specified with ±5V supply voltage, which reduces power consumption in comparison with ±15V designs. The multiplexer is available in space-saving SO-14 and DIP packages. Both are designed and specified for operation over the industrial temperature range (–40°C to +85°C.)




**TRUTH TABLE**

| $SEL_1$ | $SEL_2$ | $SEL_3$ | $SEL_4$ | $V_{OUT}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | HI-Z |
| 1 | 0 | 0 | 0 | $IN_1$ |
| 0 | 1 | 0 | 0 | $IN_2$ |
| 0 | 0 | 1 | 0 | $IN_3$ |
| 0 | 0 | 0 | 1 | $IN_4$ |

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# SPECIFICATIONS

At $V_{CC}$ = ±5V, $R_L$ = 10kΩ, $R_{SOURCE}$ = 50Ω, and $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | MPC100AP, AU MIN | MPC100AP, AU TYP | MPC100AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | |
| **INPUT OFFSET VOLTAGE** | $R_{IN}$ = 0, $R_{SOURCE}$ = 0 | | | | |
| Initial | | | +10 | ±30 | mV |
| vs Temperature | | | ±30 | | µV/°C |
| vs Supply (Tracking) | $V_{CC}$ = ±4.5V to ±5.5V | –40 | –80 | | dB |
| vs Supply (Non-tracking) | $V_{CC}$ = +4.5V to +5.5V | | –50 | | dB |
| vs Supply (Non-tracking) | $V_{CC}$ = –4.5V to –5.5V | | –50 | | dB |
| Initial Matching | Between the Four Channels | | ±3 | | mV |
| **INPUT BIAS CURRENT** | | | | | |
| Initial | | | +4 | ±10 | µA |
| vs Temperature | | | 20 | | nA/°C |
| vs Supply (Tracking) | $V_{CC}$ = ±4.5V to ±5.5V | | ±380 | | nA/V |
| vs Supply (Non-tracking) | $V_{CC}$ = +4.5V to +5.5V | | +1.0 | | µA/V |
| vs Supply (Non-tracking) | $V_{CC}$ = –4.5V to –5.5V | | –11.0 | | µA/V |
| **INPUT IMPEDANCE** | | | | | |
| Resistance | Channel On | | 0.88 | | MΩ |
| Capacitance | Channel On | | 1.0 | | pF |
| Capacitance | Channel Off | | 1.0 | | pF |
| **INPUT NOISE** | | | | | |
| Voltage Noise Density | $f_B$ = 20kHz to 10MHz | | 4.0 | | nV/√Hz |
| Signal-to-Noise Ratio | S/N = 0.7/$V_N$ • √5MHz | | 98 | | dB |
| **INPUT VOLTAGE RANGE** | Gain Error ≤ 10% | | ±4.2 | | V |
| **TRANSFER CHARACTERISTICS** | Voltage Gain | | | | |
| | $R_L$ = 1kΩ, $V_{IN}$ = ±2V | | 0.982 | | V/V |
| | $R_L$ = 10kΩ, $V_{IN}$ = ±2.8V | 0.98 | 0.992 | | V/V |
| **CHANNEL SELECTION INPUTS** | | | | | |
| Logic 1 Voltage | | +2.0 | | $V_{CC}$ | V |
| Logic 0 Voltage | | 0 | | +0.8 | V |
| Logic 1 Current | $V_{SEL}$ = 5.0V | | 100 | 150 | µA |
| Logic 0 Current | $V_{SEL}$ = 0.8V | | 0.002 | 5 | µA |
| **SWITCHING CHARACTERISTICS** | $V_I$ = –0.3V to +0.7V, f = 5MHz | | | | |
| SEL to Channel ON Time | 90% Point of $V_O$ = 1Vp-p | | 0.25 | | µs |
| SEL to Channel OFF Time | 10% Point of $V_O$ = 1Vp-p | | 0.25 | | µs |
| Switching Transient, Positive | Measured While Switching | | +2.5 | | mV |
| Switching Transient, Negative | Between Two Grounded Channels | | –1.2 | | mV |
| **OUTPUT** | | | | | |
| Voltage | $V_{IN}$ = ±3V, $R_L$ = 5kΩ | ±2.8 | ±2.98 | | V |
| Resistance | One Channel Selected | | 11 | | Ω |
| Resistance | No Channel Selected | | 900 | | MΩ |
| Capacitance | No Channel Selected | | 1.5 | | pF |
| **POWER SUPPLY** | | | | | |
| Rated Voltage | | | ±5 | | V |
| Derated Performance | | ±4.5 | | ±5.5 | V |
| Quiescent Current | One Channel Selected | | ±4.6 | ±5 | mA |
| | No Channel Selected | | ±230 | ±350 | µA |
| **TEMPERATURE RANGE** | | | | | |
| Operating, AP, AU | | –40 | | +85 | °C |
| Storage, AP, AU | | –40 | | +125 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| AP, AU | | | 90 | | °C/W |

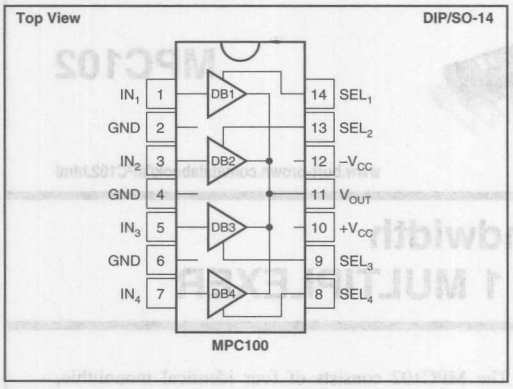


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At $V_{CC}$ = ±5V, $R_L$ = 10kΩ, $R_{SOURCE}$ = 50Ω, and $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | MPC100AP, AU MIN | MPC100AP, AU TYP | MPC100AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **AC CHARACTERISTICS** | | | | | |
| **FREQUENCY DOMAIN** | | | | | |
| **LARGE SIGNAL BANDWIDTH (–3dB)** | $V_O$ = 5.0Vp-p, $C_{OUT}$ = 1pF | | 70 | | MHz |
| | $V_O$ = 2.8Vp-p, $C_{OUT}$ = 1pF | | 140 | | MHz |
| | $V_O$ = 1.4Vp-p, $C_{OUT}$ = 1pF | | 250 | | MHz |
| **SMALL SIGNAL BANDWIDTH** | $V_O$ = 0.2Vp-p, $C_{OUT}$ = 1pF | | 450 | | MHz |
| **GROUP DELAY TIME** | | | 450 | | ps |
| **DIFFERENTIAL GAIN** | f = 4.43MHz, $V_{IN}$ = 0.3Vp-p | | | | |
| | VDC = 0 to 0.7V | | 0.05 | | % |
| | VDC = 0 to 1.4V | | 0.06 | | % |
| **DIFFERENTIAL PHASE** | f = 4.43MHz, $V_{IN}$ = 0.3Vp-p | | | | |
| | VDC = 0 to 0.7V | | 0.01 | | Degrees |
| | VDC = 0 to 1.4V | | 0.02 | | Degrees |
| **GAIN FLATNESS PEAKING** | $V_O$ = 0.2Vp-p, DC to 30MHz | | 0.04 | | dB |
| | $V_O$ = 0.2Vp-p, DC to 100MHz | | 0.05 | | dB |
| **HARMONIC DISTORTION** | f = 30MHz, $V_O$ = 1.4Vp-p, $R_L$ = 1kΩ | | | | |
| Second Harmonic | | | –53 | | dBc |
| Third Harmonic | | | –67 | | dBc |
| **CROSSTALK** | $V_I$ = 1.4Vp-p, Figures 4 and 8 | | | | |
| MPC100AP All Hostile | f = 5MHz, | | –82 | | dB |
| | f = 30MHz, | | –60 | | dB |
| Off Isolation | f = 5MHz, | | –70 | | dB |
| | f = 30MHz, | | –71 | | dB |
| MPC100AU All Hostile | f = 5MHz, | | –78 | | dB |
| | f = 30MHz, | | –70 | | dB |
| Off Isolation | f = 5MHz, | | –75 | | dB |
| | f = 30MHz | | –76 | | dB |
| **TIME DOMAIN** | | | | | |
| **RISE TIME** | $V_O$ = 1.4Vp-p, Step 10% to 90% | | | | |
| | $C_{OUT}$ = 1pF, $R_{OUT}$ = 22Ω | | 3.3 | | ns |
| **SLEW RATE** | $V_O$ = 2Vp-p | | | | |
| | $C_{OUT}$ = 1pF | | 650 | | V/µs |
| | $C_{OUT}$ = 22pF | | 460 | | V/µs |
| | $C_{OUT}$ = 47pF | | 320 | | V/µs |

## CONNECTION DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage ($\pm V_{CC}$) | ±6V |
| Analog Input Voltage ($IN_1$ through $IN_4$)(1) | $\pm V_{CC}$, ±0.7V |
| Logic Input Voltage | –0.6V to $+V_{CC}$ +0.6V |
| Operating Temperature | –40°C to +85°C |
| Storage Temperature | –40°C to +125°C |
| Output Current | ±6mA |
| Junction Temperature | +175°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Digital Input Voltages ($SEL_1$ through $SEL_4$)(1) | –0.5V to $+V_{CC}$ +0.7V |

NOTE: (1) Inputs are internally diode-clamped to $\pm V_{CC}$.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | TEMPERATURE RANGE | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|---|
| MPC100AP | –40°C to +85°C | 14-Pin Plastic DIP | 010 |
| MPC100AU | –40°C to +85°C | SO-14 Surface Mount | 235 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## FUNCTIONAL DESCRIPTION

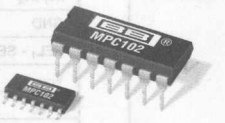
| | |
|---|---|
| $IN_1$-$IN_4$ | Four analog input channels |
| GND | Analog input shielding grounds, connect to system ground |
| $SEL_1$ - $SEL_4$ | Channel selection inputs |
| $V_{OUT}$ | Analog output; tracks selected channel |
| $-V_{CC}$ | Negative supply voltage; typical –5VDC |
| $+V_{CC}$ | Positive supply voltage; typical +5VDC |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

BURR - BROWN®



# MPC102

www.burr-brown.com/databook/MPC102.html

# Wide-Bandwidth DIFFERENTIAL 2 x 1 MULTIPLEXER

## FEATURES

- BANDWIDTH: 210MHz (1.4Vp-p)
- LOW INTERCHANNEL CROSSTALK: –68dB (30MHz, SO); –58dB (30MHz, DIP)
- LOW SWITCHING TRANSIENTS: +6mV/–8mV
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.02%, 0.02°
- LOW QUIESCENT CURRENT: One Channel Selected: ±4.6mA No Channel Selected: ±250µA

## APPLICATIONS

- VIDEO ROUTING AND MULTIPLEXING (CROSSPOINTS)
- RADAR SYSTEMS
- DATA ACQUISITION
- DISC R/W TEST SYSTEMS
- xDSL TEST SYSTEMS

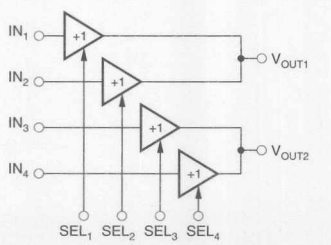
## DESCRIPTION

The MPC102 is dual, wide-bandwidth, differential 2-to-1 multiplexer, which can be used in a wide variety of applications.

It was designed for wide-bandwidth systems, including high-definition television and broadcast equipment. Although it is primarily used to route video signals, the harmonic and dynamic attributes of the MPC102 also make it appropriate for other analog signal routing applications such as radar, communications, computer graphics, and data acquisition systems.

The MPC102 consists of four identical monolithic, integrated, open-loop buffer amplifiers. Two buffer outputs are each connected internally at the output. The bipolar complementary buffers form a unidirectional transmission path and offer extremely high output-to-input isolation. The MPC102 multiplexer enables the user to connect one of two input signals to the corresponding output. The output of the multiplexer is in a high-impedance state when no channel is selected. When one channel is selected with a digital "1" at the corresponding SEL input, the component acts as a buffer with high input impedance and low output impedance.

The wide bandwidth of over 210MHz at 1.4Vp-p signal level, high linearity and low distortion, and low input voltage noise of $4nV/\sqrt{Hz}$ make this crosspoint switch suitable for RF and video applications. All performance is specified with ±5V supply voltage, which reduces power consumption in comparison with ±15V designs. The multiplexer is available in a space-saving SO-14 and DIP packages. Both are designed and specified for operation over the industrial temperature range (–40°C to +85°C.)




**TRUTH TABLE**

| $SEL_1$ | $SEL_2$ | $SEL_3$ | $SEL_4$ | $V_{OUT1}$ | $V_{OUT2}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | HI-Z | HI-Z |
| 1 | 0 | 0 | 0 | $IN_1$ | HI-Z |
| 0 | 1 | 0 | 0 | $IN_2$ | HI-Z |
| 0 | 0 | 1 | 0 | HI-Z | $IN_3$ |
| 0 | 0 | 0 | 1 | HI-Z | $IN_4$ |

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# SPECIFICATIONS

## ELECTRICAL

At $V_{CC}$ = ±5V, $R_L$ = 10kΩ, $R_{IN}$ = 150Ω, $R_{SOURCE}$ = 50Ω, and $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | MPC102AP, AU MIN | MPC102AP, AU TYP | MPC102AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | |
| **INPUT OFFSET VOLTAGE** | $R_{IN}$ = 0, $R_{SOURCE}$ = 0 | | | | |
| Initial | | | 14 | ±30 | mV |
| vs Temperature | | | 60 | | µV/°C |
| vs Supply (Tracking) | $V_{CC}$ = ±4.5V to ±5.5V | –40 | –74 | | dB |
| vs Supply (Non-tracking) | $V_{CC}$ = +4.5V to +5.5V | | –50 | | dB |
| vs Supply (Non-tracking) | $V_{CC}$ = –4.5V to –5.5V | | –50 | | dB |
| Initial Matching | All Four Buffers | | ±3 | | mV |
| **INPUT BIAS CURRENT** | | | | | |
| Initial | | | 4 | ±10 | µA |
| vs Temperature | | | 20 | | nA/°C |
| vs Supply (Tracking) | $V_{CC}$ = ±4.5V to ±5.5V | | ±710 | | nA/V |
| vs Supply (Non-tracking) | $V_{CC}$ = +4.5V to +5.5V | | 0.26 | | µA/V |
| vs Supply (Non-tracking) | $V_{CC}$ = –4.5V to –5.5V | | 1.7 | | µA/V |
| **INPUT IMPEDANCE** | | | | | |
| Resistance | Channel On | | 0.88 | | MΩ |
| Capacitance | Channel On | | 1.0 | | pF |
| Capacitance | Channel Off | | 1.0 | | pF |
| **INPUT NOISE** | | | | | |
| Voltage Noise Density | $f_{OUT}$ = 20kHz to 10MHz | | 4.0 | | nV/√Hz |
| Signal-to-Noise Ratio | S/N = 0.7/($V_{IN}$ • √5MHz) | | 98 | | dB |
| **INPUT VOLTAGE RANGE** | Gain Error ≤ 10% | | ±3.6 | | V |
| **TRANSFER CHARACTERISTICS** | | | | | |
| Voltage Gain | $R_L$ = 1kΩ, $V_{IN}$ = ±2V | | 0.982 | | V/V |
| Voltage Gain | $R_L$ = 10kΩ, $V_{IN}$ = ±2.8V | 0.98 | 0.992 | | V/V |
| **RATED OUTPUT** | | | | | |
| Voltage | $V_{IN}$ = ±3V, $R_L$ = 10kΩ | ±2.8 | ±2.98 | | V |
| Resistance | One Channel Selected | | 11 | | Ω |
| Resistance | No Channel Selected | | 900 | | MΩ |
| Capacitance | No Channel Selected | | 1.5 | | pF |
| **CHANNEL SELECTION INPUTS** | | | | | |
| Logic 1 Voltage | | +2 | | $V_{CC}$ | V |
| Logic 0 Voltage | | | | +0.8 | V |
| Logic 1 Current | $V_{SEL}$ = 5.0V | | 100 | 150 | µA |
| Logic 0 Current | $V_{SEL}$ = 0.8V | | | 5 | µA |
| **SWITCHING CHARACTERISTICS** | $V_{IN}$ = –0.3V to +0.7V, f = 5MHz | | | | |
| SEL to Channel ON Time | 90% Point of $V_{OUT}$ = 1Vp-p | | 0.25 | | µs |
| SEL to Channel OFF Time | 10% Point of $V_{OUT}$ = 1Vp-p | | 0.25 | | µs |
| Switching Transient, Positive | Measured While Switching | | 6 | | mV |
| Switching Transient, Negative | Between Two Grounded Channels | | –8 | | mV |
| **POWER SUPPLY** | | | | | |
| Rated Voltage | | | ±5 | | V |
| Derated Performance | | ±4.5 | | ±5.5 | V |
| Quiescent Current | One Channel Selected | | ±4.6 | ±5 | mA |
| | No Channel Selected | | ±250 | ±350 | µA |
| Rejection Ratio | | | –80 | | dB |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –40 | | +85 | °C |
| Storage | | –40 | | +125 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | 90 | | °C/W |

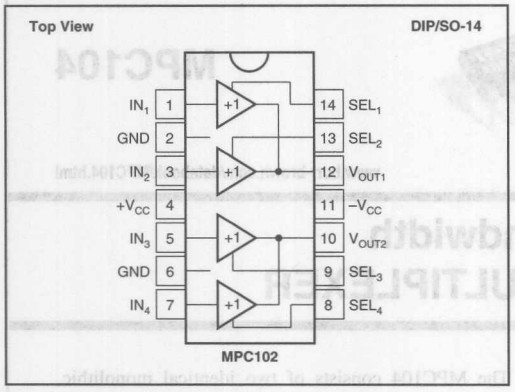


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At $V_{CC}$ = ±5V, $R_L$ = 10kΩ, $R_{IN}$ = 150Ω, $R_{SOURCE}$ = 50Ω, and $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | MPC102AP, AU MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **LARGE SIGNAL BANDWIDTH (–3dB)** | $V_{OUT}$ = 5.0Vp-p, $C_{OUT}$ = 1pF | | 55 | | MHz |
| | $V_{OUT}$ = 2.8Vp-p, $C_{OUT}$ = 1pF | | 100 | | MHz |
| | $V_{OUT}$ = 1.4Vp-p, $C_{OUT}$ = 1pF | | 210 | | MHz |
| **SMALL SIGNAL BANDWIDTH** | $V_{OUT}$ = 0.2Vp-p, $C_{OUT}$ = 1pF | | 370 | | MHz |
| **GROUP DELAY TIME** | | | 450 | | ps |
| **DIFFERENTIAL GAIN** | f = 4.43MHz, $V_{IN}$ = 0.3Vp-p VDC = 0 to 0.7V | | 0.02 | | % |
| **DIFFERENTIAL PHASE** | f = 4.43MHz, $V_{IN}$ = 0.3Vp-p VDC = 0 to 0.7V | | 0.02 | | Degrees |
| **GAIN FLATNESS PEAKING** | $V_{OUT}$ = 0.2Vp-p, DC to 30MHz | | 0.04 | | dB |
| | $V_{OUT}$ = 0.2Vp-p, DC to 100MHz | | 0.05 | | dB |
| **HARMONIC DISTORTION** | f = 30MHz, $V_{OUT}$ = 1.4Vp-p, $R_L$ = 350Ω | | | | |
| Second Harmonic | | | –64 | | dBc |
| Third Harmonic | | | –66 | | dBc |
| **CROSSTALK** | $V_{IN}$ = 1.4Vp-p | | | | |
| MPC102AP Channel-to-Channel | f = 5MHz, | | –75 | | dB |
| | f = 30MHz, | | –58 | | dB |
| Off Isolation | f = 5MHz, | | –70 | | dB |
| | f = 30MHz, | | –71 | | dB |
| MPC102AU Channel-to-Channel | f = 5MHz, | | –78 | | dB |
| | f = 30MHz, | | –68 | | dB |
| Off Isolation | f = 5MHz, | | –75 | | dB |
| | f = 30MHz | | –76 | | dB |
| **TIME DOMAIN** | | | | | |
| **RISE/FALL TIME** | $V_{OUT}$ = 1.4Vp-p, Step 10% to 90% $C_{OUT}$ = 1pF, $R_{OUT}$ = 22Ω | | 2.5 | | ns |
| **SLEW RATE** | $V_{OUT}$ = 1.4Vp-p | | | | |
| | $C_{OUT}$ = 1pF | | 500 | | V/µs |
| | $C_{OUT}$ = 22pF | | 360 | | V/µs |
| | $C_{OUT}$ = 47pF | | 260 | | V/µs |

## CONNECTION DIAGRAM




## PIN DESCRIPTION

| PIN | DESCRIPTION |
|---|---|
| $IN_1$, $IN_2$ | Analog Inputs Channel 1 and 2 |
| $IN_3$, $IN_4$ | Analog Inputs Channel 3 and 4 |
| GND | Analog Shielding Grounds, Connect to System Ground |
| $SEL_1$, $SEL_2$ | Channel Selection Inputs |
| $V_{OUT1}$ | Analog Output 1 |
| $V_{OUT2}$ | Analog Output 2 |
| $-V_{CC}$ | Negative Supply Voltage; typical –5VDC |
| $+V_{CC}$ | Positive Supply Voltage; typical +5VDC |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage ($\pm V_{CC}$) | ±6V |
| Analog Input Voltage ($IN_1$ through $IN_4$) | $\pm V_{CC}$, ±0.7V |
| Operating Temperature | –40°C to +85°C |
| Storage Temperature | –40°C to +125°C |
| Output Current | ±6mA |
| Junction Temperature | +175°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Digital Input Voltages ($SEL_1$ through $SEL_4$) | –0.5V to $+V_{CC}$ +0.7V |
| Logic Voltage Input | –0.6V to $+V_{CC}$ +0.6V |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| MPC102AP | 14-Pin DIP | 010 | –40°C to +85°C |
| MPC102AU | SO-14 Surface Mount | 235 | –40°C to +85°C |

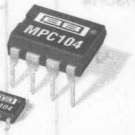
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®



# MPC104

www.burr-brown.com/databook/MPC104.html

# Wide-Bandwidth 2 x 1 VIDEO MULTIPLEXER

## FEATURES

- BANDWIDTH: 210MHz (1.4Vp-p)
- LOW INTERCHANNEL CROSSTALK: –79dB (30MHz, SO); –77dB (30MHz, DIP)
- LOW SWITCHING TRANSIENTS: +13mV/–4mV
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.03%, 0.01°
- LOW QUIESCENT CURRENT: One Channel Selected: ±4.6mA No Channel Selected: ±120µA

## APPLICATIONS

- VIDEO ROUTING AND MULTIPLEXING (CROSSPOINTS)
- RADAR SYSTEMS
- DATA ACQUISITION
- INFORMATION TERMINALS
- SATELLITE OR RADIO LINK IF ROUTING

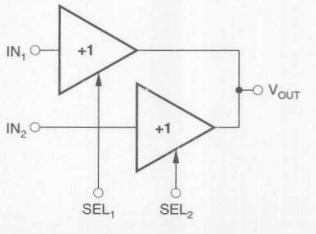
## DESCRIPTION

The MPC104 is a wide-bandwidth, 2-to-1 channel video signal multiplexer, which can be used in a wide variety of applications.

It was designed for wide-bandwidth systems, including high-definition television and broadcast equipment. Although it is primarily used to route video signals, the harmonic and dynamic attributes of the MPC104 also make it appropriate for other analog signal routing applications such as radar, communications, computer graphics, and data acquisition systems.

The MPC104 consists of two identical monolithic, integrated, open-loop buffer amplifiers, which are connected internally at the output. The bipolar complementary buffers form a unidirectional transmission path and offer extremely high output-to-input isolation. The MPC104 multiplexer enables the user to connect one of two input signals to the output. The output of the multiplexer is in a high-impedance state when no channel is selected. When one channel is selected with a digital "1" at the corresponding SEL input, the component acts as a buffer with high input impedance and low output impedance.

The wide bandwidth of over 210MHz at 1.4Vp-p signal level, high linearity and low distortion, and low input voltage noise of $5nV/\sqrt{Hz}$ make this crosspoint switch suitable for RF and video applications. All performance is specified with ±5V supply voltage, which reduces power consumption in comparison with ±15V designs. The multiplexer is available in a space-saving 8-pin SO and DIP packages. Both are designed and specified for operation over the industrial temperature range (–40°C to +85°C.)




### TRUTH TABLE

| $SEL_1$ | $SEL_2$ | $V_{OUT}$ |
|---|---|---|
| 0 | 0 | HI-Z |
| 1 | 0 | $IN_1$ |
| 0 | 1 | $IN_2$ |

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## SPECIFICATIONS–DC CHARACTERISTICS

At $V_{CC}$ = ±5VDC, $R_L$ = 10kΩ, $R_{IN}$ = 100Ω, $R_{SOURCE}$ = 50Ω, and $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | MPC104AP, AU MIN | MPC104AP, AU TYP | MPC104AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT OFFSET VOLTAGE** | | | | | |
| Initial | | | 14 | ±30 | mV |
| vs Temperature | | | 60 | | µV/°C |
| vs Supply (Tracking) | $V_{CC}$ = ±4.5V to ±5.5V | –40 | –80 | | dB |
| vs Supply (Non-tracking) | $V_{CC}$ = +4.5V to +5.5V | | –50 | | dB |
| vs Supply (Non-tracking) | $V_{CC}$ = –4.5V to –5.5V | | –50 | | dB |
| Initial Matching | All Buffers | | 3 | | mV |
| **INPUT BIAS CURRENT** | | | | | |
| Initial | | | 5 | ±10 | µA |
| vs Temperature | | | 20 | | nA/°C |
| vs Supply (Tracking) | $V_{CC}$ = ±4.5V to ±5.5V | | ±710 | | nA/V |
| vs Supply (Non-tracking) | $V_{CC}$ = +4.5V to +5.5V | | 0.26 | | µA/V |
| vs Supply (Non-tracking) | $V_{CC}$ = –4.5V to –5.5V | | 1.7 | | µA/V |
| **INPUT IMPEDANCE** | | | | | |
| Resistance | Channel On | | 0.88 | | MΩ |
| Capacitance | Channel On | | 1.0 | | pF |
| Capacitance | Channel Off | | 1.0 | | pF |
| **INPUT NOISE** | | | | | |
| Voltage Noise Density | $f_{OUT}$ = 20kHz to 10MHz | | 5 | | nV/√Hz |
| Signal-to-Noise Ratio | S/N = 0.7/$V_N$ • √5MHz | | 96 | | dB |
| **INPUT VOLTAGE RANGE** | Gain Error ≤ 10% | | ±3.6 | | V |
| **TRANSFER CHARACTERISTICS** | | | | | |
| Voltage Gain | $R_L$ = 1kΩ, $V_{IN}$ = ±2V | | 0.982 | | V/V |
| | $R_L$ = 10kΩ, $V_{IN}$ = ±2.8V | 0.98 | 0.992 | | V/V |
| **RATED OUTPUT** | | | | | |
| Voltage | $V_{IN}$ = ±3V | ±2.8 | ±2.97 | | V |
| Resistance | One Channel Selected | | 12.5 | | Ω |
| Resistance | No Channel Selected | | 900 | | MΩ |
| Capacitance | No Channel Selected | | 1.2 | | pF |
| **CHANNEL SELECTION INPUTS** | | | | | |
| Logic 1 Voltage | | +2 | | $V_{CC}$ +0.6 | V |
| Logic 0 Voltage | | | | +0.8 | V |
| Logic 1 Current | $V_{SEL}$ = 5.0V | 75 | 100 | 125 | µA |
| Logic 0 Current | $V_{SEL}$ = 0.8V | | 0.002 | 5 | µA |
| **SWITCHING CHARACTERISTICS** | $V_I$ = –0.3V to +0.7V, f = 5MHz | | | | |
| SEL to Channel ON Time | 90% Point of $V_{OUT}$ = 1Vp-p | | 0.13 | | µs |
| SEL to Channel OFF Time | 10% Point of $V_{OUT}$ = 1Vp-p | | 0.17 | | µs |
| Switching Transient, Positive | (Measured While Switching | | +13 | | mV |
| Switching Transient, Negative | Between Two Grounded Channels) | | –4 | | mV |
| **POWER SUPPLY** | | | | | |
| Rated Voltage | | | ±5 | | V |
| Derated Performance | | ±4.5 | | ±5.5 | V |
| Quiescent Current | One Channel Selected, Over Temperature | | ±4.6 | ±5.3 | mA |
| | No Channel Selected, Over Temperature | | ±120 | ±175 | µA |
| Rejection Ratio | | | –80 | | dB |



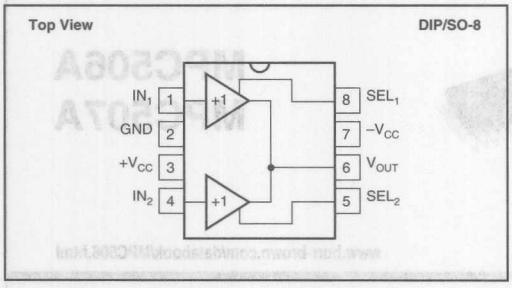
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## SPECIFICATIONS– AC CHARACTERISTICS

At $V_{CC}$ = ±5VDC, $R_L$ = 10kΩ, $R_{IN}$ = 100Ω, $R_{SOURCE}$ = 50Ω, and $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | MPC104AP, AU MIN | MPC104AP, AU TYP | MPC104AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **LARGE SIGNAL BANDWIDTH (–3dB)** | $V_{OUT}$ = 5.0Vp-p, $C_{OUT}$ = 1pF | | 55 | | MHz |
| | $V_{OUT}$ = 2.8Vp-p, $C_{OUT}$ = 1pF | | 101 | | MHz |
| | $V_{OUT}$ = 1.4Vp-p, $C_{OUT}$ = 1pF | | 210 | | MHz |
| **SMALL SIGNAL BANDWIDTH** | $V_{OUT}$ = 0.2Vp-p, $C_{OUT}$ = 1pF | | 590 | | MHz |
| **GROUP DELAY TIME** | | | 550 | | ps |
| **DIFFERENTIAL GAIN** | f = 4.43MHz, $V_{IN}$ = 0.3Vp-p | | | | |
| | VDC = 0 to 0.7V | | 0.03 | | % |
| **DIFFERENTIAL PHASE** | f = 4.43MHz, $V_{IN}$ = 0.3Vp-p | | | | |
| | VDC = 0 to 0.7V | | 0.01 | | Degrees |
| **GAIN FLATNESS PEAKING** | $V_{OUT}$ = 0.2Vp-p, DC to 30MHz | | 0.05 | | dB |
| | $V_{OUT}$ = 0.2Vp-p, DC to 100MHz | | 0.07 | | dB |
| **HARMONIC DISTORTION** | f = 30MHz, $V_{OUT}$ = 1.4Vp-p | | | | |
| Second Harmonic | | | –63 | | dBc |
| Third Harmonic | | | –65 | | dBc |
| **CROSSTALK** | $V_{IN}$ = 1.4Vp-p | | | | |
| MPC104AP Channel-to-Channel | f = 5MHz, | | –90 | | dB |
| | f = 30MHz, | | –77 | | dB |
| Off Isolation | f = 5MHz, | | –93 | | dB |
| | f = 30MHz, | | –81 | | dB |
| MPC104AU Channel-to-Channel | f = 5MHz, | | –95 | | dB |
| | f = 30MHz, | | –79 | | dB |
| Off Isolation | f = 5MHz, | | –93 | | dB |
| | f = 30MHz | | –86 | | dB |
| **RISE/FALL TIME** | $V_{OUT}$ = 1.4Vp-p, Step 10% to 90% | | | | |
| | $C_{OUT}$ = 1pF, $R_{OUT}$ = 22Ω | | 2.3 | | ns |
| **SLEW RATE** | $V_{OUT}$ = 1.4Vp-p | | | | |
| | $C_{OUT}$ = 1pF | | 500 | | V/µs |
| | $C_{OUT}$ = 22pF | | 360 | | V/µs |
| | $C_{OUT}$ = 47pF | | 260 | | V/µs |

## CONNECTION DIAGRAM




## PIN DESCRIPTION

| PIN | DESCRIPTION |
|---|---|
| $IN_1$, $IN_2$ | Analog Input Channels |
| GND | Analog Input Shielding Grounds, Connect to System Ground |
| $SEL_1$, $SEL_2$ | Channel Selection Inputs |
| $V_{OUT}$ | Analog Output; tracks selected channel |
| $-V_{CC}$ | Negative Supply Voltage; typical –5VDC |
| $+V_{CC}$ | Positive Supply Voltage; typical +5VDC |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage ($\pm V_{CC}$) | ±6VDC |
| Analog Input Voltage ($IN_1$ through $IN_2$) | $\pm V_{CC}$, ±0.7V |
| Operating Temperature | –40°C to +85°C |
| Storage Temperature | –40°C to +125°C |
| Output Current | ±6mA |
| Junction Temperature | +175°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Digital Input Voltages ($SEL_1$ through $SEL_2$) | –0.5V to $+V_{CC}$ +0.7V |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| MPC104AP | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| MPC104AU | SO-8 Surface Mount | 182 | –40°C to +85°C |

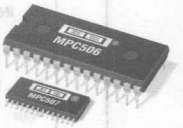
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®



# MPC506A
# MPC507A

www.burr-brown.com/databook/MPC506.html

# Single-Ended 16-Channel/Differential 8-Channel CMOS ANALOG MULTIPLEXERS

## FEATURES

- ANALOG OVERVOLTAGE PROTECTION: 70Vp-p
- NO CHANNEL INTERACTION DURING OVERVOLTAGE
- BREAK-BEFORE-MAKE SWITCHING
- ANALOG SIGNAL RANGE: ±15V
- STANDBY POWER: 7.5mW typ
- TRUE SECOND SOURCE

## DESCRIPTION

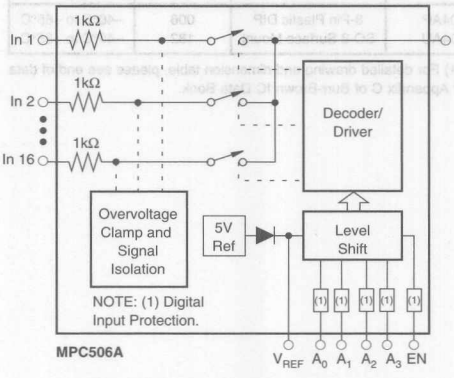
The MPC506A is a 16-channel single-ended analog multiplexer, and the MPC507A is an 8-channel differential multiplexer.

The MPC506A and MPC507A multiplexers have input overvoltage protection. Analog input voltages may exceed either power supply voltage without damaging the device or disturbing the signal path of other channels. The protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand 70Vp-p signal levels and standard ESD tests. Signal sources are protected from short circuits should multiplexer power loss occur; each input presents a 1kΩ resistance under this condition. Digital inputs can also sustain continuous faults up to 4V greater than either supply voltage.

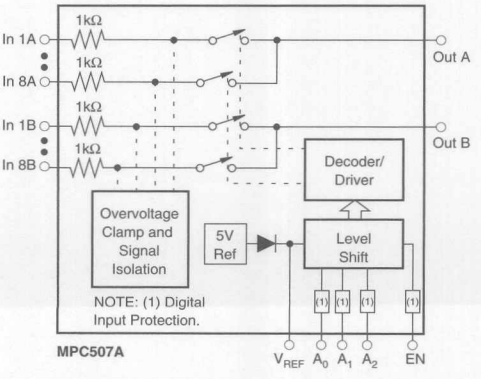
These features make the MPC506A and MPC507A ideal for use in systems where the analog signals originate from external equipment or separately powered sources.

The MPC506A and MPC507A are fabricated with Burr-Brown's dielectrically isolated CMOS technology. The multiplexers are available in plastic DIP and plastic SOIC packages. Temperature range is –40/+85°C.

### FUNCTIONAL DIAGRAMS




MPC506A




MPC507A

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PDS-774E

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# SPECIFICATIONS

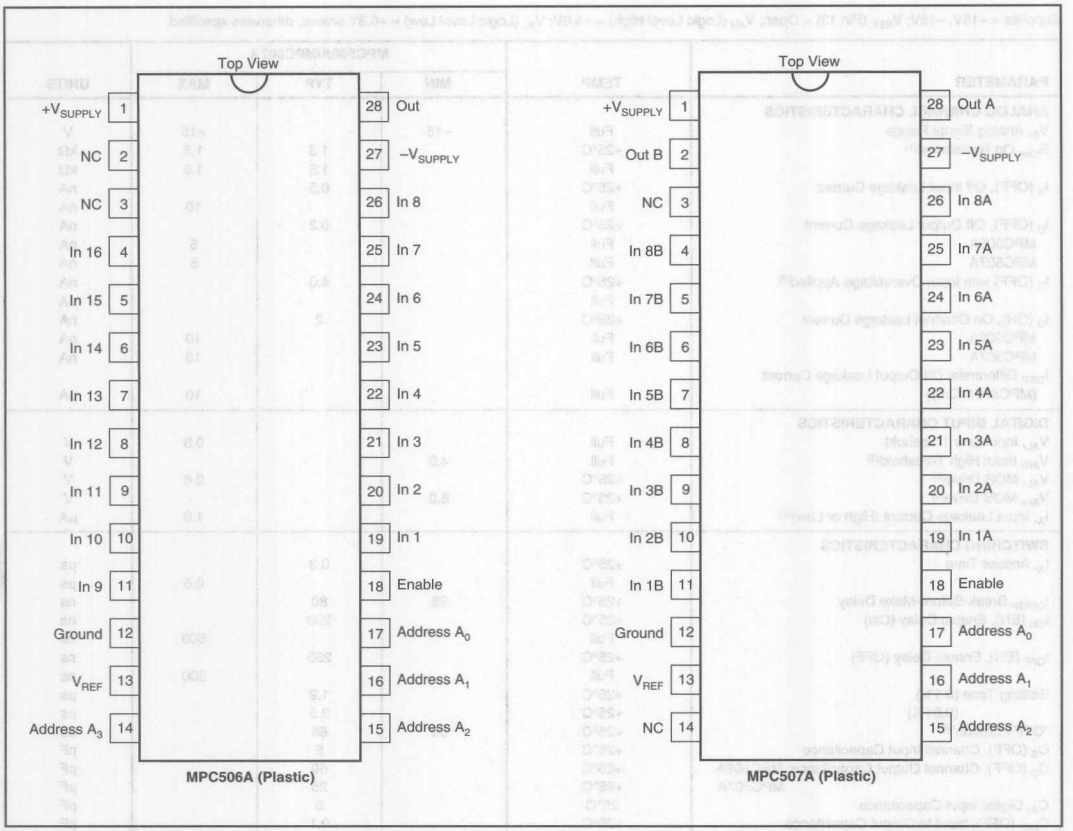
Supplies = +15V, –15V; $V_{REF}$ (Pin 13) = Open; $V_{AH}$ (Logic Level High) = +4.0V; $V_{AL}$ (Logic Level Low) = +0.8V unless, otherwise specified.

| PARAMETER | TEMP | MPC506A/MPC507A MIN | MPC506A/MPC507A TYP | MPC506A/MPC507A MAX | UNITS |
|---|---|---|---|---|---|
| **ANALOG CHANNEL CHARACTERISTICS** | | | | | |
| $V_S$, Analog Signal Range | Full | –15 | | +15 | V |
| $R_{ON}$, On Resistance(1) | +25°C | | 1.3 | 1.5 | kΩ |
| | Full | | 1.5 | 1.8 | kΩ |
| $I_S$ (OFF), Off Input Leakage Current | +25°C | | 0.5 | | nA |
| | Full | | | 10 | nA |
| $I_D$ (OFF), Off Output Leakage Current | +25°C | | 0.2 | | nA |
| MPC506A | Full | | | 5 | nA |
| MPC507A | Full | | | 5 | nA |
| $I_D$ (OFF) with Input Overvoltage Applied(2) | +25°C | | 4.0 | | nA |
| | Full | | | | µA |
| $I_D$ (ON), On Channel Leakage Current | +25°C | | 2 | | nA |
| MPC506A | Full | | | 10 | nA |
| MPC507A | Full | | | 10 | nA |
| $I_{DIFF}$ Differential Off Output Leakage Current (MPC507A Only) | Full | | | 10 | nA |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | |
| $V_{AL}$, Input Low Threshold | Full | | | 0.8 | V |
| $V_{AH}$, Input High Threshold(3) | Full | 4.0 | | | V |
| $V_{AL}$, MOS Drive(4) | +25°C | | | 0.8 | V |
| $V_{AH}$, MOS Drive(4) | +25°C | 6.0 | | | V |
| $I_A$, Input Leakage Current (High or Low)(5) | Full | | | 1.0 | µA |
| **SWITCHING CHARACTERISTICS** | | | | | |
| $t_A$, Access Time | +25°C | | 0.3 | | µs |
| | Full | | | 0.6 | µs |
| $t_{OPEN}$, Break-Before-Make Delay | +25°C | 25 | 80 | | ns |
| $t_{ON}$ (EN), Enable Delay (ON) | +25°C | | 200 | | ns |
| | Full | | | 500 | ns |
| $t_{OFF}$ (EN), Enable Delay (OFF) | +25°C | | 250 | | ns |
| | Full | | | 500 | ns |
| Settling Time (0.1%) | +25°C | | 1.2 | | µs |
| (0.01%) | +25°C | | 3.5 | | µs |
| "OFF Isolation"(6) | +25°C | 50 | 68 | | dB |
| $C_S$ (OFF), Channel Input Capacitance | +25°C | | 5 | | pF |
| $C_D$ (OFF), Channel Output Capacitance: MPC506A | +25°C | | 50 | | pF |
| MPC507A | +25°C | | 25 | | pF |
| $C_A$, Digital Input Capacitance | 25°C | | 5 | | pF |
| $C_{DS}$, (OFF), Input to Output Capacitance | +25°C | | 0.1 | | pF |
| **POWER REQUIREMENTS** | | | | | |
| $P_D$, Power Dissipation | Full | | 7.5 | | mW |
| I+, Current Pin 1(7) | Full | | 0.7 | 1.5 | mA |
| I–, Current Pin 27(7) | Full | | 5 | 20 | µA |

NOTES: (1) $V_{OUT}$ = ±10V, $I_{OUT}$ = –100µA. (2) Analog overvoltage = ±33V. (3) To drive from DTL/TTL circuits. 1kΩ pull-up resistors to +5.0V supply are recommended. (4) $V_{REF}$ = +10V. (5) Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at 25°C. (6) $V_{EN}$ = 0.8V, $R_L$ = 1kΩ, $C_L$ = 15pF, $V_S$ = 7Vrms, f = 100kHz. Worst-case isolation occurs on channel 8 due to proximity of the output pins. (7) $V_{EN}$, $V_A$ = 0V or 4.0V.



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## TRUTH TABLES

### MPC506A

| $A_3$ | $A_2$ | $A_1$ | $A_0$ | EN | "ON" CHANNEL |
|---|---|---|---|---|---|
| X | X | X | X | L | None |
| L | L | L | L | H | 1 |
| L | L | L | H | H | 2 |
| L | L | H | L | H | 3 |
| L | L | H | H | H | 4 |
| L | H | L | L | H | 5 |
| L | H | L | H | H | 6 |
| L | H | H | L | H | 7 |
| L | H | H | H | H | 8 |
| H | L | L | L | H | 9 |
| H | L | L | H | H | 10 |
| H | L | H | L | H | 11 |
| H | L | H | H | H | 12 |
| H | H | L | L | H | 13 |
| H | H | L | H | H | 14 |
| H | H | H | L | H | 15 |
| H | H | H | H | H | 16 |

### MPC507A

| $A_2$ | $A_1$ | $A_0$ | EN | "ON" CHANNEL PAIR |
|---|---|---|---|---|
| X | X | X | L | None |
| L | L | L | H | 1 |
| L | L | H | H | 2 |
| L | H | L | H | 3 |
| L | H | H | H | 4 |
| H | L | L | H | 5 |
| H | L | H | H | 6 |
| H | H | L | H | 7 |
| H | H | H | H | 8 |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| MPC506AP | 28-Pin Plastic | 215 |
| MPC506AU | 28-Pin Plastic SOIC | 217 |
| MPC507AP | 28-Pin Plastic | 215 |
| MPC507AU | 28-Pin Plastic SOIC | 217 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS[1]

Voltage between supply pins ..... 44V
$V_{REF}$ to ground, V+ to ground ..... 22V
V– to ground ..... 25V
Digital input overvoltage:
  $V_{EN}$, $V_A$: $V_{SUPPLY}$ (+) ..... +4V
  $V_{SUPPLY}$ (–) ..... –4V
  or 20mA, whichever occurs first.
Analog input overvoltage:
  $V_S$: $V_{SUPPLY}$ (+) ..... +20V
  $V_{SUPPLY}$ (–) ..... –20V
Continuous current, S or D ..... 20mA
Peak current, S or D
  (pulsed at 1ms, 10% duty cycle max) ..... 40mA
Power dissipation* ..... 2.0W
Operating temperature range ..... –40°C to +85°C
Storage temperature range ..... –65°C to +150°C

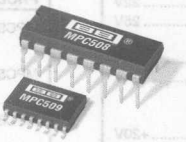
*Derate 20.0mW/°C above $T_A$ = 70

NOTE: (1) Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

## ORDERING INFORMATION

| PRODUCT | PACKAGE | TEMPERATURE RANGE | DESCRIPTION |
|---|---|---|---|
| MPC506AP | 28-Pin Plastic DIP | –40°C to +85°C | 16-Channel Single-Ended |
| MPC506AU | 28-Pin Plastic SOIC | –40°C to +85°C | 16-Channel Single-Ended |
| MPC507AP | 28-Pin Plastic DIP | –40°C to +85°C | 8-Channel Differential |
| MPC507AU | 28-Pin Plastic SOIC | –40°C to +85°C | 8-Channel Differential |

BURR-BROWN®




# MPC508A
# MPC509A

www.burr-brown.com/databook/MPC508.html

# Single-Ended 8-Channel/Differential 4-Channel CMOS ANALOG MULTIPLEXERS

## FEATURES

- ANALOG OVERVOLTAGE PROTECTION: 70Vp-p
- NO CHANNEL INTERACTION DURING OVERVOLTAGE
- BREAK-BEFORE-MAKE SWITCHING
- ANALOG SIGNAL RANGE: ±15V
- STANDBY POWER: 7.5mW typ
- TRUE SECOND SOURCE

## DESCRIPTION

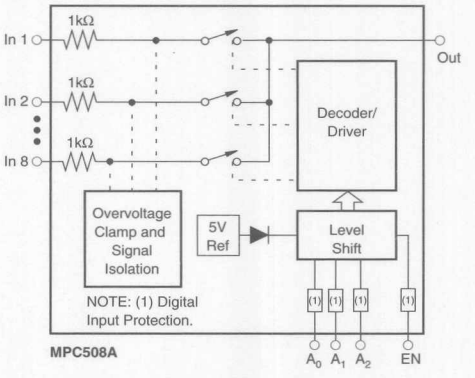
The MPC508A is an 8-channel single-ended analog multiplexer and the MPC509A is a 4-channel differential multiplexer.

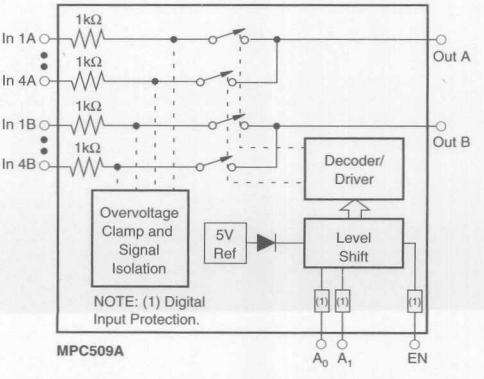
The MPC508A and MPC509A multiplexers have input overvoltage protection. Analog input voltages may exceed either power supply voltage without damaging the device or disturbing the signal path of other channels. The protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand 70Vp-p signal levels and standard ESD tests. Signal sources are protected from short circuits should multiplexer power loss occur; each input presents a 1kΩ resistance under this condition. Digital inputs can also sustain continuous faults up to 4V greater than either supply voltage.

These features make the MPC508A and MPC509A ideal for use in systems where the analog signals originate from external equipment or separately powered sources.

The MPC508A and MPC509A are fabricated with Burr-Brown's dielectrically isolated CMOS technology. The multiplexers are available in plastic DIP and plastic SOIC packages. Temperature range is –40°C to +85°C.

### FUNCTIONAL DIAGRAMS




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# SPECIFICATIONS

## ELECTRICAL

Supplies = +15V, −15V; $V_{AH}$ (Logic Level High) = +4.0V, $V_{AL}$ (Logic Level Low) = +0.8V, unless otherwise specified.

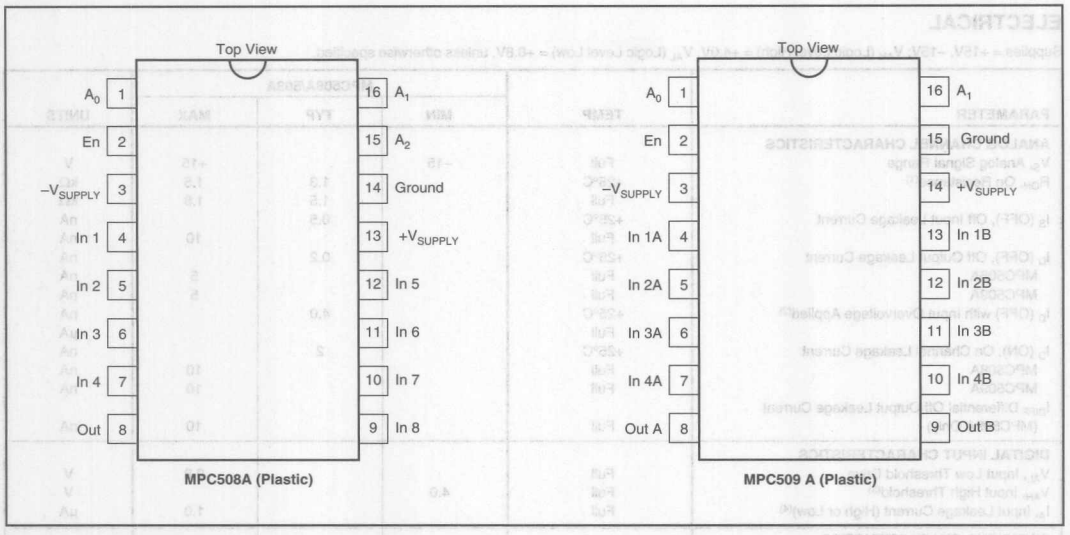
| PARAMETER | TEMP | MPC508A/509A MIN | MPC508A/509A TYP | MPC508A/509A MAX | UNITS |
|---|---|---|---|---|---|
| **ANALOG CHANNEL CHARACTERISTICS** | | | | | |
| $V_S$, Analog Signal Range | Full | −15 | | +15 | V |
| $R_{ON}$, On Resistance[1] | +25°C | | 1.3 | 1.5 | kΩ |
| | Full | | 1.5 | 1.8 | kΩ |
| $I_S$ (OFF), Off Input Leakage Current | +25°C | | 0.5 | | nA |
| | Full | | | 10 | nA |
| $I_D$ (OFF), Off Output Leakage Current | +25°C | | 0.2 | | nA |
| MPC508A | Full | | | 5 | nA |
| MPC509A | Full | | | 5 | nA |
| $I_D$ (OFF) with Input Overvoltage Applied[2] | +25°C | | 4.0 | | nA |
| | Full | | | | µA |
| $I_D$ (ON), On Channel Leakage Current | +25°C | | 2 | | nA |
| MPC508A | Full | | | 10 | nA |
| MPC509A | Full | | | 10 | nA |
| $I_{DIFF}$ Differential Off Output Leakage Current (MPC509A Only) | Full | | | 10 | nA |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | |
| $V_{AL}$, Input Low Threshold Drive | Full | | | 0.8 | V |
| $V_{AH}$, Input High Threshold[3] | Full | 4.0 | | | V |
| $I_A$, Input Leakage Current (High or Low)[4] | Full | | | 1.0 | µA |
| **SWITCHING CHARACTERISTICS** | | | | | |
| $t_A$, Access Time | +25°C | | 0.5 | | µs |
| | Full | | | 0.6 | µs |
| $t_{OPEN}$, Break-Before-Make Delay | +25°C | 25 | 80 | | ns |
| $t_{ON}$ (EN), Enable Delay (ON) | +25°C | | 200 | | ns |
| | Full | | | 500 | ns |
| $t_{OFF}$ (EN), Enable Delay (OFF) | +25°C | | 250 | | ns |
| | Full | | | 500 | ns |
| Settling Time (0.1%) | +25°C | | 1.2 | | µs |
| (0.01%) | +25°C | | 3.5 | | µs |
| "OFF Isolation"[5] | +25°C | 50 | 68 | | dB |
| $C_S$ (OFF), Channel Input Capacitance | +25°C | | 5 | | pF |
| $C_D$ (OFF), Channel Output Capacitance: MPC508A | +25°C | | 25 | | pF |
| MPC509A | +25°C | | 12 | | pF |
| $C_A$, Digital Input Capacitance | 25°C | | 5 | | pF |
| $C_{DS}$ (OFF), Input to Output Capacitance | +25°C | | 0.1 | | pF |
| **POWER REQUIREMENTS** | | | | | |
| $P_D$, Power Dissipation | Full | | 7.5 | | mW |
| I+, Current Pin 1[6] | Full | | 0.7 | 1.5 | mA |
| I−, Current Pin 27[6] | Full | | 5 | 20 | µA |

NOTES: (1) $V_{OUT}$ = ±10V, $I_{OUT}$ = −100µA. (2) Analog overvoltage = ±33V. (3) To drive from DTL/TTL circuits. 1kΩ pull-up resistors to +5.0V supply are recommended. (4) Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at 25°C. (5) $V_{EN}$ = 0.8V, $R_L$ = 1kΩ, $C_L$ = 15pF, $V_S$ = 7Vrms, f = 100kHz. Worst-case isolation occurs on channel 4 due to proximity of the output pins. (6) $V_{EN}$, $V_A$ = 0V or 4.0V.



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## PIN CONFIGURATIONS




## TRUTH TABLES

### MPC508A

| $A_2$ | $A_1$ | $A_0$ | EN | "ON" CHANNEL |
|---|---|---|---|---|
| X | X | X | L | None |
| L | L | L | H | 1 |
| L | L | H | H | 2 |
| L | H | L | H | 3 |
| L | H | H | H | 4 |
| H | L | L | H | 5 |
| H | L | H | H | 6 |
| H | H | L | H | 7 |
| H | H | H | H | 8 |

### MPC509A

| $A_1$ | $A_0$ | EN | "ON" CHANNEL PAIR |
|---|---|---|---|
| X | X | L | None |
| L | L | H | 1 |
| L | H | H | 2 |
| H | L | H | 3 |
| H | H | H | 4 |

## ABSOLUTE MAXIMUM RATINGS(1)

Voltage between supply pins ..... 44V
V+ to ground ..... 22V
V– to ground ..... 25V
Digital input overvoltage $V_{EN}$, $V_A$:
$V_{SUPPLY}$ (+) ..... +4V
$V_{SUPPLY}$ (–) ..... –4V
or 20mA, whichever occurs first.
Analog input overvoltage $V_S$:
$V_{SUPPLY}$ (+) ..... +20V
$V_{SUPPLY}$ (–) ..... –20V
Continuous current, S or D ..... 20mA
Peak current, S or D
(pulsed at 1ms, 10% duty cycle max) ..... 40mA
Power dissipation(2) ..... 1.28W
Operating temperature range ..... –40°C to +85°C
Storage temperature range ..... –65°C to +150°C

NOTE: (1) Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. (2) Derate 1.28mW/°C above $T_A$ = +70°C.

## ORDERING INFORMATION

| PRODUCT | PACKAGE | TEMPERATURE RANGE | DESCRIPTION |
|---|---|---|---|
| MPC508AP | 16-Pin Plastic DIP | –40°C to +85°C | 8-Channel Single-Ended |
| MPC508AU | 16-Pin Plastic SOIC | –40°C to +85°C | 8-Channel Single-Ended |
| MPC509AP | 16-Pin Plastic DIP | –40°C to +85°C | 4-Channel Differential |
| MPC509AU | 16-Pin Plastic SOIC | –40°C to +85°C | 4-Channel Differential |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| MPC508/509AP | 16-Pin Plastic DIP | 180 |
| MPC508/509AU | 16-Pin Plastic SOIC | 211 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

# 6 Sample/Hold Amplifiers

Sample/hold amplifiers are a key part of an A/D conversion solution. While many new A/D converters have a self-contained sample/hold on the A/D chip, sample/hold amplifiers play a role in specialized applications such as multiple channel simultaneous sampling, and ultra-high speed sampling and multichannel output applications.

Use of a sample/hold increases the sampling bandwidth of an analog-to-digital converter by up to four orders of magnitude, while insuring that an accurate value of the signal to be converter is captured at a specific instant in time.

## SAMPLE/HOLD AMPLIFIERS
### (Acquisition Time, max)

**12-BIT**
SHC605 (0.35µs)
SHC804 (0.35µs)
SHC803 (0.35µs)
SHC5320 (1.5µs)
SHC298 (10µs)

**14-BIT**
SHC76 (6µs)

**WIDE-BAND**
SHC615 (15ns)
SHC804 (0.35µs)
SHC605 (0.03µs)

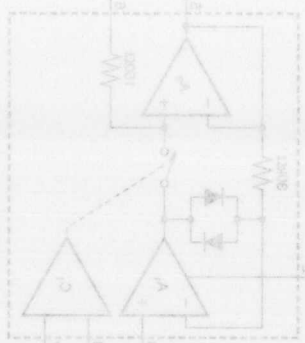
**BOLD DENOTES NEW PRODUCT**
***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

# SAMPLE/HOLD CIRCUITS

| Product | Gain Error (%) | Offset Error (mV) | Charge Offset (mV) | Small Signal Bandwidth (MHz) (typ) | Acq Time to 0.01% (µs max) | Droop Rate (µV/µs) | Temp Range[1] | Input Range (Vp-p) | Pkg[2] | Description |
|---|---|---|---|---|---|---|---|---|---|---|
| SHC76 | ±0.02 | ±3 | ±6 typ | 1.5 | 3 | ±1 | Ind, Com, Mil | 20 | HMD | Fast, High Accuracy |
| SHC298 | ±0.01 | ±7 | ±25 max | 0.125 | 10 | ±100,000 | Com, Ind | 23 | PDIP, MC, SOIC | Lowest Cost Industry Std |
| SHC605 | ±0.1 | ±5 | ±20 | 200 | 0.02* | ±8000 | Ext | 4.0 | 16-p SOIC | Low Cost |
| SHC615 | 0.1[3] | 8 (typ) | — | 750 | 15ns[3] | ±33,000[3] | Xlind | 2 | PDIP, SOIC | Wideband DC Restoration Cir |
| SHC803 | ±0.1 | ±3 | ±10 | 16 | 0.35 | ±5 | Ind | 20 | HMD | High Speed with Buffer |
| SHC804 | ±0.1 | ±3 | ±5 | 16 | 0.35 | ±5 | Ind | 20 | HMD | High Speed |
| SHC5320 | NA | ±0.5 | ±1 typ | 2 | 1.5 | ±0.5 | Com, Mil | 20 | HCD, PDIP, SOIC | Low Cost, Fast Industry Std |

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C, Ext = –40°C to +85°C. (2) MC = Metal Can, PDIP = Plastic DIP, HCD = Hermetic Ceramic DIP, CD = Ceramic DIP, HMD = Hermetic Metal DIP, SOIC = Surface Mount Package. (3) With 27pF external hold capacitor.



* DENOTES TYPICAL

**BOLD DENOTES NEW PRODUCT**

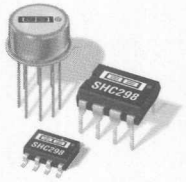
***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.



Or, Call Customer Service at 1-800-548-6132 (USA Only)

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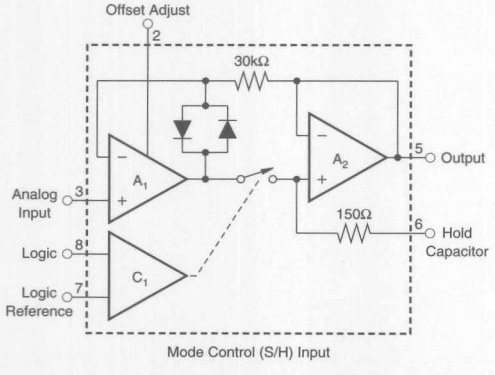
# SHC298
# SHC298A

www.burr-brown.com/databook/SHC298.html

# Monolithic SAMPLE/HOLD AMPLIFIER

## FEATURES

- 12-BIT THROUGHPUT ACCURACY
- LESS THAN 10µs ACQUISITION TIME
- WIDEBAND NOISE LESS THAN 20µVrms
- RELIABLE MONOLITHIC CONSTRUCTION
- $10^{10}\Omega$ INPUT RESISTANCE
- TTL-CMOS-COMPATIBLE LOGIC INPUT




## DESCRIPTION

The SHC298 and SHC298A are high-performance monolithic sample/hold amplifiers featuring high DC accuracy with fast acquisition times and a low droop rate. Dynamic performance and holding performance can be optimized with proper selection of the external holding capacitor. With a 1000pF holding capacitor, 12-bit accuracy can be achieved with a 6µs acquisition time. Droop rates less than 5mV/min are possible with a 1µF holding capacitor.

These sample/holds will operate over a wide supply voltage ranging from ±5V to ±18V with very little change in performance. A separate Offset Adjust pin is used to adjust the offset in either the Sample on the Hold modes. The fully differential logic inputs have low input current, and are compatible with TTL, 5V CMOS, and CMOS logic families.

The SHC298AM is available in a hermetically sealed 8-pin TO-99 package and is specified over a temperature range from –25°C to +85°C. The SHC298JP and SHC298JU are 8-pin plastic DIP and SOIC packaged parts specified over 0°C to +70°C.

The SHC298AJP, specified over 0°C to +70°C, is available in an 8-pin plastic DIP. The SHC298A grade features improved gain and offset error, improved drift over temperature, and faster acquisition time.

The SHC298 family is a price-performance bargain. It is well suited for use with several 12-bit A/D converters in data acquisition systems, data distribution systems, and analog delay circuits.

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# SPECIFICATIONS

## ELECTRICAL

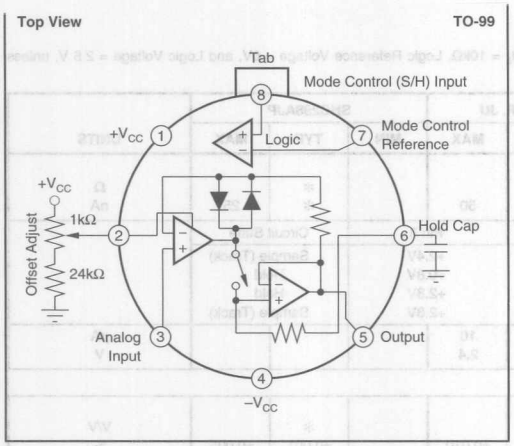
At $T_J$ = +25°C, ±15V supplies, 1000pF holding capacitor, −11.5V ≤ $V_{IN}$ ≤ +11.5, $R_L$ = 10kΩ, Logic Reference Voltage = 0V, and Logic Voltage = 2.5 V, unless otherwise noted.

| PARAMETER | SHC298AM, JP, JU MIN | SHC298AM, JP, JU TYP | SHC298AM, JP, JU MAX | SHC298AJP MIN | SHC298AJP TYP | SHC298AJP MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **ANALOG INPUT** | | | | | | | |
| Resistance | | $10^{10}$ | | | * | | Ω |
| Bias Current(1) | | 10 | 50 | | * | 25 | nA |
| **DIGITAL INPUT** | Pin 7 | | Pin 8 | | Circuit State | | |
| Mode Control Truth Table | 0V | | +2.4V | | Sample (Track) | | |
| | 0V | | +0.8V | | Hold | | |
| | +2.4V | | +2.8V | | Hold | | |
| | +0.8V | | +2.8V | | Sample (Track) | | |
| Mode Control and Mode Control Reference Input Current | | | 10 | | | | µA |
| Differential Logic Threshold | 0.8 | 1.4 | 2.4 | | | | V |
| **TRANSFER CHARACTERISTICS** | | | | | | | |
| **ACCURACY (+25°C)** | | | | | | | |
| Gain | | +1 | | | * | | V/V |
| Gain Error | | ±0.004 | ±0.010 | | ±0.001 | ±0.005 | % |
| Input Voltage Offset (adjust to zero)(1) | | ±2 | ±7 | | ±1 | ±2 | mV |
| Droop Rate(1) | | ±30 | | | * | | µV/ms |
| Power Supply Rejection | | ±25 | ±100 | | * | * | µV/V |
| **ACCURACY DRIFT** | | | | | | | |
| Gain Drift | | 3 | 4 | | 1 | 2 | ppm/°C |
| Input Offset Drift | | 15 | 70 | | * | 25 | µV/°C |
| Droop Rate at $T_J$ = +85°C | | 10 | | | * | | mV/ms |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Aperture Time : Negative Input Step | | 200 | | | * | | ns |
| Positive Input Step | | 150 | | | * | | ns |
| Acquisition Time (C = 1000pF): to ±0.1%, 10V Step | | 5 | | | 4 | 6 | µs |
| Sample/Hold Transient: Peak Amplitude | | 160 | | | * | | mV |
| Settling to 1mV | | 1 | | | * | | µs |
| Feedthrough (Response to 10V Input Step) | | ±0.007 | | | ±0.004 | | % of 20V |
| **OUTPUT** | | | | | | | |
| **ANALOG OUTPUT** | | | | | | | |
| Voltage Range | ±11.5 | | | * | | | V |
| Current Range | ±2 | | | * | | | mA |
| Impedance (in Hold Mode) | 0.5 | 4 | | * | * | | Ω |
| **POWER SUPPLY** | | | | | | | |
| Rate Voltage | | 15 | | | * | | VDC |
| Range | ±5 | | ±18 | * | | * | VDC |
| Current(1) | | ±4.5 | ±6.5 | | * | * | mA |

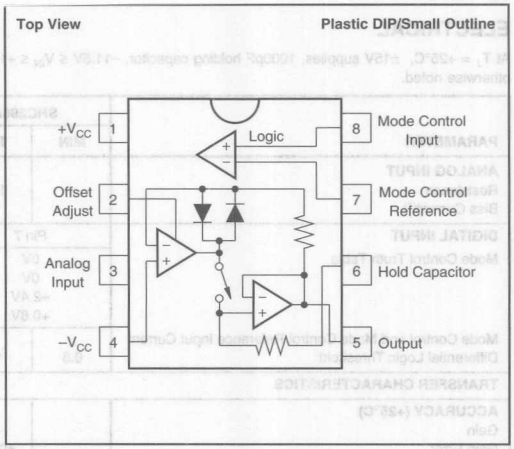
* Same as specifications for SHC298AM, JP, JU.

NOTES: (1) These parameters guaranteed over a supply voltage range of ±5V to = ±18V. (2) Charge offset is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01µF hold capacitor. Magnitude of the charge offset is inversely proportional to hold capacitor value.

Top View TO-99




Top View Plastic DIP/Small Outline




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±18V |
| Power Dissipation (Package Limitation) | 500mV |
| Junction Temperature, $T_{J\,MAX}$ | |
| AM | 125°C |
| JP, JU | 100°C |
| Operating Temperature Range | –25°C to +85°C |
| Storage Temperature Range | –65°C to +150°C |
| Input Voltage | Equal to Supply Voltage |
| Logic-to-Logic Reference Differential Voltage(1) | +7V, –30V |
| Output Short Circuit Duration | Indefinite |
| Hold Capacitor Short Circuit Duration | 10s |
| Lead Temperature (soldering, 10s) | 300°C |

NOTE: (1) Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| SHC298AM | TO-99 | 001 | –25°C to +85°C |
| SHC298JP | 8-Pin Plastic DIP | 006 | 0°C to +70°C |
| SHC298JU | 8-Lead SOIC | 182 | 0°C to +70°C |
| SHC298AJP | 8-Pin Plastic DIP | 006 | 0°C to +70°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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BURR-BROWN®




# SHC605

**DEMO BOARD AVAILABLE**
**See Appendix A**

www.burr-brown.com/databook/SHC605.html

# High-Speed Operational TRACK-AND-HOLD AMPLIFIER



## FEATURES

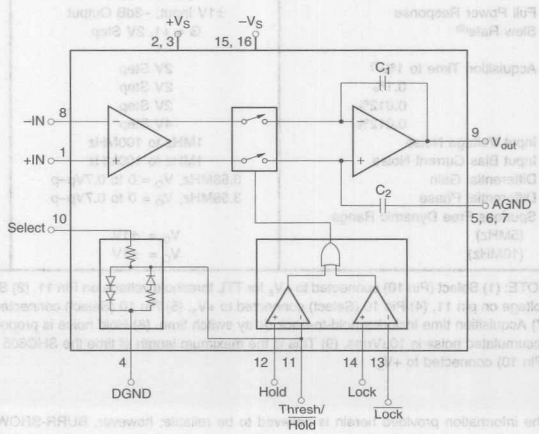
- VERY GOOD SPURIOUS FREE DYNAMIC RANGE:
  90dB at 1MHz $F_{IN}$ and 20MSPS
  86dB at 2MHz $F_{IN}$ and 20MSPS
  77dB at 5MHz $F_{IN}$ and 20MSPS
- LOW ACQUISITION TIME: 30ns to 0.01%
- LOW DROOP RATE: 8mV/μs max $T_{MIN}$ to $T_{MAX}$
- LOW POWER CONSUMPTION: 335mW
- EXTREMELY VERSATILE ARCHITECTURE: Noninverting, Inverting, and Differential Gains
- LOGIC FLEXIBILITY: TTL and ECL Compatible
- SMALL PACKAGE: SO-16
- EXTENDED TEMPERATURE SPECS: –40°C to +85°C

## APPLICATIONS

- A/D CONVERTER FRONT ENDS
- MULTIPLE CHANNEL SIMULTANEOUS SAMPLING
- IMPROVING FLASH ADC PERFORMANCE
- PEAK DETECTORS
- DAC DEGLITCHING

## DESCRIPTION

The SHC605 is a monolithic high-speed, high accuracy track-and-hold amplifier. It combines fast acquisition and low distortion to provide a complete solution for a wide range of sampling applications. Its new proprietary closed-loop architecture provides a single-chip solution to many data acquisition problems formerly requiring more than one device. Noninverting, inverting, and differential gain configurations are easy to apply with the SHC605. An on-board logic reference circuit makes the SHC605 compatible with both single-ended and differential ECL or TTL clock inputs. An internal track-mode lockout circuit allows edge-triggered operation in data acquisition systems. The SHC605 is available in a SO-16 surface-mount package specified for the –40C to +85C industrial temperature range.




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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $\pm V_S$ = ±5V, G = +1V/V, $R_L$ = 100Ω, $C_L$ = 5pF, and ECL Hold/$\overline{\text{Hold}}$ Inputs, unless otherwise noted.

| PARAMETER | CONDITION | TEMP RANGE | SHC605AU MIN | SHC605AU TYP | SHC605AU MAX | UNITS |
|---|---|---|---|---|---|---|
| **DC INPUT PARAMETERS** | | | | | | |
| Offset Voltage | | Full | | ±1 | ±7.5 | mV |
| Power Supply Rejection | $V_S$ = ±4.5 to ±5.5V | +25°C | 60 | 85 | | dB |
| Input Bias Current | $V_{CM}$ = 0V | Full | | 15 | 50 | µA |
| Input Offset Current | $V_{CM}$ = 0V | Full | | ±0.2 | ±5 | µA |
| Common-Mode Input Range | | Full | ±2.0 | ±2.5 | | V |
| Common-Mode Rejection | $V_{CM}$ = ±2VDC | Full | | 80 | | dB |
| Differential Input Impedance | | Full | | 13\|\|1 | | kΩ\|\|pF |
| Common-Mode Input Impedance | | Full | | 2\|\|1 | | MΩ\|\|pF |
| Open-Loop Voltage Gain | $V_O$ = ±2V, $R_L$ = 100Ω | +25°C | | 100 | | dB |
| **OUTPUT** | | | | | | |
| Voltage Output | $R_L$ = 50Ω | Full | ±2.0 | ±2.5 | | V |
| Current Output | | +25°C | ±40 | ±80 | | mA |
| | | Full | ±40 | ±60 | | mA |
| Short Circuit Current | | Full | | ±140 | | mA |
| Output Resistance, | | | | | | |
| Closed-Loop: Track-Mode | DC | Full | | 0.0001 | | Ω |
| Hold-Mode | DC | Full | | 0.01 | | Ω |
| **DIGITAL INPUTS/OUTPUTS** | | | | | | |
| TTL Input Levels[1] | Hold Input Only | | | | | |
| $V_{IL}$ | Logic "LO" | Full | 0 | | +1.0 | V |
| $V_{IH}$ | Logic "HI" | Full | +2.0 | | +5.0 | V |
| Single-Ended ECL Input Levels[2] | Hold/$\overline{\text{Hold}}$ and Lock/$\overline{\text{Lock}}$ Inputs | | | | | |
| $V_{IL}$ | Logic "LO" | Full | –1.80 | | –1.45 | V |
| $V_{IH}$ | Logic "HI" | Full | –1.05 | | –0.80 | V |
| Common-Mode Input Voltages | Hold/$\overline{\text{Hold}}$ | Full | –3 | | +5 | V |
| | Lock/$\overline{\text{Lock}}$ | Full | $-V_S$ | | +3 | V |
| Differential Input Voltages | Hold/$\overline{\text{Hold}}$ and Lock/$\overline{\text{Lock}}$ Inputs | Full | 0.2 | | 5.0 | V |
| Digital Input Currents | | | | | | |
| $I_{IL}$, Lock/$\overline{\text{Lock}}$ Inputs Only | ECL Logic "LO", $V_{IL}$ = –1.60V | Full | | | 5 | µA |
| $I_{IL}$, Hold/$\overline{\text{Hold}}$ Inputs Only | ECL or TTL Logic "LO" | Full | | | –100 | µA |
| $I_{IH}$, Lock/$\overline{\text{Lock}}$ Inputs Only | Logic "HI", $V_{IH}$ = –1.0V | Full | | | 50 | µA |
| $I_{IH}$, Hold/$\overline{\text{Hold}}$ Inputs Only | | Full | | | –10 | µA |
| Threshold Voltage Output[3] | | | | | | |
| TTL[4] | | Full | 1.1 | 1.5 | 1.9 | V |
| ECL[5] | $-V_S$ = –5.2V | Full | –1.40 | | –1.10 | V |
| **TRACK-MODE RESPONSE** | | | | | | |
| Closed-Loop Bandwidth | Gain = +1V/V | +25°C | 100 | 200 | | MHz |
| | Gain = +2V/V | +25°C | | 75 | | MHz |
| | Gain = +5V/V | +25°C | | 20 | | MHz |
| | Gain = +10V/V | +25°C | | 10 | | MHz |
| Full Power Response | ±1V Input, –3dB Output | Full | | 32 | | MHz |
| Slew Rate[6] | G = +1, 2V Step | +25°C | 140 | 200 | | V/µs |
| | | Full | 120 | 200 | | V/µs |
| Acquisition Time to 1%[7] | 2V Step | Full | | 15 | 25 | ns |
| 0.1% | 2V Step | Full | | 23 | 35 | ns |
| 0.012% | 2V Step | Full | | 30 | 45 | ns |
| 0.012% | 4V Step | Full | | 40 | 60 | ns |
| Input Voltage Noise | 1MHz to 100MHz | | | 2.5 | | nV/√Hz |
| Input Bias Current Noise | 1MHz to 100MHz | | | 2.5 | | pA/√Hz |
| Differential Gain | 3.58MHz, $V_O$ = 0 to 0.7Vp–p | | | 0.005 | | % |
| Differential Phase | 3.58MHz, $V_O$ = 0 to 0.7Vp–p | | | 0.005 | | Degrees |
| Spurious Free Dynamic Range | | | | | | |
| (5MHz) | $V_O$ = ±1V | | | 83 | | dBc |
| (10MHz) | $V_O$ = ±1V | | | 73 | | dBc |

NOTE: (1) Select (Pin 10) connected to $+V_S$ for TTL threshold voltage on Pin 11. (2) Select (Pin 10) connected to $-V_S$ for ECL threshold voltage on Pin 11. (3) Output voltage on pin 11. (4) Pin 10 (Select) connected to $+V_S$. (5) Pin 10 (Select) connected to $-V_S$. (6) Slew rate is rate of change from 10% to 90% of a 2V output step. (7) Acquisition time includes hold-to-track delay switch time. (8) Hold noise is proportional to the time in the hold mode. For example, if the hold time is 25ns, the accumulated noise is 10µVrms. (9) This is the maximum length of time the SHC605 can remain in the hold mode and still maintain a linear droop rate. (10) Select (Pin 10) connected to $+V_S$.

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# SPECIFICATIONS (CONT)

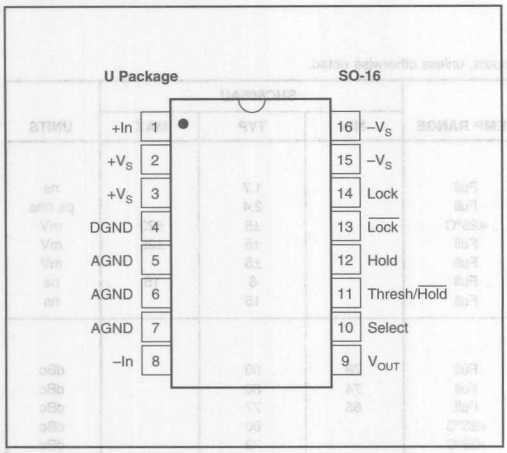
## ELECTRICAL

At $T_A$ = +25°C, $\pm V_S$ = ±5V, G = +1V/V, $R_L$ = 100Ω, $C_L$ = 5pF, and ECL Hold/$\overline{\text{Hold}}$ Inputs, unless otherwise noted.

| PARAMETER | CONDITION | TEMP RANGE | SHC605AU MIN | SHC605AU TYP | SHC605AU MAX | UNITS |
|---|---|---|---|---|---|---|
| **TRACK-TO-HOLD SWITCHING** | $V_{IN}$ = 0V | | | | | |
| Aperture Delay | | Full | | 1.7 | | ns |
| Aperture Jitter | | Full | | 2.4 | | ps rms |
| Pedestal Offset | | +25°C | | ±5 | ±20 | mV |
| over Temperature | | Full | | ±5 | ±25 | mV |
| Transient Amplitude | | Full | | ±5 | | mV |
| Settling Time to 1mV | | Full | | 8 | 15 | ns |
| 100µV | | Full | | 15 | | ns |
| **HOLD-MODE RESPONSE** | | | | | | |
| Spurious Free Dynamic Range | | | | | | |
| (1MHz, 20MSPS) | $V_O$ = ±1V | Full | 78 | 90 | | dBc |
| (2MHz, 20MSPS) | $V_O$ = ±1V | Full | 74 | 86 | | dBc |
| (5MHz, 20MSPS) | $V_O$ = ±1V | Full | 65 | 77 | | dBc |
| (10MHz, 20MSPS) | $V_O$ = ±1V | +25°C | | 60 | | dBc |
| (10MHz, 20MSPS) | $V_O$ = ±0.5 | +25°C | | 72 | | dBc |
| Hold Noise[8] | | | | $400xt_H$ | | V/s rms |
| Droop Rate | | Full | | ±1 | ±8 | mV/µs |
| Hold Time[9] | | Full | | | 2 | µs |
| Feedthrough Rejection (20MHz) | | +25°C | | 85 | | dB |
| **POWER SUPPLY** | | | | | | |
| Specified Operating Voltage | | Full | ±4.50 | ±5 | ±5.50 | V |
| Positive Supply Current[10] | | Full | | 34 | 39 | mA |
| Negative Supply Current[10] | | Full | | 33 | 39 | mA |
| Total Power Dissipation | | Full | | 335 | 390 | mW |
| **TEMPERATURE RANGE** | | | | | | |
| Specification | Ambient | Full | –40 | | +85 | °C |
| Storage | | | –55 | | +150 | °C |
| Thermal Resistance, $\theta_{JA}$ | | Full | | 100 | | °C/W |

NOTE: (1) Select (Pin 10) connected to $+V_S$ for TTL threshold voltage on Pin 11. (2) Select (Pin 10) connected to $-V_S$ for ECL threshold voltage on Pin 11. (3) Output voltage on pin 11. (4) Pin 10 (Select) connected to $+V_S$. (5) Pin 10 (Select) connected to $-V_S$. (6) Slew rate is rate of change from 10% to 90% of a 2V output step. (7) Acquisition time includes hold-to-track delay switch time. (8) Hold noise is proportional to the time in the hold mode. For example, if the hold time is 25ns, the accumulated noise is 10µVrms. (9) This is the maximum length of time the SHC605 can remain in the hold mode and still maintain a linear droop rate. (10) Select (Pin 10) connected to $+V_S$.

## PIN CONFIGURATION




## PIN DESCRIPTION

| PIN # | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | +In | Non-Inverting Input |
| 2 | $+V_S$ | +5V Supply |
| 3 | $+V_S$ | +5V Supply |
| 4 | DGND | Digital Ground |
| 5 | AGND | Analog Ground |
| 6 | AGND | Analog Ground |
| 7 | AGND | Analog Ground |
| 8 | –In | Inverting Input |
| 9 | $V_{OUT}$ | Output Voltage |
| 10 | Select | +5V Selects TTL; –5V Selects ECL |
| 11 | Thresh/$\overline{\text{Hold}}$ | Logic threshold for single-ended operation or complement Hold input for differential operation |
| 12 | Hold | True Hold input |
| 13 | $\overline{\text{Lock}}$ | Complement Lock Input |
| 14 | Lock | True Lock input; Locks SHC605 in Hold-mode regardless of Hold/$\overline{\text{Hold}}$ Inputs |
| 15 | $-V_S$ | –5V Supply |
| 16 | $-V_S$ | –5V Supply |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply | ±7VDC |
| Input Voltage Range | ±5V |
| Differential Input Voltage | ±5.5V (between +In and –In inputs) |
| Storage Temperature Range | –40°C to +125°C |
| Lead Temperature (soldering, SOIC 3s) | +260°C |
| Output Short Circuit to Ground (+25°C) | Continuous to Ground |
| Junction Temperture ($T_j$) | +175°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

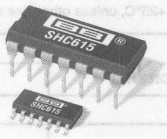
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| SHC605AU | SO-16 Surface-Mount | 265 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

BURR-BROWN®



# SHC615

www.burr-brown.com/databook/SHC615.html

# Wide-Bandwidth, DC RESTORATION CIRCUIT

## FEATURES

- PROPAGATION DELAY: 2.2ns
- BANDWIDTH: OTA: 750MHz
  Comparator: 280MHz
- LOW INPUT BIAS CURRENT: –0.3µA
- SAMPLE/HOLD SWITCHING TRANSIENTS: +1/–7mV
- SAMPLE/HOLD FEEDTHROUGH REJECTION: 100dB
- CHARGE INJECTION: 40fC
- HOLD COMMAND DELAY TIME: 3.8ns
- TTL/CMOS HOLD CONTROL

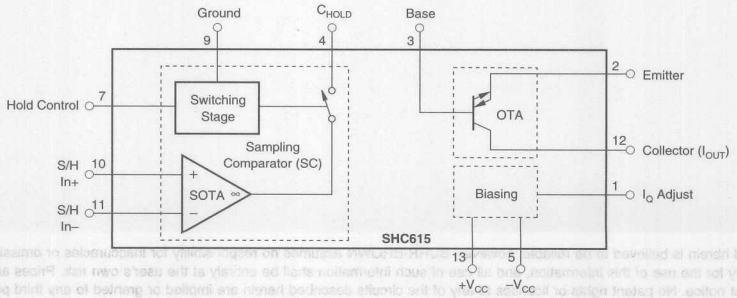
## APPLICATIONS

- BROADCAST/HDTV EQUIPMENT
- TELECOMMUNICATIONS EQUIPMENT
- HIGH-SPEED DATA ACQUISITION
- CAD MONITORS/CCD IMAGE PROCESSING
- NANO SECOND PULSE INTEGRATOR/ PEAK DETECTORS
- PULSE CODE MODULATOR/ DEMODULATOR
- COMPLETE VIDEO DC LEVEL RESTORATION
- SAMPLE/HOLD AMPLIFIER

## DESCRIPTION

The SHC615 is a complete subsystem for very fast and precise DC restoration, offset clamping, and low frequency hum suppression of wideband amplifiers or buffers. Designed to stabilize the performance of video signals, it can also be used as a sample/hold amplifier, high-speed integrator, or peak detector for nanosecond pulses. A wideband Operational Transconductance Amplifier (OTA) with a high-impedance cascode current source output and fast sampling comparator set a new standard for high-speed applications. Both can be used as stand-alone circuits or combined to form a more complex signal processing stage. The self-biased, bipolar OTA can be viewed as an ideal voltage-controlled current source and is optimized for low input bias current. The sampling comparator has two identical high-impedance inputs and a current source output optimized for low output bias current and offset voltage; it can be controlled by a TTL-compatible switching stage within a few nanoseconds. The transconductance of the OTA and sampling comparator can be adjusted by an external resistor, allowing bandwidth, quiescent current, and gain tradeoffs to be optimized.

The SHC615 is available in SO-14 surface mount and 14-pin plastic DIPs, and is specified over the extended temperature range of –40°C to +85°C.




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# DC SPECIFICATIONS

At $V_{CC}$ = ±5V, $R_{LOAD}$ = 100Ω, $R_Q$ = 300Ω, $R_{IN}$ = 150Ω and $T_A$ = +25°C, unless otherwise specified.

| PARAMETER | CONDITIONS | SHC615AP, AU | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **OFFSET VOLTAGE, $V_E$ at $V_B$ = 0** | | | | | |
| Initial | | | 8 | ±40 | mV |
| vs Temperature | | | 40 | | µV/°C |
| vs Supply (tracking) | $V_{CC}$ = ±4.5V to ±5.5V | 50 | 55 | | dB |
| **B-INPUT BIAS CURRENT** | | | | | |
| Initial | | | –0.3 | ±0.9 | µA |
| vs Temperature | | | 1 | | nA/°C |
| **C-OUTPUT BIAS CURRENT, $I_C$ at $V_B$ = 0** | | | | | |
| Initial | | –200 | –77 | +100 | µA |
| **B-INPUT IMPEDANCE** | | | 4.4 | | MΩ |
| **INPUT NOISE** | | | | | |
| Voltage Noise Density, B-to-E | $f_{OUT}$ = 100kHz to 100MHz | | 2.2 | | nV/√Hz |
| Voltage Noise Density, B-to-C | $f_{OUT}$ = 100kHz to 100MHz | | 4.5 | | nV/√Hz |
| **INPUT VOLTAGE RANGE** | | | ±3.4 | | V |
| **OUTPUT** | | | | | |
| Output Voltage Compliance | | | ±3.2 | | V |
| C-Current Output | | ±18 | ±20 | | mA |
| E-Current Output | | ±18 | ±20 | | mA |
| C-Output Impedance | | | 0.5 | | MΩ |
| E-Output Impedance | | | 12 | | Ω |
| Open-Loop Gain | | | 96 | | dB |
| **TRANSCONDUCTANCE** | Small Signal, <200mV | | 70 | | mA/V |

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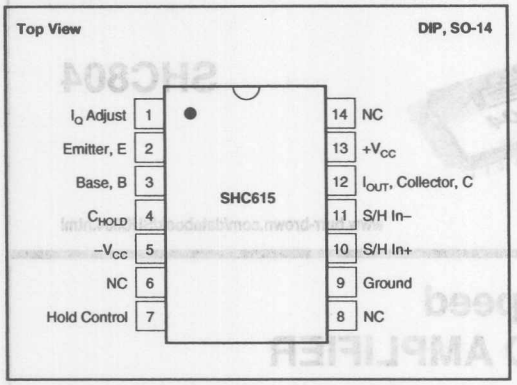
## DC SPECIFICATIONS (CONT)

At $V_{CC}$ = ±5V, $R_{LOAD}$ = 1kΩ, $R_Q$ = 300Ω, and $T_A$ = +25°C, unless otherwise specified.

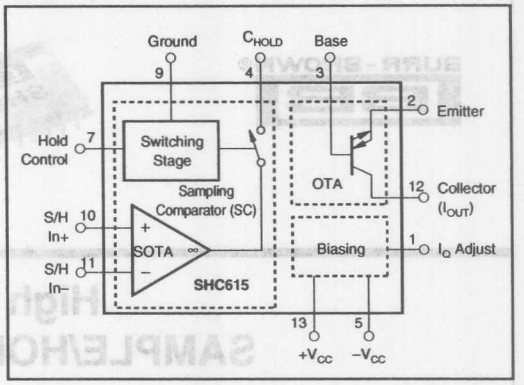
| PARAMETER | CONDITIONS | SHC615AP, AU MIN | SHC615AP, AU TYP | SHC615AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **COMPARATOR** | | | | | |
| **INPUT BIAS CURRENT** | | | | | |
| Initial | | | 1.0 | ±5 | µA |
| vs Temperature | | | –2.3 | | nA/°C |
| **C-OUTPUT BIAS CURRENT** | | | | | |
| Initial | | | ±10 | ±50 | µA |
| vs Temperature | | | ±13 | | nA/°C |
| **INPUT IMPEDANCE** | | | | | |
| Input Impedance | | | 0.2 | | MΩ |
| **INPUT NOISE** | | | | | |
| Voltage Noise Density | $f_{OUT}$ = 100kHz to 100MHz | | 5 | | nV/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | |
| Input Voltage Range | | | ±3.0 | | V |
| Common-Mode Input Range | | | ±3.2 | | V |
| **OUTPUT** | | | | | |
| Output Voltage Compliance | | | ±3.5 | | V |
| C-Current Output | | ±2.5 | ±3.2 | | mA |
| C-Output Impedance | | | 620 ll 2 | | kΩ ll pF |
| Open-Loop Gain | | | 83 | | dB |
| **TRANSCONDUCTANCE** | | | | | |
| Transconductance | | | 22 | | mA/V |
| **HOLD CONTROL** | | | | | |
| Logic 1 Voltage | | +2 | | $+V_{CC}$ +0.6 | V |
| Logic 0 Voltage | | 0 | | 0.8 | V |
| Logic 1 Current | V Hold Control = 5.0V | | 1 | | µA |
| Logic 0 Current | V Hold Control = 0.8V | | 0.05 | | µA |
| **TRANSFER CHARACTERISTICS** | | | | | |
| Charge Injection | Track-To-Hold | | 40 | | fC |
| Feedthrough Rejection | Hold Mode | | –100 | | dB |
| **COMPLETE SHC615** | | | | | |
| **POWER SUPPLY** | | | | | |
| Rated Voltage | | | ±5 | | V |
| Derated Performance | | ±4.5 | | ±5.5 | V |
| Quiescent Current | $R_Q$ = 300Ω | ±12 | ±15 | ±18 | mA |
| Quiescent Current Range | Programmable (Useful Range) | | ±3 to ±36 | | mA |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –40 | | +85 | °C |
| Storage | | –40 | | +125 | °C |

| PARAMETER | CONDITIONS | SHC615AP, AU MIN | SHC615AP, AU TYP | SHC615AP, AU MAX | UNITS |
|---|---|---|---|---|---|
| **FREQUENCY DOMAIN** | | | | | |
| **OTA** | | | | | |
| **LARGE-SIGNAL BANDWIDTH** (–3dB), (B-to-E) | $V_{OUT}$ = 5.0Vp-p | | 430 | | MHz |
| | $V_{OUT}$ = 2.8Vp-p | | 540 | | MHz |
| | $V_{OUT}$ = 1.4Vp-p | | 620 | | MHz |
| **SMALL-SIGNAL BANDWIDTH B-TO-E** | $V_{OUT}$ = 0.2Vp-p | | 520 | | MHz |
| **DIFFERENTIAL GAIN (B-TO-E)** | f = 4.43MHz, $V_{OUT}$ = 0.7Vp-p, | | | | |
| | $R_L$ = 150Ω | | 1.8 | | % |
| | $R_L$ = 500Ω | | 0.1 | | % |
| **DIFFERENTIAL PHASE** | f = 4.43MHz, $V_{OUT}$ = 0.7Vp-p, | | | | |
| | $R_L$ = 150Ω | | 0.07 | | ° |
| (B-to-E) | $R_L$ = 500Ω | | 0.01 | | ° |
| **HARMONIC DISTORTION (B-TO-E)** | f = 30MHz, $V_{OUT}$ = 1.4Vp-p | | | | |
| Second Harmonic | | | –50 | | dBc |
| Third Harmonic | | | –46 | | dBc |
| **LARGE SIGNAL BANDWIDTH** (–3dB), (B-to-C) | $V_{OUT}$ = 5.0Vp-p | | 250 | | MHz |
| | $V_{OUT}$ = 2.8Vp-p | | 580 | | MHz |
| | $V_{OUT}$ = 1.4Vp-p | | 750 | | MHz |
| **SMALL SIGNAL BANDWIDTH** B-to-C | $V_{OUT}$ = 0.2Vp-p | | 680 | | MHz |
| **COMPARATOR** | Sample Mode | | | | |
| **BANDWIDTH** (–3dB) | $I_{OUT}$ = 4mAp-p | | 240 | | MHz |
| | $I_{OUT}$ = 2mAp-p | | 270 | | MHz |
| | $I_{OUT}$ = 1mAp-p | | 280 | | MHz |
| **TIME DOMAIN** | | | | | |
| **OTA** | | | | | |
| **RISE TIME** | 2Vp-p Step, 10% to 90% | | | | |
| | B-to-E | | 1.1 | | ns |
| | B-to-C | | 1.2 | | ns |
| **SLEW RATE** | 2Vp-p, B-to-E | | 1800 | | V/µs |
| | B-to-C | | 1700 | | V/µs |
| | 5Vp-p, B-to-E | | 3300 | | V/µs |
| | B-to-C | | 3000 | | V/µs |
| **COMPARATOR** | | | | | |
| **RISE TIME** | 10% to 90%, $R_L$ = 50Ω, $I_{OUT}$ = ±2mA | | | | |
| (Sample Mode) | $C_{LOAD}$ = 1pF | | 2.5 | | ns |
| **SLEW RATE** | 10% to 90%, $R_L$ = 50Ω, $I_{OUT}$ = ±2mA | | | | |
| (Sample Mode) | $C_{LOAD}$ = 1pF | | 0.95 | | mA/ns |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Propagation Delay Time | $t_{PDH}$, $V_{OD}$ = 200mV | | 2.2 | | ns |
| Propagation Delay Time | $t_{PDL}$, $V_{OD}$ = 200mV | | 2.15 | | ns |
| Delay Time | Sample-to-Hold | | 3.8 | | ns |
| | Hold-to-Sample | | 3.0 | | ns |

## PIN CONFIGURATION




## BLOCK DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage ($\pm V_{CC}$) | ±6V |
| Input Voltage[1] | $\pm V_{CC}$ ±0.7V |
| Operating Temperature | –40°C to +85°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Hold Control | –0.5V to $+V_{CC}$ +0.7V |

NOTE: (1) Inputs are internally diode-clamped to $\pm V_{CC}$.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| SHC615AP | Plastic 14-Pin DIP | 010 | –40°C to +85°C |
| SHC615AU | SO 14-Lead Surface-Mount | 235 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

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# SHC804

www.burr-brown.com/databook/SHC804.html

# High Speed SAMPLE/HOLD AMPLIFIER

## FEATURES

- 350ns max ACQUISITION TIME
- ±0.01% THROUGHPUT NONLINEARITY
- 150ns max SAMPLE-TO-HOLD SETTLING TIME
- 24-PIN HERMETICALLY-SEALED METAL PACKAGE

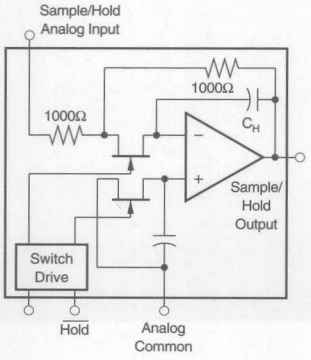
## DESCRIPTION

The SHC804 is a high speed sample/hold amplifier designed for use in fast 12-bit data acquisition systems and signal processing systems.

The SHC804 acquires a 10V signal change in less than 350ns to ±1/2LSB at 12 bits. Throughput nonlinearity error is guaranteed to be within ±1/2LSB for 12-bit systems. Stability over temperature is excellent, with only ±5ppm/°C of gain drift and ±4ppm of FSR/°C of charge offset drift over the –25 to +85°C temperature range.

The ±25ps maximum aperture uncertainty of the SHC804 permits sampling (to ±0.01% of Full Scale Range) of signals with rates of change of up to 100V/µs. This component is capable of accurately digitizing fast changing signals at sample rates as high as 500k samples per second.

The digital inputs (HOLD and $\overline{\text{HOLD}}$) are TTL-compatible. Power supply requirements are ±15V and +5V and the specification temperature range is –25°C to +85°C. The SHC804 is packaged in a 24-pin dual-in-line hermetic metal package. SHC804 is pin-compatible with other sample/holds on the market with similar performance characteristics.




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# SPECIFICATIONS

At +25°C, rated power supplies and a 1kΩ output load, unless otherwise specified.

| PARAMETER | SHC804BM MIN | SHC804BM TYP | SHC804BM MAX | SHC804CM MIN | SHC804CM TYP | SHC804CM MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **SAMPLE/HOLD INPUTS (without Input Buffer)** | | | | | | | |
| **ANALOG** | | | | | | | |
| Voltage Range | ±10.25 | ±11 | | * | * | | V |
| $R_{IN}$ | | 1.00 | | | * | | kΩ |
| **DIGITAL (HOLD, $\overline{HOLD}$)** | | | | | | | |
| $V_{IH}$ | +2.0 | | | * | | | V |
| $V_{IL}$ | | | +0.8 | | | * | V |
| $I_{IH}$, $V_{IN}$ = +2.7V | | | +60 | | | * | µA |
| $I_{IL}$, $V_{IN}$ = +0.4V | | | –1.2 | | | * | mA |
| **SAMPLE/HOLD TRANSFER CHARACTERISTICS (without Input Buffer)** | | | | | | | |
| **ACCURACY** | | | | | | | |
| Sample Mode | | | | | | | |
| Gain | | –1 | | | * | | V/V |
| Gain Error | | | ±0.1 | | | * | % |
| Temperature Coefficient | | ±3 | ±10 | | ±1 | ±5 | ppm/°C |
| Linearity Error | | ±0.001 | ±0.005 | | * | * | % of FSR(1) |
| Zero Offset | | ±1 | ±5 | | ±0.5 | ±3 | mV |
| Temperature Coefficient | | ±1 | ±2.5 | | ±0.5 | ±1.5 | ppm of FSR/°C |
| Hold Mode | | | | | | | |
| Charge Offset | | ±2 | ±10 | | ±1 | ±5 | mV |
| Temperature Coefficient | | ±3 | ±10 | | ±2 | ±4 | ppm of FSR/°C |
| Droop Rate: at +25°C | | ±0.5 | ±5 | | * | * | µV/µs |
| +85°C | | | ±0.5 | | | ±0.1 | mV/µs |
| Throughput Nonlinearity | | | ±0.01 | | | * | % of FSR |
| Power Supply Sensitivity(2): ±$V_{CC}$ | | | ±0.002 | | | * | % of FSR/%$V_{CC}$ |
| $V_{DD}$ | | | ±0.003 | | | * | % of FSR/%$V_{DD}$ |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Acquisition Time (with 10V Step) | | | | | | | |
| to within: ±0.1% (±10mV) | | 220 | | | * | | ns |
| ±0.01% (±1mV) | | 250 | 350 | | * | * | ns |
| Sample-to-Hold Settling Time | | | | | | | |
| to within ±0.01% (±1mV) | | 100 | 150 | | * | * | ns |
| Sample-to-Hold Transient Amplitude | | 60 | 150 | | * | * | $mV_{PEAK}$ |
| Aperture Delay TIme(3) | | 15 | 25 | | * | * | ns |
| Aperture Uncertainty | | ±10 | ±25 | | * | * | ps |
| Sample Mode: Output Slew Rate | | 160 | | | * | | V/µs |
| Full Power Bandwidth | | 1 | | | * | | MHz |
| Small Signal Bandwidth | | 16 | | | * | | MHz |
| Hold Mode Feedthrough Rejection | | | | | | | |
| (10V Square Wave Input) | ±0.03 | ±0.005 | | | * | | % |
| **SAMPLE/HOLD OUTPUT** | | | | | | | |
| Voltage Range | ±10.25 | ±11 | | * | * | | V |
| Output Current | ±50 | | | * | | | mA |
| Short Circuit Protection | | Indefinite to Common | | | * | | |
| Output Impedance (at DC) | | 0.01 | 0.1 | | * | * | Ω |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | |
| Rated Voltage: ±$V_{CC}$ | ±13.5 | ±15 | ±16.5 | * | * | * | V |
| $V_{DD}$ | +4.75 | +5.00 | +5.25 | * | * | * | V |
| Quiescent Current (No Load) | | | | | | | |
| SHC804: +$V_{CC}$ | | 30 | 35 | | * | * | mA |
| –$V_{CC}$ | | 15 | 20 | | * | * | mA |
| $V_{DD}$ | | 5 | 10 | | * | * | mA |
| SHC803: +$V_{CC}$ | | 33 | 40 | | * | * | mA |
| –$V_{CC}$ | | 18 | 25 | | * | * | mA |
| $V_{DD}$ | | 5 | 10 | | * | * | mA |
| Power Dissipation: SHC804 | | 700 | 875 | | * | * | mW |
| **TEMPERATURE RANGE** | | | | | | | |
| Specification | –25 | | +85 | * | | * | °C |
| Storage | –55 | | +125 | * | | * | °C |

* Specification same as SHC804BM.

NOTES: (1) FSR means Full Scale Range and is 20V for SHC804. (2) Sensitivity of offset plus charge offset. (3) With respect to HOLD. For $\overline{HOLD}$ add 5ns typical. (4) With buffer connected to the sample/hold amplifier.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Input Overvoltage | ±15V |
| $+V_{CC}$ to $V_{CC}$ COMMON | 0 to +18V |
| $-V_{CC}$ to $V_{CC}$ COMMON | 0 to –18V |
| Voltage on Digital Inputs (pins 11 and 12) | –0.5V to +7V |
| Power Dissipation | 1500mW |
| $V_{DD}$ to DCOM | –0.5V |
| Analog Output | Indefinite Short to $V_{CC}$ COM |

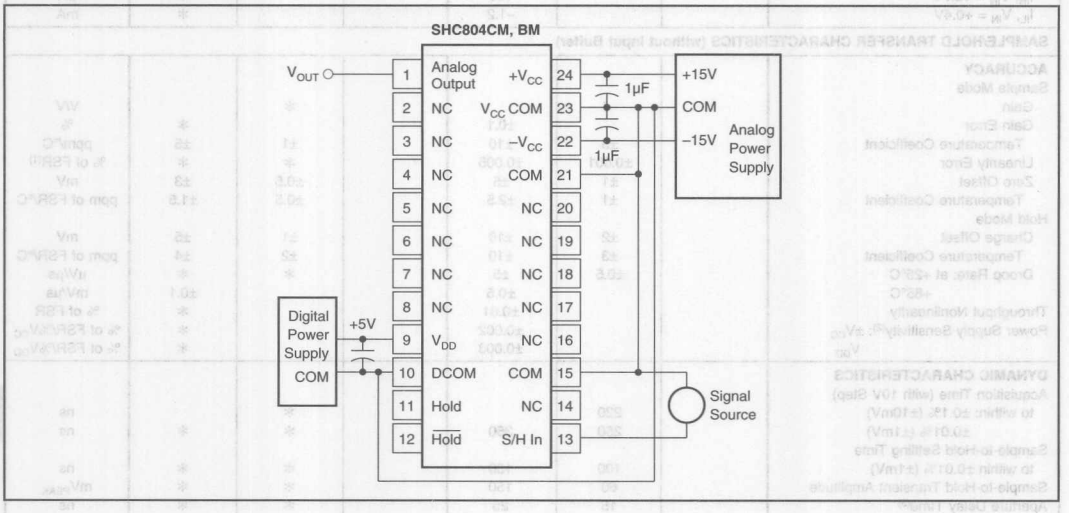
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| SHC804BM | 24-Pin | 037 |
| SHC804CM | 24-Pin | 037 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## CONNECTION DIAGRAMS




## PIN ASSIGNMENTS

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | Sample/Hold Output | Analog voltage output |
| 2 | NC | Not connected |
| 3 | NC | Not connected |
| 4 | NC | Not connected |
| 5 | NC | Not connected |
| 6 | NC | Not connected |
| 7 | NC | Not connected |
| 8 | NC | Not connected |
| 9 | $V_{DD}$ | Logic supply |
| 10 | DCOM | Logic supply common |
| 11 | HOLD | Logic "1" = HOLD |
| 12 | $\overline{HOLD}$ | Logic "0" = HOLD |
| 13 | S/H In | SHC804 input |
| 14 | NC | Not connected |
| 15 | COM | Signal common |
| 16 | NC | Not connected |
| 17 | NC | Not connected |
| 18 | NC | Not connected |
| 19 | NC | Not connected |
| 20 | NC | Not connected |
| 21 | COM | Signal common |
| 22 | $-V_{CC}$ | –15V supply |
| 23 | $V_{CC}$ COM | Analog to power common, connected to case |
| 24 | $+V_{CC}$ | +15V supply |

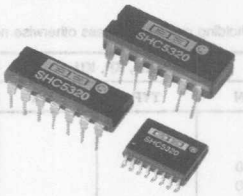
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# SHC5320

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# High-Speed Bipolar Monolithic SAMPLE/HOLD AMPLIFIER

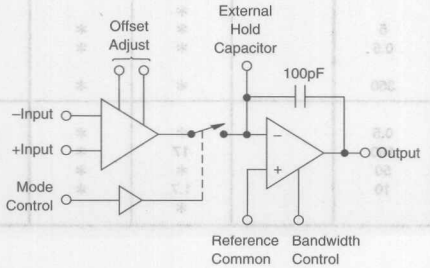


## FEATURES

- ACQUISITION TIME TO 0.01%: 1.5µs max
- HOLD MODE SETTLING TIME: 350ns max
- DROOP RATE AT +25°C: 0.5µV/µs max
- TTL COMPATIBLE
- FULL DIFFERENTIAL INPUTS
- INTERNAL HOLDING CAPACITOR
- TWO TEMPERATURE RANGES:
  –40°C to +85°C (KH, KP, KU)
  –55°C to +125°C (SH)
- PACKAGE OPTIONS: 14-pin Ceramic, Plastic DIP, and 16-pin SOIC

## APPLICATIONS

- PRECISION DATA ACQUISITION SYSTEMS
- DIGITAL-TO-ANALOG CONVERTER DEGLITCHER
- AUTO ZERO CIRCUITS
- PEAK DETECTORS




## DESCRIPTION

The SHC5320 is a bipolar monolithic sample/hold circuit designed for use in precision high-speed data acquisition applications.

The circuit employs an input transconductance amplifier capable of providing large amounts of charging current to the holding capacitor, thus enabling fast acquisition times. It also incorporates a low leakage analog switch and an output integrating amplifier with input bias current optimized to assure low droop rates. Since the analog switch always drives into a load at virtual ground, charge injection into the holding capacitor is constant over the entire input voltage range. As a result, the charge offset (pedestal voltage) resulting from this charge injection can be adjusted to zero by use of the offset adjustment capability. The device includes an internal holding capacitor to simplify ease of application; however, provision is also made to add additional external capacitance to improve the output voltage droop rate.

The SHC5320 is manufactured using a dielectric isolation process which minimizes stray capacitance (enabling higher-speed operation), and eliminates latch-up associated with substrate SCRs. The SHC5320KH, KP, and KU feature fully specified operation over the extended industrial temperature range of –40°C to +85°C, while the SHC5320SH operates over the temperature range of –55°C to +125°C. The device requires ±15V supplies for operation, and is packaged in a reliable 14-pin ceramic or plastic dual-in-line package, as well as a 16-pin surface-mount plastic package.

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## SPECIFICATIONS

### ELECTRICAL

At +25°C, rated power supplies, gain = +1, and with internal holding capacitor, unless otherwise noted.

| PARAMETERS | SHC5320KH, KP, KU | | | SHC5320SH | | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT CHARACTERISTICS** | | | | | | | |
| **ANALOG** | | | | | | | |
| Voltage Range | ±10 | | | * | | | V |
| Common-Mode Range | ±10 | | | * | | | V |
| Input Resistance | 1 | 5 | | * | * | | MΩ |
| Input Capacitance | | 3 | | | | * | pF |
| Bias Current | | ±100 | ±300 | | ±70 | ±200 | nA |
| Bias Current Over Temperature Range | | | ±300 | | | ±200 | nA |
| Offset Current | | ±30 | ±300 | | * | ±100 | nA |
| Offset Current Over Temperature Range | | | ±300 | | | ±100 | nA |
| **DIGITAL** (Over Temperature Range) | | | | | | | |
| $V_{IH}$ (Logic "1") | 2.0 | | | * | | | V |
| $V_{IL}$ (Logic "0") | | | 0.8 | | | * | V |
| $I_{IH}$ ($V_I$ = +5V) | | | 0.1 | | | * | µA |
| $I_{IL}$ ($V_I$ = 0V) | | | 4 | | | * | µA |
| Logic "0" = SAMPLE | | | | | | | |
| Logic "1" = HOLD | | | | | | | |
| **OUTPUT CHARACTERISTICS** | | | | | | | |
| Voltage Range | ±10 | | | * | | | V |
| Current | ±10 | | | * | | | mA |
| Output Impedance (Hold Mode) | | 1 | | | * | | Ω |
| Noise, DC to 10MHz: Sample Hold | | 125 | 200 | | * | * | µVrms |
| Hold Mode | | 125 | 200 | | * | * | µVrms |
| **DC ACCURACY/STABILITY** | | | | | | | |
| Gain, Open Loop, DC | $3 \times 10^5$ | $2 \times 10^6$ | | $10^6$ | * | | V/V |
| Input Offset Voltage | | ±0.5 | | | ±0.2 | | mV |
| Input Offset Voltage Over Temperature Range | | | ±1.5 | | | ±2 | mV |
| Input Offset Voltage Drift | | ±5 | ±20 | | * | ±15 | µV/°C |
| CMRR[1] | 72 | 90 | | 80 | * | | dB |
| Power Supply Rejection[2]: $+V_{CC}$ | 80 | | | * | * | | dB |
| $-V_{CC}$ | 65 | | | * | | | dB |
| **HOLD-TO-SAMPLE MODE** | | | | | | | |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Acquisition Time, A = −1, 10V Step[3]: | | | | | | | |
| to ±0.01% | | 1 | 1.5 | | * | * | µs |
| to ±0.1% | | 0.8 | 1.2 | | * | * | µs |
| **SAMPLE MODE** | | | | | | | |
| Gain-Bandwidth Product (Gain = +1)[4]: | | | | | | | |
| $C_H$ = 100pF | | 2 | | | * | * | MHz |
| $C_H$ = 1000pF | | 180 | | | * | | kHz |
| Full Power Bandwidth[5] | | 600 | | | * | | kHz |
| Slew Rate[6] | | 45 | | | * | | V/µs |
| Rise Time[4] | | 100 | | | * | | ns |
| Overshoot[4] | | 15 | | | * | | % |
| **SAMPLE-TO-HOLD MODE** | | | | | | | |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Aperture Time[7] | | 25 | | | * | | ns |
| Effective Aperture Time | −50 | −25 | 0 | * | * | * | ns |
| Aperture Uncertainty (Aperture Jitter) | | 0.3 | | | * | | ns |
| Charge Offset (Pedestal)[8] (Adjustable to Zero) | | 1 | 5 | | * | * | mV |
| Charge Transfer[8] | | 0.1 | 0.5 | | * | * | pC |
| Sample-to-Hold Transient Settling Time | | | | | | | |
| to ±0.01% of FSR | | 165 | 350 | | * | * | ns |
| **HOLD MODE** | | | | | | | |
| Droop[9] | | 0.08 | 0.5 | | * | * | µV/µs |
| Droop at Maximum Temperature[9] | | 1.2 | 100 | | 17 | * | µV/µs |
| Drift Current[9] | | 8 | 50 | | * | * | pA |
| Drift Current at Maximum Temperature[9] | | 0.12 | 10 | | 1.7 | * | nA |
| Feedthrough, 10Vp-p, 100kHz Sinewave | | 2 | | | * | | mV |

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# SPECIFICATIONS (CONT)

## ELECTRICAL

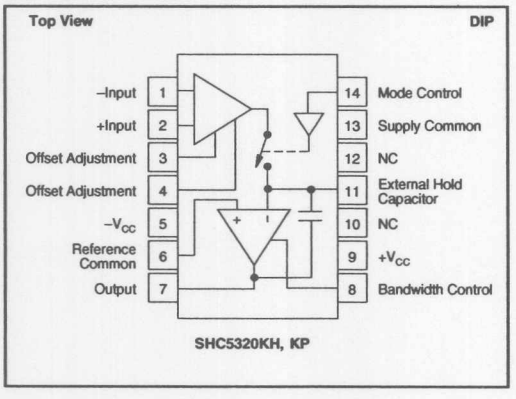
At +25°C, rated power supplies, gain = +1, and with internal holding capacitor, unless otherwise noted.

| PARAMETERS | SHC5320KH, KP, KU | | | SHC5320SH | | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | |
| **POWER SUPPLIES** | | | | | | | |
| $+V_{CC}$ | +12 | +15 | +18 | * | * | * | V |
| $-V_{CC}$ | –12 | –15 | –18 | * | * | * | V |
| $+I_{CC}$ ($+V_{CC}$ = 15V)[9] | | 11 | 13 | | * | * | mA |
| $-I_{CC}$ ($-V_{CC}$ = 15V)[9] | | –11 | –13 | | * | * | mA |
| **TEMPERATURE** | | | | | | | |
| Specification | –40 | | +85 | –55 | | +125 | °C |
| Storage | –65 | | +150 | * | | * | °C |
| **PACKAGE** | Hermetic Ceramic, Plastic DIP, SOIC | | | Hermetic Ceramic | | | |

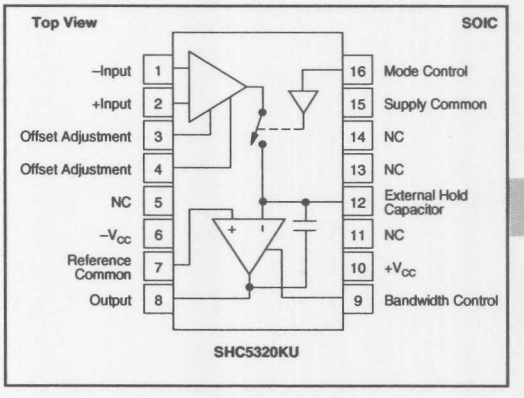
*Specification same as grade to the left.

NOTES: (1) $V_{CM}$ = ±5VDC. (2) Based on a ±0.5V swing for each supply with all other supplies held constant. (3) $V_O$ = 10V step, $R_L$ = 2kΩ, $C_L$ = 50pF. (4) $V_O$ = 200mVp-p, $R_L$ = 2kΩ, $C_L$ = 50pF. (5) $V_{IN}$ = 20Vp-p, $R_L$ = 2kΩ, $C_L$ = 50pF, unattenuated output. (6) $V_O$ = 20V step, $R_L$ = 2kΩ, $C_L$ = 50pF. (7) Simulated only, not tested. (8) $V_{IN}$ = 0V, $V_{IH}$ = +3.5V, $t_R$ <20ns ($V_{IL}$ to $V_{IH}$). (9) Specified for zero differential input voltage between pins 1 and 2. Supply current will increase with differential input (as may occur in the Hold mode) to approximately ±28mA average at 20V differential.

## PIN CONNECTIONS




SHC5320KH, KP




SHC5320KU

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Voltage Between $+V_{CC}$ and $-V_{CC}$ Terminals | 40V |
| Input Voltage | Actual Supply Voltage |
| Differential Input Voltage | ±24V |
| Digital Input Voltage | +15V, –1V |
| Output Current, continuous[2] | ±20mA |
| Internal Power Dissipation | 450mW |
| Storage Temperature Range | –65°C < $T_A$ < +150°C |
| Output Short-Circuit Duration[3] | None |
| Lead Temperature (soldering, 10s) | 300°C |

NOTES: (1) Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Absolute maximum ratings apply to both dice and package parts, unless otherwise noted. (2) Internal power dissipation may limit output current to less than +20mA. (3) **WARNING: This device cannot withstand even a momentary short circuit to either supply.**

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| SHC5320KP | 14-Pin Plastic DIP | 010 | –40°C to +125°C |
| SCH5320KU | 16-Pin SOIC | 211 | –40°C to +125°C |
| SHC5320KH | 14-Pin Cerdip | 163 | –40°C to +125°C |
| SHC5320SH | 14-Pin Cerdip | 163 | –55°C to +125°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# SPECIFICATIONS (cont)

## ELECTRICAL

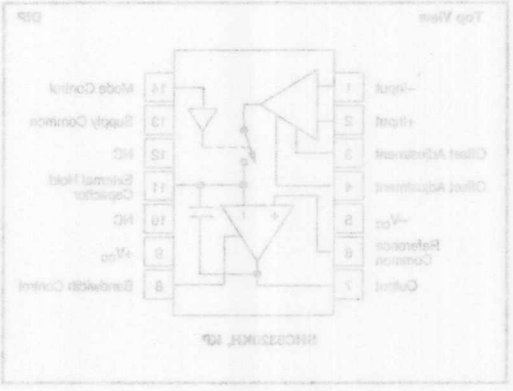
At +25°C, rated power supplies, gain = +1, and with internal holding capacitor, unless otherwise noted.

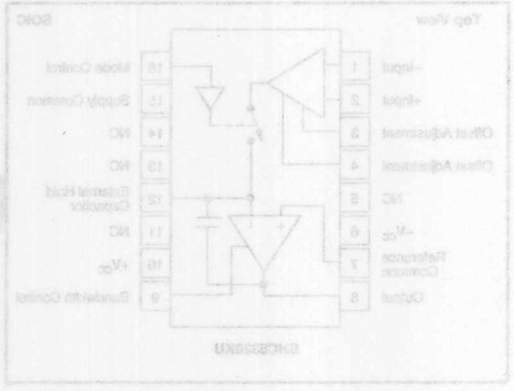
| PARAMETERS | SHC5320KH, KP, KU | | | SHC5320SH | | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | |
| POWER SUPPLIES | | | | | | | |
| $+V_{CC}$ | +12 | +15 | +18 | * | * | * | V |
| $-V_{CC}$ | –12 | –15 | –18 | * | * | * | V |
| $+I_{CC}$ ($+V_{CC}$ = 15V)[6] | | 11 | 13 | | * | * | mA |
| $-I_{CC}$ ($-V_{CC}$ = 15V)[6] | | –11 | –13 | | * | * | mA |
| TEMPERATURE | | | | | | | |
| Specification | –40 | | +85 | –55 | | +125 | °C |
| Storage | –65 | | +150 | * | | * | °C |
| PACKAGE | Hermetic Ceramic, Plastic DIP, SOIC | | | Hermetic Ceramic | | | |

Specification same as grade to the left.

NOTES: (1) $V_{CM}$ = ±10VDC. (2) Based on a ±0.5V swing for each supply with all other supplies held constant. (3) $V_O$ = 10V step, $R_L$ = 2kΩ, $C_L$ = 0.05pF. (4) $V_O$ = 20mVp-p, $R_L$ = 2kΩ, $C_L$ = 50pF. (5) $V_{IN}$ = 20Vp-p, $R_L$ = 2kΩ, $C_L$ = 50pF. unbalanced output. (6) $V_O$ = 20V step, $R_L$ = 2kΩ, $C_L$ = 50pF. (7) Simulated only, not tested. (8) $V_{IN}$ = 0V, $V_{IN}$ = +3.5V, $R_L$ <20ns ($V_L$ to $V_{HL}$). (9) Specified for zero differential input voltage between pins 1 and 2. Supply current will increase with differential input (as may occur in the Hold mode) to approximately ±25mA average at 20V differential.

## PIN CONNECTIONS




## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Voltage Between $+V_{CC}$ and $-V_{CC}$ Terminals | 40V |
| Input Voltage | Actual Supply Voltage |
| Differential Input Voltage | ±32V |
| Digital Input Voltage | +15V, –1V |
| Output Current, continuous[2] | ±25mA |
| Internal Power Dissipation | 450mW |
| Storage Temperature Range | –65°C < $T_A$ < +150°C |
| Output Short-Circuit Duration[3] | Momentary |
| Lead Temperature (soldering, 10s) | 300°C |

NOTES: (1) Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Absolute maximum ratings apply to both dice and packaged parts, unless otherwise noted. (2) Internal power dissipation may limit output current to less than ±40mA. (3) WARNING: This device cannot withstand even a momentary short circuit to ratiny supply.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[7] | TEMPERATURE RANGE |
|---|---|---|---|
| SHC5320KP | 14-Pin Plastic DIP | 010 | –40°C to +125°C |
| SHC5320KU | 16-Pin SOIC | 211 | –40°C to +125°C |
| SHC5320KH | 14-Pin Cerdip | 160 | –40°C to +125°C |
| SHC5320SH | 14-Pin Cerdip | 160 | –55°C to +125°C |

NOTE: (7) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ⚠ ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# 7 Voltage-to-Frequency Converters

Voltage-to-frequency converters provide a simple, low-cost alternative to A/D converters. The frequency output is easily isolated, transmitted or recorded. It can be interfaced to many commonly used micro-controllers and processors through counter input ports or counter/timer peripheral ICs.

The voltage-to-frequency converters' integrating input properties make them ideal for high noise industrial environments. Connected in frequency-to-voltage mode, they are useful for tachometer and rate control circuitry, motor control and telemetry.

Choose from a variety of popular devices, including:

**VFC32**—Low cost V/F converter operates up to 500kHz.

**VFC320**—Operates up to 1MHz full-scale with improved accuracy for high performance A/D conversion.

**VFC100, VFC101**—Synchronized V/F converter up to 2MHz full-scale frequency is precisely determined by your system clock frequency. Excellent for A/D conversion.

**VFC121**—Operates from a single 4.5V to 36V power supply. Full-scale output frequency up to 1.5MHz.

**VFC110**—High performance V/F converter operates to 4MHz with low frequency jitter.

Other products provide special features and performance. Use our selection guide below to locate the V/F converter for your application.

## VOLTAGE-TO-FREQUENCY CONVERTERS

**ASYNCHRONOUS**
VFC32 (Low Cost)
VFC320 (0.005% Linearity)
VFC110 (4MHz)
VFC121 (Single Supply)

**SYNCHRONIZED**
VFC100 (4MHz Clock)

**BOLD DENOTES NEW PRODUCT**
***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

## VOLTAGE-TO-FREQUENCY CONVERTERS

| Product | Frequency Range (kHz) | $V_{IN}$ Range (V) | Linearity, max (% of FSR) | Temp Range[1] | Pkg | Description |
|---|---|---|---|---|---|---|
| VFC32 | User-selected 500kHz, max | User-selected | ±0.01 at 10kHz<br>±0.05 at 100kHz | Com<br>Ind, Mil | DIP, SOIC<br>TO-100 | Low-Cost Monolithic |
| VFC100 | Clock-Programmed 2MHz max | 0 to +10 | 0.1 at 1MHz | Ind, Mil | DIP | Synchronized Monolithic |
| VFC110 | User-selected 4MHz max | 0 to +10 | ±0.05 at 1MHz | Ind | DIP | High-Performance |
| VFC121 | User-selected 1.5MHz max | User-selected | ±0.03 at 100kHz | Ind | DIP | Single Supply, Low Power |
| VFC320 | User-selected 1MHz max | User-selected | ±0.002 at 10kHz | Ind, Mil | DIP, TO-100 | Precision Monolithic |

NOTE: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C.



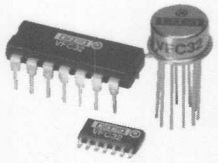
**BOLD DENOTES NEW PRODUCT**

***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

BURR-BROWN®



# VFC32

www.burr-brown.com/databook/VFC32.html

# Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

## FEATURES

- OPERATION UP TO 500kHz
- EXCELLENT LINEARITY
  ±0.01% max at 10kHz FS
  ±0.05% max at 100kHz FS
- V/F OR F/V CONVERSION
- MONOTONIC
- VOLTAGE OR CURRENT INPUT

## APPLICATIONS

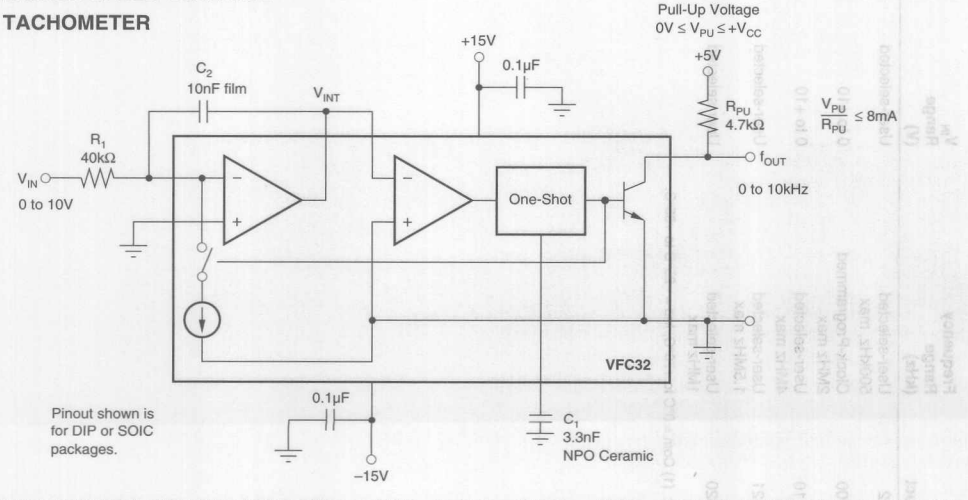
- INTEGRATING A/D CONVERTER
- SERIAL FREQUENCY OUTPUT
- ISOLATED DATA TRANSMISSION
- FM ANALOG SIGNAL MOD/DEMOD
- MOTOR SPEED CONTROL
- TACHOMETER

## DESCRIPTION

The VFC32 voltage-to-frequency converter provides an output frequency accurately proportional to its input voltage. The digital open-collector frequency output is compatible with all common logic families. Its integrating input characteristics give the VFC32 excellent noise immunity and low nonlinearity.

Full-scale output frequency is determined by an external capacitor and resistor and can be scaled over a wide range. The VFC32 can also be configured as a frequency-to-voltage converter.

The VFC32 is available in 14-pin plastic DIP, SO-14 surface-mount, and metal TO-100 packages. Commercial, industrial, and military temperature range models are available.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At $T_A$ = +25°C and $V_{CC}$ = ±15V, unless otherwise noted.

| PARAMETER | CONDITIONS | VFC32KP, KU MIN | VFC32KP, KU TYP | VFC32KP, KU MAX | VFC32BM MIN | VFC32BM TYP | VFC32BM MAX | VFC32SM MIN | VFC32SM TYP | VFC32SM MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **INPUT (V/F CONVERTER)** $F_{OUT} = V_{IN}/7.5\ R_1\ C_1$ | | | | | | | | | | | |
| Voltage Range[1] | | | | | | | | | | | |
| Positive Input | | >0 | | +0.25mA x $R_1$ | * | | * | * | | * | V |
| Negative Input | | >0 | | −10 | * | | * | * | | * | V |
| Current Range[1] | | >0 | | +0.25 | * | | * | * | | * | mA |
| Bias Current | | | | | | | | | | | |
| Inverting Input | | | 20 | 100 | | * | * | | * | * | nA |
| Noninverting Input | | | 100 | 250 | | * | * | | * | * | nA |
| Offset Voltage[2] | | | 1 | 4 | | * | * | | * | * | mV |
| Differential Impedance | | 300 II 10 | 650 II 10 | | * | * | | * | * | | kΩ II pF |
| Common-mode Impedance | | 300 II 3 | 500 II 3 | | * | * | | * | * | | MΩ II pF |
| **INPUT (F/V CONVERTER)** $V_{OUT} = 7.5\ R_1\ C_1\ F_{IN}$ | | | | | | | | | | | |
| Impedance | | 50 II 10 | 150 II 10 | | * | * | | * | * | | kΩ II pF |
| Logic "1" | | | +1.0 | | * | | * | * | | * | V |
| Logic "0" | | | −0.05 | | * | | * | * | | * | V |
| Pulse-width Range | | 0.1 | | 150k/$F_{MAX}$ | * | | * | * | | * | µs |
| **ACCURACY** | | | | | | | | | | | |
| Linearity Error[3] | 0.01Hz ≤ Oper Freq ≤ 10kHz | | ±0.005 | ±0.010[4] | | * | * | | * | * | % of FSR[5] |
| | 0.1Hz ≤ Oper Freq ≤ 100kHz | | ±0.025 | ±0.05 | | * | * | | * | * | % of FSR |
| | 0.5Hz ≤ Oper Freq ≤ 500kHz | | ±0.05 | | | * | | | * | | % of FSR |
| Offset Error Input Offset Votlage[2] | | | 1 | 4 | | * | * | | * | * | mV |
| Offset Drift[6] | | | ±3 | | | * | | | * | | ppm of FSR/°C |
| Gain Error[2] | | | 5 | | | * | | | * | | % of FSR |
| Gain Drift[6] | f = 10kHz | | ±75 | | | ±50 | ±100 | | ±70 | ±150 | ppm/°C |
| Full Scale Drift (offset drift and gain drift)[6, 7] | f = 10kHz | | ±75 | | | ±50 | ±100 | | ±70 | ±150 | ppm of FSR/°C |
| Power Supply Sensitivity | f = DC, $\pm V_{CC}$ = 12VDC to 18VDC | | | ±0.015 | | | * | | | * | % of FSR/% |
| **OUTPUT (V/F CONVERTER) (open collector output)** | | | | | | | | | | | |
| Voltage, Logic "0" | $I_{SINK}$ = 8mA | 0 | 0.2 | 0.4 | * | * | * | * | * | * | V |
| Leakage Current, Logic "1" | $V_O$ = 15V | | 0.01 | 1.0 | | * | * | | * | * | µA |
| Voltage, Logic "1" | External Pull-up Resistor Required (see Figure 4) | | | $V_{PU}$ | | | * | | | * | V |
| Pulse Width | For Best Linearity | | 0.25/$F_{MAX}$ | | | * | | | * | | s |
| Fall Time | $I_{OUT}$ = 5mA, $C_{LOAD}$ = 500pF | | | 400 | | | * | | | * | ns |
| **OUTPUT (F/V CONVERTER)** $V_{OUT}$ | | | | | | | | | | | |
| Voltage | $I_O \leq$ 7mA | 0 to +10 | | | * | | | * | | | V |
| Current | $V_O \leq$ 7VDC | +10 | | | * | | | * | | | mA |
| Impedance | Closed Loop | | | 1 | | | * | | | * | Ω |
| Capacitive Load | Without Oscillation | | | 100 | | | * | | | * | pF |
| **DYNAMIC RESPONSE** | | | | | | | | | | | |
| Full Scale Frequency | | | | 500[8] | * | | | * | | | kHz |
| Dynamic Range | | 6 | | | * | | | * | | | decades |
| Settling Time | (V/F) to Specified Linearity for a Full Scale Input Step | | [9] | | | * | | | * | | |
| Overload Recovery | < 50% Overload | | [9] | | | * | | | * | | |
| **POWER SUPPLY** | | | | | | | | | | | |
| Rated Voltage | | | ±15 | | | | | | | | V |
| Voltage Range | | ±11 | | ±20 | | | | | * | | V |
| Quiescent Current | | | ±5.5 | ±6.0 | | * | * | | * | | mA |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification | | 0 | | +70 | −25 | | +85 | −55 | | +125 | °C |
| Operating | | −25 | | +85 | −55 | | +125 | −55 | | +125 | °C |
| Storage | | −25 | | +85 | −65 | | +150 | −65 | | +150 | °C |

* Specification same as VFC32KP.

NOTES: (1) A 25% duty cycle (0.25mA input current) is recommended for best linearity. (2) Adjustable to zero. See Offset and Gain Adjustment section. (3) Linearity error is specified at any operating frequency from the straight line intersecting 90% of full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section. Above 200kHz, it is recommended all grades be operated below +85°C. (4) ±0.015% of FSR for negative inputs shown in Figure 5. Positive inputs are shown in Figure 1. (5) FSR = Full Scale Range (corresponds to full scale frequency and full scale input voltage). (6) Exclusive of external components' drift. (7) Positive drift is defined to be increasing frequency with increasing temperature. (8) For operations above 200kHz up to 500kHz, see Discussion of Specifications and Installation and Operation sections. (9) One pulse of new frequency plus 1µs.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±22V |
| Output Sink Current ($F_{OUT}$) | 50mA |
| Output Current ($V_{OUT}$) | +20mA |
| Input Voltage, –Input | ±Supply |
| Input Voltage, +Input | ±Supply |
| Comparator Input | ±Supply |
| Storage Temperature Range: | |
| VFC32BM, SM | –65°C to +150°C |
| VFC32KP, KU | –25°C to +85°C |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| VFC32KP | 14-Pin Plastic DIP | 010 | 0°C to 70°C |
| VFC32BM | TO-100 Metal | 007 | –25°C to +85°C |
| VFC32SM | TO-100 Metal | 007 | –55°C to +125°C |
| VFC32KU | SO-14 SOIC | 235 | 0°C to +70°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

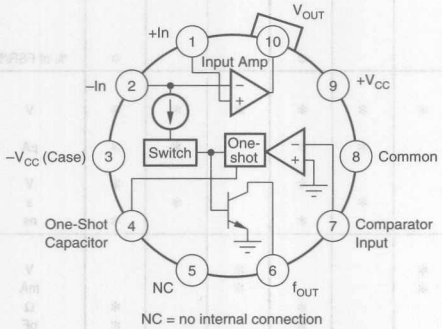
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN CONFIGURATIONS

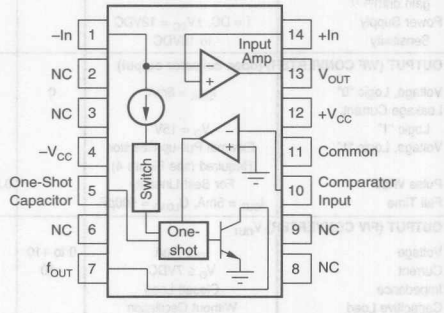
Top View

M Package
(TO-100)



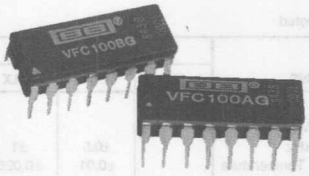

NC = no internal connection
External connection permitted.

P Package
U Package
(Epoxy Dual-in-line)




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BURR-BROWN®




# VFC100

www.burr-brown.com/databook/VFC100.html

# Synchronized VOLTAGE-TO-FREQUENCY CONVERTER

## FEATURES

- FULL-SCALE FREQUENCY SET BY SYSTEM CLOCK; NO CRITICAL EXTERNAL COMPONENTS REQUIRED
- PRECISION 10V FULL-SCALE INPUT, 0.5% max GAIN ERROR
- ACCURATE 5V REFERENCE VOLTAGE
- EXCELLENT LINEARITY:
  0.02% max at 100kHz FS
  0.1% max at 1MHz FS
- VERY LOW GAIN DRIFT: 50ppm/°C

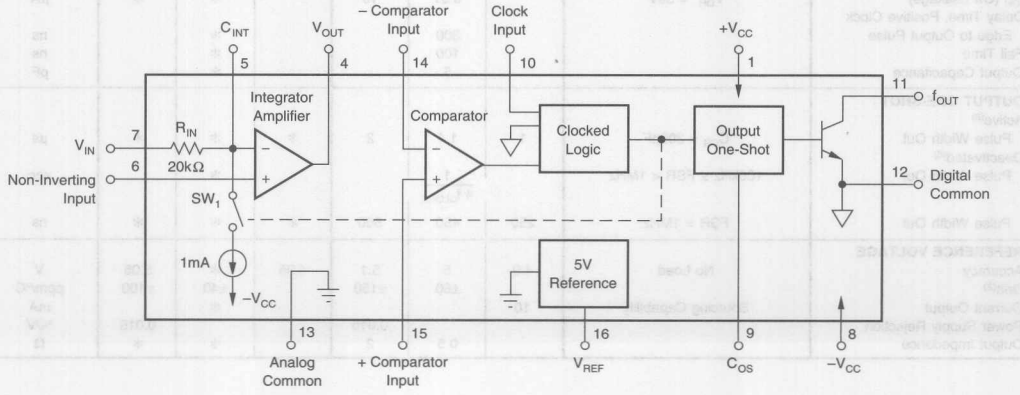
## APPLICATIONS

- A/D CONVERSION
- PROCESS CONTROL
- DATA ACQUISITION
- VOLTAGE ISOLATION

## DESCRIPTION

The VFC100 voltage-to-frequency converter is an important advance in VFCs. The well-proven charge balance technique is used; however, the critical reset integration period is derived from an external clock frequency. The external clock accurately sets an output full-scale frequency, eliminating error and drift from the external timing components required for other VFCs. A precision input resistor is provided which accurately sets a 10V full-scale input voltage. In many applications the required accuracy can be achieved without external adjustment.

The open collector active-low output provides fast fall time on the important leading edge of output pulses, and interfaces easily with TTL and CMOS circuitry. An output one-shot circuit is particularly useful to provide optimum output pulse widths for optical couplers and transformers to achieve voltage isolation. An accurate 5V reference is also provided which is useful for applications such as offsetting for bipolar input voltages, exciting bridges and sensors, and autocalibration schemes.




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# SPECIFICATIONS

At $T_A$ = +25°C and ±15VDC supplies, unless otherwise noted.

| PARAMETER | CONDITIONS | VFC100AG MIN | VFC100AG TYP | VFC100AG MAX | VFC100BG MIN | VFC100BG TYP | VFC100BG MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **TRANSFER FUNCTION** | | | | | | | | |
| **Voltage-to-Frequency Mode** | $f_{OUT} = f_{CLOCK} \times (V_{IN}/20V)$ | | | | | | | |
| Gain Error[1] | FSR = 100kHz | | ±0.5 | ±1 | | ±0.2 | ±0.5 | % of FSR[4] |
| Linearity Error | FSR = 100kHz, Over Temperature | | ±0.01 | ±0.025 | | * | ±0.02 | % of FSR |
| | FSR = 500kHz, $C_{OS}$ = 60pF | | ±0.015 | | | * | ±0.05 | % of FSR |
| | FSR = 1MHz, $C_{OS}$ = 60pF | | ±0.025 | | | * | ±0.1 | % of FSR |
| Gain Drift[2] | FSR = 100kHz | | ±70 | ±100 | | ±30 | ±50 | ppm of FSR/°C |
| Referred to Internal $V_{REF}$ | | | ±70 | ±100 | | ±30 | ±50 | ppm of FSR/°C |
| Offset Referred to Input | | | ±1 | ±3 | | ±1 | ±2 | mV |
| Offset Drift | | | ±12 | ±100 | | ±6.5 | ±25 | µV/°C |
| Power Supply Rejection | Full Supply Range | | | 0.01 | | | * | %/V |
| Response Time | To Step Input Change | One Period of New Output Frequency Plus One Clock Period | | | | | | |
| **Current-to-Frequency Mode** | $f_{OUT} = f_{CLOCK} \times (I_{IN}/1mA)$ | | | | | | | |
| Gain Error | | | ±0.5 | ±1 | | ±0.2 | ±0.5 | % of FSR |
| Gain Drift[2] | | | ±120 | ±200 | | ±80 | ±140 | ppm of FSR/°C |
| **Frequency-to-Voltage Mode[3]** | $V_{OUT} = 20V \times (f_{IN}/f_{CLOCK})$ | | | | | | | |
| Gain Accuracy[1] | FSR = 100kHz | | ±0.5 | ±1 | | ±0.2 | ±0.5 | % |
| Linearity | FSR = 100kHz | | ±0.01 | ±0.025 | | * | ±0.02 | % |
| **Input Resistor ($R_{IN}$)** | | | | | | | | |
| Resistance | | 19.8 | 20 | 20.2 | * | * | * | kΩ |
| Temperature Coefficient ($T_C$)[2] | | | ±50 | ±100 | | * | * | ppm°C |
| **INTEGRATOR OP AMP** | | | | | | | | |
| $V_{OS}$[1] | | | ±150 | ±1000 | | * | * | µV |
| $V_{OS}$ Drift | | | ±5 | | | * | | µV/°C |
| $I_B$ | | | ±50 | ±100 | | ±25 | ±50 | nA |
| $I_{OS}$ | | | 100 | 200 | | 50 | 100 | nA |
| $A_{OL}$ | $Z_{LOAD}$ = 5kΩ/10,000pF | 100 | 120 | | * | * | | dB |
| CMRR | | 80 | 105 | | * | * | | dBV |
| CM Range | | –7.5 | | +0.1 | * | | * | V |
| $V_{OUT}$ Range | $Z_{LOAD}$ = 5kΩ/10,000pF | –0.2 | | +12 | | * | * | V |
| Bandwidth | | | 14 | | | * | | MHz |
| **COMPARATOR INPUTS** | | | | | | | | |
| Input Current (Operating) | $-11V < V_{COMPARATOR} < +V_{CC} - 2V$ | | | 5 | | | * | µA |
| **CLOCK INPUT** | | | | | | | | |
| **(Referred to Digital Common)** | | | | | | | | |
| Frequency (Maximum Operating) | | | 4 | | | * | | MHz |
| Threshold Voltage | | | 1.4 | | | * | | V |
| | Over Temperature | 0.8 | | 2 | * | | * | V |
| Voltage Range (Operating) | | $-V_{CC}$ + 2V | | $+V_{CC}$ | * | | * | V |
| Input Current | $-V_{CC} < V_{CLOCK} < +V_{CC}$ | | 0.5 | 5 | | * | * | µA |
| Rise Time | | | | 2 | | | * | µs |
| **OPEN COLLECTOR OUTPUT** | | | | | | | | |
| **(Referred to Digital Common)** | | | | | | | | |
| $V_{OL}$ | $I_{OUT}$ = 10mA | | | 0.4 | | | * | V |
| $I_{OL}$ | | | | 15 | | | * | mA |
| $I_{OH}$ (Off Leakage) | $V_{OH}$ = 30V | | 0.01 | 10 | | * | * | µA |
| Delay Time, Positive Clock | | | | | | | | |
| Edge to Output Pulse | | | 300 | | | * | | ns |
| Fall Time | | | 100 | | | * | | ns |
| Output Capacitance | | | 5 | | | * | | pF |
| **OUTPUT ONE-SHOT** | | | | | | | | |
| Active[6] | | | | | | | | |
| Pulse Width Out | $C_{OS}$ = 300pF | 1 | 1.4 | 2 | * | * | * | µs |
| Deactivated[5] | | | | | | | | |
| Pulse Width Out | 100kHz ≤ FSR < 1MHz | | $\frac{1}{4 f_{CLOCK}}$ | | | * | | sec |
| Pulse Width Out | FSR = 1MHz | 250 | 450 | 500 | * | * | * | ns |
| **REFERENCE VOLTAGE** | | | | | | | | |
| Accuracy | No Load | 4.9 | 5 | 5.1 | 4.95 | * | 5.05 | V |
| Drift[2] | | | ±60 | ±150 | | ±40 | ±100 | ppm/°C |
| Current Output | Sourcing Capability | 10 | | | | * | | mA |
| Power Supply Rejection | | | | 0.015 | | | 0.015 | %/V |
| Output Impedance | | | 0.5 | 2 | | * | * | Ω |

## SPECIFICATIONS (CONT)

At $T_A$ = +25°C and ±15VDC supplies, unless otherwise noted.

| PARAMETER | CONDITIONS | VFC100AG MIN | VFC100AG TYP | VFC100AG MAX | VFC100BG MIN | VFC100BG TYP | VFC100BG MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | | |
| Rated Voltage | | | ±15 | | | * | | V |
| Operating Voltage Range | | | | | | | | |
| (See Figure 9) | $+V_{CC}$ | +7.5 | | +28.5 | * | | * | V |
| | $-V_{CC}$ | –7.5 | | –28.5 | * | | * | V |
| Total Supply | $+V_{CC} - (-V_{CC})$ | 15 | | 36 | * | | * | V |
| Digital Common | | $-V_{CC}$ + 2 | | $+V_{CC}$ – 4 | * | | * | V |
| Quiescent Current: $+I_{CC}$ | Over Temperature | | 10.6 | 15 | | * | * | mA |
| $-I_{CC}$ | | | 9.6 | 15 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –25 | | +85 | * | | * | °C |
| Storage | | –65 | | +150 | * | | * | °C |
| $\theta_{JA}$ | | | 150 | | | * | | °C/W |
| $\theta_{JC}$ | | | 100 | | | * | | °C/W |

* Specification same as AG grade.

NOTES: (1) Offset and gain error can be trimmed to zero. See text. (2) Specified by the box method: (max. – min.) ÷ (FSR x ΔT). (3) Refer to detailed timing diagram in Figure 16 for frequency input signal timing requirements. (4) FSR = Full Scale Range. (5) Pin 9 connected to $+V_{CC}$. (6) Nominal $PW_{OUT}$ = (5ns/pF) x $C_{OS}$ – 90ns.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage ($+V_{CC}$ to $-V_{CC}$) | 36V |
| $+V_{CC}$ to Analog Common | 28V |
| $-V_{CC}$ to Analog Common | 28V |
| Integrator Out Short-Circuit to Ground | Indefinite |
| Integrator Differential Input | ±10V |
| Integrator Common-Mode Input | $-V_{CC}$ +5V to +2V |
| $V_{IN}$ (pin 7) | $\pm V_{CC}$ |
| Clock Input | $\pm V_{CC}$ |
| $V_{REF}$ Out Short-Circuit to Ground | Indefinite |
| Pin 9 ($C_{OS}$) | 0 to $+V_{CC}$ |
| $f_{OUT}$ (referred to digital common) | –0.5V to 36V |
| Digital Common | $\pm V_{CC}$ |
| Storage Temperature Range | –65°C to +150°C |
| Lead Temperature (soldering, 10s) | 300°C |

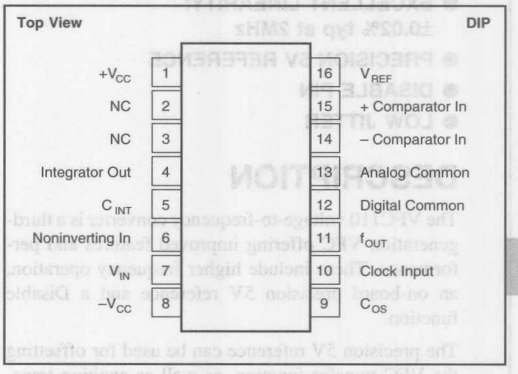
### PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| VFC100AG | 16-Pin Ceramic DIP | 129 |
| VFC100BG | 16-Pin Ceramic DIP | 129 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### PIN CONFIGURATION

Top View — DIP



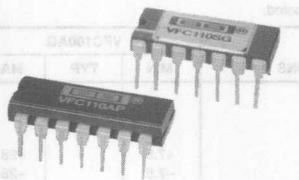

### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# VFC110

www.burr-brown.com/databook/VFC110.html

# High-Frequency VOLTAGE-TO-FREQUENCY CONVERTER

## FEATURES

- HIGH-FREQUENCY OPERATION: 4MHz FS max
- EXCELLENT LINEARITY: ±0.02% typ at 2MHz
- PRECISION 5V REFERENCE
- DISABLE PIN
- LOW JITTER

## APPLICATIONS

- INTEGRATING A/D CONVERSION
- PROCESS CONTROL
- VOLTAGE ISOLATION
- VOLTAGE-CONTROLLED OSCILLATOR
- FM TELEMETRY

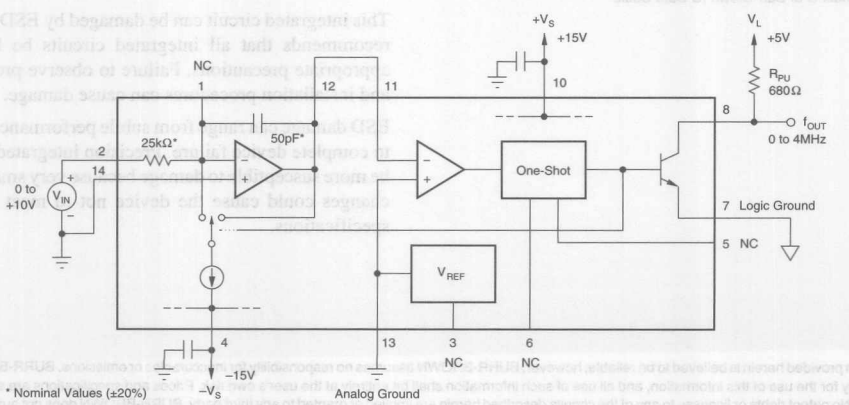
## DESCRIPTION

The VFC110 voltage-to-frequency converter is a third-generation VFC offering improved features and performance. These include higher frequency operation, an on-board precision 5V reference and a Disable function.

The precision 5V reference can be used for offsetting the VFC transfer function, as well as exciting transducers or bridges. The Enable pin allows several VFCs' outputs to be paralleled, multiplexed, or simply to shut off the VFC. The open-collector frequency output is TTL/CMOS-compatible. The output may be isolated by using an opto-coupler or transformer.

Internal input resistor, one-shot and integrator capacitors simplify applications circuits. These components are trimmed for a full-scale output frequency of 4MHz at 10V input. No additional components are required for many applications.

The VFC110 is packaged in plastic and ceramic 14-pin DIPs. Industrial and military temperature range gradeouts are available.




* Nominal Values (±20%)

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# SPECIFICATIONS

At $T_A$ = +25°C and $V_S$ = ±15V, unless otherwise noted.

| PARAMETER | CONDITIONS | VFC110BG | | | VFC110AG/SG/AP | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **VOLTAGE-TO-FREQUENCY OPERATION** | | | | | | | | |
| Nonlinearity[1]: $f_{FS}$ = 100kHz | $C_{OS}$ = 2.2nF, $R_{IN}$ = 44kΩ | | 0.005 | 0.01 | | 0.01 | 0.05 | %FS |
| $f_{FS}$ = 1MHz | $C_{OS}$ = 150pF, $R_{IN}$ = 40kΩ | | 0.01 | 0.05 | | | 0.1 | %FS |
| $f_{FS}$ = 2MHz | $C_{OS}$ = 56pF, $R_{IN}$ = 34kΩ | | 0.02 | | | * | | %FS |
| $f_{FS}$ = 4MHz | $C_{OS}$ = (Int), $R_{IN}$ = (Int) | | 1 | | | * | | %FS |
| Gain Error, f = 1MHz | $C_{OS}$ = 150pF, $R_{IN}$ = 40kΩ | | | 5 | | | * | % |
| Gain Drift, f = 1MHz | Specified Temp Range | | | 50 | | | 100 | ppm/°C |
| Relative to $V_{REF}$ | Specified Temp Range | | 50 | | | 100 | | ppm/°C |
| PSRR | $V_S$ = ±8V to ±18V | | | 0.05 | | | 0.1 | %/V |
| **INPUT** | | | | | | | | |
| Full Scale Input Current | | | 250 | 500 | | * | * | µA |
| $I_{B-}$ (Inverting Input) | | | 15 | 60 | | 20 | 100 | nA |
| $I_{B+}$ (Non-Inverting Input) | | | 250 | | | * | | nA |
| $V_{OS}$ | | | | 3 | | | 3 | mV |
| $V_{OS}$ Drift | Specified Temp Range | | 35 | | | * | | µV/°C |
| **INTEGRATOR AMPLIFIER OUTPUT** | | | | | | | | |
| Output Voltage Range | $R_L$ = 2kΩ | –0.2 | | $+V_S$ – 4 | * | | * | V |
| Output Current Drive | | 5 | 20 | | * | * | | mA |
| Capacitive Load | No Oscillations | | 10 | | | 10 | | nF |
| **COMPARATOR INPUT** | | | | | | | | |
| $I_B$ (Input Bias Current) | | | –5 | | | * | | µA |
| Trigger Voltage | | | ±50 | | | * | | mV |
| Input Voltage Range | | –5 | | $+V_S$ | * | | * | V |
| **OPEN COLLECTOR OUTPUT** | | | | | | | | |
| $V_O$ Low | | | | 0.4 | | | * | V |
| $I_{LEAKAGE}$ | | | 0.1 | 1 | | * | * | µA |
| Fall Time | | | 25 | | | * | | ns |
| Delay to Rise | | | 25 | | | * | | ns |
| Settling Time | To Specified Linearity for a Full-Scale Input Step | | One Pulse of New Frequency Plus 1µs | | | | | |
| **REFERENCE VOLTAGE** | | | | | | | | |
| Voltage | | 4.97 | 5 | 5.03 | * | * | * | V |
| Voltage Drift | | | | 20 | | | 50 | ppm/°C |
| Load Regulation | $I_O$ = 0 to 10mA | | 2 | 10 | | * | * | mV |
| PSRR | $V_S$ = ±8V to ±18V | | 5 | | | * | | mV/V |
| Current Limit | Short Circuit | 15 | 20 | | | * | | mA |
| **ENABLE INPUT** | | | | | | | | |
| $V_{HIGH}$ ($f_{OUT}$ Enabled) | Specified Temp Range | 2 | | | * | | | V |
| $V_{LOW}$ ($f_{OUT}$ Disabled) | Specified Temp Range | | | 0.4 | | | * | V |
| $I_{HIGH}$ | | | 0.1 | | | * | | µA |
| $I_{LOW}$ | | | 1 | | | * | | µA |
| **POWER SUPPLY** | | | | | | | | |
| Voltage, $\pm V_S$ | | ±8 | ±15 | ±18 | * | * | * | V |
| Current | | | 13 | 16 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified | | | | | | | | |
| AG, BG, AP | | –25 | | +85 | * | | * | °C |
| SG | | –55 | | +125 | | | | °C |
| Storage | | | | | | | | |
| AG, BG, SG | | –65 | | +150 | * | | * | °C |
| AP | | –40 | | +125 | * | | * | °C |

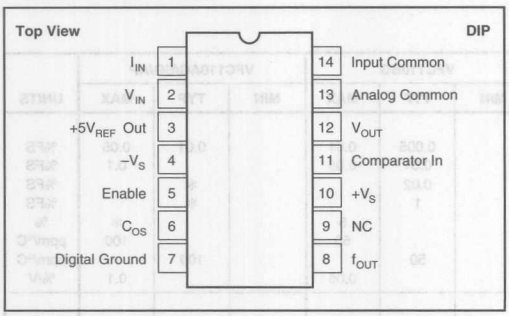
* Specification same as VFC110BG.

NOTE: (1) Nonlinearity measured from 1V to 10V input.



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## PIN CONFIGURATION




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltages ($+V_S$ to $-V_S$) | 40V |
| $f_{OUT}$ Sink Current | 50mA |
| Comparator In Voltage | $-5V$ to $+V_S$ |
| Enable Input | $+V_S$ to $-V_S$ |
| Integrator Common-Mode Voltage | $-1.5V$ to $+1.5V$ |
| Integrator Differential Input Voltage | $+0.5V$ to $-0.5V$ |
| Integrator Out (short-circuit) | Indefinite |
| $V_{REF}$ Out (short-circuit) | Indefinite |
| Operating Temperature Range | |
| G Package | –55°C to +125°C |
| P Package | –40°C to +85°C |
| Storage Temperature | |
| G Package | –60°C to +150°C |
| P Package | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| VFC110AG | 14-Pin Ceramic DIP | 169 | –25°C to +85°C |
| VFC110BG | 14-Pin Ceramic DIP | 169 | –25°C to +85°C |
| VFC110SG | 14-Pin Ceramic DIP | 169 | –55°C to +125°C |
| VFC110AP | 14-Pin Plastic DIP | 010 | –25°C to +85°C |

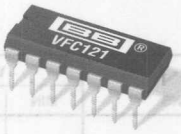
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# VFC121

www.burr-brown.com/databook/VFC121.html

# Precision Single Power Supply VOLTAGE-TO-FREQUENCY CONVERTER

## FEATURES

- SINGLE SUPPLY OPERATION: +4.5V to +36V
- $f_o$ = 1.5MHz max
- LOW NONLINEARITY: 0.03% max at 100kHz, 0.1% max at 1MHz
- HIGH INPUT IMPEDANCE
- VOLTAGE REFERENCE OUTPUT
- THERMOMETER OUTPUT: 1mV/°K

## APPLICATIONS

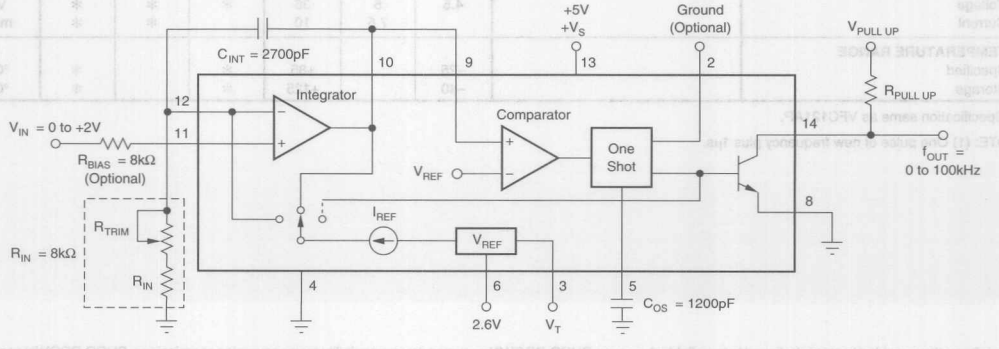
- INTEGRATING A/D CONVERSION
- ANALOG SIGNAL TRANSMISSION
- PHASE-LOCKED LOOP VCO
- GALVANICALLY ISOLATED SYSTEMS

## DESCRIPTION

The VFC121 is a monolithic voltage-to-frequency converter consisting of an integrating amplifier, voltage reference, and one-shot charge pump circuitry. High-frequency complementary NPN/PNP circuitry is used to implement the charge-balance technique, achieving speed and accuracy far superior to previous single power supply VFCs.

The high-impedance input accepts signals from ground potential to $V_S$ – 2.5V. Power supplies from 4.5V to 36V may be used. A 2.6V reference voltage output may be used to excite sensors or bias external circuitry. A thermometer output voltage proportional to absolute temperature (°K) may be used as a temperature sensor or for temperature compensation of applications circuits.

Frequency output is an open-collector transistor. A disable pin forces the output to the high impedance state, allowing multiple VFCs to share a common transmission path.



# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $V_S$ = +5V, and $R_{IN}$ = 8kΩ, unless otherwise noted.

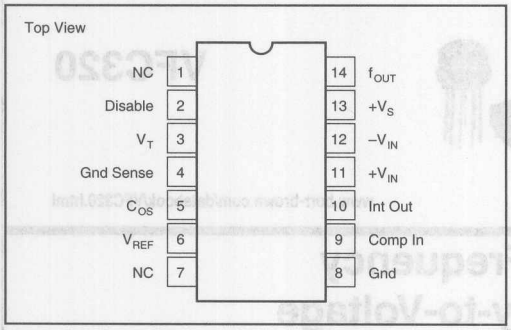
| PARAMETER | CONDITIONS | VFC121AP MIN | VFC121AP TYP | VFC121AP MAX | VFC121BP MIN | VFC121BP TYP | VFC121BP MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **ACCURACY** | | | | | | | | |
| Nonlinearity: $f_{FS}$ = 100kHz | $C_{OS}$ 1200pF, $C_{INT}$ = 2700pF | | | 0.05 | | | 0.03 | %FS |
| $f_{FS}$ = 1MHz | $C_{OS}$ 68pF, $C_{INT}$ = 270pF | | 0.1 | | | | 0.1 | %FS |
| Gain Error: $f_{FS}$ = 100kHz | $C_{OS}$ 1200pF, $C_{INT}$ = 2700pF | | | 10 | | | * | %FS |
| Gain Drift: $f_{FS}$ = 100kHz | $T_{MIN}$ to $T_{MAX}$ | | | 80 | | | 40 | ppm/°C |
| Relative to $V_{REF}$ | $+V_S$ = +5V to +36V | | | 100 | | | 40 | ppm/°C |
| PSRR | | | | 0.025 | | | * | %/V |
| **INPUT** | | | | | | | | |
| Minimum Input Voltage | | | | 0 | | | * | V |
| Maximum Input Voltage | | $V_S$ – 2.5 | $V_S$ – 2 | | * | * | | V |
| Impedance | | 10 | 100 | | * | * | | MΩ |
| $I_{BIAS}$ | | | 150 | 300 | | * | * | nA |
| $V_{OS}$ | | | 300 | 800 | | 100 | 400 | µV |
| $V_{OS}$ Drift | $T_{MIN}$ to $T_{MAX}$ | | 10 | | | * | | µV/°C |
| **OPEN COLLECTOR OUTPUT** | | | | | | | | |
| $V_{SAT}$ | $I_{PULL\ UP}$ = 10mA | | | 0.4 | | | * | V |
| $I_{LEAKAGE}$ | $V_{PULL\ UP}$ = 5V | | | 1 | | | * | µA |
| | $V_{PULL\ UP}$ = 36V | | | 10 | | | * | µA |
| Fall Time | | | | 100 | | | * | ns |
| Delay to Rise | $R_{PULL\ UP}$ = 470Ω | | | 100 | | | * | ns |
| Settling Time | To Specified Linearity for Full Scale Input Step | (1) | | | | | | |
| **REFERENCE VOLTAGE** | | | | | | | | |
| Voltage | | 2.59 | 2.6 | 2.61 | * | * | * | V |
| Voltage Drift | | | | 100 | | | 50 | ppm/°C |
| Load Regulation | $I_O$ = 0 to 10mA | | | 10 | | | * | mV |
| PSRR | $V_S$ = +5V to +36V | | | 10 | | | * | mV |
| Current Limit | | | | Short Circuit Protected | | | | |
| **INTEGRATOR AMPLIFIER OUTPUT** | | | | | | | | |
| Output Voltage Range | $R_L$ = 100kΩ | 0.8 | | 2.9 | * | | * | V |
| **COMPARATOR INPUT** | | | | | | | | |
| $I_{BIAS}$ | | | +1 | | | * | | µA |
| Trigger Voltage | | | 2.6 | | | * | | V |
| Input Voltage Range | | 0 | | 2.9 | * | | * | V |
| **THERMOMETER** | | | | | | | | |
| $V_T$ | $T_A$ = +25°C | | 298 | | | * | | mV |
| $V_T$ Slope | $T_{MIN}$ to $T_{MAX}$ | | 1 | | | * | | mV/°K |
| **DISABLE INPUT** | | | | | | | | |
| $V_{HIGH}$ (Disabled) | | 2 | | | * | | | V |
| $V_{LOW}$ | | | | 0.8 | | | * | V |
| $I_{HIGH}$ (Disabled) | $V_{HIGH}$ = 2V | | 10 | | | * | | µA |
| $I_{LOW}$ | $V_{LOW}$ = 0.8V | | 10 | | | * | | µA |
| **POWER SUPPLY** | | | | | | | | |
| Voltage | | 4.5 | 5 | 36 | * | * | * | V |
| Current | | | 7.5 | 10 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified | | –25 | | +85 | * | | * | °C |
| Storage | | –40 | | +125 | * | | * | °C |

* Specification same as VFC121AP.

NOTE: (1) One pulse of new frequency plus 1µs.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN CONFIGURATION




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage ($+V_S$) | 40V |
| $f_{OUT}$ Sink Current | 20mA |
| Comparator In Voltage | –0.5V to +3V |
| Enable Input | –0.3V to $+V_S$ |
| Integrator Common-Mode Voltage | 0V to $+V_S$ – 2V |
| Integrator Differential Input Voltage | –0.3V to +0.3V |
| $V_{REF}$ Out (short-circuit) | Indefinite |
| Operating Temperature Range | –40°C to +85°C |
| Storage Temperature | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |

Stresses above these ratings may permanently damage the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ORDERING INFORMATION

| PRODUCT | PACKAGE | LINEARITY ERROR, MAX ($f_S$ = 100kHz) | TEMPERATURE RANGE |
|---|---|---|---|
| VFC121AP | Plastic DIP | 0.05% | –25°C to +85°C |
| VFC121BP | Plastic DIP | 0.03% | –25°C to +85°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN CONFIGURATION

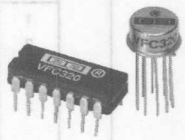
| PIN # | NAME | DESCRIPTION |
|---|---|---|
| 1 | NC | Not Connected |
| 2 | Disable | Input logic Low for normal operation. Input logic High to disable the VFC121. Has internal pull-down, for normal operation if not connected. |
| 3 | $V_T$ | Temperature compensation voltage proportional to absolute temperature. Typically 298mV at room temperature (298°K), with a change of 1mV per °C (°K). |
| 4 | Gnd Sense | Defines ground for the internal voltage reference. |
| 5 | $C_{OS}$ | One-shot capacitor is connected between here and ground to set full scale output frequency. |
| 6 | $V_{REF}$ | Output from the internal band-gap voltage reference, typically 2.6V. Can be used externally to set levels or excite sensors. |
| 7 | NC | Not Connected |
| 8 | Gnd | Ground |
| 9 | Comp In | Comparator In |
| 10 | Int Out | Integrator Out |
| 11 | $+V_{IN}$ | Non-inverting input of the integrating op amp. The input signal is applied here. |
| 12 | $-V_{IN}$ | Inverting input of the integrating op amp. $C_{INT}$ is connected between here and the integrator output (pin 10), and $R_{IN}$ is connected between here and ground. |
| 13 | $+V_S$ | Supply voltage connected here. Range is +4.5V to +36V. |
| 14 | $f_{OUT}$ | Frequency output pin. This is the output of an open-collector transistor, and an external pull-up circuit should be used to generate the appropriate logic levels. |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| VFC121AP | 14-Pin Plastic DIP | 010 |
| VFC121BP | 14-Pin Plastic DIP | 010 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR - BROWN®



# VFC320

www.burr-brown.com/databook/VFC320.html

# Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

## FEATURES

- HIGH LINEARITY, 12 to 14 bits
  ±0.005% max at 10kHz FS
  ±0.03% max at 100kHz FS
  ±0.1% typ at 1MHz FS
- V/F OR F/V CONVERSION
- 6-DECADE DYNAMIC RANGE
- 20ppm/°C max GAIN DRIFT
- OUTPUT TTL/CMOS COMPATIBLE

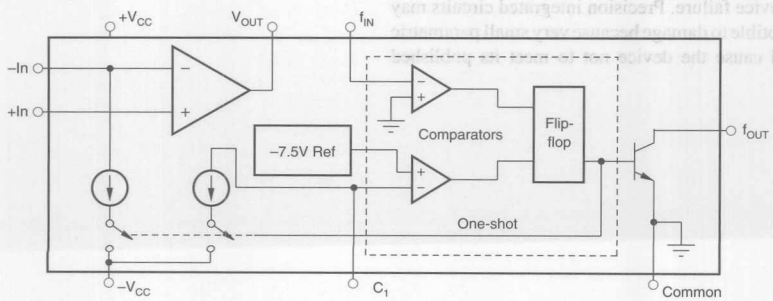
## APPLICATIONS

- INEXPENSIVE A/D AND D/A CONVERTER
- DIGITAL PANEL METERS
- TWO-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY
- FM MOD/DEMOD OF TRANSDUCER SIGNALS
- PRECISION LONG TERM INTEGRATOR
- HIGH RESOLUTION OPTICAL LINK FOR ISOLATION
- AC LINE FREQUENCY MONITOR
- MOTOR SPEED MONITOR AND CONTROL

## DESCRIPTION

The VFC320 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital output is an open collector and the digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with TTL, and CMOS logic families.

High linearity (0.005%, max at 10kHz FS) is achieved with relatively few external components. Two external resistors and two external capacitors are required to operate. Full scale frequency and input voltage are determined by a resistor in series with –In and two capacitors (one-shot timing and input amplifier integration). The other resistor is a non-critical open collector pull-up ($f_{OUT}$ to $+V_{CC}$). The VFC320 is available in three performance/temperature grades and two package configurations. The TO-100 versions are hermetically sealed, and specified for the –25°C to +85°C and –55°C to +125°C ranges, and the dual-in-line units are specified from –25°C to +85°C.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

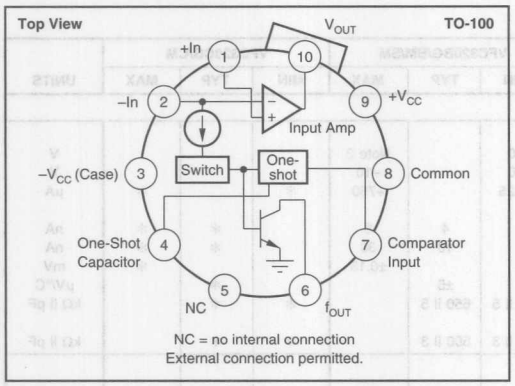
At $T_A$ = +25°C and ±15VDC power supply, unless otherwise noted.

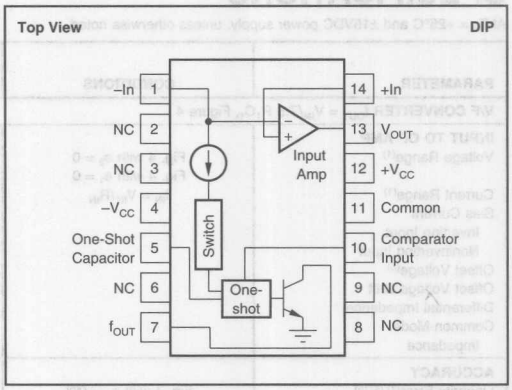
| PARAMETER | CONDITIONS | VFC320BG/BM/SM MIN | VFC320BG/BM/SM TYP | VFC320BG/BM/SM MAX | VFC320CG/CM MIN | VFC320CG/CM TYP | VFC320CG/CM MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **V/F CONVERTER** $f_{OUT} = V_{IN}/7.5\ R_1C_1$, Figure 4 | | | | | | | | |
| **INPUT TO OP AMP** | | | | | | | | |
| Voltage Range[1] | Fig. 4 with $e_2 = 0$ | >0 | | Note 2 | | | | V |
| | Fig. 4 with $e_1 = 0$ | <0 | | –10 | | | | V |
| Current Range[1] | $I_{IN} = V_{IN}/R_{IN}$ | +0.25 | | +750 | * | | * | µA |
| Bias Current | | | | | | | | |
| Inverting Input | | | 4 | 8 | | * | * | nA |
| Noninverting Input | | | 10 | 30 | | * | * | nA |
| Offset Voltage[3] | | | | ±0.15 | | | * | mV |
| Offset Voltage Drift | | | ±5 | | | * | | µV/°C |
| Differential Impedance | | 300 ll 5 | 650 ll 5 | | * | * | | kΩ ll pF |
| Common-Mode Impedance | | 300 ll 3 | 500 ll 3 | | * | * | | kΩ ll pF |
| **ACCURACY** | | | | | | | | |
| Linearity Error[1] [4] [5] | Fig. 4 with $e_2 = 0$[6] | | | | | | | |
| | 0.01Hz ≤ $f_{OUT}$ ≤ 10kHz | | ±0.004 | ±0.005 | | ±0.0015 | ±0.002 | % FSR |
| | 0.1Hz ≤ $f_{OUT}$ ≤ 100kHz | | ±0.008 | ±0.030 | | * | * | % FSR |
| | 1Hz ≤ $f_{OUT}$ ≤ 1MHz | | ±0.1 | | | * | | % FSR |
| Offset Error Input Offset Voltage[3] | | | | ±15 | | | * | ppm FSR |
| Offset Drift[7] | | | ±0.5 | | | * | | ppm FSR/°C |
| Gain Error[3] | | | ±5 | ±10 | | * | * | % FSR |
| Gain Drift[7] | f = 10kHz | | | 50 | | | 20 | ppm FSR/°C |
| Full Scale Drift (Offset Drift and Gain Drift)[7][8][9] | f = 10kHz | | | 50 | | | 20 | ppm FSR/°C |
| Power Supply Sensitivity | $\pm V_{CC}$ = 14VDC to 18VDC | | | ±0.015 | | | * | % FSR% |
| **DYNAMIC RESPONSE** | | | | | | | | |
| Full Scale Frequency | $C_{LOAD} \leq 50pF$ | | | 1 | | | * | MHz |
| Dynamic Range | | 6 | | | * | | | Decades |
| Settling Time | (V/F) to Specified Linearity For a Full Scale Input Step | | Note 10 | | | * | | |
| Overload Recovery | <50% Overload | | Note 10 | | | * | | |
| **OPEN COLLECTOR OUTPUT** | | | | | | | | |
| Voltage, Logic "0" | $I_{SINK}$ = 8mA, max | | | 0.4 | | | * | V |
| Leakage Current, Logic "1" | $V_O$ = 15V | | 0.01 | 1.0 | | * | * | µA |
| Voltage, Logic "1" | External Pull-up Resistor Required (See Figure 4) | | | $V_{PU}$ | | | * | V |
| Duty Cycle at FS | For Best Linearity | | 25 | | | * | | % |
| Fall Time | $I_{OUT}$ = 5mA, $C_{LOAD}$ = 500pF | | 100 | | | * | | ns |
| **F/V CONVERTER** $V_{OUT} = 7.5\ R_1C_1\ f_{IN}$, Figure 9 | | | | | | | | |
| **INPUT TO COMPARATOR** | | | | | | | | |
| Impedance | | 50 ll 10 | 150 ll 10 | | * | * | | kΩ ll pF |
| Logic "1" | | +1.0 | | $+V_{CC}$ | * | | * | V |
| Logic "0" | | $-V_{CC}$ | | –0.05 | * | | * | V |
| Pulse-width Range | | 0.25 | | | * | | | µs |
| **OUTPUT FROM OP AMP** | | | | | | | | |
| Voltage | $I_O$ = 6mA | 0 to +10 | | | * | | | V |
| Current | $V_O$ = 7VDC | +10 | | | * | | | mA |
| Impedance | Closed-Loop | | | 0.1 | | | * | Ω |
| Capacitive Load | Without Oscillation | | | 100 | | | * | pF |
| **POWER SUPPLY** | | | | | | | | |
| Rated Voltage | | | ±15 | | | * | | V |
| Voltage Range | | ±13 | | ±20 | * | | * | V |
| Quiescent Current | | | ±6.5 | ±7.5 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | | | | | | | |
| B and C Grades | | –25 | | +85 | * | | * | °C |
| S Grade | | –55 | | +125 | | | | °C |
| Operating | | | | | | | | |
| B and C Grades | | –40 | | +85 | * | | * | °C |
| S Grade | | –55 | | +125 | | | | °C |
| Storage | | –65 | | +150 | * | | * | °C |

* Specification the same as for VFC320BG/BM/SM.

NOTES: (1) A 25% duty cycle at full scale (0.25mA input current) is recommended where possible to achieve best linearity. (2) Determined by $R_{IN}$ and full scale current range constraints. (3) Adjustable to zero. See Offset and Gain Adjustment section. (4) Linearity error at any operating frequency is defined as the deviation from a straight line drawn between the full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section. (5) When offset and gain errors are nulled, at an operating temperature, the linearity error determines the final accuracy. (6) For $e_1$ = 0 typical linearity errors are: 0.01% at 10kHz, 0.2% at 100kHz, 0.1% at 1MHz. (7) Exclusive of external components' drift. (8) FSR = Full Scale Range (corresponds to full scale and full scale input voltage.) (9) Positive drift is defined to be increasing frequency with increasing temperature. (10) One pulse of new frequency plus 50ns typical.

## CONNECTION DIAGRAM




## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | TEMPERATURE RANGE |
|---|---|---|---|
| VFC320BG | 14-Pin Ceramic DIP | 163 | –40°C to +85°C |
| VFC320BM | TO-100 | 007 | –40°C to +85°C |
| VFC320SM | TO-100 | 007 | –40°C to +85°C |
| VFC320CG | 14-Pin Ceramic DIP | 163 | –40°C to +85°C |
| VFC320CM | TO-100 | 007 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | ±20V |
| Output Sink Current at $f_{OUT}$ | 50mA |
| Output Current at $V_{OUT}$ | +20mA |
| Input Voltage, –Input | $\pm V_{CC}$ |
| Input Voltage, +Input | $\pm V_{CC}$ |
| Storage Temperature Range | –65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# 8 Digital Audio Products

Burr-Brown pioneered the digital audio industry over a decade ago with the introduction of the world's first IC digital-to-analog converter specifically designed for audio applications. Burr-Brown continues to be a leader in this field with a complete line of D/As, A/Ds, CODEC and digital filters for all ranges of digital audio—from consumer to professional.

The selection guide on the following pages will assist in the selection of the proper component for each application—some of the newer products are:

**PCM1710**—This dual D/A offers the maximum performance (–88dB THD+N) in an economy converter for consumer applications. It is a complete converter and contains a digital filter, output low pass filters and op amps.

**PCM1716**—A complete 24-bit, 96kHz ΔΣ stereo D/A with volume control. PCM1716 is a high performance CMOS enhanced multi-level D/A with TTL input interface, 8X oversampling digital filter, 106dB dynamic range, and –96dB THD+N. Functions include digital de-emphasis, L/R independent digital attenuation, soft mute, and zero detect mute.

**PCM1717**—A complete 16- or 18-bit stereo, audio D/A converter, including digital interpolation filter, 3rd-order delta-sigma D/A, and analog output amplifiers—fabricated using a highly advanced 0.6μ CMOS process.

**PCM1718**—Another in the *SoundPlus* line, this converter accepts 18-bit normal input data format, or 16- or 18-bit I²S data format.

**PCM1720**—A complete, stereo audio D/A converter, the PCM1720 can accept 16-, 20-, or 24-bit input data in either normal or I²S formats. It can also accept standard digital audio sampling fre

**PCM1723**—Based on the PCM1720, the PCM1723 also contains a phase-locked loop (PLL) circuit. The PLL derives either 256$f_S$ or 384$f_S$ system clock from an external 27MHz frequency.

**PCM1725**—A low cost stereo audio D/A converter featuring 16 bits and 96kHz sampling. PCM1725 contains a 3rd order ΔΣ modulator, digital interpolation filter, analog output amplifier, and operates off a 256$f_S$ or 384$f_S$ system clock.

**PCM1727**—A complete stereo audio D/A converter with a dual phase-locked loop (PLL) circuit, the PCM1727 is similar to the PCM1723 but with 2 PLLs on board. PLL-1 derives a fixed 33.8688MHz system clock (SCKO-1), and PLL-2 derives both the 384$f_S$ system clock (SCKO-2) and the 768$f_S$/384$f_S$ system clock (SCKO-3) from an external 27MHz reference frequency.

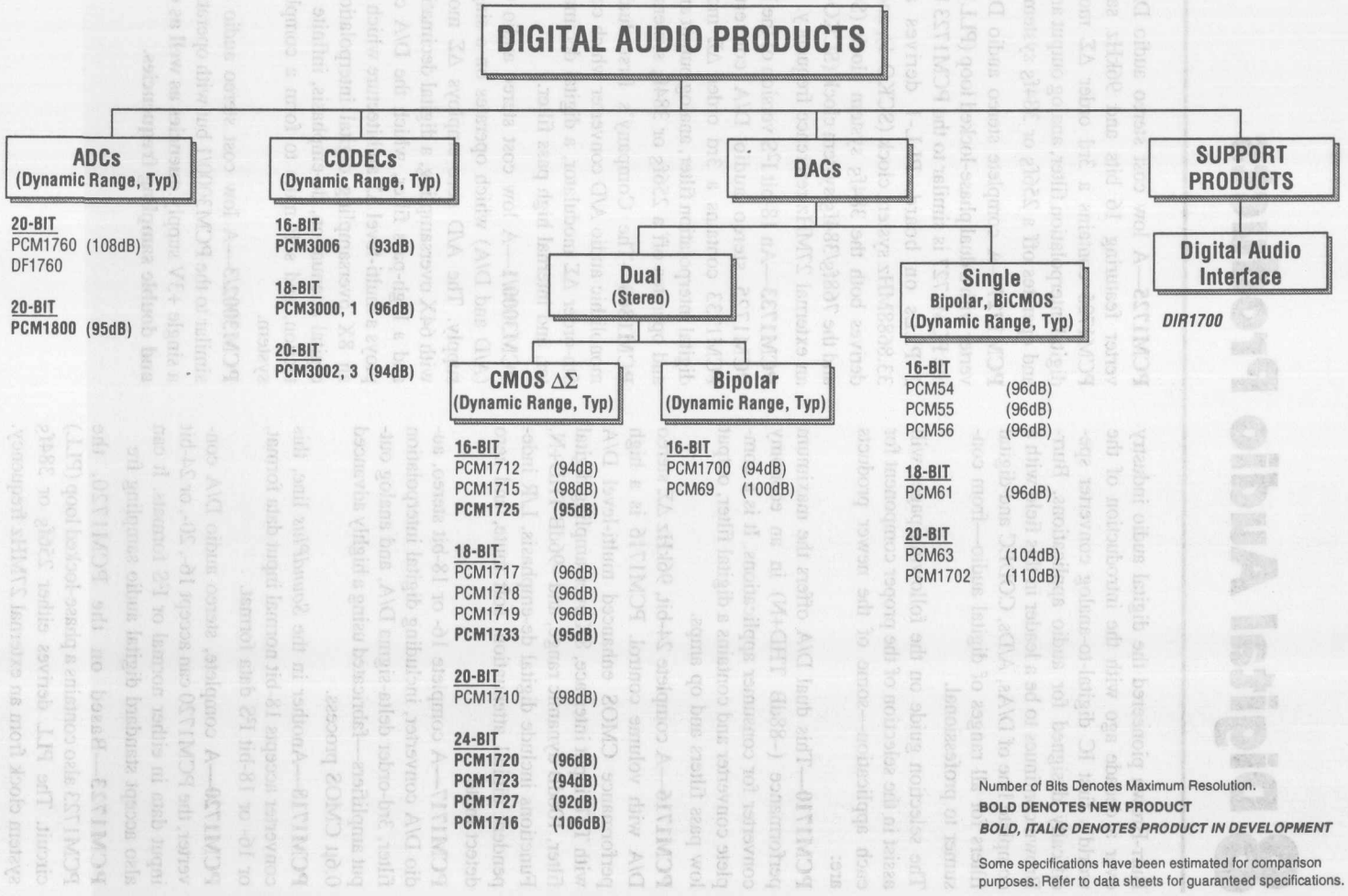
**PCM1733**—An 18-bit I²S version of the low cost PCM1725 stereo audio D/A converter, the PCM1733 contains a 3rd order ΔΣ modulator, digital interpolation filter, analog output amplifier, and operates off a 256$f_S$ or 384$f_S$ system clock.

**PCM1800**—The Company's first dual 20-bit monolithic audio A/D converter which contains a 5th-order ΔΣ modulator, a digital decimation filter, and internal high pass filter.

**PCM3000/1**—A low cost stereo audio CODEC (A/D and D/A) which operates on a single +5V supply. The A/D core employs ΔΣ modulation with 64X oversampling, a digital decimation filter and a high-pass filter, which the D/A core employs a multi-level ΔΣ architecture which includes an 8X oversampling digital interpolation filter, digital attenuation, de-emphasis, infinite zero detection, and soft mute to form a complete subsystem.

**PCM3002/3**—A low cost stereo audio CODEC similar to the PCM3000/1 but with operation from a single +3V supply.**quencies as well as one-half and double sampling frequencies.**

# Digital Audio Products




Number of Bits Denotes Maximum Resolution.
**BOLD DENOTES NEW PRODUCT**
***BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT***

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

*For Immediate Assistance, Contact Your Local Salesperson*

## AUDIO QUALITY DIGITAL-TO-ANALOG

| Product | Description | Maximum Resolution (Bits) | Maximum Sampling Rate[1] | Dynamic Range (Typ in dB) | Configuration | Audio Data Format | Power Supply | Package | Comments |
|---|---|---|---|---|---|---|---|---|---|
| PCM54 | DAC | 16 | 500kHz | 96 | Mono | Parallel | ±5 to ±15 | DDIP-28 | Bipolar, R-2R, Parallel Input |
| PCM55 | DAC | 16 | 500kHz | 96 | Mono | Parallel | ±5 | SOIC-24 | Bipolar, R-2R, Parallel Input |
| PCM56 | DAC | 16 | 800kHz | 96 | Mono | Serial Latched | ±5 to ±12 | DIP-16, SO-16 | Bipolar, R-2R |
| PCM61 | DAC | 18 | 800kHz | 96 | Mono | Serial Latched | ±5 to ±12 | DIP-16 | Bipolar, R-2R |
| PCM63 | DAC | 20 | 1MHz | 104 | Mono | Serial Latched | ±5 | DIP-28 | Bipolar, Sign-Magnitude |
| PCM69A | DAC | 18 | 1MHz | 100 | Stereo | Serial Latched | ±5 | DIP-16, SO-20 | BiCMOS, Advanced 1-Bit |
| PCM1700 | DAC | 18 | 800kHz | 94 | Stereo | Serial Latched | ±5 | DIP-28, SO-28 | Bipolar, R-2R |
| PCM1702 | DAC | 20 | 1MHz | 110 | Mono | Serial Latched | ±5 | DIP-16, SO-20 | BiCMOS, Sign-Magnitude |
| PCM1710 | DAC | 20 | 48kHz | 98 | Stereo | Normal, Continuous I²S | +5 | SO-28 | CMOS, Multi-Level ΔΣ |
| PCM1712 | DAC | 16 | 48kHz | 94 | Stereo | Normal | +5 | SO-28 | CMOS, Multi-Level ΔΣ |
| PCM1715 | DAC | 16 | 48kHz | 98 | Stereo | Normal | +5 | SO-28 | CMOS, Multi-Level ΔΣ |
| **PCM1716** | **DAC** | **24** | **96kHz** | **106** | **Stereo** | **Normal, I²S** | **+5** | **SSOP-28** | **CMOS, Multi-Level ΔΣ** |
| PCM1717 | DAC | 18 | 48kHz | 96 | Stereo | Normal, I²S | +3 to +5 | SSOP-20 | CMOS, Multi-Level ΔΣ |
| PCM1718 | DAC | 18 | 48kHz | 96 | Stereo | Normal, I²S | +3 to +5 | SSOP-20 | CMOS, Multi-Level ΔΣ |
| PCM1719 | DAC | 18 | 48kHz | 96 | Stereo | Normal, I²S | +5 | SSOP-28 | CMOS, Multi-Level ΔΣ, Headphone Amp |
| **PCM1720** | **DAC** | **24** | **96kHz** | **96** | **Stereo** | **Normal, I²S** | **+5** | **SSOP-20** | **CMOS, Multi-Level ΔΣ** |
| **PCM1723** | **DAC** | **24** | **96kHz** | **94** | **Stereo** | **Normal, I²S** | **+5** | **SSOP-24** | **CMOS, Multi-Level ΔΣ, w/ PLL** |
| **PCM1725** | **DAC** | **16** | **96kHz** | **95** | **Stereo** | **Normal, I²S** | **+5** | **SOIC-14** | **CMOS, Multi-Level ΔΣ** |
| **PCM1727** | **DAC** | **24** | **96kHz** | **92** | **Stereo** | **Normal, I²S** | **+5** | **SSOP-24** | **CMOS, Multi-Level ΔΣ, w/ Dual PLL** |
| **PCM1733** | **DAC** | **18** | **96kHz** | **95** | **Stereo** | **Normal, I²S** | **+5** | **SOIC-14** | **CMOS, Multi-Level ΔΣ** |
| PCM1760 | ADC | 20 | 48kHz | 108 | Stereo | Normal | ±5 | DIP-28, SOIC | CMOS, Multi-Level ΔΣ |
| **PCM1800** | **ADC** | **20** | **48kHz** | **95** | **Stereo** | **Normal, I²S** | **+5** | **SSOP-24** | **CMOS, Multi-Level ΔΣ** |
| **PCM3000, 1** | **CODEC** | **18** | **48kHz** | **96** | **Stereo** | **Normal, I²S** | **+5** | **SSOP-28** | **CMOS, Multi-Level ΔΣ** |
| **PCM3002, 3** | **CODEC** | **20** | **48kHz** | **94** | **Stereo** | **Normal, I²S** | **+5** | **SSOP-24** | **CMOS, Multi-Level ΔΣ** |
| **PCM3006** | **CODEC** | **16** | **48kHz** | **93** | **Stereo** | **Normal, I²S** | **+5** | **TSSOP** | **CMOS, Multi-Level ΔΣ** |

NOTE: (1) Sampling rate for R-2R type products are based on settling time.

**BOLD DENOTES NEW PRODUCT**

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Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

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# PCM78

www.burr-brown.com/databook/PCM78.html

# 16-Bit Audio ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- LOW COST/HIGH PERFORMANCE 16-BIT AUDIO A/D CONVERTER
- FAST 5µs MAX CONVERSION TIME (4µs typ)
- VERY LOW THD+N ( typ –88dB at FS; max –82dB)
- ±3V INPUT RANGE
- TWO SERIAL OUTPUT MODES PROVIDE VERSATILE INTERFACING
- COMPLETE WITH INTERNAL REFERENCE AND CLOCK IN 28-PIN PLASTIC DIP
- ±5V TO ±15V SUPPLY RANGE (600mW Power Dissipation)

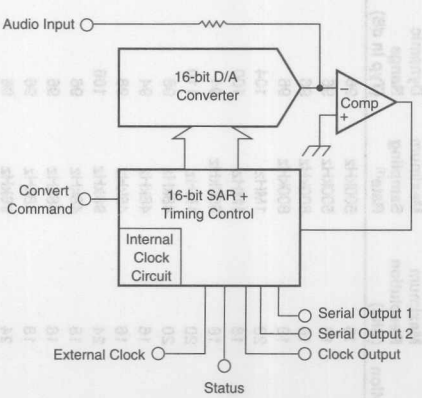
## APPLICATIONS

- DSP DATA ACQUISITION
- TEST INSTRUMENTATION
- SAMPLING KEYBOARD SYNTHESIZERS
- DIGITAL AUDIO TAPE
- BROADCAST AUDIO PROCESSING
- TELECOMMUNICATIONS

## DESCRIPTION

The PCM78P is a low-cost 16-bit analog-to-digital converter which is specifically designed and tested for dynamic applications. It features very fast, low distortion performance (4µs/–88dB THD+N typical) and is complete with internal clock and reference circuitry. The PCM78P is packaged in a reliable, low-cost 28-pin plastic DIP and data output is available in user-selectable serial output formats. The PCM78P is ideal for digital audio tape (DAT) recorders. Many similar applications such as digital signal processing and telecom applications are equally well served by the PCM78P.

The PCM78P uses a SAR technique. Analog and digital portions are efficiently partitioned into a high-speed, bipolar section and a low-power CMOS section. The PCM78P has been optimized for excellent dynamic performance and low cost.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $T_C$ = +25°C, $+V_{DD}$ = +5V, and $\pm V_{CC}$ = ±12V, and one minute warm-up in convection environment, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM78P MIN | PCM78P TYP | PCM78P MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | | 16 | Bits |
| **INPUT/OUTPUT** | | | | | |
| **ANALOG INPUT** | | | | | |
| Input Range | | –3 | | +3 | V |
| Input Impedance | | | 1.5 | | kΩ |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic Family | | | TTL Compatible CMOS | | |
| Logic Level: $V_{IH}$ | $I_{IH}$ = +40µA | +2 | | +5.5 | V |
| $V_{IL}$ | $I_{IL}$ = –100µA | 0 | | +0.8 | V |
| $V_{OH}$ | $I_{OH}$ = 2TTL Loads | +2.4 | | | V |
| $V_{OL}$ | $I_{OL}$ = 2TTL Loads | | | +0.4 | V |
| Data Format | | | Serial BOB or BTC | | |
| Convert Command | | | Negative Edge [1] | | |
| Pulse Width | | 25 | 50 | | ns |
| **CONVERSION TIME** | | | 4 | 5 | µs |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| **SIGNAL-TO-NOISE RATIO (SNR)[2]** | $f_S$ = 200kHz/$T_{CONV}$ = 4µs[3] | | | | |
| f = 1kHz (0dB) | BW = 20kHz | | 90 | | dB[4] |
| f = 10kHz (0dB) | BW = 100kHz | | 80 | | dB |
| **TOTAL HARMONIC DISTORTION[5]** | $f_S$ = 200kHz/$T_{CONV}$ = 4µs | | | | |
| f = 1kHz (0dB) | BW = 20kHz | | –91 | | dB |
| f = 19kHz (0dB) | BW = 20kHz | | –90 | | dB |
| f = 10kHz (0dB) | BW = 100kHz | | –90 | | dB |
| f = 90kHz (0dB) | BW = 100kHz | | –89 | | dB |
| **TOTAL HARMONIC DISTORTION + NOISE[6]** | $f_S$ = 200kHz/$T_{CONV}$ = 4µs | | | | |
| f = 1kHz (0dB) | BW = 20kHz | | –88 | –82 | dB |
| f = 1kHz (–20dB) | BW = 20kHz | | –74 | –68 | dB |
| f = 1kHz (–60dB) | BW = 20kHz | | –34 | | dB |
| f = 19kHz (0dB) | BW = 20kHz | | –87 | | dB |
| f = 10kHz (0dB) | BW = 100kHz | | –82 | | dB |
| f = 90kHz (0dB) | BW = 100kHz | | –81 | | dB |
| **TRANSFER CHARACTERISTICS** | | | | | |
| **ACCURACY** | | | | | |
| Gain Error | | | ±2 | | % |
| Bipolar Zero Error | | | ±20 | | mV |
| Differential Linearity Error | | | ±0.002 | | % of FSR[7] |
| Integral Linearity Error | | | ±0.003 | | % of FSR |
| Missing Codes | | | None | | 14 Bits[8] |
| **DRIFT** | | | | | |
| Gain | 0°C to +70°C | | ±25 | | ppm/°C |
| Bipolar Zero | 0°C to +70°C | | ±4 | | ppm of FSR/°C |
| **POWER SUPPLY SENSITIVITY** | | | | | |
| $+V_{CC}$ | | | ±0.008 | | %FSR/%$V_{CC}$ |
| $-V_{CC}$ | | | ±0.003 | | %FSR/%$V_{CC}$ |
| $+V_{DD}$ | | | ±0.003 | | %FSR/%$V_{DD}$ |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range: $+V_{CC}$ | | +4.75 | | +15.6 | V |
| $-V_{CC}$ | | –4.75 | | –15.6 | V |
| $+V_{DD}$ | | +4.75 | | +5.25 | V |
| Current: $+V_{CC}$ | $+V_{CC}$ = +12V | | +15 | | mA |
| $-V_{CC}$ | $-V_{CC}$ = –12V | | –21 | | mA |
| $+V_{DD}$ | $+V_{DD}$ = +5V | | +7 | | mA |
| Power Dissipation | $\pm V_{CC}$ = ±12V | | 575 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | 0 | | +70 | °C |
| Storage | | –50 | | +100 | °C |
| Operating | | –25 | | +85 | °C |

NOTES: (1) When convert command is high, converter is in a halt/reset mode. Actual conversion begins on negative edge. See detailed text on timing for convert command description when using external clock. (2) Ratio of Noise rms/Signal rms. (3) f = input frequency; $f_S$ = sample frequency (PCM78P and SHC702 in combination); BW = bandwidth of output (based on FFT or actual analog reconstruction using a 20kHz low-pass filter). (4) Referred to input signal level. (5) Ratio of Distortion rms/Signal rms. (6) Ratio of Distortion rms + Noise rms/Signal rms. (7) FSR: Full-Scale Range = 6Vp-p. (8) Typically no missing Codes at 14-bit resolution.

| | | | |
|---|---|---|---|
| 1 | Analog In | I | Analog Signal Input (1.5kΩ impedance). |
| 2 | $-V_{CC}$ | I | Analog power supply (–5V to –15V). |
| 3 | MSB Adjust | I | Internal adjustment point to allow adjustment of MSB major carry. |
| 4 | $+V_{DD}$ | I | Power connection for comparator (+5V). |
| 5 | No Connection | — | No internal connection. |
| 6 | Comparator Common | I | Comparator common connection. Connect to ground. |
| 7 | MSB | O | Parallel output of bit 1 (MSB) inverted. |
| 8 | BTC/BOB Select | I | Two's complement (open) or straight binary (grounded) data output format selection. |
| 9 | Status | O | Output signal held high until conversion is complete. |
| 10 | Clock Out | O | Internal clock output generated from RC network on pins 11 and 12 (also present when external clock is used lagging external clock by ~24ns and same duty cycle). |
| 11 | $R_1C_1$ | I | RC connection point used to generate internal clock. Sets clock high time. See text for details. |
| 12 | $R_2C_2$ | I | RC connection point used to generate internal clock. Sets clock low time. See text for details. |
| 13 | $S_{OUT2}$ | O | Internal shift register containing the previous conversion result. (Alternate latched data output mode). |
| 14 | $+V_{DD}$ | I | Power connection for +5V logic supply. |
| 15 | $S_{OUT1}$ | O | Primary real-time data output synchronized to clock out. |
| 16 | External Clock | I | External clock input point (internal clock must be disabled). |
| 17 | Int/Ext Clock Select | I | Selects either internal or external clock mode (low = internal; open = external). |
| 18 | Short Cycle | I | Terminates conversion at less than 16 bits (open for 16-bit mode). See text for details. |
| 19 | Convert Command | I | Starts conversion process (can optionally be generated internally). |
| 20 | $S_{OUT2}$ Latch | I | Latches previous conversion result for readout (must be issued with the $S_{OUT2}$ clock to initiate latch and an internal convert command). |
| 21 | $S_{OUT2}$ Clock | I | Used to read out internally latched data from previous conversion. |
| 22 | Digital Common | I | Digital grounding pin. |
| 23 | $+V_{CC}$ | I | Analog supply connection (+5V to +15V). |
| 24 | $V_{POT}$ | O | Voltage output (~2.5V) for optional adjustment of MSB transition. |
| 25 | Reference Decouple | I | Reference decoupling point. |
| 26 | Analog Common | I | Analog grounding pin. |
| 27 | Reference Out | O | 2V reference out. Should not be used except as shown in connection diagram. |
| 28 | Speed Up | I | Connection point for a capacitor to speed reference settling. See text for details. |

NOTE: Analog and digital commons are connected internally.

## INPUT/OUTPUT RELATIONSHIPS

| ANALOG INPUT | CONDITION | DIGITAL OUTPUT BTC | DIGITAL OUTPUT BOB |
|---|---|---|---|
| +2.999908V | + Full Scale | 7FFF Hex | FFFF Hex |
| –3.000000V | –Full Scale | 8000 Hex | 0000 Hex |
| 0.000000V | Bipolar Zero | 0000 Hex | 8000 Hex |
| –0.000092V | Zero-1 LSB | FFFF Hex | 7FFF Hex |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| PCM78P | 28-Pin Plastic DIP | 215 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_{CC}$ to Analog Common | 0 to +16.5V |
| $-V_{CC}$ to Analog Common | 0 to –16.5V |
| $-V_{DD}$ to Analog Common | 0 to +7V |
| Analog Common to Digital Common | ±0.5V |
| Logic Inputs to Digital Common | –0.3V to $V_{DD}$ + 0.5V |
| Analog Inputs to Analog Common | ±16.5V |
| Lead Temperature (soldering, 10s) | +300°C |

Stresses above these ratings may permanently damage the device.

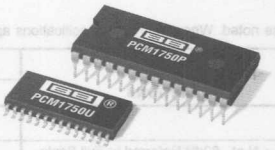
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# PCM1750P
# PCM1750U

www.burr-brown.com/databook/PCM1750.html

# Dual CMOS 18-Bit Monolithic Audio ANALOG-TO-DIGITAL CONVERTER

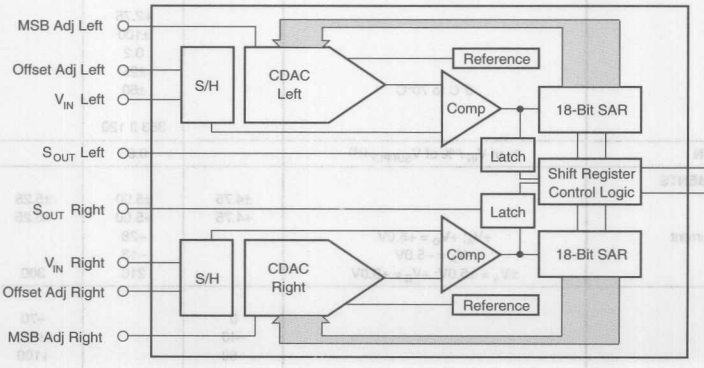
## FEATURES

- DUAL 18-BIT LOW-POWER CMOS AUDIO A/D CONVERTER
- FAST 4.5µs MIN CONVERSION TIME INCLUDING S/H
- VERY LOW MAX THD+N: –88dB Without External Adjust
- COMPLETE WITH INTERNAL REFERENCE AND DUAL S/H FUNCTION
- TWO CO-PHASE SAMPLED, ±2.75V AUDIO INPUTS
- CAPABLE OF 4X PER CHANNEL OVERSAMPLING RATE
- RUNS ON ±5V SUPPLIES AND DISSIPATES 300mW MAX
- COMPACT 28-PIN PLASTIC DIP OR SOIC

## DESCRIPTION

The PCM1750 is a low cost, dual 18-bit CMOS analog-to-digital converter optimized for dynamic signal applications. The PCM1750 features true co-phased inputs with an internal sample/hold function for each channel. The PCM1750 also comes complete with an internal reference. Total power dissipation is less than 300mW max using ±5V voltage supplies. Low maximum Total Harmonic Distortion + Noise (–88dB max) is 100% tested. The very fast PCM1750 is capable of 4 times oversampling of the audio bandwidth on both input channels simultaneously, providing greater freedom to designers in selecting input anti-aliasing filters.

PCM1750 outputs serial data in a format that is compatible with many digital filter chips and comes packaged in a space saving 28-pin plastic DIP or SOIC.




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# SPECIFICATIONS

## ELECTRICAL

At 25°C, and $\pm V_A = \pm 5.0V$; $+V_D = +5.0V$, unless otherwise noted. Where relevant, specifications apply to both left and right input/output channels.

| PARAMETER | CONDITIONS | PCM1750P, U MIN | PCM1750P, U TYP | PCM1750P, U MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | 18 | | | Bits |
| **DYNAMIC RANGE** | THD + N at –60dB Referred to Full Scale | +88 | +90 | | dB |
| **ANALOG INPUT** | | | | | |
| Input Range | | | ±2.75 | | V |
| Input Capacitance | | | 20 | | pF |
| Aperture Delay | | | 10 | | ns |
| Aperture Uncertainty (Jitter) | | | 50 | | $ps_{rms}$ |
| Full Power Input Bandwidth | | | 500 | | kHz |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic Family | | | CMOS Compatible | | |
| Logic Level: $V_{IH}$ | $I_{IH} = \pm 5\mu A$ | +3.5 | | $+V_D + 0.3$ | V |
| $V_{IL}$ | $I_{IL} = \pm 5\mu A$ | –0.3 | | +1.5 | V |
| $V_{OH}$ | $I_{SOURCE} = 1.0mA$ | +2.7 | +4.7 | | V |
| $V_{OL}$ | $I_{SINK} = 3.2mA$ | | +0.2 | +0.4 | V |
| Output Data Format | | | Serial, MSB First, BTC[1] | | |
| Convert Command | | | Positive Edge | | |
| Convert Command Pulse Width | | | 81 | | ns |
| Conversion Time | Throughput Including Sample/Hold[2] | 4.5 | 5.2 | 20.8 | µs |
| **DYNAMIC CHARACTERISTICS** (20Hz to 24kHz; 4X data decimated to 1X) | | | | | |
| Signal-to-Noise Ratio[3] | fs = 192kHz[4]; $f_{IN}$ = 1kHz (0dB)[5] | +88 | +90 | | dB[6] |
| Total Harmonic Distortion + N[7] | Without External Adjustments | | | | |
| $f_{IN}$ = 1kHz (0dB) | fs = 192kHz | | –90 | –88 | dB |
| $f_{IN}$ = 1kHz (–20dB) | fs = 192kHz | | –70 | –68 | dB |
| $f_{IN}$ = 1kHz (–60dB) | fs = 192kHz | | –30 | –28 | dB |
| Channel Separation | fs = 192kHz; $f_{IN}$ = 1kHz (0dB) and 0V | +96 | +108 | | dB |
| **ACCURACY** | | | | | |
| Gain Error | | | ±2 | ±5 | % |
| Gain Mismatch | Channel to Channel | | ±0.5 | ±2.0 | % |
| BPZ (Bipolar Zero) Error[8] | | | ±2 | | mV |
| BPZ Error Mismatch | Channel to Channel | | ±3 | | mV |
| BPZ Differential Linearity Error[9] | | | ±0.002 | | % of FSR[10] |
| Linearity Error | | | ±0.003 | | % of FSR |
| Warm-up Time | | | 1 | | ms |
| **DRIFT (With Internal Reference)** | | | | | |
| Gain | 0°C to 70°C | | ±50 | | ppm/°C |
| Bipolar Zero | 0°C to 70°C | | ±10 | | ppm of FSR/°C |
| **DRIFT (Exclusive of Internal Reference)** | | | | | |
| Gain | 0°C to 70°C | | ±10 | | ppm/°C |
| Bipolar Zero | 0°C to 70°C | | ±3 | | ppm of FSR/°C |
| **REFERENCE** | | | | | |
| $V_{REF}$ Output (Pins 19, 24): | | | | | |
| Voltage | | | +2.75 | | V |
| Current | | | ±100 | | µA |
| Impedance | | | 0.2 | | Ω |
| Accuracy | | | ±25 | | mV |
| Drift | 0°C to 70°C | | ±50 | | ppm/°C |
| $V_{REF}$ Input (Pins 18, P25): | | | | | |
| Impedance[11] | | | 363 II 120 | | Ω II pF |
| **POWER SUPPLY REJECTION** | % of $V_{IN}$ / % of $V_{SUPPLY}$ [12] | | 0.03 | | % / % |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| $\pm V_A$ Supply Voltage Range | | ±4.75 | ±5.00 | ±5.25 | V |
| $+V_D$ Supply Voltage Range | | +4.75 | +5.00 | +5.25 | V |
| $+I_A$; $+I_D$ Combined Supply Current | $+V_A$; $+V_D$ = +5.0V | | +28 | | mA |
| $-I_A$ Supply Current | $-V_A$ = –5.0V | | –13 | | mA |
| Power Dissipation | $\pm V_A = \pm 5.0V$; $+V_D$ = +5.0V | | 210 | 300 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | 0 | | +70 | °C |
| Operating | | –40 | | +85 | °C |
| Storage | | –60 | | +100 | °C |

NOTES: (1) Binary Two's Complement coding. (2) The PCM1750 is tested and guaranteed at 5.2µs, however it will operate at 4.5µs. The dynamic performance is not guaranteed or tested at this conversion rate. (3) Ratio of $Signal_{RMS}$ / ($Distortion_{RMS}$ + $Noise_{RMS}$). (4) A/D converter sample frequency (4 x 48kHz; 4X oversampling per channel). (5) A/D converter input frequency (signal level). (6) Referred to input signal level. (7) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$) / $Signal_{RMS}$. (8) Externally adjustable to zero error. (9) Differential non-linearity error at bipolar major carry input code. Externally adjustable to zero error. (10) Full scale range (5.50V). (11) Refer to equivalent circuit in Figure 1. (12) Worst case operating condition. Refer to typical performance curves.

## PIN ASSIGNMENTS

| PIN | DESCRIPTION | MNEMONIC |
|---|---|---|
| 1 | –5V Analog Supply Voltage | $-V_A$ |
| 2 | +5V Analog Supply Voltage | $+V_A$ |
| 3 | Serial Output (Left Channel) | SOUTL |
| 4 | External Clock Input | CLK |
| 5 | +5V Analog Supply Voltage | $+V_A$ |
| 6 | +5V Digital Voltage Supply | $+V_D$ |
| 7 | +5V Digital Voltage Supply | $+V_D$ |
| 8 | Digital Common Connection | DCOM |
| 9 | Analog Common Connection | ACOM |
| 10 | Digital Common Connection | DCOM |
| 11 | Convert Command Input | CONVERT |
| 12 | Serial Output (Right Channel) | SOUTR |
| 13 | +5V Analog Supply Voltage | $+V_A$ |
| 14 | –5V Analog Supply Voltage | $-V_A$ |
| 15 | Offset Adjust (Right Channel) | $OFF_{ADJR}$ |
| 16 | MSB Adjust (Right Channel) | $MSB_{ADJR}$ |
| 17 | Analog Voltage Input (Right Channel; ±2.75V) | $V_{INR}$ |
| 18 | Reference Voltage Input (Right Channel) | $VREF_{INR}$ |
| 19 | Reference Voltage Output (Right Channel) | $VREF_{OUTR}$ |
| 20 | Analog Common Connection | ACOM |
| 21 | Reference Voltage Decouple | $VREF_{CAP}$ |
| 22 | Reference Common Connection | RCOM |
| 23 | Analog Common Connection | ACOM |
| 24 | Reference Voltage Output (Left Channel) | $VREF_{OUTL}$ |
| 25 | Reference Voltage Input (Left Channel) | $VREF_{INL}$ |
| 26 | Analog Voltage Input (Left Channel; ±2.75V) | $V_{INL}$ |
| 27 | MSB Adjust (Left Channel) | $MSB_{ADJL}$ |
| 28 | Offset Adjust (Left Channel) | $OFF_{ADJL}$ |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Input Voltage ($V_{IN}$) | $-V_A$ –0.3V to $+V_A$ + 0.3V |
| $+V_A$; $+V_D$ to ACOM/DCOM | 0 to +7V |
| $-V_A$ to ACOM/DCOM | 0 to –7V |
| $-V_A$ to $+V_A$; $+V_D$ | 0 to +14V |
| ACOM to DCOM | ±1V |
| Digital Inputs (pins 4, 11) to DCOM | –0.3V to $+V_D$ + 0.3V |
| Power Dissipation | 400mW |
| Lead Temperature, (soldering 10s) | +300°C |
| Max Junction Temperature | 165°C |
| Thermal Resistance, $\theta_{JA}$: Plastic DIP | 80°C/W |
| Thermal Resistance, $\theta_{JA}$: Plastic SOIC | 100°C/W |

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

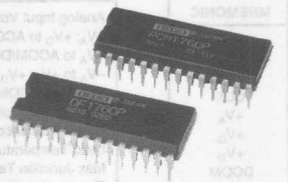
## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| PCM1750P | 28-Pin Plastic DIP | 215 |
| PCM1750U | 28-Pin Plastic SOIC | 217 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# PCM1760P/U
# DF1760P/U

**DEMO BOARD AVAILABLE**
**See Appendix A**

www.burr-brown.com/databook/PCM1760.html

# Multi-Bit Enhanced Noise Shaping 20-Bit ANALOG-TO-DIGITAL CONVERSION SYSTEM

## FEATURES

- **DUAL 20-BIT MONOLITHIC MODULATOR (PCM1760) AND MONOLITHIC DECIMATING DIGITAL FILTER (DF1760)**
- **HIGH PERFORMANCE:**
  **THD+N: –92dB typ, –90dB max**
  **Dynamic Range: 108dB typ**
  **SNR: 108dB min, 110dB typ**
  **Channel Separation: 98dB typ, 94dB min**
- **64X OVERSAMPLING**
- **CO-PHASE CONVERSION**
- **RUNS ON 256fs OR 384fs SYSTEM CLOCK**
- **VERSATILE INTERFACE CAPABILITY:**
  **16-, 20-Bit Output**
  **MSB First or LSB First Format**
- **OPTIONAL FUNCTIONS:**
  **Offset Error Calibration**
  **Overflow Detection**
  **Power Down Mode (DF1760)**
- **RUNS ON ±5V SUPPLIES (PCM1760) AND 5V SUPPLY (DF1760)**
- **COMPACT 28-PIN PACKAGES:**
  **28-Pin DIP and SOIC**

## DESCRIPTION

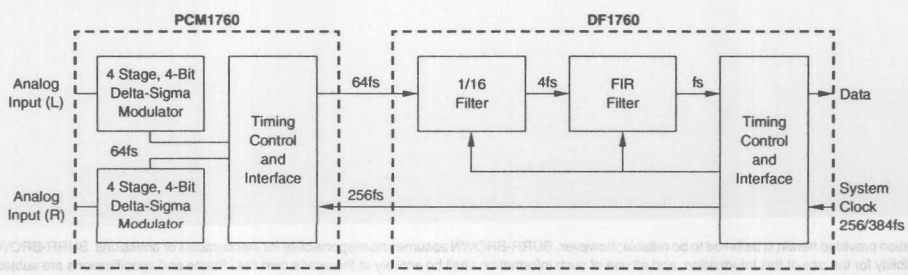
The PCM1760 and DF1760 combine for a low-cost, high-performance dual 20-bit, 48kHz sampling analog-to-digital conversion system which is specifically designed for dynamic applications.

The PCM1760/DF1760 pair form a 4-bit, 4th order, 64X oversampling analog-to-digital converter.

The PCM1760 is a delta-sigma modulator that uses a 4-bit quantizer within the modulation loop to achieve very high dynamic range.

The DF1760 is a high-performance decimating digital filter. The DF1760 accepts 4-bit 64fs data from the PCM1760 and decimates to 20-bit 1fs data.

The FIR filter of the DF1760 has pass-band ripple of less than ±0.001dB and greater than 100dB of the reject band attenuation.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $\pm V_{CC}$, $\pm V_{dd}$ = +5V, $+V_{DD}$ = +5V, $f_s$ = 48kHz and ext. components = ±2%, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1760/DF1760 MIN | PCM1760/DF1760 TYP | PCM1760/DF1760 MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | 20 | | | Bits |
| **ANALOG INPUT** | | | | | |
| Input Range | $R_{IN}1$ = 2.2kΩ | | ±2.5 | | Vp-p |
| Input Impedance | $R_{IN}1$ = 2.2kΩ | | $R_{IN}1$ | | Ω |
| **SAMPLING FREQUENCY** | | | | | |
| Cover Range of fs | Integrator Constants: Application(1) | 30 | 48 | 50 | kHz |
| **ACCURACY** | | | | | |
| Gain Error | | | ±0.5 | ±1.0 | dB |
| Gain Mismatch | | | | ±0.5 | dB |
| Bipolar Zero Error | $V_{IN}$ = 0 at 20s After Power-On | | | ±0.4 | % FSR(2) |
| Gain Drift | 0°C to +70°C | | ±100 | | ppmfs/°C |
| Bipolar Zero Drift | 0°C to +70°C | | ±20 | | ppmfs/°C |
| **DYNAMIC CHARACTERISTICS(4)** | | | | | |
| THD+N/(0dBFS) P, U | $f_{IN}$ = 1kHz | | –92 | –90 | dB |
| P-L, U-L | | | –90 | –88 | dB |
| THD+N/(–20dBFS) P, U | $f_{IN}$ = 1kHz | | –76 | –70 | dB |
| P-L, U-L | | | –76 | –70 | dB |
| THD+N/(–60dBFS) P, U | $f_{IN}$ = 1kHz | | –44 | –42 | dB |
| P-L, U-L | | | –44 | –42 | dB |
| Dynamic Range P, U | $f_{IN}$ = 1kHz, $V_{IN}$ = –60dBFS, A Filter | 104 | 108 | | dB |
| P-L, U-L | | 104 | 108 | | dB |
| SNR P, U | $V_{IN}$ = 0, A Filter | 108 | 110 | | dB |
| P-L, U-L | | 106 | 110 | | dB |
| Frequency Response | $f_{IN}$ = 20kHz | | ±0.1 | | dB |
| Channel Separation | $f_{IN}$ = 1kHz, A Filter | 94 | 98 | | dB |
| **DIGITAL FILTER** | | | | | |
| Over Sample Rate | | | 64 | | fs |
| Ripple in Band | 0 - 0.04535fs | | | ±0.0001 | dB |
| Stopband Attenuation –1 | 0.5465fs - 63.4535fs | –94 | | | dB |
| Stopband Attenuation –2 | 0.5465fs - 3.4535fs | –100 | | | dB |
| **LOGIC INPUTS AND OUTPUTS** | | | | | |
| Logic Family Input | | | TTL Level Compatible CMOS | | |
| Frequency (System Clock 1) | 256fs | | 12.288 | | MHz |
| Frequency (System Clock 2) | 384fs | | 18.432 | | MHz |
| Duty Cycle (System Clock 1) | 256fs | 40 | 50 | 60 | % |
| Duty Cycle (System Clock 2) | 384fs | 45 | 50 | 55 | % |
| Data Clock Input | | 32 | 48 | 64 | fs |
| Logic Family Output | | | CMOS | | |
| Data Clock Output | | | 64 | | fs |
| Data Coding | | | Two's Complement | | |
| Data Bit Length | | 16 | 20 | | Bits |
| Data Format | | | Selectable | | |
| Output Data Delay | fs = 48kHz | | 1.5 | | ms |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Supply Voltage | | | | | |
| $\pm V_{CC}$ | PCM1760 | ±4.75 | ±5.0 | ±5.25 | V |
| $\pm V_{dd}$ | PCM1760 | ±4.75 | ±5.0 | ±5.25 | V |
| $+V_{DD}$ | DF1760 | 4.75 | 5.0 | 5.25 | V |
| Supply Current | | | | | |
| $+I_{CC}$ | PCM1760 | | 24 | 36 | mA |
| $-I_{CC}$ | PCM1760 | | –30 | –45 | mA |
| $+I_{dd}$ | PCM1760 | | 12 | 18 | mA |
| $-I_{DD}$ | PCM1760 | | –8 | –12 | mA |
| $+I_{DD}$ –1 | DF1760, Normal Mode | | 40 | 55 | mA |
| $+I_{DD}$ –2 | DF1760, Power-Down Mode | | 4 | 6.6 | mA |
| Power Consumption | PCM1760 | | 370 | 500 | mW |
| | DF1760, Normal Mode | | 200 | 275 | mW |
| | DF1760, Power-Down Mode | | 20 | 33 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Operating | PCM1760/DF1760 | 0 | +25 | +70 | °C |
| Storage | PCM1760/DF1760 | –50 | | +125 | °C |

NOTES: (1) Integrator Constants are determined by the external components shown in the block diagram. (2) FSR means Full Scale Range, digital output code is from 90000H to 70000H, FSR = 5.0V. (3) Use 20-bit DAC, 20kHz LPF, 400Hz HPF, average response. (4) Average response using a 20-bit reconstruction DAC with 20kHz low-pass filter and 400Hz high-pass filter.

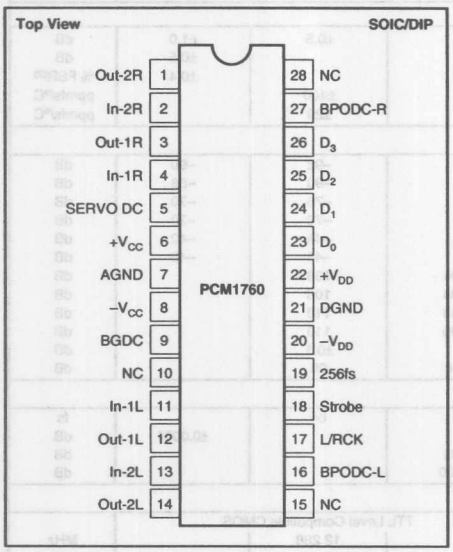
## ABSOLUTE MAXIMUM RATINGS—PCM1760

| | |
|---|---|
| Supply Voltage | ±6V |
| Voltage Mismatch | 0.1V |
| Analog Input | $\pm V_{CC}$ |
| Digital Input | $+V_{DD}$ +0.3V |
| | GND –0.3V |
| Power Dissipation/P | 580mW |
| Power Dissipation/U | 550mW |
| Lead Temperature/P (soldering, 10s) | 260°C |
| Lead Temperature/U (soldering, 10s) | 235°C |
| Operating Temperature | 0°C to +70°C |
| Storage Temperature | –50°C to +125°C |

## ABSOLUTE MAXIMUM RATINGS—DF1760

| | |
|---|---|
| Supply Voltage | 7.0V |
| Voltage Mismatch | 0.1V |
| Digital Input | $+V_{DD}$ +0.5V |
| | $V_{SS}$ –0.5V |
| Input Current | ±20mA |
| Power Dissipation/P | 460mW |
| Power Dissipation/U | 440mW |
| Lead Temperature/P (soldering, 10s) | 260°C |
| Lead Temperature/U (soldering, 10s, reflow) | 235°C |
| Operating Temperature | 0°C to +70°c |
| Storage Temperature | –50°C to +125°C |

## PIN CONFIGURATION—PCM1760




## PIN ASSIGNMENTS—PCM1760

| PIN | I/O[1] | NAME | DESCRIPTION |
|---|---|---|---|
| 1 | O | Out-2R | Right Channel Second Integrator Output |
| 2 | I | In-2R | Right Channel Second Integrator Input |
| 3 | O | Out-1R | Right Channel First Integrator Output |
| 4 | I | In-1R | Right Channel First Integrator Input |
| 5 | – | SERVO DC | Servo Amp Decoupling Capacitor |
| 6 | – | $+V_{CC}$ | +5V Analog Supply Voltage |
| 7 | – | AGND | Analog Common |
| 8 | – | $-V_{CC}$ | –5V Analog Supply Voltage |
| 9 | – | BGDC | Band Gap Reference Decoupling Capacitor |
| 10 | – | NC | No Connection |
| 11 | I | In-1L | Left Channel First Integrator Input |
| 12 | O | Out-1L | Left Channel First Integrator Output |
| 13 | I | In-2L | Left Channel Second Integrator Input |
| 14 | O | Out-2L | Left Channel Second Integrator Output |
| 15 | – | NC | No Connection |
| 16 | – | BPODC-L | Left Channel Bipolar Offset Decoupling Capacitor |
| 17 | O | L/RCK | LR Clock Output (64fs) |
| 18 | O | Strobe | Data Strobe Output (128fs) |
| 19 | I | 256fs | 256fs Clock Input |
| 20 | – | $-V_{DD}$ | –5V Digital Supply Voltage |
| 21 | – | DGND | Digital Common |
| 22 | – | $+V_{DD}$ | +5V Digital Supply Voltage |
| 23 | O | $D_0$ | $D_0$ Data Output (LSB) |
| 24 | O | $D_1$ | $D_1$ Data Output |
| 25 | O | $D_2$ | $D_2$ Data Output |
| 26 | O | $D_3$ | $D_3$ Data Output (MSB) |
| 27 | – | BPODC-R | Right Channel Bipolar Offset Decoupling Capacitor |
| 28 | – | NC | No Connection |

NOTE: (1) O = Output terminal; I = Input terminal.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| PCM1760P | 28-Pin PDIP | 215 |
| PCM1760U | 28-Pin SOIC | 217 |
| PCM1760P-L | 28-Pin PDIP | 215 |
| PCM1760U-L | 28-Pin SOIC | 217 |
| DF1760P | 28-Pin PDIP | 215 |
| DF1760U | 28-Pin SOIC | 341 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

| PRODUCT | PACKAGE | THD +N (fs) | SNR |
|---|---|---|---|
| PCM1760P | PDIP | –90dB | 108dB |
| PCM1760U | SOIC | –90dB | 108dB |
| PCM1760P-L | PDIP | –88dB | 106dB |
| PCM1760U-L | SOIC | –88dB | 106dB |
| DF1760P | PDIP | NA | NA |
| DF1760U | SOIC | NA | NA |

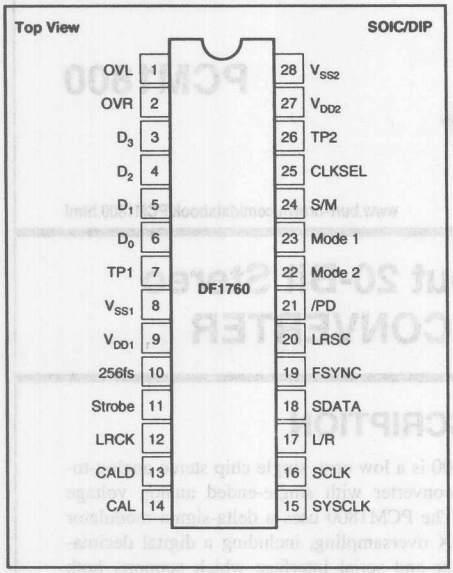
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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## PIN CONFIGURATION—DF1760

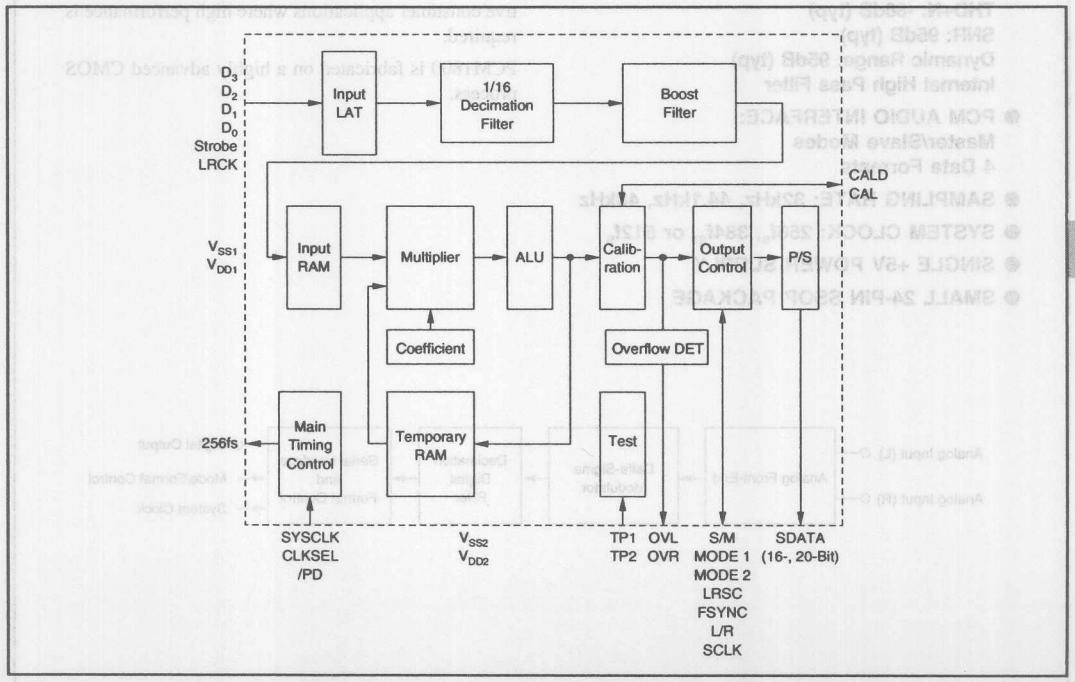



## PIN ASSIGNMENTS—DF1760

| PIN | I/O(1) | NAME | DESCRIPTION |
|---|---|---|---|
| 1 | O | OVL | Left Channel Overflow Output (Active High) |
| 2 | O | OVR | Right Channel Overflow Output (Active High) |
| 3 | I | $D_3$ | D3 Data Input (MSB) |
| 4 | I | $D_2$ | D2 Data Input |
| 5 | I | $D_1$ | D1 Data Input |
| 6 | I | $D_0$ | D0 Data Input (LSB) |
| 7 | – | TP1 | Test Pin (No Connection) |
| 8 | – | $V_{SS1}$ | Common Channel 1 |
| 9 | – | $V_{DD1}$ | +5V Channel 1 |
| 10 | O | 256fs | 256fs Clock Output |
| 11 | I | Strobe | Data Strobe Clock Input (128fs) |
| 12 | I | LRCK | LR Clock Input |
| 13 | I↑ | CALD | Calibration Function Enable (Active Low) |
| 14 | O | CAL | Calibration Output (High During Calibration) |
| 15 | I | SYSCLK | System Clock Input (256fs or 384fs) |
| 16 | I↑/O | SCLK | Data Clock |
| 17 | I↑/O | L/R | LR Channel Phase Clock |
| 18 | O | SDATA | Serial Data Output (1fs) |
| 19 | I↑/O | FSYNC | Frame Clock (2fs) |
| 20 | I↑ | LRSC | Phase Control of LR Channel Phase Clock |
| 21 | I↑ | /PD | Power Down Mode Enable Input (Active Low) |
| 22 | I↑ | Mode2 | Output Format Selection Input 2 |
| 23 | I↑ | Mode1 | Output Format Selection Input 1 |
| 24 | I↑ | S/M | Slave/Master Mode Selection Input (High Makes Slave Mode |
| 25 | I↑ | CLKSEL | System Clock Selection Input (High Makes 256fs) |
| 26 | – | TP2 | Test Pin (No Connection) |
| 27 | – | $V_{DD2}$ | +5V Channel 2 |
| 28 | – | $V_{SS2}$ | Common Channel 2 |

NOTE: (1) O = Output terminal; I = Input terminal.

## BLOCK DIAGRAM OF DF1760



BURR-BROWN®




# PCM1800

www.burr-brown.com/databook/PCM1800.html

# Single-Ended Analog Input 20-Bit Stereo ANALOG-TO-DIGITAL CONVERTER

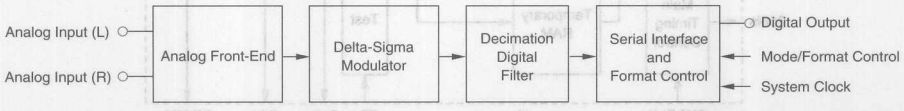
## FEATURES

- DUAL 20-BIT MONOLITHIC ΔΣ ADC
- SINGLE-ENDED VOLTAGE INPUT
- 64X OVERSAMPLING DECIMATION FILTER:
  Passband Ripple: ±0.05dB
  Stopband Attenuation: –65dB
- HIGH PERFORMANCE:
  THD+N: -88dB (typ)
  SNR: 95dB (typ)
  Dynamic Range: 95dB (typ)
  Internal High Pass Filter
- PCM AUDIO INTERFACE:
  Master/Slave Modes
  4 Data Formats
- SAMPLING RATE: 32kHz, 44.1kHz, 48kHz
- SYSTEM CLOCK: $256f_S$, $384f_S$, or $512f_S$
- SINGLE +5V POWER SUPPLY
- SMALL 24-PIN SSOP PACKAGE

## DESCRIPTION

PCM1800 is a low cost, single chip stereo analog-to-digital converter with single-ended analog voltage inputs. The PCM1800 uses a delta-sigma modulator with 64X oversampling, including a digital decimation filter and serial interface which supports both Master and Slave Modes and four data formats. PCM1800 is suitable for a wide variety of cost-sensitive consumer applications where high performance is required.

PCM1800 is fabricated on a highly advanced CMOS process.




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# SPECIFICATIONS

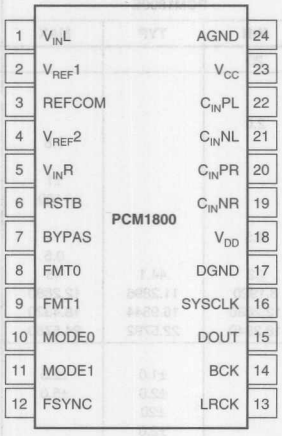
All specifications at +25°C, $+V_{DD} = +V_{CC} = +5V$, $f_S = 44.1kHz$, and 20-bit input data, SYSCLK = $384f_S$, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1800E MIN | PCM1800E TYP | PCM1800E MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | 20 | | | Bits |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Input Logic Level: | | | | | |
| $V_{IH}$(1) | | 2.0 | | | V |
| $V_{IL}$(1) | | | | 0.8 | V |
| Input Logic Current: | | | | | |
| $I_{IN}$(2) | | | | ±1 | µA |
| $I_{IN}$(3) | | | | +100 | µA |
| Output Logic Level: | | | | | |
| $V_{OH}$(4) | $I_{OH} = -1.6mA$ | 4.5 | | | V |
| $V_{OL}$(4) | $I_{OL} = +3.2mA$ | | | 0.5 | V |
| Sampling Frequency | | 32 | 44.1 | 48 | kHz |
| System Clock Frequency | $256f_S$ | 8.1920 | 11.2896 | 12.2880 | MHz |
| | $384f_S$ | 12.2880 | 16.9344 | 18.4320 | MHz |
| | $512f_S$ | 16.3840 | 22.5792 | 24.5760 | MHz |
| **DC ACCURACY** | | | | | |
| Gain Mismatch Channel-to-Channel | | | ±1.0 | ±2.5 | % of FSR |
| Gain Error | | | ±2.0 | ±5.0 | % of FSR |
| Gain Drift | | | ±20 | | ppm of FSR/°C |
| Bipolar Zero Error | High Pass Filter Bypass | | ±2.0 | | % of FSR |
| Bipolar Zero Drift | High Pass Filter Bypass | | ±20 | | ppm of FSR/°C |
| **DYNAMIC PERFORMANCE**(5) | | | | | |
| THD+N at FS (–0.5dB) | | | –88 | –80 | dB |
| THD+N at –60dB | | | –92 | | dB |
| Dynamic Range | EIAJ, A-weighted | 90 | 95 | | dB |
| Signal-To-Noise Ratio | EIAJ, A-weighted | 90 | 95 | | dB |
| Channel Separation | | 88 | 93 | | dB |
| **DYNAMIC PERFORMANCE**(5) | | | | | |
| Dynamic Range | 16-Bit, A-weighted | | 94 | | dB |
| Signal-To-Noise Ratio | 16-Bit, A-weighted | | 94 | | dB |
| Channel Separation | 16-Bit | | 92 | | dB |
| **ANALOG OUTPUT** | | | | | |
| Input Range | FS ($V_{IN}$ = 0dB) | | 2.828 | | Vp-p |
| Center Voltage | | | 2.1 | | V |
| Input Impedance | | | 30 | | kΩ |
| Anti-Aliasing Filter Frequency Response | $C_{EXT}$ = 470pF, –3dB | | 170 | | kHz |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Passband | | | | $0.454f_S$ | Hz |
| Stopband | | $0.583f_S$ | | | Hz |
| Passband Ripple | | | | ±0.05 | dB |
| Stopband Attenuation | | –65 | | | dB |
| Delay Time (Latency) | | | $17.4/f_S$ | | sec |
| High Pass Frequency Response | –3dB | | | $0.019f_S$ | mHz |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range | $+V_{CC}$ | +4.5 | +5.0 | +5.5 | VDC |
| | $+V_{DD}$ | +4.5 | +5.0 | +5.5 | VDC |
| Supply Current(6) | $+V_{CC} = +V_{DD} = +5V$ | | 18 | 25 | mA |
| Power Dissipation | $+V_{CC} = +V_{DD} = +5V$ | | 90 | 125 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Operation | | –25 | | +85 | °C |
| Storage | | –55 | | +125 | °C |
| Thermal Resistance, $\theta_{JA}$ | | | 100 | | °C/W |

NOTES: (1) Pins 6, 7, 8, 9, 10, 11, 16 and 12, 13, 14: RSTB, BYPAS, FMT0, FMT1, MODE0, MODE1, SYSCLK, and FSYNC, LRCK, BCK under Slave Mode. (2) Pins 16 and 12, 13, 14: SYSCLK and FSYNC, LRCK, BCK under Slave Mode (Schmitt Trigger input). (3) Pins 6, 7, 8, 9, 10, 11: RSTB, BYPAS, FMT0, FMT1, MODE0, MODE1 (Schmitt Trigger input, with 100kΩ typical pull-down resistor). (4) Pins 15 and 12, 13, 14: DOUT and FSYNC, LRCK, BCK under Master Mode. (5) $f_{IN}$ = 1kHz, using Audio Precisions System II, rms Mode with 20kHz LPF and 400Hz HPF in calculation. (6) No load on DOUT (pin 15) in the Slave Mode.

## PIN CONFIGURATION

Top View SSOP




## PIN ASSIGNMENTS

| PIN | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $V_{IN}L$ | IN | Analog Input, Lch |
| 2 | $V_{REF}1$ | — | Reference 1 Decoupling Capacitor |
| 3 | REFCOM | — | Reference Decoupling Common |
| 4 | $V_{REF}2$ | — | Reference 2 Decoupling Capacitor |
| 5 | $V_{IN}R$ | IN | Input Reference, Rch |
| 6 | RSTB | IN | Reset Input, Active LOW(1) |
| 7 | BYPAS | IN | High Pass Filter Bypass Control(1) |
| 8 | FMT0 | IN | Audio Data Format 0(1) |
| 9 | FMT1 | IN | Audio Data Format 1(1) |
| 10 | MODE0 | IN | Master/Slave Mode Selection 0(1) |
| 11 | MODE1 | IN | Master/Slave Mode Selection 1(1) |
| 12 | FSYNC | IN/OUT | Frame Synchronization |
| 13 | LRCK | IN/OUT | Sampling Clock Input/Output ($f_S$) |
| 14 | BCK | IN/OUT | Bit Clock Input/Output |
| 15 | DOUT | OUT | Audio Data Output |
| 16 | SYSCLK | IN | System Clock Input, $256f_S$, $384f_S$, or $512f_S$ |
| 17 | DGND | — | Digital Ground |
| 18 | $V_{DD}$ | — | Digital Power Supply |
| 19 | $C_{IN}NR$ | — | Anti-alias Filter Capacitor (–), Rch |
| 20 | $C_{IN}PR$ | — | Anti-alias Filter Capacitor (+), Rch |
| 21 | $C_{IN}NL$ | — | Anti-alias Filter Capacitor (–), Lch |
| 22 | $C_{IN}PL$ | — | Anti-alias Filter Capacitor (+), Lch |
| 23 | $V_{CC}$ | — | Analog Power Supply |
| 24 | AGND | — | Analog Ground |

NOTE: (1) With 100kΩ typical pull-down resistor.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| PCM1800E | 24-Lead SSOP | 338 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage: $+V_{DD}$, $+V_{CC}$ | +6.5V |
| Supply Voltage Differences | ±0.1V |
| GND Voltage Differences | ±0.1V |
| Digital Input Voltage | –0.3V to ($V_{DD}$ + 0.3V) |
| Analog Input Voltage | –0.3V to ($V_{CC}$ + 0.3V) |
| Input Current (any pin except supplies) | ±10mA |
| Power Dissipation | 300mW |
| Operating Temperature Range | –25°C to +85°C |
| Storage Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |
| (reflow, 10s) | +235°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# DIR1700

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

www.burr-brown.com/databook/DIR1700.html

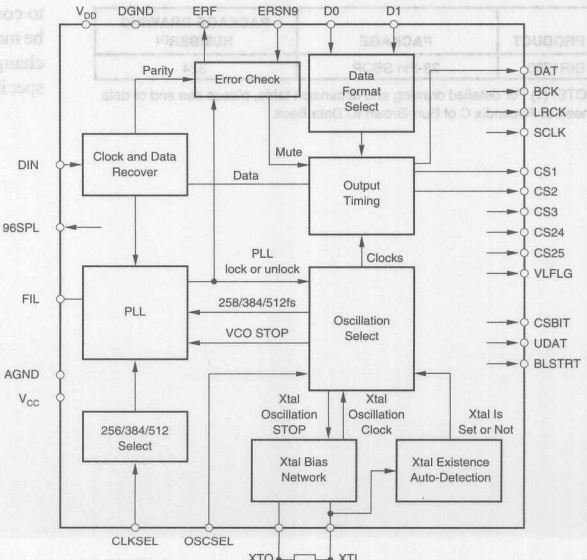
# DIGITAL AUDIO INTERFACE RECEIVER

## FEATURES

- STANDARD DIGITAL AUDIO INTERFACE RECEIVER (EIAJ1201)
- SAMPLING RATE: 32/44.1/48/96kHz
- RECOVERS 256/384/512fs SYSTEM CLOCKS
- VERY LOW JITTER SYSTEM CLOCK OUTPUT
- FLEXIBLE SYSTEM CLOCK OUTPUT
- XTAL CLOCK/PLL CLOCK OPERATION MODES
- SELECTABLE ERROR FLAG FUNCTION
- SELECTABLE OUTPUT PCM AUDIO DATA FORMAT
- OUTPUTS CHANNEL STATUS DATA FLAG WITH BLOCK START SIGNAL
- OUTPUTS USER BIT DATA
- SINGLE +5V POWER SUPPLY
- 28-PIN SSOP PACKAGE

## DESCRIPTION

DIR1700 is a Digital Audio Interface Receiver (DIR) which is designed for consumer and professional digital audio applications, such as Digital AV Receivers. DIR1700 has two system clock operation modes, "Internal PLL operation mode" and "XTAL clock operation mode", for systems which contain both digital and analog inputs. The advantages of the DIR1700 are "Very low jitter system clock output" and "96kHz sampling rate capability". These features are now required for consumer and professional audio systems.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

All specifications at +25°C, $V_{CA}$ = $V_{CP}$ = $V_{DD}$ = +5V, unless otherwise noted.

| PARAMETER | CONDITIONS | DIR1700 MIN | DIR1700 TYP | DIR1700 MAX | UNITS |
|---|---|---|---|---|---|
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Input Logic Level: $V_{IH}$(1) | | 2.0 | | | VDC |
| $V_{IL}$(1) | | | | 0.8 | VDC |
| $V_{IH}2$(2) | | 70% VDD | | | VDC |
| $V_{IL}2$(2) | | | | 30% $V_{DD}$ | VDC |
| $V_{IH}3$(3) | | TBD | | | VDC |
| $V_{IL}3$(3) | | | | TBD | VDC |
| Output Logic Level: $V_{OH}$(4) | $I_O$ = 2mA | $V_{DD}$ 0.4 | | | VDC |
| $V_{OL}$(4) | $I_O$ = –4mA | | | 0.5 | VDC |
| Input Leakage Current: $I_{IN}$ | | | ±1.0 | ±10 | µA |
| Input Sampling Frequency: $F_S$ | | +32 | | 96 | kHz |
| System Clock Frequency SCLK(5) | | 8.192 | 256, 384, 512fs | 36.864 | MHz |
| SCLK Clock Jitter | | | 200 | | ps rms |
| SCLK Duty Cycle | | | 50 | | % |
| Crystal Resonator Frequency | | 8.192 | | 24.576 | MHz |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range | $V_{DD}$, $V_{CC}$ | +4.5 | +5 | +5.5 | VDC |
| Supply Current: $I_A$ ($V_{CC}$) | | | TBD | | mA |
| $I_D$ ($V_{DD}$) | | | TBD | | mA |
| Power Consumption | $P_D$ | | TBD | | mA |

NOTES: (1) Except CLKSEL DIN; TTL Compatible. (2) CLKSEL. (3) DIN, CMOS Logic Level. (4) Pins 6-8, 11-21, 23. (5) FS is defined as the incoming audio sampling frequency per channel. (6) DIR1700 without load at SCLK, LRCK, BCK, DAT. Power supply current varies with system clock frequency.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltages: +$V_{DD}$ | ±6.5V |
| +$V_{CC}$ | ±6.5V |
| Input Voltage | –0.3 to $V_{DD}$ +0.3V |
| Input Current | ±10mA |
| Operating Temperature Range | –25°C to +85°C |
| Storage Temperature Range | –55°C to +125°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| DIR1700 | 28-Pin SSOP | 324 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

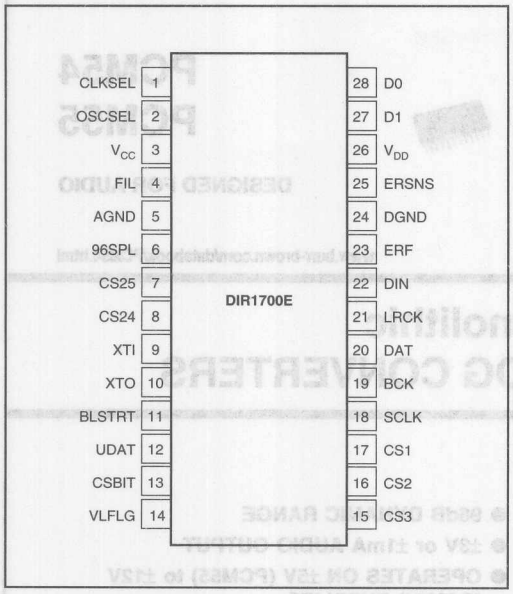
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



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## PIN CONFIGURATION




## PIN ASSIGNMENTS

| PIN | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| 1 | CLKSEL | In | Clock Select (256fs, 384fs and 512fs)(1) |
| 2 | OSCSEL | In | Oscillation Select (PLL/Xtal)(2) |
| 3 | $V_{CC}$ | — | Analog Power Supply |
| 4 | FIL | — | PLL filter |
| 5 | AGND | — | Analog Ground |
| 6 | 96SPL | Out | 96kHz Sampling Flag |
| 7 | CS25 | Out | Fs Rate Flag (32k, 44.1k and 48k)(4) |
| 8 | CS24 | Out | Fs Rate Flag (32k, 44.1k and 48k)(4) |
| 9 | XTI | In | Crystal In |
| 10 | XTO | Out | Crystal Out |
| 11 | BLSTRT | Out | Block Start Clock(5) |
| 12 | UDAT | Out | User Data Out(5) |
| 13 | CSBIT | Out | Channel Status Bit(5) |
| 14 | VLFLG | Out | Validity flag |
| 15 | CS3 | Out | Emphasis Flag(4) |
| 16 | CS2 | Out | Copy Guard Flag(4) |
| 17 | CS1 | Out | Audio Data Flag (PCM/DATA)(4) |
| 18 | SCLK | Out | Audio System Clock Out |
| 19 | BCK | Out | Audio Bit Clock Out |
| 20 | DAT | Out | Audio Data Out |
| 21 | LRCK | Out | Audio Left/Right Clock Out |
| 22 | DIN | In | Data Input |
| 23 | ERF | Out | Error Flag Out (PLL Unlock/Parity Error) |
| 24 | DGND | — | Digital Ground |
| 25 | ERSNS | In | Error Sense Switch(2) |
| 26 | $V_{DD}$ | — | Digital Power Supply |
| 27 | D1 | In | Data Format Select 1(3) |
| 28 | D0 | In | Data Format Select 0(3) |

NOTES: (1) When "CLKSEL" is open, input level becomes Middle ($1/2V_{DD}$) by the pull-up and pull-down resistors. (2) Pull-up. (3) Pull-down. (4) Channel status output pins become active for consumer application. (5) Serial outputs are utilized for both consumer and professional application.

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# PCM54
# PCM55

**DESIGNED FOR AUDIO**

www.burr-brown.com/databook/PCM54.html

# 16-Bit Monolithic DIGITAL-TO-ANALOG CONVERTERS

## FEATURES

- PARALLEL INPUT FORMAT
- 16-BIT RESOLUTION
- 15-BIT MONOTONICITY (typ)
- –92dB TOTAL HARMONIC DISTORTION (K Grade)
- 3µs SETTLING TIME (Voltage Out)
- 96dB DYNAMIC RANGE
- ±3V or ±1mA AUDIO OUTPUT
- OPERATES ON ±5V (PCM55) to ±12V (PCM54) SUPPLIES
- 28-PIN DIP (PCM54)
- 24-LEAD SOIC (PCM55)

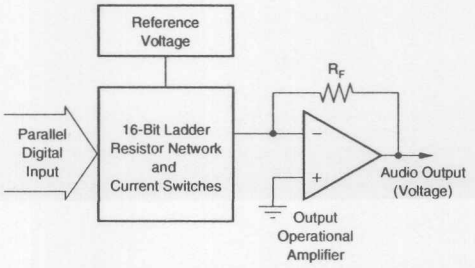
## DESCRIPTION

The PCM54 and PCM55 family of converters are parallel input, fully monotonic, 16-bit digital-to-analog converters that are designed and specified for digital audio applications. These devices employ ultra-stable nichrome (NiCr) thin-film resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature.

These converters are completely self-contained with a stable, low noise, internal, zener voltage reference; high speed current switches; a resistor ladder network; and a fast settling, low noise output operational amplifier all on a single monolithic chip. The converters are operated using two power supplies that can range from ±5V (PCM55) to ±12V (PCM54). Power dissipation with ±5V supplies is typically less than 200mW. Also included is a provision for external adjustment of the MSB error (differential linearity error at bipolar zero, PCM54 only) to further improve THD specifications if desired.

A current output ($I_{OUT}$) wiring option is provided. This output typically settles to within ±0.006% of FSR final value in 350ns (in response to a full-scale change in the digital input code).

The PCM54 is packaged in 28-pin plastic DIP package. The PCM55 is available in a 24-pin plastic mini-flatpak.




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# SPECIFICATIONS

## ELECTRICAL

At +25°C, $\pm V_{CC}$ = 12V, unless otherwise noted.

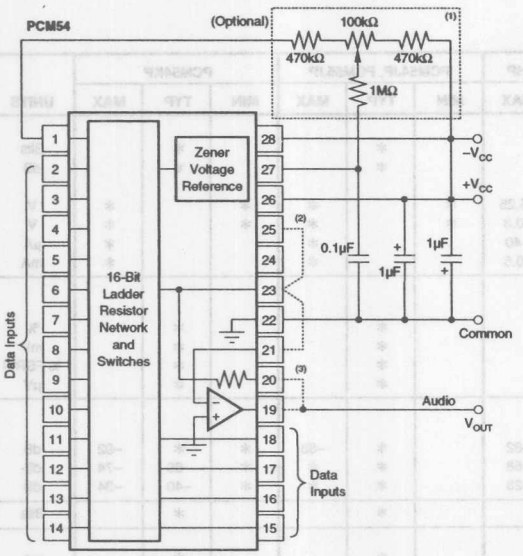
| PARAMETER | PCM54HP, PCM55HP MIN | PCM54HP, PCM55HP TYP | PCM54HP, PCM55HP MAX | PCM54JP, PCM55JP MIN | PCM54JP, PCM55JP TYP | PCM54JP, PCM55JP MAX | PCM54KP MIN | PCM54KP TYP | PCM54KP MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| **DIGITAL INPUTS** | | | | | | | | | | |
| Resolution | | 16 | | | * | | | * | | Bits |
| Dynamic Range | | 96 | | | * | | | * | | dB |
| Logic Levels (TTL/CMOS Compatible): | | | | | | | | | | |
| $V_{IH}$ | +2.4 | | +5.25 | * | | * | * | | * | V |
| $V_{IL}$ | 0 | | +0.8 | * | | * | * | | * | V |
| $I_{IH}$, $V_{IN}$ = +2.7V | | | +40 | | | * | | | * | µA |
| $I_{IL}$, $V_{IN}$ = +0.4V | | | –0.5 | | | * | | | * | mA |
| **TRANSFER CHARACTERISTICS** | | | | | | | | | | |
| **ACCURACY** | | | | | | | | | | |
| Gain Error | | ±2 | | | * | | | * | | % |
| Bipolar Zero Error | | ±30 | | | * | | | * | | mV |
| Differential Linearity Error at Biploar Zero[1] | | ±0.001 | | | * | | | * | | % FSR[2] |
| Noise (rms) (20Hz to 20kHz) at Bipolar Zero | | 12 | | | * | | | * | | µV |
| **TOTAL HARMONIC DISTORTION[3]** | | | | | | | | | | |
| (16-Bit Resolution) | | | | | | | | | | |
| $V_O$ = ±FS at f = 991Hz | | –94 | –82 | | * | –88 | * | * | –92 | dB |
| $V_O$ = –20dB at f = 991Hz | | –74 | –68 | | * | * | * | –80 | –74 | dB |
| $V_O$ = –60dB at f = 991Hz | | –34 | –28 | | * | * | * | –40 | –34 | dB |
| **MONOTONICITY** | | 15 | | | * | | | * | | Bits |
| **SETTLING TIME** (to ±0.006% of FSR) | | | | | | | | | | |
| Voltage Output: 6V Step | | 3 | | | * | | | * | | µs |
| 1LSB Step | | 1 | | | * | | | * | | µs |
| Current Output (1mA Step): 10Ω to 100Ω Load | | 350 | | | * | | | * | | ns |
| 1kΩ Load[4] | | 350 | | | * | | | * | | ns |
| Deglitcher Delay (THD Test)[5] | | 2.5 | 4 | | * | * | | * | * | µs |
| Slew Rate | | 10 | | | * | | | * | | V/µs |
| **WARM-UP TIME** | 1 | | | * | | | * | | | Min |
| **ANALOG OUTPUT** | | | | | | | | | | |
| Voltage Output: Bipolar Range | | ±3 | | | * | | | * | | V |
| Output Current | ±2 | | | * | | | * | | | mA |
| Output Impedance | | 0.1 | | | * | | | * | | Ω |
| Short-Circuit Duration | | Indefinite to Common | | | * | | | * | | |
| Current Output:[6] | | | | | | | | | | |
| Bipolar Range (±30%) | | ±1 | | | * | | | * | | mA |
| Bipolar Output Impedance (±30%) | | 1.2 | | | * | | | * | | kΩ |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | | | |
| Voltage: $+V_{CC}$ (PCM54) | +4.75 | +12 | +15.75 | * | * | * | * | * | * | V |
| $-V_{CC}$ (PCM54) | –4.75 | –12 | –15.75 | * | * | * | * | * | * | V |
| $+V_{CC}$ (PCM55) | +4.75 | +5 | +7.5 | * | * | * | * | * | * | V |
| $-V_{CC}$ (PCM55) | –4.75 | –5 | –7.5 | * | * | * | * | * | * | V |
| Supply Drain: $+V_{CC}$ | | +13 | +20 | | * | * | | * | * | mA |
| $-V_{CC}$ | | –16 | –25 | | * | * | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | | | |
| Operating | 0 | | +70 | * | | * | * | | * | °C |
| Storage | –55 | | +100 | * | | * | * | | * | °C |

* Specification same as for PCM54HP.

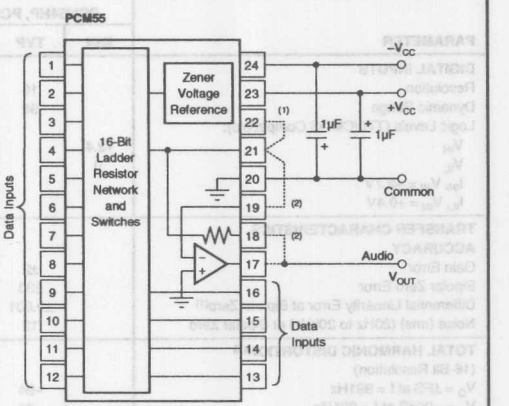
NOTES: (1) Externally adjustable. If external adjustment is not used, connect a 0.01µF capacitor to Common to reduce noise pickup. (2) FSR means Full-Scale Range and is 6V for ±3V output. (3) The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit. Burr-Brown may calculate THD from the measured linearity errors using equation 2 in the section on "Total Harmonic Distortion," but specifies that the maximum THD measured with the circuit shown in Figure 2 will be less than the limits indicated. (4) Measured with an active clamp to provide a low impedance for approximately 200ns. (5) Deglitcher or sample/hold delay used in THD measurement test circuit. See Figures 2 and 3. (6) Output amplifier disconnected.

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## CONNECTION DIAGRAMS




NOTES: (1) MSB error (BPZ differential linearity error) can be adjusted to zero using this external circuit. (2) Connect to bipolar operation ($+V_{CC} \geq 8.5V$ for unipolar operation). (3) Connect for $V_{OUT}$ operation. When $V_{OUT}$ amp is not being used ($I_{OUT}$ mode), terminate with an external 3kΩ feedback resistor between pin 19 and pin 21, and a 1kΩ resistor between pin 21 and pin 22 to reduce possible noise effects.




NOTES: (1) Connect for bipolar operation. ($+V_{CC} \geq 8.5V$ for unipolar operation). (2) Connect for $V_{OUT}$ operation. When $V_{OUT}$ amp is not being used ($I_{OUT}$ mode), terminate with an external 3kΩ feedback resistor between pin 17 and pin 19, and a 1kΩ resistor between pin 19 and pin 20 to reduce possible noise effects.

## PIN ASSIGNMENTS

| PIN | PCM54-DIP | PIN | PCM54-DIP |
|---|---|---|---|
| 1 | Trim | 15 | Bit 13 |
| 2 | Bit 1 (MSB) | 16 | Bit 14 |
| 3 | Bit 2 | 17 | Bit 15 |
| 4 | NC | 18 | Bit 16 (LSB) |
| 5 | Bit 3 | 19 | $V_{OUT}$ |
| 6 | Bit 4 | 20 | $R_{FB}$ |
| 7 | Bit 5 | 21 | SJ |
| 8 | Bit 6 | 22 | Common |
| 9 | Bit 7 | 23 | $I_{OUT}$ |
| 10 | Bit 8 | 24 | NC |
| 11 | Bit 9 | 25 | $I_{BPO}$ |
| 12 | Bit 10 | 26 | $+V_{CC}$ |
| 13 | Bit 11 | 27 | MSB Adjust |
| 14 | Bit 12 | 28 | $-V_{CC}$ |

## PIN ASSIGNMENTS

| PIN | PCM55-SOIC | PIN | PCM55-SOIC |
|---|---|---|---|
| 1 | Bit 1 (MSB) | 13 | Bit 13 |
| 2 | Bit 2 | 14 | Bit 14 |
| 3 | Bit 3 | 15 | Bit 15 |
| 4 | Bit 4 | 16 | Bit 16 |
| 5 | Bit 5 | 17 | $V_{OUT}$ |
| 6 | Bit 6 | 18 | Feedback Resistor |
| 7 | Bit 7 | 19 | Summing Junction |
| 8 | Bit 8 | 20 | Common |
| 9 | Bit 9 | 21 | Current Output |
| 10 | Bit 10 | 22 | Bipolar Offset |
| 11 | Bit 11 | 23 | $+V_{CC}$ |
| 12 | Bit 12 | 24 | $-V_{CC}$ |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| DC Supply Voltage | ±18VDC |
| Input Logic Voltage | −1V to +5.5V |
| Power Dissipation | PCM54 800mW, PCM55 400mW |
| Storage Temperature | −55°C to +100°C |
| Lead Temperature, (soldering, 10s) | +300°C |

## PACKAGE INFORMATION

| PRODUCT | THD at FS | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|---|
| PCM54HP | 0.008 | 28-Pin DIP | 215 |
| PCM54JP | 0.004 | 28-Pin DIP | 215 |
| PCM54KP | 0.0025 | 28-Pin DIP | 215 |
| PCM55HP | 0.008 | 24-Lead SOIC | 178 |
| PCM55JP | 0.004 | 24-Lead SOIC | 178 |

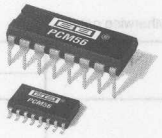
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# PCM56P
# PCM56U

**DESIGNED FOR AUDIO**

www.burr-brown.com/databook/PCM56.html

# Serial Input 16-Bit Monolithic DIGITAL-TO-ANALOG CONVERTER

## FEATURES

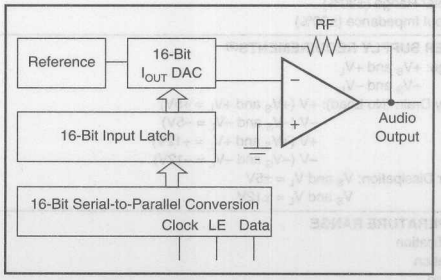
- SERIAL INPUT
- –92dB MAX THD: FS Input, K Grade
- –74dB MAX THD: –20dB Input, K Grade
- 96dB DYNAMIC RANGE
- NO EXTERNAL COMPONENTS REQUIRED
- 16-BIT RESOLUTION
- 15-BIT MONOTONICITY, TYP
- 0.001% OF FSR TYP DIFFERENTIAL LINEARITY ERROR
- 1.5µs SETTLING TIME, TYP: Voltage Out
- ±3V OR ±1mA AUDIO OUTPUT
- EIAJ STC-007-COMPATIBLE
- OPERATES ON ±5V TO ±12V SUPPLIES
- PINOUT ALLOWS $I_{OUT}$ OPTION
- PLASTIC DIP OR SOIC PACKAGE

## DESCRIPTION

The PCM56 is a state-of-the-art, fully monotonic, digital-to-analog converter that is designed and specified for digital audio applications. This device employs ultra-stable nichrome (NiCr) thin-film resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature.

This converter is completely self-contained with a stable, low noise, internal zener voltage reference; high speed current switches; a resistor ladder network; and a fast settling, low noise output operational amplifier all on a single monolithic chip. The converters are operated using two power supplies that can range from ±5V to ±12V. Power dissipation with ±5V supplies is typically less than 200mW. Also included is a provision for external adjustment of the MSB error (differential linearity error at bipolar zero) to further improve total harmonic distortion (THD) specifications if desired. Few external components are necessary for operation, and all critical specifications are 100% tested. This helps assure the user of high system reliability and outstanding overall system performance.

The PCM56 is packaged in a high-quality 16-pin molded plastic DIP package or SOIC and has passed operating life tests under simultaneous high-pressure, high-temperature, and high-humidity conditions.




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# SPECIFICATIONS

## ELECTRICAL

Typical at +25°C, and nominal power supply voltages ±5V, unless otherwise noted.

| PARAMETER | PCM56U, PCM56P-J, -K MIN | TYP | MAX | UNITS |
|---|---|---|---|---|
| **DIGITAL INPUT** | | | | |
| Resolution | | 16 | | Bits |
| Digital Inputs[1]: $V_{IH}$ | +2.4 | | $+V_L$ | V |
| $V_{IL}$ | 0 | | +0.8 | V |
| $I_{IH}$, $V_{IN}$ = +2.7V | | | +1.0 | µA |
| $I_{IL}$, $V_{IN}$ = +0.4V | | | –50 | µA |
| Input Clock Frequency | 10.0 | | | MHz |
| **TRANSFER CHARACTERISTICS** | | | | |
| **ACCURACY** | | | | |
| Gain Error | | ±2.0 | | % |
| Bipolar Zero Error | | ±30 | | mV |
| Differential Linearity Error | | ±0.001 | | % of FSR[2] |
| Noise (rms, 20Hz to 20kHz) at Bipolar Zero ($V_{OUT}$ models) | | 6 | | µV |
| **TOTAL HARMONIC DISTORTION** | | | | |
| $V_O$ = ±FS at f = 991Hz: PCM56P-K | | –94 | –92 | dB |
| PCM56P-J | | –94 | –88 | dB |
| PCM56P, PCM56U | | –94 | –82 | dB |
| PCM56P-L | | –94 | –80 | dB |
| $V_O$ = –20dB at f = 991Hz: PCM56P-K | | –75 | –74 | dB |
| PCM56P-J | | –75 | –68 | dB |
| PCM56P, PCM56U | | –75 | –68 | dB |
| PCM56P-L | | –75 | –60 | dB |
| $V_O$ = –60dB at f = 991Hz: PCM56P-K | | –35 | –34 | dB |
| PCM56P-J | | –35 | –28 | dB |
| PCM56P, PCM56U | | –35 | –28 | dB |
| PCM56P-L | | –35 | –20 | dB |
| **MONOTONICITY** | | 15 | | Bits |
| **DRIFT** (0°C to +70°C) | | | | |
| Total Drift[3] | | ±25 | | ppm of FSR/°C |
| Bipolar Zero Drift | | ±4 | | ppm of FSR/°C |
| **SETTLING TIME** (to ±0.006% of FSR) | | | | |
| Voltage Output: 6V Step | | 1.5 | | µs |
| 1LSB | | 1.0 | | µs |
| Slew Rate | | 10 | | V/µs |
| Current Output, 1mA Step: 10Ω to 100Ω Load | | 350 | | ns |
| 1kΩ Load[4] | | 350 | | ns |
| **WARM-UP TIME** | 1 | | | Min |
| **OUTPUT** | | | | |
| Voltage Output Configuration: Bipolar Range | | ±3.0 | | V |
| Output Current | ±2.0 | | | mA |
| Output Impedance | | 0.10 | | Ω |
| Short Circuit Duration | | Indefinite to Common | | |
| Current Output Configuration: | | | | |
| Bipolar Range (±30%) | | ±1.0 | | mA |
| Output Impedance (±30%) | | 1.2 | | kΩ |
| **POWER SUPPLY REQUIREMENTS**[5] | | | | |
| Voltage: $+V_S$ and $+V_L$ | +4.75 | +5.00 | +13.2 | V |
| $–V_S$ and $–V_L$ | –4.75 | –5.00 | –13.2 | V |
| Supply Drain (No Load): +V ($+V_S$ and $+V_L$ = +5V) | | +10.00 | +17.0 | mA |
| –V ($–V_S$ and $–V_L$ = –5V) | | –25.0 | –35.0 | mA |
| +V ($+V_S$ and $+V_L$ = +12V) | | +12.0 | | mA |
| –V ($–V_S$ and $–V_L$ = –12V) | | –27.0 | | mA |
| Power Dissipation: $V_S$ and $V_L$ = ±5V | | 175 | 260 | mW |
| $V_S$ and $V_L$ = ±12V | | 468 | | mW |
| **TEMPERATURE RANGE** | | | | |
| Specification | 0 | | +70 | °C |
| Operation | –25 | | +70 | °C |
| Storage | –60 | | +100 | °C |

NOTES: (1) Logic input levels are TTL/CMOS-compatible. (2) FSR means full-scale range and is equivalent to 6V (±3V) for PCM56 in the $V_{OUT}$ mode. (3) This is the combined drift error due to gain, offset, and linearity over temperature. (4) Measured with an active clamp to provide a low impedance for approximately 200ns. (5) All specifications assume $+V_S$ connected to $+V_L$ and $–V_S$ connected to $–V_L$. If supplies are connected separately, $–V_L$ must not be more negative than $–V_S$ supply voltage to assure proper operation. No similar restriction applies to the value of $+V_L$ with respect to $+V_S$.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| DC Supply Voltages | ±16VDC |
| Input Logic Voltage | –1V to $+V_S$/$+V_L$ |
| Power Dissipation | 850mW |
| Operating Temperature | –25°C to +70°C |
| Storage Temperature | –60°C to +100°C |
| Lead Temperature (soldering, 10s) | +300°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| PCM56U | 16-Pin SOIC | 211 |
| PCM56P | 16-Pin Plastic DIP | 180 |
| PCM56P-J | 16-Pin Plastic DIP | 180 |
| PCM56P-K | 16-Pin Plastic DIP | 180 |
| PCM56P-L | 16-Pin Plastic DIP | 180 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN ASSIGNMENTS

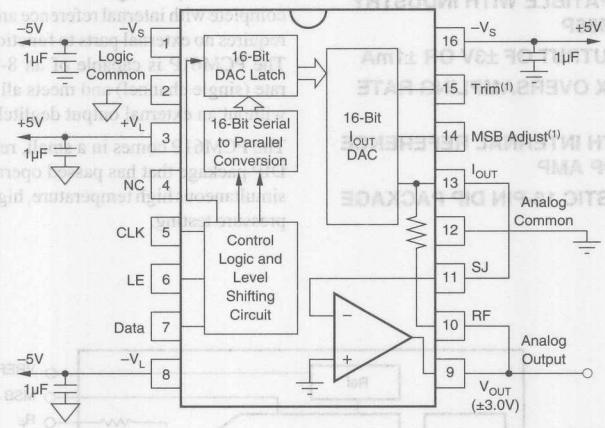
| PIN | DESCRIPTION | MNEMONIC |
|---|---|---|
| P1 | Analog Negative Supply | $-V_S$ |
| P2 | Logic Common | LOG COM |
| P3 | Logic Positive Supply | $+V_L$ |
| P4 | No Connection | NC |
| P5 | Clock Input | CLK |
| P6 | Latch Enable Input | LE |
| P7 | Serial Data Input | DATA |
| P8 | Logic Negative Supply | $-V_L$ |
| P9 | Voltage Output | $V_{OUT}$ |
| P10 | Feedback Resistor | RF |
| P11 | Summing Junction | SJ |
| P12 | Analog Common | ANA COM |
| P13 | Current Output | $I_{OUT}$ |
| P14 | MSB Adjustment Terminal | MSB ADJ |
| P15 | MSB Trim-pot Terminal | TRIM |
| P16 | Analog Positive Supply | $+V_S$ |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## CONNECTION DIAGRAM




NOTE: (1) MSB error (Bipolar Zero differential linearity error) can be adjusted to zero using the external circuit shown in Figure 6.



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# PCM61P

www.burr-brown.com/databook/PCM61.html

# Serial Input 18-Bit Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

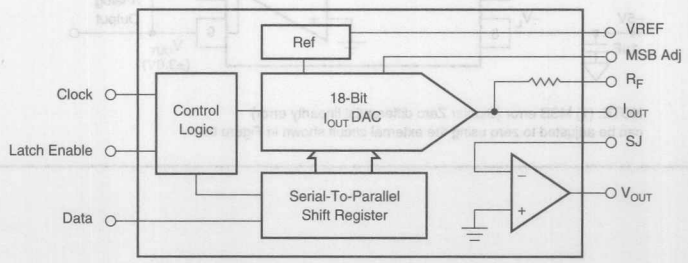
## FEATURES

- 18-BIT MONOLITHIC AUDIO D/A CONVERTER
- LOW MAX THD + N: –92dB Without External Adjust
- 100% PIN COMPATIBLE WITH INDUSTRY STD 16-BIT PCM56P
- LOW GLITCH OUTPUT OF ±3V OR ±1mA
- CAPABLE OF 8X OVERSAMPLING RATE IN $V_{OUT}$ MODE
- COMPLETE WITH INTERNAL REFERENCE AND OUTPUT OP AMP
- RELIABLE PLASTIC 16-PIN DIP PACKAGE

## DESCRIPTION

The PCM61P is an 18-bit totally pin compatible performance replacement for the popular 16-bit PCM56P. With the addition of two extra bits, lower max THD+N (–92dB; PCM61P-K) can be achieved in audio applications already using the PCM56P. The PCM61P is complete with internal reference and output op amp and requires no external parts to function as an 18-bit DAC. The PCM61P is capable of an 8-times oversampling rate (single channel) and meets all of its specifications without an external output deglitcher.

The PCM61P comes in a small, reliable 16-pin plastic DIP package that has passed operating life tests under simultaneous high temperature, high humidity and high pressure testing.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

All specifications at 25°C, and $+V_{CC}$ = +5V, unless otherwise noted.

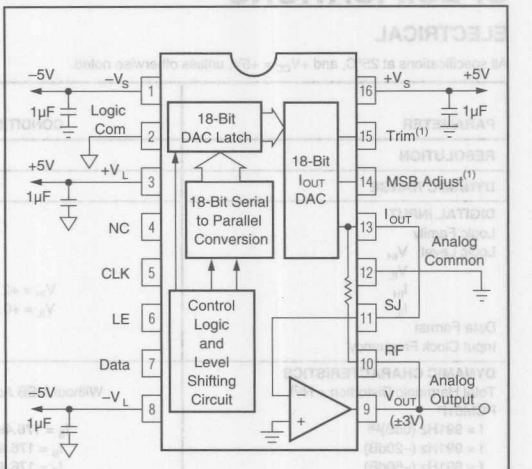
| PARAMETER | CONDITIONS | PCM61P-P, J-P, K MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | | 18 | Bits |
| **DYNAMIC RANGE** | | | 108 | | dB |
| **DIGITAL INPUT** | | | | | |
| Logic Family | | | TTL/CMOS Compatible | | |
| Logic Level: $V_{IH}$ | | +2.4 | | $+V_L$ | V |
| $V_{IL}$ | | 0 | | +0.8 | V |
| $I_{IH}$ | $V_{IH}$ = +2.7V | | | +1 | µA |
| $I_{IL}$ | $V_{IL}$ = +0.4V | | | –50 | µA |
| Data Format | | | Serial BTC[1] | | |
| Input Clock Frequency | | | | 16.9 | MHz |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Total Harmonic Distortion + N[2] | Without MSB Adjustments | | | | |
| PCM61P | | | | | |
| f = 991Hz (0dB)[3] | $f_S$ = 176.4kHz[4] | | –88 | –82 | dB |
| f = 991Hz (–20dB) | $f_S$ = 176.4kHz | | –74 | –68 | dB |
| f = 991Hz (–60dB) | $f_S$ = 176.4kHz | | –34 | –28 | dB |
| PCM61P-J | | | | | |
| f = 991Hz (0dB) | $f_S$ = 176.4kHz | | –94 | –88 | dB |
| f = 991Hz (–20dB) | $f_S$ = 176.4kHz | | –76 | –74 | dB |
| f = 991Hz (–60dB) | $f_S$ = 176.4kHz | | –36 | –34 | dB |
| PCM61P-K | | | | | |
| f = 991Hz (0dB) | $f_S$ = 176.4kHz | | –98 | –92 | dB |
| f = 991Hz (–20dB) | $f_S$ = 176.4kHz | | –80 | –74 | dB |
| f = 991Hz (–60dB) | $f_S$ = 176.4kHz | | –40 | –34 | dB |
| **IDLE CHANNEL SNR** | 20Hz to 20kHz at BPZ[5] | | 112 | | dB |
| **TRANSFER CHARACTERISTICS** | | | | | |
| **ACCURACY** | | | | | |
| Gain Error | | | ±2 | | %FSR |
| Bipolar Zero Error | | | ±30 | | mV |
| Differential Linearity Error | | | ±0.001 | | %FSR |
| Total Drift[6] | 0°C to 70°C | | ±25 | | ppm of FSR/°C |
| Bipolar Zero Drift | 0°C to 70°C | | ±4 | | ppm of FSR/°C |
| Warm-up Time | | 1 | | | Minute |
| **MONOTONICITY** | | | 16 | | Bits |
| **ANALOG OUTPUT** | | | | | |
| Voltage: Output Range | | | ±3 | | V |
| Output Current | | ±2 | | | mA |
| Output Impedance | | | 0.1 | | Ω |
| Current: Output Range | ±30% | | ±1 | | mA |
| Output Impedance | ±30% | | 1.2 | | kΩ |
| **SETTLING TIME** | To ±0.006% of FSR | | | | |
| Voltage: 6V Step | | | 1.5 | | µs |
| 1 LSB | | | 1.0 | | µs |
| Slew Rate | | | 12 | | V/µs |
| Current: 1mA Step | 10Ω to 100Ω Load | | 250 | | ns |
| 1mA Step | 1kΩ Load | | 350 | | ns |
| Glitch Energy | Meets all THD+N specs without external deglitching | | | | |
| **POWER SUPPLY REQUIREMENTS**[7] | | | | | |
| $\pm V_{CC}$ Supply Voltage | | ±4.75 | ±5 | ±13.2 | V |
| Supply Current: $+I_{CC}$ | $+V_{CC}$ = +5V | | +10 | +17 | mA |
| $+I_{CC}$ | $+V_{CC}$ = +12V | | +12 | | mA |
| $-I_{CC}$ | $-V_{CC}$ = –5V | | –25 | –35 | mA |
| $-I_{CC}$ | $-V_{CC}$ = –12V | | –27 | | mA |
| Power Dissipation | $\pm V_{CC}$ = ±5V | | 175 | 260 | mW |
| | $\pm V_{CC}$ = ±12V | | 475 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | 0 | | +70 | °C |
| Operating | | –30 | | +70 | °C |
| Storage | | –60 | | +100 | °C |

NOTES: (1) Binary Two's Complement coding. (2) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$)/$Signal_{RMS}$. (3) D/A converter output frequency/signal level. (4) D/A converter sample frequency (4 x 44.1kHz; 4 times oversampling). (5) Bipolar zero, using A-weighted filter. (6) This is the combined drift error due to gain, offset, and linearity over temperature. (7) All positive and all negative supply pins must be tied together respectively.

## PIN ASSIGNMENTS

| PIN | FUNCTION | DESCRIPTION |
|---|---|---|
| 1 | $-V_S$ | Analog Negative Supply |
| 2 | LOG COM | Logic Common |
| 3 | $+V_L$ | Logic Positive Supply |
| 4 | NC | No Connection |
| 5 | CLK | Clock Input |
| 6 | LE | Latch Enable Input |
| 7 | DATA | Serial Data Input |
| 8 | $-V_L$ | Logic Negative Supply |
| 9 | $V_{OUT}$ | Voltage Output |
| 10 | RF | Feedback Resistance |
| 11 | SJ | Summing Junction |
| 12 | ANA COM | Analog Common |
| 13 | $I_{OUT}$ | Current Output |
| 14 | MSB ADJ | MSB Adjustment Terminal |
| 15 | TRIM | MSB Trim-pot Terminal |
| 16 | $+V_S$ | Analog Positive Supply |

## CONNECTION DIAGRAM




NOTE: (1) MSB error (Bipolar Zero differential linearity error) can be adjusted to zero using the external circuit shown in Figure 4.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| DC Supply Voltages | ±16VDC |
| Input Logic Voltage | –1V to $V_S$ /$+V_L$ |
| Power Dissipation | 850mW |
| Operating Temperature Range | –25°C to +70°C |
| Storage Temperature Range | –60°C to +100°C |
| Lead Temperature (soldering, 10s) | +300°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| PCM61P-P | 16-Pin Plastic DIP | 180 |
| PCM61P-J | 16-Pin Plastic DIP | 180 |
| PCM61P-K | 16-Pin Plastic DIP | 180 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

| DIGITAL INPUT | ANALOG OUTPUT | | |
|---|---|---|---|
| Binary Two's Complement (BTC) | DAC Output | Voltage (V) $V_{OUT}$ Mode | Current (mA) $I_{OUT}$ Mode |
| 1FFFF Hex | +FS | –0.99999237 | +2.99997711 |
| 00000 Hex | BPZ | 0.00000000 | 0.00000000 |
| 3FFFF Hex | BPZ – 1LSB | +0.00000763 | –0.00002289 |
| 20000 Hex | –FS | +1.00000000 | –3.00000000 |

TABLE I. PCM61P Input/Output Relationships.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# PCM63P

www.burr-brown.com/databook/PCM63.html

# *Colinear*™ 20-Bit Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

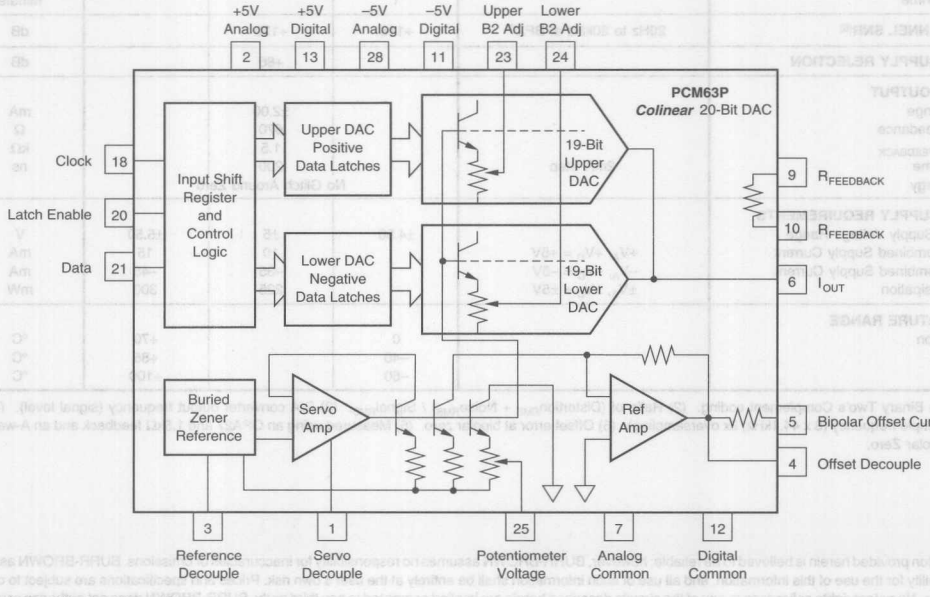
## FEATURES

- ***COLINEAR*** **20-BIT AUDIO DAC**
- **NEAR-IDEAL LOW LEVEL OPERATION**
- **GLITCH-FREE OUTPUT**
- **ULTRA LOW –96dB max THD+N (Without External Adjustment)**
- **116dB SNR min (A-Weight Method)**
- **INDUSTRY STD SERIAL INPUT FORMAT**
- **FAST (200ns) CURRENT OUTPUT (±2mA; ±2% max)**
- **CAPABLE OF 16x OVERSAMPLING**
- **COMPLETE WITH REFERENCE**

## DESCRIPTION

The PCM63P is a precision 20-bit digital-to-analog converter with ultra-low distortion (–96dB max with a full scale output; PCM63P-K). Incorporated into the PCM63P is a unique ***Colinear*** dual-DAC per channel architecture that eliminates unwanted glitches and other nonlinearities around bipolar zero. The PCM63P also features a very low noise (116dB max SNR; A-weighted method) and fast settling current output (200ns typ, 2mA step) which is capable of 16-times oversampling rates.

Applications include very low distortion frequency synthesis and high-end consumer and professional digital audio applications.




*Colinear*™, Burr-Brown Corp.

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# SPECIFICATIONS

## ELECTRICAL

All specifications at 25°C and $\pm V_A$ and $\pm V_D$ = ±5V, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM63P, PCM63P-J, PCM63P-K MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | 20 | | | Bits |
| **DYNAMIC RANGE,** THD+N at –60dB Referred to Full Scale | | | | | |
| PCM63P | | 96 | 100 | | dB |
| PCM63P-J | | 100 | 104 | | dB |
| PCM63P-K | | 104 | 108 | | dB |
| **DIGITAL INPUT** | | | | | |
| Logic Family | | | TTL/CMOS Compatible | | |
| Logic Level: $V_{IH}$ | | +2.4 | | $+V_D$ | V |
| $V_{IL}$ | | 0 | | 0.8 | V |
| $I_{IH}$ | $V_{IH}$ = +2.7V | | | +1 | µA |
| $I_{IL}$ | $V_{IL}$ = +0.4V | | | –50 | µA |
| Data Format | | | Serial, MSB First, BTC[1] | | |
| Input Clock Frequency | | | 12.5 | 25 | MHz |
| **TOTAL HARMONIC DISTORTION + N**[2], Without Adjustments | | | | | |
| PCM63P | | | | | |
| f = 991Hz (0dB)[3] | $f_S$ = 352.8kHz[4] | | –92 | –88 | dB |
| f = 991Hz (–20dB) | $f_S$ = 352.8kHz | | –80 | –74 | dB |
| f = 991Hz (–60dB) | $f_S$ = 352.8kHz | | –40 | –36 | dB |
| PCM63P-J | | | | | |
| f = 991Hz (0dB) | $f_S$ = 352.8kHz | | –96 | –92 | dB |
| f = 991Hz (–20dB) | $f_S$ = 352.8kHz | | –82 | –76 | dB |
| f = 991Hz (–60dB) | $f_S$ = 352.8kHz | | –44 | –40 | dB |
| PCM63P-K | | | | | |
| f = 991Hz (0dB) | $f_S$ = 352.8kHz | | –100 | –96 | dB |
| f = 991Hz (–20dB) | $f_S$ = 352.8kHz | | –88 | –82 | dB |
| f = 991Hz (–60dB) | $f_S$ = 352.8kHz | | –48 | –44 | dB |
| **ACCURACY** | | | | | |
| Level Linearity | at –90dB Signal Level | | ±0.3 | ±1 | dB |
| Gain Error | | | ±1 | ±2 | % |
| Bipolar Zero Error[5] | | | ±12 | | µA |
| Gain Drift | 0°C to 70°C | | 25 | | ppm/°C |
| Bipolar Zero Drift | 0°C to 70°C | | 4 | | ppm of FSR/°C |
| Warm-up Time | | 1 | | | Minute |
| **IDLE CHANNEL SNR**[6] | 20Hz to 20kHz at BPZ[7] | +116 | +120 | | dB |
| **POWER SUPPLY REJECTION** | | | +86 | | dB |
| **ANALOG OUTPUT** | | | | | |
| Output Range | | | ±2.00 | | mA |
| Output Impedance | | | 670 | | Ω |
| Internal $R_{FEEDBACK}$ | | | 1.5 | | kΩ |
| Settling Time | 2mA Step | | 200 | | ns |
| Glitch Energy | | | No Glitch Around Zero | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| $\pm V_A$, $\pm V_D$ Supply Voltage Range | | ±4.50 | ±5 | ±5.50 | V |
| $+I_A$, $+I_D$ Combined Supply Current | $+V_A$, $+V_D$ = +5V | | 10 | 15 | mA |
| $-I_A$, $-I_D$ Combined Supply Current | $-V_A$, $-V_D$ = –5V | | –35 | –45 | mA |
| Power Dissipation | $\pm V_A$, $\pm V_D$ = ±5V | | 225 | 300 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | 0 | | +70 | °C |
| Operating | | –40 | | +85 | °C |
| Storage | | –60 | | +100 | °C |

NOTES: (1) Binary Two's Complement coding. (2) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$) / $Signal_{RMS}$. (3) D/A converter output frequency (signal level). (4) D/A converter sample frequency (8 x 44.1kHz; 8x oversampling). (5) Offset error at bipolar zero. (6) Measured using an OPA27 and 1.5kΩ feedback and an A-weighted filter. (7) Bipolar Zero.

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## PIN ASSIGNMENTS

| PIN | DESCRIPTION | MNEMONIC |
|---|---|---|
| P1 | Servo Amp Decoupling Capacitor | CAP |
| P2 | +5V Analog Supply Voltage | $+V_A$ |
| P3 | Reference Decoupling Capacitor | CAP |
| P4 | Offset Decoupling Capacitor | CAP |
| P5 | Bipolar Offset Current Output (+2mA) | BPO |
| P6 | DAC Current Output (0 to –4mA) | $I_{OUT}$ |
| P7 | Analog Common Connection | ACOM |
| P8 | No Connection | NC |
| P9 | Feedback Resistor Connection (1.5kΩ) | $RF_1$ |
| P10 | Feedback Resistor Connection (1.5kΩ) | $RF_2$ |
| P11 | –5V Digital Supply Voltage | $-V_D$ |
| P12 | Digital Common Connection | DCOM |
| P13 | +5V Digital Voltage Supply | $+V_D$ |
| P14 | No Connection | NC |
| P15 | No Connection | NC |
| P16 | No Connection | NC |
| P17 | No Connection | NC |
| P18 | DAC Data Clock Input | CLK |
| P19 | No Connection | NC |
| P20 | DAC Data Latch Enable | LE |
| P21 | DAC Data Input | DATA |
| P22 | No Connection | NC |
| P23 | Optional Upper DAC Bit-2 Adjust (–4.29V)* | UB2 Adj |
| P24 | Optional Lower DAC Bit-2 Adjust (–4.29V)* | LB2 Adj |
| P25 | Bit Adjust Reference Voltage Tap (–3.52V)* | $V_{POT}$ |
| P26 | No Connection | NC |
| P27 | No Connection | NC |
| P28 | –5V Analog Supply Voltage | $-V_A$ |

*Nominal voltages at these nodes assuming $\pm V_A$; $\pm V_D$ = ±5V.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_A$, $+V_D$ to ACOM/DCOM | 0V to +8V |
| $-V_A$, $-V_D$ to ACOM/DCOM | 0V to –8V |
| $-V_A$, $-V_D$ to $+V_A$, $+V_D$ | 0V to +16V |
| ACOM to DCOM | ±0.5V |
| Digital Inputs (pins 18, 20, 21) to DCOM | –1V to $+V_D$ |
| Power Dissipation | 500mW |
| Lead Temperature, (soldering, 10s) | +300°C |
| Max Junction Temperature | 165°C |
| Thermal Resistance, $\theta_{JA}$ | 70°C/W |

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## PACKAGE INFORMATION

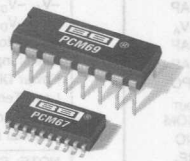
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| PCM63P | 28-Pin Plastic DIP | 215 |
| PCM63P-J | 28-Pin Plastic DIP | 215 |
| PCM63P-K | 28-Pin Plastic DIP | 215 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

| PRODUCT | PACKAGE | TEMPERATURE RANGE | MAX THD+N, AT 0dB |
|---|---|---|---|
| PCM63P | 28-Pin Plastic DIP | 0°C to +70°C | –88dB |
| PCM63P-J | 28-Pin Plastic DIP | 0°C to +70°C | –92dB |
| PCM63P-K | 28-Pin Plastic DIP | 0°C to +70°C | –96dB |

BURR - BROWN®




# PCM67
# PCM69

www.burr-brown.com/databook/PCM67.html

# Advanced 1-Bit BiCMOS Dual 18-Bit DIGITAL-TO-ANALOG CONVERTER

## FEATURES

- 18-BIT RESOLUTION DUAL AUDIO DAC
- EXCELLENT THD PERFORMANCE:
  0.0025% (–92dB) at F/S, K Grade
  1.0% (–40dB) at –60dB, K Grade
- HIGH S/N RATIO: 110dB typ (IHF-A)
- DUAL, CO-PHASE
- SINGLE SUPPLY +5V OPERATION
- LOW POWER: 75mW typical
- CAPABLE OF 16X OVERSAMPLING
- AVAILABLE IN SPACE SAVING
  16-PIN DIP OR 20-PIN SOIC
- OPERATING TEMP RANGE:
  –25°C to +85°C
- EXTREMELY LOW GLITCH ENERGY

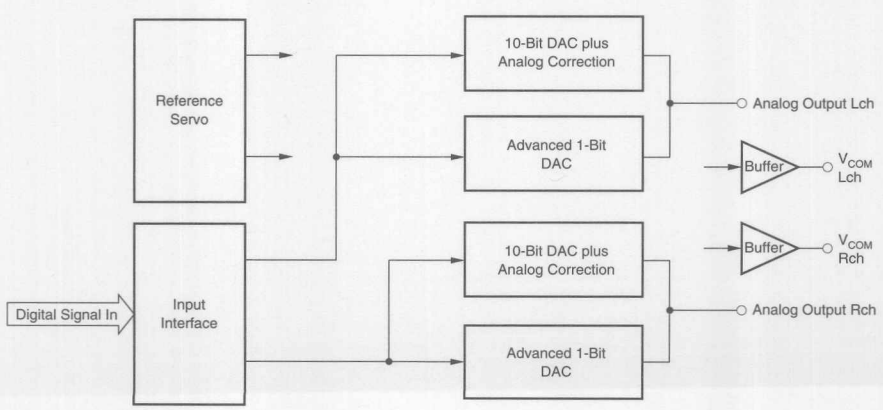
## DESCRIPTION

The PCM67 and PCM69A dual 18-bit DAC are low cost, dual output 18-bit BiCMOS digital-to-analog converters utilizing a novel architecture to achieve excellent low level performance.

By combining a conventional thin-film R-2R ladder DAC, a digital offset technique with analog correction and an advanced one-bit DAC using first order noise shaping technique, the PCM67 and PCM69A achieve high resolution, minimal glitch, and low zero-crossing distortion.

PCM67 digital offset occurs at bit 9, making it ideal for high-performance CD players. PCM69A digital offset occurs at bit 4, making it an excellent choice for digital musical instruments and audio DSP.

Both PCM67 and PCM69A operate from a single +5V supply. The low power consumption and small size (16-pin PDIP or 20-pin SOIC) make these converters ideal for a variety of digital audio applications.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

All specifications at +25°C and $+V_A$, $+V_D$ = +5V, unless otherwise noted

| PARAMETER | CONDITIONS | PCM67/69A MIN | PCM67/69A TYP | PCM67/69A MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | 18 | | Bits |
| **DYNAMIC RANGE**, THD+N at –60dB Referred to Full Scale | | | 106 | | dB |
| **DIGITAL INPUT** | | | | | |
| Logic Family | | | TTL/CMOS Compatible | | |
| Logic Level: $V_{IH}$ | $I_{IH}$ = ±5µA | +2 | | $+V_D$ | V |
| $V_{IL}$ | $I_{IL}$ = ±5µA | 0 | | 0.8 | V |
| Data Format | | | Serial, MSB First, BTC[1] | | |
| Input System Clock Frequency | | | 16.9344 | | MHz |
| **TOTAL HARMONIC DISTORTION + N**[2,3,4] | | | | | |
| PCM67P/69AP, PCM67U/69AU | | | | | |
| f = 991Hz (0dB) | $f_S$ = 352.8kHz | | –86 | –82 | dB |
| f = 991Hz (–20dB) | $f_S$ = 352.8kHz | | –68 | | dB |
| f = 991Hz (–60dB) | $f_S$ = 352.8kHz | | –40 | –34 | dB |
| PCM67P-J/69AP-J, PCM67U-J/69AU-J | | | | | |
| f = 991Hz (0dB) | $f_S$ = 352.8kHz | | –91 | –88 | dB |
| f = 991Hz (–20dB) | $f_S$ = 352.8kHz | | –72 | | dB |
| f = 991Hz (–60dB) | $f_S$ = 352.8kHz | | –46 | –40 | dB |
| PCM67P-K/69AP-K, PCM67U-K/69AU-K | | | | | |
| f = 991Hz (0dB) | $f_S$ = 352.8kHz | | –95 | –92 | dB |
| f = 991Hz (–20dB) | $f_S$ = 352.8kHz | | –74 | | dB |
| f = 991Hz (–60dB) | $f_S$ = 352.8kHz | | –46 | –40 | dB |
| **CHANNEL SEPARATION** | (f = 1kHz) | | 106 | | dB |
| **ACCURACY** | | | | | |
| Level Linearity | at –90dB Signal Level | | ±1 | | dB |
| Gain Error | | | ±3 | ±10 | % |
| Gain Mismatch, Channel-to-Channel | | | ±1 | ±5 | % |
| Gain Drift | 0°C to +70°C | | 95 | | ppm/°C |
| Warm-up Time | | | 1 | | Minute |
| **IDLE CHANNEL SNR**[5] | 20Hz to 40kHz at BPZ[6] | | 110 | | dB |
| **ANALOG OUTPUT** | | | | | |
| Output Range (±3%) | | | 1.2 | | mA |
| Output Impedance (±30%) | | | 1.8 | | kΩ |
| $V_{COM}$ | | 3.35 | 3.50 | 3.65 | V |
| Glitch Energy | | | No Glitch Around Zero | | |
| **POWER SUPPLY REQUIREMENTS**, System Clock = 16.9344MHz | | | | | |
| $+V_A$, $+V_D$ Supply Voltage Range | $+V_A = +V_D$ | +4.75 | +5.00 | +5.25 | V |
| $+I_A$, $+I_D$ Combined Supply Current | $+V_A$, $+V_D$ = +5V | | 15 | 20 | mA |
| Power Dissipation | $+V_A$, $+V_D$ = +5V | | 75 | 105 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –25 | | +85 | °C |
| Storage | | –55 | | +100 | °C |

NOTES: (1) Binary Two's Complement coding. (2) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$)/$Signal_{RMS}$. (3) D/A converter output frequency/signal level (both left and right channels are "on"). (4) D/A converter sample frequency (8 x 44.1kHz; 8X oversampling per channel). (5) Ratio of $Noise_{RMS}$/$Signal_{RMS}$. Measured using a 40kHz 3rd-order GIC (Generalized Immittance Converter) filter and an A-weighted filter. (6) Bipolar Zero.



The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN ASSIGNMENTS

| PCM67P PCM69AP | PCM67U PCM69AU | DESCRIPTION | MNEMONIC |
|---|---|---|---|
| 1 | 1 | +5V Analog Supply Voltage | $+V_A$ |
| 2 | 2 | Left Voltage Common | $LV_{COM}$ |
| | 3 | No Connection | NC |
| 3 | 4 | Left Current Output (0 to 1.2mA) | $LI_{OUT}$ |
| 4 | 5 | Servo Decoupling Capacitor | SRVCAP |
| 5 | 6 | Reference Decoupling Capacitor | REFCAP |
| 6 | 7 | Right Current Output (0 to 1.2mA) | $RI_{OUT}$ |
| | 8 | No Connection | NC |
| 7 | 9 | Right Voltage Common | $RV_{COM}$ |
| 8 | 10 | Analog Common | ACOM |
| 9 | 11 | Digital Common | DCOM |
| | 12 | Mode Control 2 | MC2 |
| 10 | 13 | Right Data Input | RDATA |
| 11 | 14 | Bit Clock | BTCK |
| 12 | 15 | System Clock | SYSCK |
| 13 | 16 | Word Clock | WDCK |
| 14 | 17 | Left Data Input | LDATA |
| | 18 | Mode Control 3 | MC3 |
| 15 | 19 | Mode Control 1 | MC1 |
| 16 | 20 | +5V Digital Supply Voltage | $+V_D$ |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| PCM67P/69AP | 16-Pin Plastic DIP | 180 |
| PCM67U/69AU | 20-Pin SOIC | 248 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_A$, $+V_D$ to ACOM, DCOM | 0V to +6.5V |
| ACOM to DCOM | ±0.5V |
| Digital Inputs to DCOM | –0.3V to $+V_D$ + 0.3V |
| Power Dissipation | 300mW (U Package), 500mW (P Package) |
| Lead Temperature, (soldering, 10s) | +260°C |
| Max Junction Temperature | +165°C |

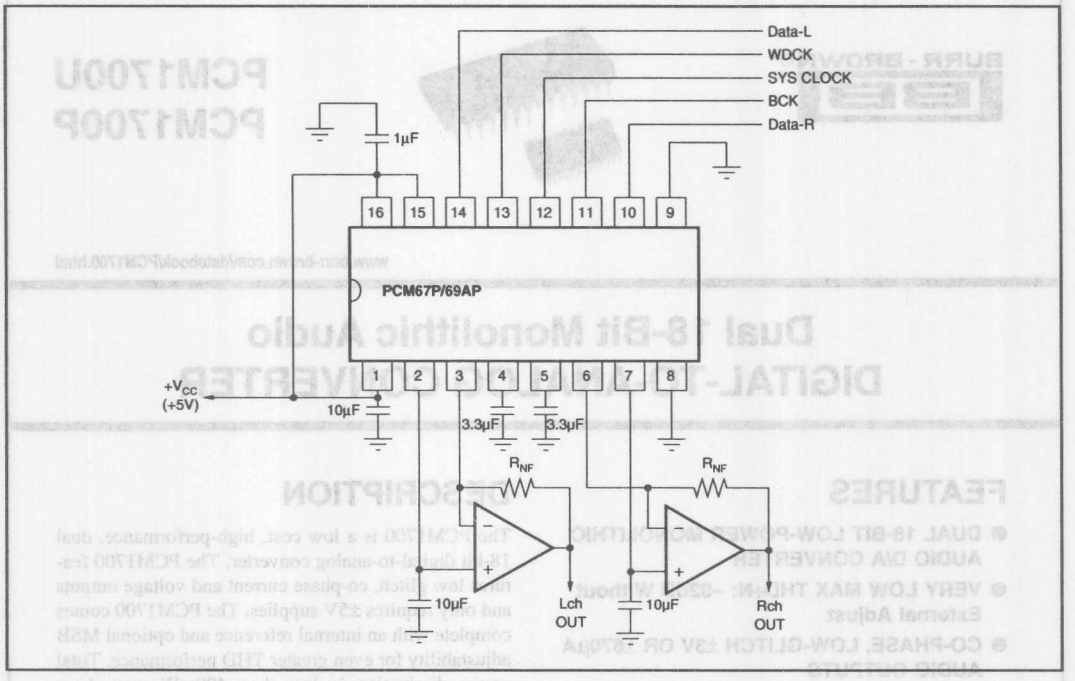
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTROSTATIC DISCHARGE SENSITIVITY

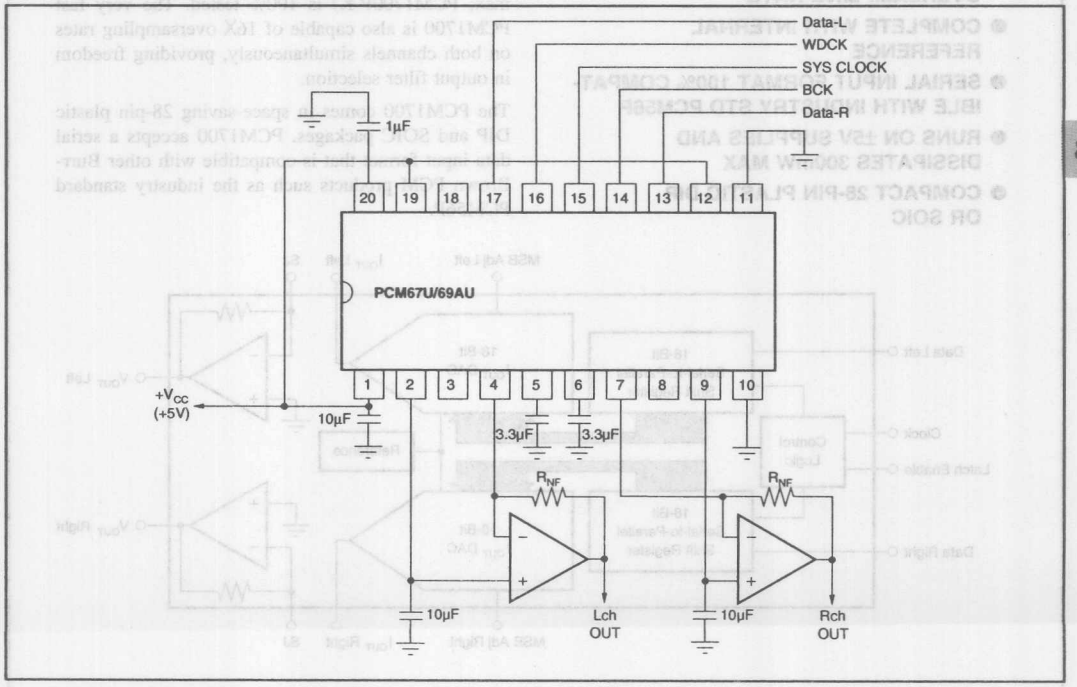
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

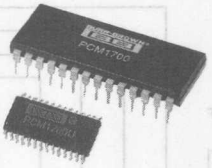
**PIN CONFIGURATION — PCM67P/69AP (16-Pin DIP)**




**PIN CONFIGURATION — PCM67U/69AU (20-Pin SOIC)**



BURR-BROWN®



# PCM1700U
# PCM1700P

www.burr-brown.com/databook/PCM1700.html

# Dual 18-Bit Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

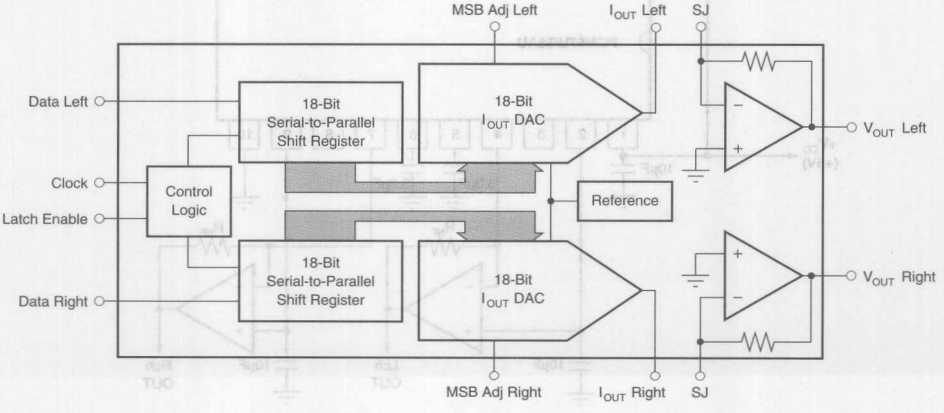
## FEATURES

- DUAL 18-BIT LOW-POWER MONOLITHIC AUDIO D/A CONVERTER
- VERY LOW MAX THD+N: –92dB Without External Adjust
- CO-PHASE, LOW-GLITCH ±3V OR ±670µA AUDIO OUTPUTS
- CAPABLE OF 16X PER CHANNEL OVERSAMPLING RATE
- COMPLETE WITH INTERNAL REFERENCE
- SERIAL INPUT FORMAT 100% COMPATIBLE WITH INDUSTRY STD PCM56P
- RUNS ON ±5V SUPPLIES AND DISSIPATES 300mW MAX
- COMPACT 28-PIN PLASTIC DIP OR SOIC

## DESCRIPTION

The PCM1700 is a low cost, high-performance, dual 18-bit digital-to-analog converter. The PCM1700 features low glitch, co-phase current and voltage outputs and only requires ±5V supplies. The PCM1700 comes complete with an internal reference and optional MSB adjustability for even greater THD performance. Total power dissipation is less than 400mW max. Low maximum Total Harmonic Distortion + Noise (–92dB max; PCM1700P-K) is 100% tested. The very fast PCM1700 is also capable of 16X oversampling rates on both channels simultaneously, providing freedom in output filter selection.

The PCM1700 comes in space-saving 28-pin plastic DIP and SOIC packages. PCM1700 accepts a serial data input format that is compatible with other Burr-Brown PCM products such as the industry standard PCM56P.




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# SPECIFICATIONS

## ELECTRICAL

At 25°C, and $\pm V_{CC}$ = ±5.00V, unless otherwise noted. Where relevant, specifications apply to both left and right input/output channels.

| PARAMETER | CONDITIONS | PCM1700U/U-J/U-K, PCM1700P/P-J/P-K MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | 18 | | | Bits |
| **DYNAMIC RANGE** | | | +108 | | dB |
| **INPUT** | | | | | |
| **DIGITAL INPUT** | | | | | |
| Logic Family | | | TTL Compatible | | |
| Logic Level: $V_{IH}$ | | +2 | | $+V_{DD}$ | V |
| $V_{IL}$ | | 0 | | +0.8 | V |
| $I_{IH}$ | $V_{IH}$ = +2.7V | | | +1 | µA |
| $I_{IL}$ | $V_{IL}$ = +0.4V | | | –50 | µA |
| Data Format | | | Serial BTC[1] | | |
| Input Clock Frequency | | 11.288 | 20 | | MHz |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| **TOTAL HARMONIC DISTORTION + N[6]** | | | | | |
| PCM1700_: | | | | | |
| f = 991kHz (0dB) | $f_S$ = 352.8kHz[4] | | –88 | –82 | dB |
| f = 991kHz (–20dB) | $f_S$ = 352.8kHz | | –74 | –68 | dB |
| $f_{IN}$ = 991kHz (–60dB) | $f_S$ = 352.8kHz | | –34 | –28 | dB |
| PCM1700_-J: | | | | | |
| f = 991kHz (0dB) | $f_S$ = 352.8kHz | | –94 | –88 | dB |
| f = 991kHz (–20dB) | $f_S$ = 352.8kHz | | –76 | –74 | dB |
| f = 991kHz (–60dB) | $f_S$ = 352.8kHz | | –36 | –34 | dB |
| PCM1700_-K: | | | | | |
| f = 991kHz (0dB) | $f_S$ = 352.8kHz | | –98 | –92 | dB |
| f = 991kHz (–20dB) | $f_S$ = 352.8kHz | | –80 | –74 | dB |
| f = 991kHz (–60dB) | $f_S$ = 352.8kHz | | –40 | –34 | dB |
| **CHANNEL SEPARATION** | | +96 | +108 | | dB |
| **SIGNAL-TO-NOISE RATIO[5]** | 20Hz to 20kHz at BPZ[6] | | +108 | | dB |
| **TRANSFER CHARACTERISTICS** | | | | | |
| **ACCURACY** | | | | | |
| Gain Error | | | ±1 | ±3 | % |
| Gain Mismatch | Channel to Channel | | ±1 | ±3 | % |
| Bipolar Zero Error | | | 10 | | mV |
| BPZ Error Mismatch | Channel to Channel | | 5 | | mV |
| BPZ Differential Linearity Error[7] | | | ±1 | | LSB |
| Gain Drift | | | 100 | | ppm/°C |
| Bipolar Zero Drift | | | 20 | | ppm of FSR/°C |
| Warm-up Time | | 1 | | | minute |
| **POWER SUPPLY REJECTION** | $\pm V_{CC}$ to $V_{OUT}$ | | +86 | | dB |
| **ANALOG OUTPUT** | | | | | |
| Voltage: Output Range | | | ±3 | | V |
| Output Impedance | | | 0.1 | | Ω |
| Current Output | | | ±2 | | mA |
| Capacitive Load Drive | $R_{LOAD}$ = 1.5kΩ | | TBD | | pF |
| Short Circuit Duration | | | Indefinite | | |
| Settling Time | | | Sufficient to Meet THD+N Specs | | |
| Glitch Energ | | | Meets All THD+N Specs Without External Output Deglitching | | |
| Current: Output Range | (±2%) | | ±670 | | µA |
| Output Impedance | (±2%) | | 1.67 | | kΩ |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| $\pm V_{CC}$ Supply Voltage | | +4.75 | +5.00 | +5.25 | V |
| Supply Current: $+I_{CC}$ | $+V_{CC}$ = +5.0V | | +18 | +30 | mA |
| $-I_{CC}$ | $-V_{CC}$ = –5.0V | | –42 | –65 | mA |
| Power Dissipation | $\pm V_{CC}$ = ±5.0V | | 280 | 475 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | 0 | | +70 | °C |
| Operating | | –30 | | +70 | °C |
| Storage | | –60 | | +100 | °C |

NOTES: (1) Binary Two's Complement coding. (6) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$) / $Signal_{RMS}$. (3) D/A converter input frequency/signal level on both left and right channels. (4) D/A converter sample frequency (8 X 44.1kHz; 8X oversampling per channel). (5) Ratio of $Noise_{RMS}$ / $Signal_{RMS}$. Measured using an A-weighted filter. (6) Bipolar zero. (7) Differential non-linearity at bipolar major carry input code. Measured in 16-bit LSBs. Adjustable to zero error.

## PIN ASSIGNMENTS (Plastic PKG)

| PIN | DESCRIPTION | MNEMONIC |
|---|---|---|
| 1 | –5V Analog Supply | $-V_{CC}$ |
| 2 | Left Channel Servo-Amp Decoupling Point | CAP |
| 3 | Left Channel MSB Adjustment | MSB ADJ (L) |
| 4 | No Connect | NC |
| 5 | Left Channel Bipolar Offset Decoupling Point | CAP |
| 6 | Left Channel Current Output | IOUT (L) |
| 7 | Left Channel Analog Common | ACOM |
| 8 | Left Channel Summing Junction | SJ (L) |
| 9 | Left Channel Voltage Output | VOUT (L) |
| 10 | No Connect | NC |
| 11 | +5V Digital Supply | $+V_{DD}$ |
| 12 | Left Channel Data Input | DATA |
| 13 | Clock Input | CLOCK |
| 14 | –5V Logic Supply | $-V_{DD}$ |
| 15 | Latch Enable Input | LE |
| 16 | Right Channel Data Input | DATA (R) |
| 17 | Digital Common | DCOM |
| 18 | No Connect | NC |
| 19 | Right Channel Voltage Output | VOUT (R) |
| 20 | Right Channel Summing Junction | SJ (R) |
| 21 | Right Channel Analog Common | ACOM |
| 22 | Right Channel Current Output | IOUT (R) |
| 23 | Right Channel Bipolar Offset Decoupling Point | CAP |
| 24 | Right Channel MSB Adjustment | MSB ADJ (R) |
| 25 | Right Channel Servo-Amp Decoupling Point | CAP |
| 26 | MSB Adjustment Potentiometer Voltage Output | VPOT |
| 27 | +5V Analog Supply | $+V_{CC}$ |
| 28 | Digital Common | DCOM |

## PIN ASSIGNMENTS (SOIC PKG)

| PIN | DESCRIPTION | MNEMONIC |
|---|---|---|
| 9 | –5V Analog Supply | $-V_{CC}$ |
| 10 | Left Channel Servo-Amp Decoupling Point | CAP |
| 11 | Left Channel MSB Adjustment | MSB ADJ (L) |
| 19 | No Connect | NC |
| 12 | Left Channel Bipolar Offset Decoupling Point | CAP |
| 13 | Left Channel Current Output | $I_{OUT}$ (L) |
| 14 | Left Channel Analog Common | ACOM |
| 15 | Left Channel Summing Junction | SJ (L) |
| 16 | Left Channel Voltage Output | $V_{OUT}$ (L) |
| 17 | No Connect | NC |
| 18 | +5V Digital Supply | $+V_{DD}$ |
| 20 | Left Channel Data Input | DATA |
| 21 | Clock Input | CLOCK |
| 22 | –5V Logic Supply | $-V_{DD}$ |
| 23 | Latch Enable Input | LE |
| 24 | Right Channel Data Input | DATA (R) |
| 25 | Digital Common | DCOM |
| 26 | No Connect | NC |
| 27 | Right Channel Voltage Output | $V_{OUT}$ (R) |
| 28 | Right Channel Summing Junction | SJ (R) |
| 1 | Right Channel Analog Common | ACOM |
| 2 | Right Channel Current Output | $I_{OUT}$ (R) |
| 3 | Right Channel Bipolar Offset Decoupling Point | CAP |
| 4 | Right Channel MSB Adjustment | MSB ADJ (R) |
| 5 | Right Channel Servo-Amp Decoupling Point | CAP |
| 6 | MSB Adjustment Potentiometer Voltage Output | $V_{POT}$ |
| 7 | +5V Analog Supply | $+V_{DD}$ |
| 8 | Digital Common | DCOM |

NOTE: In the SOIC (PCM1700U) package, the die is rotated 90°. Therefore, the pin assignments are different from the DIP. See pin assignments on page 4 for details.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| DC Supply Voltages | ±7.5VDC |
| Input Logic Voltage | –1V to $+V_{CC}$ |
| Power Dissipation | 500mW |
| Operating Temperature | –25°C to +70°C |
| Storage Temperature | –60°C to +100°C |
| Lead Temperature (soldering, 10s) | +300°C |

## ORDERING INFORMATION

PCM1700 ( ) ( )

Basic model Number
P: Plastic U: SOIC
Performance Grade Code

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| PCM1700U | 28-Lead SOIC | 217 |
| PCM1700U-J | 28-Lead SOIC | 217 |
| PCM1700U-K | 28-Lead SOIC | 217 |
| PCM1700P | 28-Pin Plastic DIP | 126 |
| PCM1700P-J | 28-Pin Plastic DIP | 126 |
| PCM1700P-K | 28-Pin Plastic DIP | 126 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

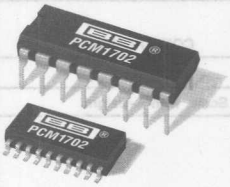
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# PCM1702P
# PCM1702U

www.burr-brown.com/databook/PCM1702.html

# BiCMOS Advanced Sign Magnitude 20-Bit DIGITAL-TO-ANALOG CONVERTER

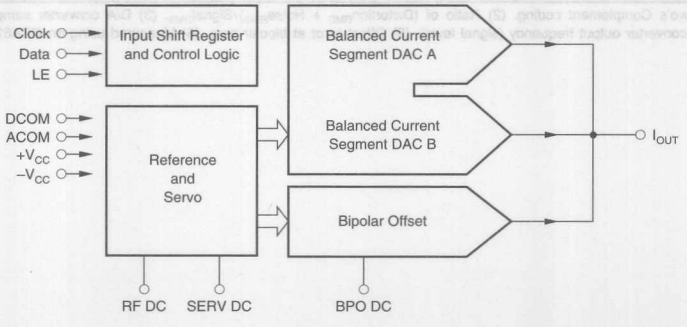
## FEATURES

- ULTRA LOW –96dB max THD+N (No External Adjustment Required)
- NEAR-IDEAL LOW LEVEL OPERATION
- GLITCH-FREE OUTPUT
- 120dB SNR TYP (A-Weight Method)
- INDUSTRY STD SERIAL INPUT FORMAT
- FAST (200ns) CURRENT OUTPUT (±1.2mA)
- CAPABLE OF 16X OVERSAMPLING
- COMPLETE WITH REFERENCE
- LOW POWER (150mW typ)

## DESCRIPTION

The PCM1702 is a precision 20-bit digital-to-analog converter with ultra-low distortion (–96dB typ with a full scale output). Incorporated into the PCM1702 is an advanced sign magnitude architecture that eliminates unwanted glitches and other nonlinearities around bipolar zero. The PCM1702 also features a very low noise (120dB typ SNR: A-weighted method) and fast settling current output (200ns typ, 1.2mA step) which is capable of 16X oversampling rates.

Applications include very low distortion frequency synthesis and high-end consumer and professional digital audio applications.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

All specifications at 25°C, $\pm V_{CC}$ and $+V_{DD} = \pm 5V$, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1702P/U, -J, -K MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | 20 | | | Bits |
| **DYNAMIC RANGE, THD + N at –60dB Referred to Full Scale, with A-weight** | | | 110 | | dB |
| **DIGITAL INPUT** | | | | | |
| Logic Family | | | TTL/CMOS Compatible | | |
| Logic Level: $V_{IH}$ | | +2.4 | | $+V_{DD}$ | V |
| $V_{IL}$ | | 0 | | 0.8 | V |
| $I_{IH}$ | $V_{IH} = +V_{DD}$ | | | ±10 | µA |
| $I_{IL}$ | $V_{IL} = 0V$ | | | ±10 | µA |
| Data Format | | | Serial, MSB First, BTC[1] | | |
| Input Clock Frequency | | | 12.5 | 20.0 | MHz |
| **TOTAL HARMONIC DISTORTION + N[2]** | | | | | |
| P/U $V_O$ = 0dB | $f_S$ = 352.8kHz[3], f = 1002Hz[4] | | –92 | –88 | dB |
| $V_O$ = –20dB | $f_S$ = 352.8kHz[3], f = 1002Hz[4] | | –82 | –74 | dB |
| $V_O$ = –60dB | $f_S$ = 352.8kHz[3], f = 1002Hz[4] | | –46 | –40 | dB |
| P/U, -J $V_O$ = 0dB | $f_S$ = 352.8kHz[3], f = 1002Hz[4] | | –96 | –92 | dB |
| $V_O$ = –20dB | $f_S$ = 352.8kHz[3], f = 1002Hz[4] | | –83 | –76 | dB |
| $V_O$ = –60dB | $f_S$ = 352.8kHz[3], f = 1002Hz[4] | | –48 | –42 | dB |
| P/U, -K $V_O$ = 0dB | $f_S$ = 352.8kHz[3], f = 1002Hz[4] | | –100 | –96 | dB |
| $V_O$ = –20dB | $f_S$ = 352.8kHz[3], f = 1002Hz[4] | | –84 | –80 | dB |
| $V_O$ = –60dB | $f_S$ = 352.8kHz[3], f = 1002Hz[4] | | –50 | –44 | dB |
| **ACCURACY** | | | | | |
| Level Linearity | At –90dB Signal Level | | ±0.5 | | dB |
| Gain Error | | | ±0.5 | ±3 | % |
| Bipolar Zero Error[5] | | | ±0.25 | | % |
| Gain Drift | 0°C to 70°C | | ±25 | | ppm of FSR/°C |
| Bipolar Zero Drift | 0°C to 70°C | | ±5 | | ppm of FSR/°C |
| Warm-up Time | | | 1 | | minute |
| **IDLE CHANNEL SNR[6]** | Bipolar Zero, A-weighted Filter | 110 | 120 | | dB |
| **ANALOG OUTPUT** | | | | | |
| Output Range | | | ±1.2 | | mA |
| Output Impedance | | | 1.0 | | kΩ |
| Settling Time | (±0.003% of FSR, 1.2mA Step) | | 200 | | ns |
| Glitch Energy | | | No Glitch Around Zero | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Supply Voltage Range: $+V_{CC} = +V_{DD}$ | | +4.75 | +5.00 | +5.25 | V |
| $-V_{CC} = -V_{DD}$ | | –4.75 | –5.00 | –5.25 | V |
| Combined Supply Current: $+I_{CC}$ | $+V_{CC} = +V_{DD} = +5V$ | | +5.00 | +9.0 | mA |
| Combined Supply Current: $-I_{CC}$ | $-V_{CC} = -V_{DD} = -5V$ | | –25.00 | –41.0 | mA |
| Power Dissipation | $\pm V_{CC} = \pm V_{DD} = \pm 5V$ | | 150 | 250 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –25 | | +85 | °C |
| Storage | | –55 | | +125 | °C |

NOTES: (1) Binary Two's Complement coding. (2) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$)/$Signal_{RMS}$. (3) D/A converter sample frequency (8 x 44.1kHz; 8x oversampling). (4) D/A converter output frequency (signal level). (5) Offset error at bipolar zero. (6) Measured using an OPA627 and 5kΩ feedback and an A-weighted filter.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## ABSOLUTE MAXIMUM RATINGS (DIP Package)

| | |
|---|---|
| Power Supply Voltage | ±6.5VDC |
| Input Logic Voltage | DGND—0.3V~+$V_{DD}$+0.3V |
| Operating Temperature | –25°C to +85°C |
| Storage Temperature | –55°C to +125°C |
| Power Dissipation | 500mW |
| Lead Temperature (soldering, 10s) | 260°C |

## ABSOLUTE MAXIMUM RATINGS (SOP Package)

| | |
|---|---|
| Power Supply Voltage | ±6.5VDC |
| Input Logic Voltage | DGND—0.3V~+$V_{DD}$+0.3V |
| Operating Temperature | –25°C to +85°C |
| Storage Temperature | –55°C to +125°C |
| Power Dissipation | 300mW |
| Lead Temperature (soldering, 5s) | 260°C |

## PIN ASSIGNMENTS (DIP Package)

| PIN | MNEMONIC | PIN | MNEMONIC |
|---|---|---|---|
| 1 | DATA | 9 | +$V_{CC}$ |
| 2 | CLOCK | 10 | BPO DC |
| 3 | +$V_{DD}$ | 11 | $I_{OUT}$ |
| 4 | DCOM | 12 | ACOM |
| 5 | –$V_{DD}$ | 13 | ACOM |
| 6 | LE | 14 | SERV DC |
| 7 | NC | 15 | REF DC |
| 8 | NC | 16 | –$V_{CC}$ |

## PIN ASSIGNMENTS (SOP Package)

| PIN | MNEMONIC | PIN | MNEMONIC |
|---|---|---|---|
| 1 | DATA | 11 | +$V_{CC}$ |
| 2 | CLOCK | 12 | BPO DC |
| 3 | NC | 13 | NC |
| 4 | +$V_{DD}$ | 14 | $I_{OUT}$ |
| 5 | DCOM | 15 | ACOM |
| 6 | –$V_{DD}$ | 16 | ACOM |
| 7 | LE | 17 | SERV DC |
| 8 | NC | 18 | NC |
| 9 | NC | 19 | RFE DC |
| 10 | NC | 20 | –$V_{CC}$ |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| PCM1702P | 16-Pin Plastic DIP | 180 |
| PCM1702U | 20-Pin Plastic SOP | 248 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## GRADE MARKING (SOP Package)

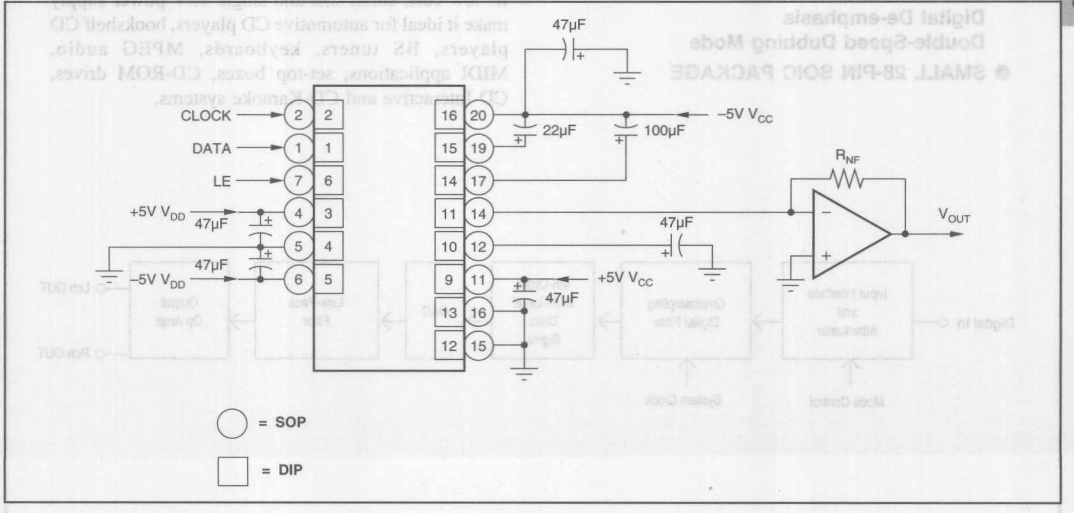
| PRODUCT | PACKAGE |
|---|---|
| PCM1702U | Marked PCM1702. |
| PCM1702U-J | Marked with white dot by pin 10. |
| PCM1702U-K | Marked with red dot by pin 10. |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## CONNECTION DIAGRAM



BURR-BROWN®




# PCM1710U

www.burr-brown.com/databook/PCM1710.html

## SoundPLUS Stereo Audio DIGITAL-TO-ANALOG CONVERTER

## FEATURES

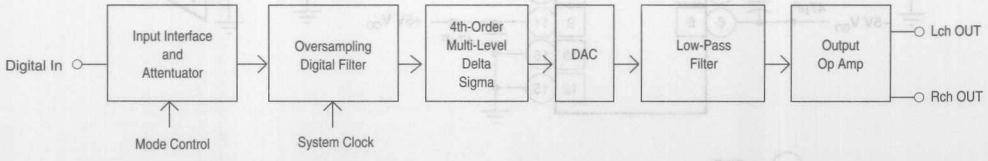
- **COMPLETE STEREO DAC:**
  **8X Oversampling Digital Filter**
  **Multi-Level Delta-Sigma DAC**
  **Analog Low Pass Filter**
  **Output Amplifier**
- **HIGH PERFORMANCE:**
  **–92dB THD+N**
  **98dB Dynamic Range**
  **110dB SNR**
- **ACCEPTS 16 OR 20 BITS INPUT DATA**
- **SYSTEM CLOCK: 256fs or 384fs**
- **SINGLE +5V POWER SUPPLY**
- **ON-CHIP DIGITAL FILTER:**
  **Soft Mute and Attenuator**
  **Digital De-emphasis**
  **Double-Speed Dubbing Mode**
- **SMALL 28-PIN SOIC PACKAGE**

## DESCRIPTION

The PCM1710 is a complete stereo audio digital-to-analog converter, including digital interpolation filter, delta-sigma DAC, and analog voltage output. PCM1710 can accept either 16-bit normal or 20-Bit normal input data (MSB first, right justified), or 16-bit IIS data (32-bits per word, continuous clock).

The digital filter performs an 8X interpolation function, as well as special functions such as soft mute, digital attenuation, de-emphasis and double-speed dubbing. Performance of the digital feature is excellent, featuring –62dB stop band attenuation and ±0.008dB ripple in the pass band.

PCM1710 is suitable for a wide variety of consumer applications where good performance is required. Its low cost, small size and single +5V power supply make it ideal for automotive CD players, bookshelf CD players, BS tuners, keyboards, MPEG audio, MIDI applications, set-top boxes, CD-ROM drives, CD-Interactive and CD-Karaoke systems.




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# SPECIFICATIONS

All specifications at +25°C, $+V_{CC} = +V_{DD} = +5V$, $f_S = 44.1kHz$, $f_{SYS} = 384/256fs$, and 16-bit data, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1710U MIN | PCM1710U TYP | PCM1710U MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | 16 | | 20 | Bits |
| **DIGITAL INPUT** | | | | | |
| Logic Family | | | | | |
| Input Logic Level (except XTI) | | | | | |
| $V_{IH}$ | | 2.0 | | | VDC |
| $V_{IL}$ | | | | 0.8 | VDC |
| Input Logic Current (except XTI) | | | | –200 | µA |
| Input Logic Level (XTI) | | | | | |
| $V_{IH}$ | | 3.2 | | | VDC |
| $V_{IL}$ | | | | 1.4 | VDC |
| Input Logic Current (XTI) | | | | ±50 | µA |
| Output Logic Level (CLKO): | | | | | |
| $V_{OH}$ | | 4.5 | | | VDC |
| $V_{OL}$ | | | | 0.5 | VDC |
| Output Logic Current (CLKO) | | | ±10 | | mA |
| Data Format | Normal (16/20-bit)/IIS (16-bit) selectable | | | | |
| Sampling Frequency | | 32 | 44.1 | 48 | kHz |
| System Clock Frequency | $384f_S$ | 12.288 | 16.934 | 18.432 | MHz |
| System Clock Frequency | $256f_S$ | 8.192 | 11.2894 | 12.288 | MHz |
| **DC ACCURACY** | | | | | |
| Gain Error | | | ±1.0 | ±5.0 | % of FSR |
| Gain Mis-Match Channel-To-Channel | | | ±1.0 | ±5.0 | % of FSR |
| Bipolar Zero Error | $V_O = 1/2V_{CC}$ at Bipolar Zero | | ±20.0 | | mV |
| Gain Drift | | | ±50 | | ppm of FSR/°C |
| Bipolar Gain Drift | | | ±20 | | ppm of FSR/°C |
| **DYNAMIC PERFORMANCE**(1) | | | | | |
| THD+N at F/S (0dB)(2) | $f_{IN} = 991kHz$ | | –92 | –88 | dB |
| THD+N at –60fdB(2) | $f_{IN} = 991kHz$ | | –36 | –32 | dB |
| Dynamic Range | EIAJ A-weighted | | 98 | | dB |
| S/N Ratio | EIAJ A-weighted | 104 | 110 | | dB |
| Channel Separation | | 90 | 94 | | dB |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Pass Band Ripple | Normal Mode | | | ±0.008 | dB |
| Pass Band Ripple | Double Speed Mode | | | ±0.018 | dB |
| Stop Band Attenuation | Normal Mode | –62 | | | dB |
| Stop Band Attenuation | Double Speed Mode | –58 | | | dB |
| Pass Band | Normal Mode | | | 0.4535 | fs |
| Pass Band | Double Speed Mode | | | 0.4535 | fs |
| Stop Band | Normal Mode | | | 0.5465 | fs |
| Stop Band | Double Speed Mode | | | 0.5465 | fs |
| De-emphasis Error | ($f_S$ 32kHz ~ 48kHz) | –0.05 | | +0.03 | dB |
| **ANALOG OUTPUT** | | | | | |
| Voltage Range | | | 3.2 | | Vp-p |
| Load Impedance | | 5 | | | kΩ |
| Center Voltage | | | $+1/2V_{CC}$ | | V |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range: $+V_{CC}$ | | +4.5 | +5.0 | +5.5 | VDC |
| $+V_{DD}$ | | +4.5 | +5.0 | +5.5 | VDC |
| Supply Current $(+I_{CC}) + (+I_{DD})$ | | | 45 | 70 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Operation | | –25 | | +85 | °C |
| Storage | | –55 | | +100 | °C |

NOTE: (1) Dynamic performance specs are tested with external 20kHz low pass filter. (2) 30kHz LPF, 400Hz HPF, Average Mode. Shibusoku #725 THD Meter.



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## PIN ASSIGNMENTS

| PIN NAME | NUMBER | FUNCTION |
|---|---|---|
| **Input Interface Pins** | | |
| LRCIN | 1 | Sample Rate Clock Input. Controls the update rate (fs). |
| DIN | 2 | Serial Data Input. MSB first, right justified format contains a frame of 16-bit or 20-bit data. |
| BCKIN | 3 | Bit Clock Input. Clocks in the data present on DIN input. |
| **Mode Controls and Clock Signals** | | |
| CLKO | 4 | Buffered Output of Oscillator. Equivalent to fs. |
| XTI | 5 | Oscillator Input (External Clock Input). For an internal clock, tie XTI to one side of the crystal oscillator. For an external clock, tie XTI to the output of the chosen external clock. |
| XTO | 6 | Oscillator Output. When using the internal clock, tie to the opposite side (from pin 5) of the crystal oscillator. When using an external clock, leave XTO open. |
| CKSL | 23 | System Clock Select. For 384fs, tie CKSL "High". For 256fs, tie CKSL "Low". |
| MODE | 24 | Operation Mode Select. For serial mode, tie MODE "High". For parallel mode, tie MODE "Low". |
| MUTE | 25 | Mute Control. To disable soft mute, tie MUTE "High". To enable soft mute, tie MUTE "Low". |
| MD/DM1 | 26 | Mode Control for Data/De-emphasis. See "Mode Control Functions" on page 11. |
| MC/DM2 | 27 | Mode Control for BCKIN/De-emphasis. See "Mode Control Functions" on page 11. |
| ML/DSD | 28 | Mode Control for WDCK/Double speed dubbing. See "Mode Control Functions" on page 11. |
| **Analog Functions** | | |
| $V_{OUT}R$ | 13 | Right Channel Analog Output. |
| $V_{OUT}L$ | 16 | Left Channel Analog Output. |
| **Power Supply Connections** | | |
| DGND | 7, 22 | Digital Ground. |
| $V_{DD}$ | 8, 21 | Digital Power Supply (+5V). |
| $V_{CC}2R$ | 9 | Analog Power Supply (+5V), Right Channel DAC. |
| AGND2R | 10 | Analog Ground (DAC), Right Channel. |
| EXT1R | 11 | Output Amplifier Common, Right Channel. Bypass to ground with a 10µF capacitor. |
| EXT2R | 12 | Output Amplifier Bias, Right Channel. Connect to EXT1R. |
| AGND | 14 | Analog Ground. |
| $V_{CC}$ | 15 | Analog Power Supply (+5V). |
| EXT2L | 17 | Output Amplifier Bias, Left Channel. Connect to EXT1L. |
| EXT1L | 18 | Output Amplifier Common, Left Channel. Bypass to ground with a 10µF capacitor. |
| AGND2L | 19 | Analog Ground (DAC), Left Channel. |
| $V_{CC}2L$ | 20 | Analog Power Supply (+5V), Left Channel DAC. |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltages | ±6.5VDC |
| $+V_{CC}$ to $V_{DD}$ Voltage | ±0.1V |
| Input Logic Voltage | –0.3V to $V_{DD}$ +0.3V |
| Power Dissipation | 400mW |
| Operating Temperature Range | –25°C to +85°C |
| Storage Temperature Range | –55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| PCM1710U | 28-Pin SOIC | 217 |

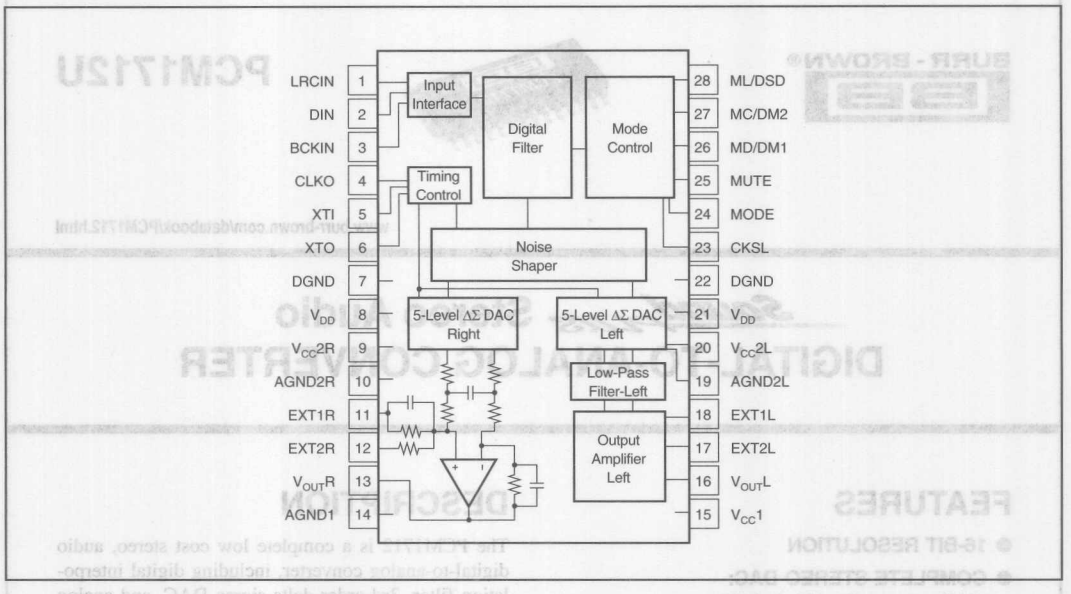
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

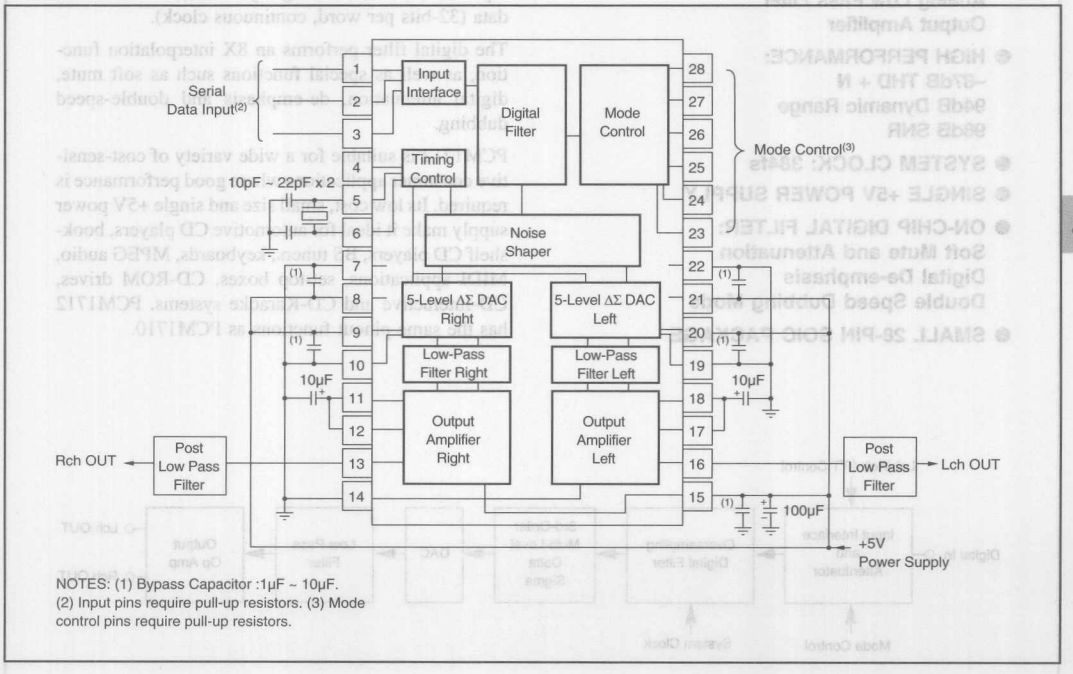
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN CONFIGURATION




## CONNECTION DIAGRAM



BURR - BROWN®




# PCM1712U

www.burr-brown.com/databook/PCM1712.html

## *Sound PLUS* Stereo Audio DIGITAL-TO-ANALOG CONVERTER

## FEATURES

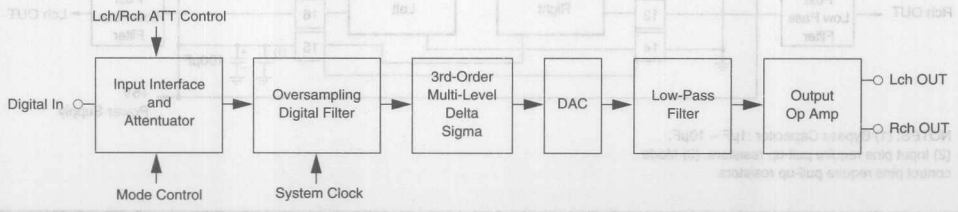
- **16-BIT RESOLUTION**
- **COMPLETE STEREO DAC:**
  **8X Oversampling Digital Filter**
  **Multi-Level Delta-Sigma DAC**
  **Analog Low Pass Filter**
  **Output Amplifier**
- **HIGH PERFORMANCE:**
  **–87dB THD + N**
  **94dB Dynamic Range**
  **98dB SNR**
- **SYSTEM CLOCK: 384fs**
- **SINGLE +5V POWER SUPPLY**
- **ON-CHIP DIGITAL FILTER:**
  **Soft Mute and Attenuation**
  **Digital De-emphasis**
  **Double Speed Dubbing Mode**
- **SMALL 28-PIN SOIC PACKAGE**

## DESCRIPTION

The PCM1712 is a complete low cost stereo, audio digital-to-analog converter, including digital interpolation filter, 3rd-order delta-sigma DAC, and analog output amplifiers. PCM1712 accepts 16-bit normal input data (MSB first, right justified), or 16-bit IIS data (32-bits per word, continuous clock).

The digital filter performs an 8X interpolation function, as well as special functions such as soft mute, digital attenuation, de-emphasis and double-speed dubbing.

PCM1712 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required. Its low cost, small size and single +5V power supply make it ideal for automotive CD players, bookshelf CD players, BS tuners, keyboards, MPEG audio, MIDI applications, set-top boxes, CD-ROM drives, CD-Interactive and CD-Karaoke systems. PCM1712 has the same pinout functions as PCM1710.




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# SPECIFICATIONS

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, $f_S$ = 44.1kHz, and 16-bit data, SYSCLK = 384fs, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1712U MIN | PCM1712U TYP | PCM1712U MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | 16 | | Bits |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic Family | | | | | |
| Input Logic Level (pins 1 to 3) | | | | | |
| $V_{IH}$ | | 2.0 | | | VDC |
| $V_{IL}$ | | | | 0.8 | VDC |
| Input Logic Current (pins 1 to 3) | | | | | |
| $I_I$ | | | | –200 | µA |
| Input Logic Level (pins 24 to 28) | | | | | |
| $V_{IH}$ | | 3.5 | | | VDC |
| $V_{IL}$ | | | | 1.5 | VDC |
| Input Logic Level (pins 24 to 28) | | | | | |
| $I_I$ | | | | –200 | µA |
| Input Logic Level (XTI) | | | | | |
| $V_{IH}$ | | 3.2 | | | VDC |
| $V_{IL}$ | | | | 1.4 | VDC |
| Input Logic Current (XTI) | | | | | |
| $I_I$ | | | | –120 | µA |
| Output Logic Level (CLKO): | | | | | |
| $V_{OH}$ | | 4.5 | | | VDC |
| $V_{OL}$ | | | | 0.5 | VDC |
| Output Logic Current | | | | | |
| $I_O$ | | ±10 | | | mA |
| Data Format | | Normal/IIS (see Timing) SELECTABLE | | | |
| Data Bit | | 16-Bit/MSB First, Two's Complement | | | |
| Sampling Frequency | | 32 | 44.1 | 48 | kHz |
| System Clock Frequency | 384fs | 12.288 | 16.934 | 18.432 | MHz |
| **DC ACCURACY** | | | | | |
| Gain Error | | | ±1.0 | ±5.0 | % of FSR |
| Gain Mis-Match Channel-To-Channel | | | ±1.0 | ±5.0 | % of FSR |
| Bipolar Zero Error | $V_O$ = 1/2$V_{CC}$ at Bipolar Zero | | ±20 | | mV |
| Gain Drift | | | ±50 | | ppm of FSR/°C |
| Bipolar Gain Drift | | | ±20 | | ppm of FSR/°C |
| **DYNAMIC PERFORMANCE**(1) | | | | | |
| THD+N at F/S (0dB) | $f_{IN}$ = 991Hz | –82 | –87 | | dB |
| THD+N at –60fdB | $f_{IN}$ = 991kHz | | –34 | | dB |
| Dynamic Range | EIAJ A-weighted | | 94 | | dB |
| S/N Ratio | EIAJ A-weighted | 92 | 98 | | dB |
| Channel Separation | $f_{IN}$ = 991Hz | 90 | 96 | | dB |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Pass Band Ripple | Normal Mode | | | ±0.17 | dB |
| Pass Band Ripple | Double Speed Mode | | | ±0.22 | dB |
| Stop Band Attenuation | Normal Mode | –35 | | | dB |
| Stop Band Attenuation | Double Speed Mode | –34 | | | dB |
| Pass Band | Normal Mode | | 0.4535 | | fs |
| Pass Band | Double Speed Mode | | 0.4535 | | fs |
| Stop Band | Normal Mode | | 0.5465 | | fs |
| Stop Band | Double Speed Mode | | 0.5465 | | fs |
| De-emphasis Error | ($f_S$ 32kHz ~ 48kHz) | –0.2 | | +0.55 | dB |
| **ANALOG OUTPUT** | | | | | |
| Voltage Range | | | 3.1 | | Vp-p |
| Load Impedance | | 5k | | | Ω |
| Center Voltage | | | +1/2$V_{CC}$ | | V |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range: $+V_{CC}$ | | +4.5 | +5.0 | +5.5 | VDC |
| $+V_{DD}$ | | +4.5 | +5.0 | +5.5 | VDC |
| Supply Current $+I_{CC}$ $+I_{DD}$ | $+V_{CC}$ = $+V_{DD}$ = +5.0V | | 28 | 40 | mA |
| Power Dissipation | $+V_{CC}$ = $+V_{DD}$ = +5.0V | | 140 | 200 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Operation | | –25 | | +85 | °C |
| Storage | | –55 | | +100 | °C |

NOTE: (1) Tested with Shibasoku #725 THD. Meter 400Hz HPF, 30kHz LPF On, Average Mode with 20kHz bandwidth limiting.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN ASSIGNMENTS

| PIN NAME | NUMBER | FUNCTION |
|---|---|---|
| **Input Interface Pins** | | |
| LRCIN | 1 | Sample Rate Clock Input. Controls the update rate (fs). |
| DIN | 2 | Serial Data Input. MSB first, right justified format contains a frame of 16-bit or 20-bit data. |
| BCKIN | 3 | Bit Clock Input. Clocks in the data present on DIN input. |
| **Mode Controls and Clock Signals** | | |
| CLKO | 4 | Buffered Output of Oscillator. Equivalent to fs. |
| XTI | 5 | Oscillator Input (External Clock Input). For an internal clock, tie XTI to one side of the crystal oscillator. For an external clock, tie XTI to the output of the chosen external clock. |
| XTO | 6 | Oscillator Output. When using the internal clock, tie to the opposite side (from pin 5) of the crystal oscillator. When using an external clock, leave XTO open. |
| MODE | 24 | Operation Mode Select. For serial mode, tie MODE "High". For parallel mode, tie MODE "Low". |
| MUTE | 25 | Mute Control. To disable soft mute, tie MUTE "High". To enable soft mute, tie MUTE "Low". |
| MD/DM1 | 26 | Mode Control for Data/De-emphasis. See "Mode Control Functions" on page 10. |
| MC/DM2 | 27 | Mode Control for BCKIN/De-emphasis. See "Mode Control Functions" on page 10. |
| ML/DSD | 28 | Mode Control for WDCK/Double speed dubbing. See "Mode Control Functions" on page 10. |
| **Analog Functions** | | |
| $V_{OUT}R$ | 13 | Right Channel Analog Output. |
| $V_{OUT}L$ | 16 | Left Channel Analog Output. |
| **Power Supply Connections** | | |
| DGND | 7, 22 | Digital Ground. |
| $V_{DD}$ | 8, 21 | Digital Power Supply (+5V). |
| $V_{CC}2R$ | 9 | Analog Power Supply (+5V), Right Channel DAC. |
| AGND2R | 10 | Analog Ground (DAC), Right Channel. |
| EXT1R | 11 | Output Amplifier Common, Right Channel. Bypass to ground with a 10µF capacitor. |
| EXT2R | 12 | Output Amplifier Bias, Right Channel. Connect to EXT1R. |
| AGND | 14 | Analog Ground. |
| $V_{CC}$ | 15 | Analog Power Supply (+5V). |
| EXT2L | 17 | Output Amplifier Bias, Left Channel. Connect to EXT1L. |
| EXT1L | 18 | Output Amplifier Common, Left Channel. Bypass to ground with a 10µF capacitor. |
| AGND2L | 19 | Analog Ground (DAC), Left Channel. |
| $V_{CC}2L$ | 20 | Analog Power Supply (+5V), Left Channel DAC. |
| NC | 23 | No Connection. |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | +6.5V |
| $+V_{CC}$ to $V_{DD}$ Voltage | ±0.1V |
| Input Logic Voltage | $-0.3V$~$V_{DD}+0.3V$ |
| Power Dissipation | 300mW |
| Operating Temperature Range | –25°C to +85°C |
| Storage Temperature Range | –55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| PCM1712U | 28-Pin SOIC | 217 |

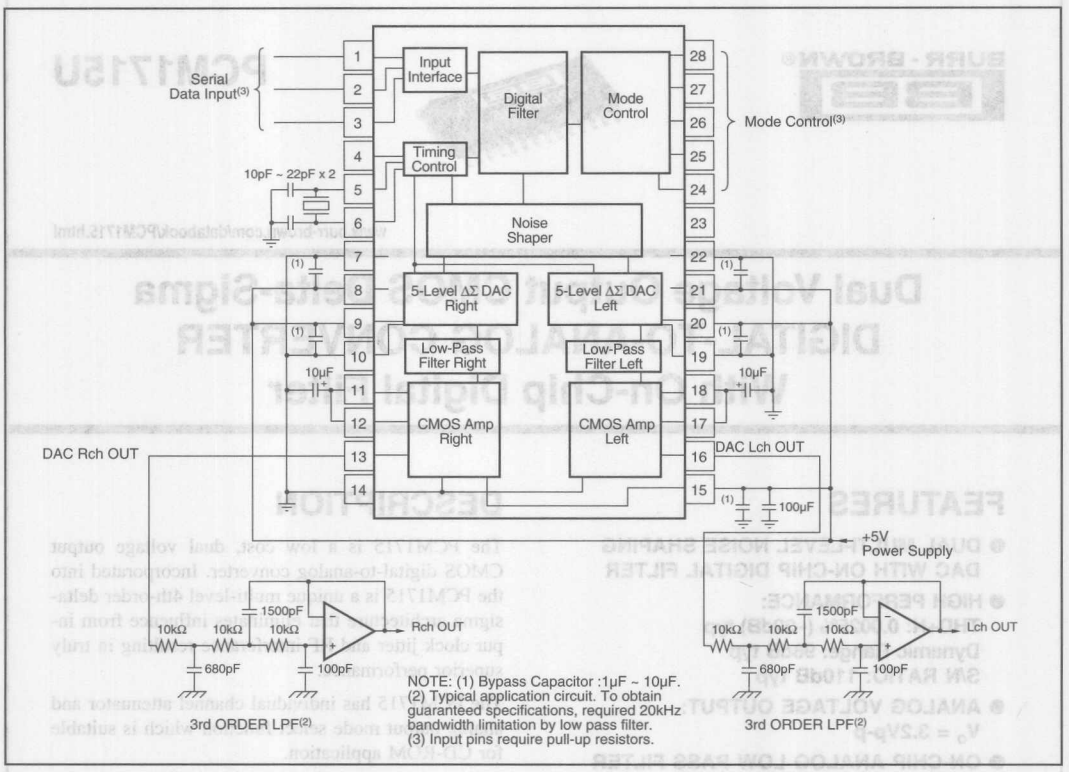
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

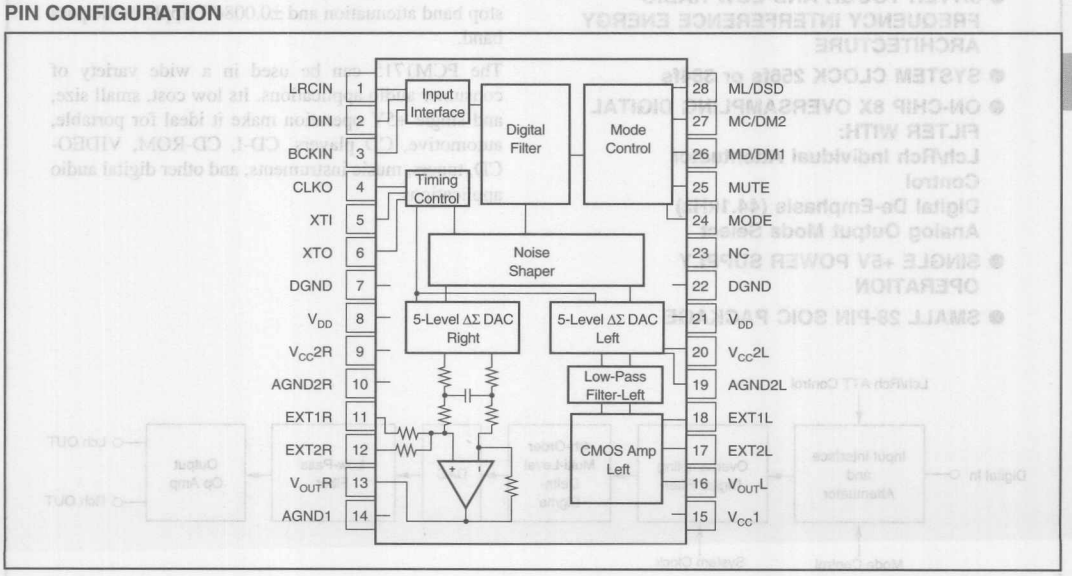
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## CONNECTION DIAGRAM




## PIN CONFIGURATION



BURR - BROWN®




# PCM1715U

www.burr-brown.com/databook/PCM1715.html

# Dual Voltage Output CMOS Delta-Sigma DIGITAL-TO-ANALOG CONVERTER With On-Chip Digital Filter

## FEATURES

- DUAL MULTI-LEVEL NOISE SHAPING DAC WITH ON-CHIP DIGITAL FILTER
- HIGH PERFORMANCE:
  THD+N: 0.0025% (–92dB) typ
  Dynamic Range: 98dB typ
  S/N RATIO: 110dB typ
- ANALOG VOLTAGE OUTPUT:
  $V_O$ = 3.2Vp-p
- ON-CHIP ANALOG LOW PASS FILTER
- JITTER TOUGH AND LOW RADIO FREQUENCY INTERFERENCE ENERGY ARCHITECTURE
- SYSTEM CLOCK 256fs or 384fs
- ON-CHIP 8X OVERSAMPLING DIGITAL FILTER WITH:
  Lch/Rch Individual Attentuator Control
  Digital De-Emphasis (44.1kHz)
  Analog Output Mode Select
- SINGLE +5V POWER SUPPLY OPERATION
- SMALL 28-PIN SOIC PACKAGE

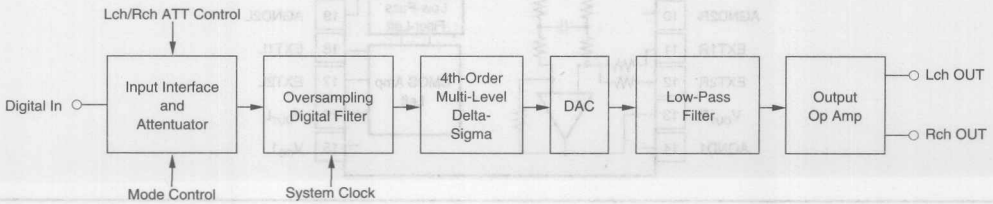
## DESCRIPTION

The PCM1715 is a low cost, dual voltage output CMOS digital-to-analog converter. Incorporated into the PCM1715 is a unique multi-level 4th-order delta-sigma architecture that eliminates influence from input clock jitter and RF interferance resulting in truly superior performance.

The PCM1715 has individual channel attenuator and analog output mode select function which is suitable for CD-ROM application.

The on-chip digital filter of the PCM1715 has –62dB stop band attenuation and ±0.008dB ripple in the pass band.

The PCM1715 can be used in a wide variety of consumer audio applications. Its low cost, small size, and single +5V operation make it ideal for portable, automotive, CD players, CD-I, CD-ROM, VIDEO-CD, tuners, music instruments, and other digital audio applications.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, fs = 44.1kHz, SYSCLK = 384fs/256fs, and 16-bit data, unless otherwise noted.

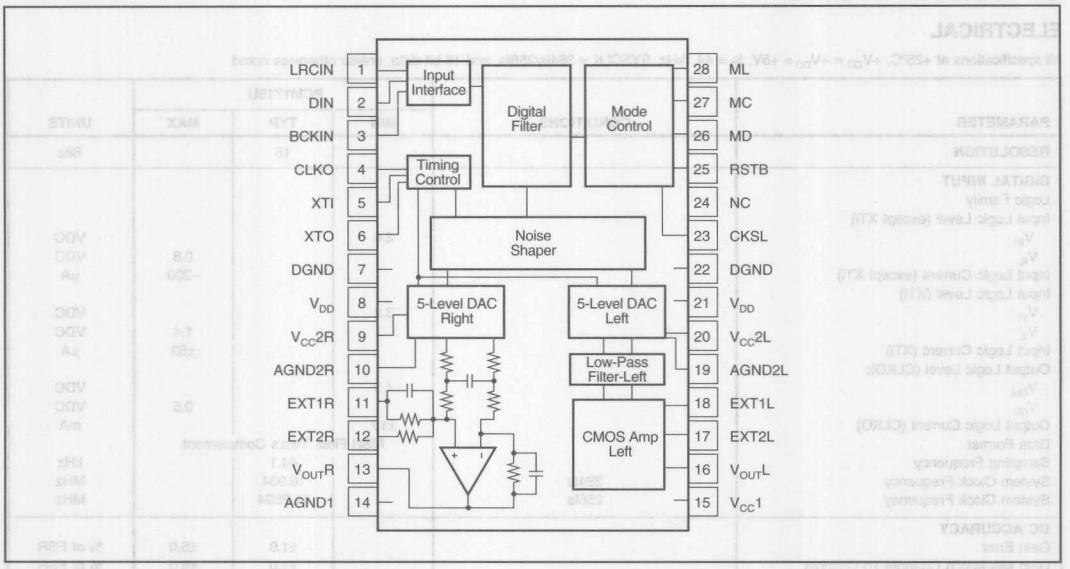
| PARAMETER | CONDITIONS | PCM1715U MIN | PCM1715U TYP | PCM1715U MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | 16 | | Bits |
| **DIGITAL INPUT** | | | | | |
| Logic Family | | | | | |
| Input Logic Level (except XTi) | | | | | |
| $V_{IH}$ | | 2.0 | | | VDC |
| $V_{IL}$ | | | | 0.8 | VDC |
| Input Logic Current (except XTi) | | | | –200 | µA |
| Input Logic Level (XTi) | | | | | |
| $V_{IH}$ | | 3.2 | | | VDC |
| $V_{IL}$ | | | | 1.4 | VDC |
| Input Logic Current (XTi) | | | | ±50 | µA |
| Output Logic Level (CLKO): | | | | | |
| $V_{OH}$ | | 4.5 | | | VDC |
| $V_{OL}$ | | | | 0.5 | VDC |
| Output Logic Current (CLKO) | | ±10 | | | mA |
| Data Format | | | MSB First, Two's Complement | | |
| Sampling Frequency | | | 44.1 | | kHz |
| System Clock Frequency | 384fs | | 16.934 | | MHz |
| System Clock Frequency | 256fs | | 11.2894 | | MHz |
| **DC ACCURACY** | | | | | |
| Gain Error | | | ±1.0 | ±5.0 | % of FSR |
| Gain Mis-Match Channel-To-Channel | | | ±1.0 | ±5.0 | % of FSR |
| Bipolar Zero Error | $V_O$ = 1/2$V_{CC}$ at Bipolar Zero | | ±20.0 | | mV |
| Gain Drift | | | ±50 | | ppm of FSR/°C |
| Bipolar Gain Drift | | | ±20 | | ppm of FSR/°C |
| **DYNAMIC PERFORMANCE** | | | | | |
| THD+N at F/S (0dB)[1] | $f_{IN}$ = 991Hz | | –92 | –88 | dB |
| THD+N at –60dB[1] | $f_{IN}$ = 991Hz | | –36 | –32 | dB |
| Dynamic Range | EIAJ A-weighted | | 98 | | dB |
| S/N Ratio | EIAJ A-weighted | 104 | 110 | | dB |
| Channel Separation | $f_{IN}$ = 991Hz | 90 | 94 | | dB |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Pass Band Ripple | | | | ±0.008 | dB |
| Stop Band Attenuation | | –62 | | | dB |
| Pass Band | | | 0.4535 | | fs |
| Stop Band | | | 0.5465 | | fs |
| De-emphasis Error | (fs = 44.1kHz) | | | +0.03 | dB |
| **ANALOG OUTPUT** | | | | | |
| Voltage Range | fs (0dB) OUT | | 3.2 | | Vp-p |
| Load Impedance | | 5 | | | kΩ |
| Center Voltage | | | +1/2$V_{CC}$ | | V |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range: $+V_{CC}$ | | +4.5 | +5.0 | +5.5 | VDC |
| $+V_{DD}$ | | +4.5 | +5.0 | +5.5 | VDC |
| Supply Current: $+I_{CC}$ $+I_{DD}$ | $+V_{CC}$ = $+V_{DD}$ = +5.0V | | 45 | 70 | mA |
| Power Dissipation | $+V_{CC}$ = $+V_{DD}$ = +5.0V | | 225 | 350 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Operation | | –25 | | +85 | °C |
| Storage | | –55 | | +100 | °C |

NOTE: (1) 30kHz LPF, 400Hz HPF, Average Mode.



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## PIN CONFIGURATION




## PIN ASSIGNMENTS

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | LRCIN | Sample Rate Clock Input (fs) |
| 2 | DIN | Data Input |
| 3 | BCKIN | Bit Clock Input |
| 4 | CLKO | Buffered Output of Oscillator |
| 5 | XTI | Oscillator Input (External Clock Input) |
| 6 | XTO | Oscillator Output |
| 7 | DGND | Digital Ground |
| 8 | $V_{DD}$ | Digital Power Supply (+5V) |
| 9 | $V_{CC}2R$ | Analog (DAC) +$V_{CC}$, Rch |
| 10 | AGND2R | Analog (DAC) Ground, Rch |
| 11 | EXT1R | Output Amp Common, Rch |
| 12 | EXT2R | Output Amp Bias, Rch |
| 13 | $V_{OUT}R$ | Rch Analog Output |
| 14 | AGND | Analog Ground |

| PIN | NAME | FUNCTION |
|---|---|---|
| 15 | $V_{CC}1$ | Analog Power Supply (+5V) |
| 16 | $V_{OUT}L$ | Lch Analog Output |
| 17 | EXT2L | Output Amp Bias, Lch |
| 18 | EXT1L | Output Amp Common, Lch |
| 19 | AGND2L | Analog (DAC) Ground, Lch |
| 20 | $V_{CC}2L$ | Analog (DAC) +$V_{CC}$, Lch |
| 21 | $V_{DD}$ | Digital Power Supply, (+5V) |
| 22 | DGND | Digital Ground |
| 23 | CKSL | System Clock Select (H:384fs, L:256fs) |
| 24 | NC | No Connection |
| 25 | RSTB | Reset |
| 26 | MD | Mode Control |
| 27 | MC | Mode Control, BCK |
| 28 | ML | Mode Control, WDCK |

NOTE: All input pins require pull up resistors.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | ±6.5VDC |
| +$V_{CC}$ to $V_{DD}$ Voltage | ±0.1V |
| Input Logic Voltage | –0.3V ~ $V_{DD}$ +0.3V |
| Power Dissipation | 400mW |
| Operating Temperature | –25°C to +85°C |
| Storage Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

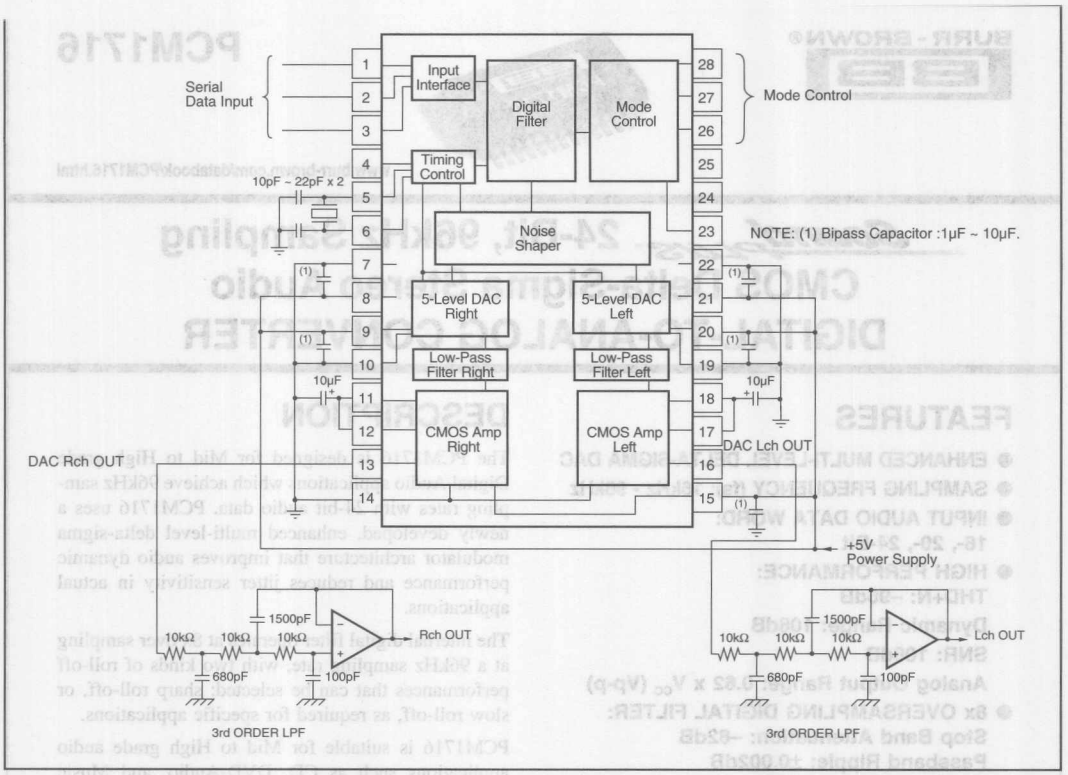
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| PCM1715U | 28-Pin SOIC | 217 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.


Serial
Data Input
Input
Interface
Digital
Filter
Mode
Control
Mode Control
Timing
Control
10pF ~ 22pF x 2
Noise
Shaper
NOTE: (1) Bipass Capacitor :1µF ~ 10µF.
5-Level DAC
Right
5-Level DAC
Left
Low-Pass
Filter Right
Low-Pass
Filter Left
10µF
CMOS Amp
Right
CMOS Amp
Left
DAC Rch OUT
DAC Lch OUT
+5V
Power Supply
1500pF
10kΩ
10kΩ
10kΩ
Rch OUT
680pF
100pF
3rd ORDER LPF
1500pF
10kΩ
10kΩ
10kΩ
Lch OUT
680pF
100pF
3rd ORDER LPF

BURR-BROWN®




# PCM1716

www.burr-brown.com/databook/PCM1716.html

## SoundPLUS™ 24-Bit, 96kHz Sampling CMOS Delta-Sigma Stereo Audio DIGITAL-TO-ANALOG CONVERTER

## FEATURES

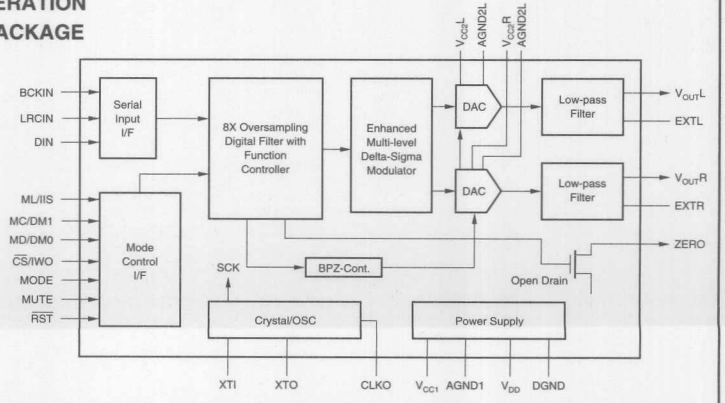
- ENHANCED MULTI-LEVEL DELTA-SIGMA DAC
- SAMPLING FREQUENCY (fs): 16kHz - 96kHz
- INPUT AUDIO DATA WORD:
  16-, 20-, 24-Bit
- HIGH PERFORMANCE:
  THD+N: –96dB
  Dynamic Range: 106dB
  SNR: 106dB
  Analog Output Range: 0.62 x $V_{CC}$ (Vp-p)
- 8x OVERSAMPLING DIGITAL FILTER:
  Stop Band Attenuation: –82dB
  Passband Ripple: ±0.002dB
  Slow Roll Off
- MULTI FUNCTIONS:
  Digital De-emphasis
  L/R Independent Digital Attenuation
  Soft Mute
  Zero Detect Mute
  Zero Flag
  Chip Select
  Reversible Output Phase
- +5V SINGLE SUPPLY OPERATION
- SMALL 28-LEAD SSOP PACKAGE

## DESCRIPTION

The PCM1716 is designed for Mid to High grade Digital Audio applications which achieve 96kHz sampling rates with 24-bit audio data. PCM1716 uses a newly developed, enhanced multi-level delta-sigma modulator architecture that improves audio dynamic performance and reduces jitter sensitivity in actual applications.

The internal digital filter operates at 8x over sampling at a 96kHz sampling rate, with two kinds of roll-off performances that can be selected: sharp roll-off, or slow roll-off, as required for specific applications.

PCM1716 is suitable for Mid to High grade audio applications such as CD, DVD-Audio, and Music Instruments, since the device has superior audio dynamic performance, 24-bit resolution and 96kHz sampling.




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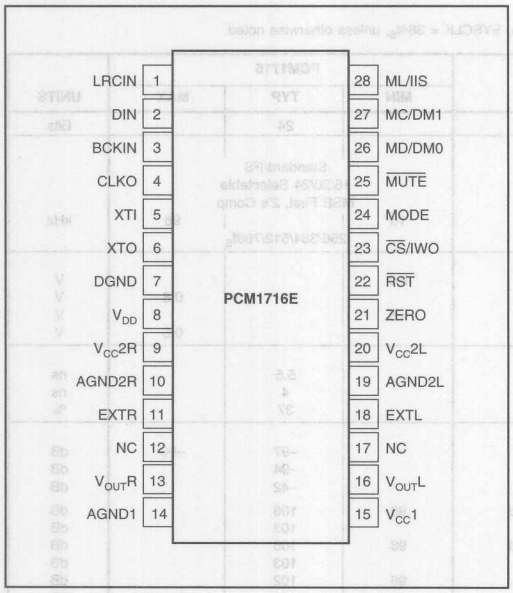
# SPECIFICATIONS

All specifications at +25°C, $+V_{CC} = +V_{DD} = +5V$, $f_S = 44.1kHz$, and 24-bit input data, SYSCLK = $384f_S$, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1716 MIN | PCM1716 TYP | PCM1716 MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | 24 | | Bits |
| **DATA FORMAT** | | | | | |
| Audio Data Interface Format | | | Standard/I²S | | |
| Data Bit Length | | | 16/20/24 Selectable | | |
| Audio Data Format | | | MSB First, 2's Comp | | |
| Sampling Frequency ($f_S$) | | 16 | | 96 | kHz |
| System Clock Frequency[1] | | | 256/384/512/768$f_S$ | | |
| **DIGITAL INPUT/OUTPUT LOGIC LEVEL** | | | | | |
| Input Logic Level $V_{IH}$ | | 2.0 | | | V |
| $V_{IL}$ | | | | 0.8 | V |
| Output Logic Level (CLKO) $V_{OH}$ | $I_{OH}$ = 2mA | 4.5 | | | V |
| $V_{OL}$ | $I_{OL}$ = 4mA | | | 0.5 | V |
| **CLKO PERFORMANCE[2]** | | | | | |
| Output Rise Time | 20 ~ 80% $V_{DD}$, 10pF | | 5.5 | | ns |
| Output Fall Time | 80 ~ 20% $V_{DD}$, 10pF | | 4 | | ns |
| Output Duty Cycle | 10pF Load | | 37 | | % |
| **DYNAMIC PERFORMANCE[3] (24-Bit Data)** | | | | | |
| THD+N $V_O$ = 0dB | $f_S$ = 44.1kHz | | –97 | –90 | dB |
| | $f_S$ = 96kHz | | –94 | | dB |
| $V_O$ = –60dB | $f_S$ = 44.1kHz | | –42 | | dB |
| Dynamic Range | $f_S$ =44.1kHz EIAJ A-weighted | 98 | 106 | | dB |
| | $f_S$ = 96kHz A-weighted | | 103 | | dB |
| Signal-to-Noise Ratio[4] | $f_S$ =44.1kHz EIAJ A-weighted | 98 | 106 | | dB |
| | $f_S$ = 96kHz A-weighted | | 103 | | dB |
| Channel Separation | $f_S$ = 44.1kHz | 96 | 102 | | dB |
| | $f_S$ = 96kHz | | 101 | | dB |
| **DYNAMIC PERFORMANCE[3] (16-Bit Data)** | | | | | |
| THD+N $V_O$ = 0dB | $f_S$ = 44.1kHz | | –94 | | dB |
| | $f_S$ = 96kHz | | –92 | | dB |
| Dynamic Range | $f_S$ = 44.1kHz EIAJ A-weighted | | 98 | | dB |
| | $f_S$ = 96kHz A-weighted | | 97 | | dB |
| **DC ACCURACY** | | | | | |
| Gain Error | | | ±1.0 | ±3.0 | % of FSR |
| Gain Mismatch: Channel-to-Channel | | | ±1.0 | ±3.0 | % of FSR |
| Bipolar Zero Error | $V_O$ = 0.5$V_{CC}$ at Bipolar Zero | | ±30 | ±60 | mV |
| **ANALOG OUTPUT** | | | | | |
| Output Voltage | Full Scale (0dB) | | 0.62 $V_{CC}$ | | Vp-p |
| Center Voltage | | | 0.5 $V_{CC}$ | | V |
| Load Impedance | AC Load | 5 | | | kΩ |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Filter Characteristics 1 | | | | | |
| (Sharp Roll-Off) | | | | | |
| Passband | ±0.002dB | | | 0.454$f_S$ | |
| | –3dB | | | 0.490$f_S$ | |
| Stopband | | 0.546$f_S$ | | | |
| Passband Ripple | | | | ±0.002 | dB |
| Stopband Attenuation | Stop Band = 0.546$f_S$ | –75 | | | dB |
| | Stop Band = 0.567$f_S$ | –82 | | | dB |
| Filter Characteristics 2 | | | | | |
| (Slow Roll-Off) | | | | | |
| Passband | ±0.002dB | | | 0.274$f_S$ | |
| | –3dB | | | 0.454$f_S$ | |
| Stopband | | 0.732$f_S$ | | | |
| Passband Ripple | | | | ±0.002 | dB |
| Stopband Attenuation | Stopband = 0.732$f_S$ | –82 | | | dB |
| Delay Time | | | 30/$f_S$ | | sec |
| De-emphasis Error | | | | ±0.1 | dB |
| **INTERNAL ANALOG FILTER** | | | | | |
| –3dB Bandwidth | | | 100 | | kHz |
| Passband Response | f = 20kHz | | –0.16 | | dB |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range | $V_{DD}$, $V_{CC}$ | 4.5 | 5 | 5.5 | VDC |
| Supply Current: $I_{CC}$ +$I_{DD}$ | $f_S$ = 44.1kHz | | 32 | 45 | mA |
| | $f_S$ = 96kHz | | 45 | | mA |
| Power Dissipation | $f_S$ = 44.1kHz | | 160 | 225 | mW |
| | $f_S$ = 96kHz | | 225 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Operation | | –25 | | +85 | °C |
| Storage | | –55 | | +100 | °C |

NOTES: (1) Refer section of system clock. (2) External buffer is recommended. (3) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average Mode. (4) SNR is tested at internally infinity zero detection off.

## PIN CONFIGURATION




## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| PCM1716E | 28-Pin SSOP | 324 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | +6.5V |
| $+V_{CC}$ to $+V_{DD}$ Difference | ±0.1V |
| Input Logic Voltage | –0.3V to ($V_{DD}$ + 0.3V) |
| Input Current (except power supply) | ±10mA |
| Power Dissipation | 400mW |
| Operating Temperature Range | –25°C to +85°C |
| Storage Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |

## PIN ASSIGNMENTS

| PIN | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| 1 | LRCIN | IN | Left and Right Clock Input. This clock is equal to the sampling rate - $f_S$.[1] |
| 2 | DIN | IN | Serial Audio Data Input[1] |
| 3 | BCKIN | IN | Bit Clock Input for Serial Audio Data.[1] |
| 4 | CLKO | OUT | Buffered Output of Oscillator. Equivalent to System Clock. |
| 5 | XTI | IN | Oscillator Input (External Clock Input) |
| 6 | XTO | OUT | Oscillator Output |
| 7 | DGND | — | Digital Ground |
| 8 | $V_{DD}$ | — | Digital Power +5V |
| 9 | $V_{CC}2R$ | — | Analog Power +5V |
| 10 | AGND2R | — | Analog Ground |
| 11 | EXTR | OUT | Rch, Common Pin of Analog Output Amp |
| 12 | NC | — | No Connection |
| 13 | $V_{OUT}R$ | OUT | Rch, Analog Voltage Output of Audio Signal |
| 14 | AGND1 | — | Analog Ground |
| 15 | $V_{CC}1$ | — | Analog Power +5V |
| 16 | $V_{OUT}L$ | OUT | Lch, Analog Voltage Output of Audio Signal |
| 17 | NC | — | No Connection |
| 18 | EXTL | OUT | Lch, Common Pin of Analog Output Amp |
| 19 | AGND2L | — | Analog Ground |
| 20 | $V_{CC}2L$ | — | Analog Power +5V |
| 21 | ZERO | OUT | Zero Data Flag |
| 22 | $\overline{RST}$ | IN | Reset. When this pin is low, the DF and modulators are held in reset.[2] |
| 23 | $\overline{CS}$/IWO | IN | Chip Select/Input Format Selection. When this pin is low, the Mode Control is effective.[3] |
| 24 | MODE | IN | Mode Control Select. (H: Software, L: Hardware)[2] |
| 25 | $\overline{MUTE}$ | IN | Mute Control |
| 26 | MD/DM0 | IN | Mode Control, DATA/De-emphasis Selection 1[2] |
| 27 | MC/DM1 | IN | Mode Control, BCK/De-emphasis Selection 2[2] |
| 28 | ML/I²S | IN | Mode Control, WDCK/Input Format Selection[2] |

NOTES: (1) Pins 1, 2, 3; Schmitt Trigger input. (2) Pins 22, 24, 25, 26, 27, 28; Schmitt Trigger input with pull-up resister. (3) Pin 23; Schmitt Trigger input with pull-down resister.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# PCM1717

www.burr-brown.com/databook/PCM1717.html

## SoundPLUS Stereo Audio DIGITAL-TO-ANALOG CONVERTER

## FEATURES

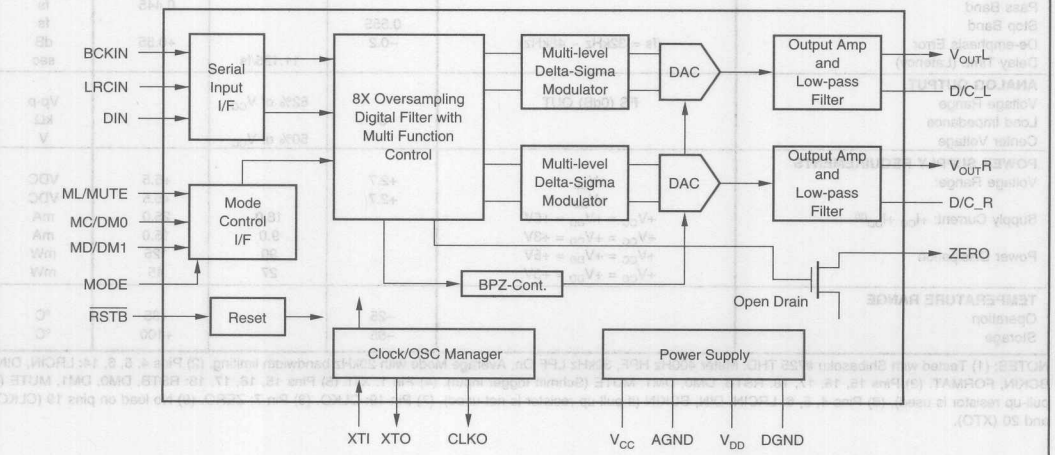
- ACCEPTS 16- OR 18-BIT INPUT DATA
- COMPLETE STEREO DAC:
  - 8X Oversampling Digital Filter
  - Multi-Level Delta-Sigma DAC
  - Analog Low Pass Filter
  - Output Amplifier
- HIGH PERFORMANCE:
  - –90dB THD+N
  - 96dB Dynamic Range
  - 100dB SNR
- SYSTEM CLOCK: 256fs or 384fs
- WIDE POWER SUPPLY: +2.7V to +5.5V
- SELECTABLE FUNCTIONS:
  - Soft Mute
  - Digital Attenuation (256 Steps)
  - Digital De-emphasis
  - Output Mode: L, R, Mono, Mute
- SMALL 20-PIN SSOP PACKAGE

## DESCRIPTION

The PCM1717 is a complete low cost stereo, audio digital-to-analog converter, including digital interpolation filter, 3rd-order delta-sigma DAC, and analog output amplifiers. PCM1717 is fabricated on a highly advanced 0.6µ CMOS process. PCM1717 accepts 16- or 18-bit normal input data format, or 16- or 18-bit IIS data format.

The digital filter performs an 8X interpolation function, as well as special functions such as soft mute, digital attenuation, and digital de-emphasis. The digital filter features –35dB stop band attenuation and ±0.17dB ripple in the pass band.

PCM1717 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required. Its low cost, small size, and single +5V power supply make it ideal for automotive CD players, bookshelf CD players, BS tuners, keyboards, MPEG audio, MIDI applications, set-top boxes, CD-ROM drives, CD-Interactive, and CD-Karaoke systems.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

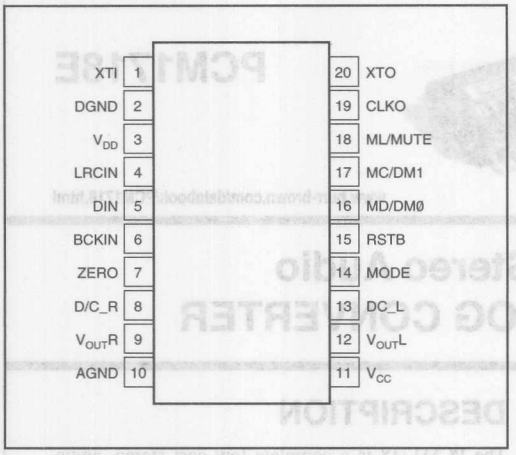
# SPECIFICATIONS

All specifications at +25°C, $+V_{CC} = +V_{DD} = +5V$, fs = 44.1kHz, and 16-bit input data, SYSCLK = 384fs, unless otherwise noted. Measurement bandwidth is 20kHz.

| PARAMETER | CONDITIONS | PCM1717E MIN | PCM1717E TYP | PCM1717E MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | 16 | | 18 | Bits |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic Family | | | CMOS | | |
| Input Logic Level: | | | | | |
| $V_{IH}$(2) | | 70% of $V_{DD}$ | | | V |
| $V_{IL}$(2) | | | | 30% of $V_{DD}$ | V |
| $V_{IH}$(3) | | 70% of $V_{DD}$ | | | V |
| $V_{IL}$(3) | | | | 30% of $V_{DD}$ | V |
| $V_{IH}$(4) | | 64% of $V_{DD}$ | | | V |
| $V_{IL}$(4) | | | | 28% of $V_{DD}$ | V |
| Input Logic Current: | | | | | |
| $I_{IH}$(5) | | | | –6.0 | µA |
| $I_{IL}$(5) | | | | –120 | µA |
| $I_{IH}$(6) | | | | –2 | µA |
| $I_{IL}$(6) | | | | 0.02 | µA |
| $I_{IH}$(4) | $V_{IN}$ = 3.2V | | | 40 | µA |
| $I_{IL}$(4) | $V_{IN}$ = 1.4V | | | –40 | µA |
| Output Logic Level: ($+V_{DD}$ = +5V) | | | | | |
| $V_{OH}$(7) | $I_{OH}$ = –5mA | 3.8 | | | V |
| $V_{OL}$(7) | $I_{OL}$ = +5mA | | | 1.0 | V |
| $V_{OL}$(8) | $I_{OL}$ = +5mA | | | 1.0 | V |
| Interface Format | | | Selectable Normal, I²S | | |
| Data Format | | | 16/18 Bits MSB First Binary Two's Complement | | |
| Sampling Frequency | | 32 | 44.1 | 48 | kHz |
| System Clock Frequency | 256fs/384fs | 8.192/12.288 | 11.2896/16.9344 | 12.288/18.432 | MHz |
| **DC ACCURACY** | | | | | |
| Gain Error | | | ±1.0 | ±5.0 | % of FSR |
| Gain Mismatch Channel-to-Channel | | | ±1.0 | ±5.0 | % of FSR |
| Bipolar Zero Error | $V_O$ = 1/2 $V_{CC}$ at Bipolar Zero | | ±30 | | mV |
| **DYNAMIC PERFORMANCE**(1) | $V_{CC}$ = +5V, f = 991Hz | | | | |
| THD+N at FS (0dB) | | | –90 | –80 | dB |
| THD+N at –60dB | | | –34 | | dB |
| Dynamic Range | EIAJ, A-weighted | 90 | 96 | | dB |
| Signal-To-Noise Ratio | EIAJ, A-weighted | 92 | 100 | | dB |
| Channel Separation | | 90 | 97 | | dB |
| Level Linearity Error (–90dB) | | | ±0.5 | | dB |
| **DYNAMIC PERFORMANCE**(1) | $V_{CC}$ = +3V, f = 991Hz | | | | |
| THD+N at FS (0dB) | | | –86 | | dB |
| Dynamic Range | EIAJ, A-weighted | | 91 | | dB |
| Signal-To-Noise Ratio | EIAJ, A-weighted | | 94 | | dB |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Pass Band Ripple | | | | ±0.17 | dB |
| Stop Band Attenuation | | –35 | | | dB |
| Pass Band | | | | 0.445 | fs |
| Stop Band | | 0.555 | | | fs |
| De-emphasis Error | (fs = 32kHz ~ 48kHz) | –0.2 | | +0.55 | dB |
| Delay Time (Latency) | | | 11.125/fs | | sec |
| **ANALOG OUTPUT** | | | | | |
| Voltage Range | FS (0dB) OUT | | 62% of $V_{CC}$ | | Vp-p |
| Load Impedance | | 5 | | | kΩ |
| Center Voltage | | | 50% of $V_{CC}$ | | V |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range: | $+V_{CC}$ | +2.7 | | +5.5 | VDC |
| | $+V_{DD}$ | +2.7 | | +5.5 | VDC |
| Supply Current: $+I_{CC}$ $+I_{DD}$(9) | $+V_{CC}$ = $+V_{DD}$ = +5V | | 18.0 | 25.0 | mA |
| | $+V_{CC}$ = $+V_{DD}$ = +3V | | 9.0 | 15.0 | mA |
| Power Dissipation | $+V_{CC}$ = $+V_{DD}$ = +5V | | 90 | 125 | mW |
| | $+V_{CC}$ = $+V_{DD}$ = +3V | | 27 | 45 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Operation | | –25 | | +85 | °C |
| Storage | | –55 | | +100 | °C |

NOTES: (1) Tested with Shibasoku #725 THD. Meter 400Hz HPF, 30kHz LPF On, Average Mode with 20kHz bandwidth limiting. (2) Pins 4, 5, 6, 14: LRCIN, DIN, BCKIN, FORMAT. (3) Pins 15, 16, 17, 18: RSTB, DM0, DM1, MUTE (Schmitt trigger input). (4) Pin 1: XTI. (5) Pins 15, 16, 17, 18: RSTB, DM0, DM1, MUTE (if pull-up resistor is used). (6) Pins 4, 5, 6: LRCIN, DIN, BCKIN (if pull-up resistor is not used). (7) Pin 19: CLKO. (8) Pin 7: ZERO. (9) No load on pins 19 (CLKO) and 20 (XTO).

## PIN CONFIGURATION




## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| PCM1717E | 20-Pin SSOP | 334-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | +6.5V |
| $+V_{CC}$ to $+V_{DD}$ Difference | ±0.1V |
| Input Logic Voltage | –0.3V to ($V_{DD}$ + 0.3V) |
| Power Dissipation | 200mW |
| Operating Temperature Range | –25°C to +85°C |
| Storage Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |
| Thermal Resistance, $\theta_{JA}$ | +70°C/W |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN ASSIGNMENTS

| PIN | NAME | FUNCTION |
|---|---|---|
| **Data Input Interface Pins** | | |
| 4 | LRCIN | Sample Rate Clock Input. Controls the update rate (fs). |
| 5 | DIN | Serial Data Input. MSB first, right justified (Sony format) or I²S (Philips). Contains a frame of 16- or 18-bit data. |
| 6 | BCKIN | Bit Clock Input. Clocks in the data present on DIN input. |
| **Mode Control and Clock Signals** | | |
| 1 | XTI | Oscillator Input (External Clock Input). For an internal clock, tie XTI to one side of the crystal oscillator. For an external clock, tie XTI to the output of the chosen external clock. |
| 14 | MODE | Operation Mode Select. For Software Mode, tie Mode "HIGH". For Hardware Mode, tie Mode "LOW". |
| 16 | MD/DM0 | Mode Control for Data Input or De-emphasis. When "HIGH" MD is selected, and a "LOW" selects DM0. |
| 17 | MC/DM1 | Mode Control for BCKIN or De-emphasis. When "HIGH", MC is selected, and a "LOW" selects DM1. |
| 18 | ML/MUTE | Mode Control for Strobe Clock or Mute. When "HIGH", ML is selected, and a "LOW" selects mute. |
| 19 | CLKO | Buffered Output of Oscillator. Equivalent to XTI. |
| 20 | XTO | Oscillator Output. When using the internal clock, tie to the opposite side (from pin 1) of the crystal oscillator. When using an external clock, leave XTO open. |
| **Operational Controls and Flags** | | |
| 7 | ZERO | Infinite Zero Detection Flag, open drain output. When the zero detection feature is muting the output, ZERO is "LOW". When non-zero input data is present, ZERO is in a high impedance state. When the input data is continuously zero for 65.536 BCKIN cycles, zero will be low. |
| 15 | RSTB | Resets DAC operation with an active "LOW" pulse. |
| **Analog Output Functions** | | |
| 8 | D/C_R | Right Channel Output Amplifier Common. Bypass to ground with 10µF capacitor. |
| 9 | $V_{OUT}R$ | Right Channel Analog Output. $V_{OUT}$ max = 0.62 x $V_{CC}$. |
| 12 | $V_{OUT}L$ | Left Channel Analog Output. $V_{OUT}$ max = 0.62 x $V_{CC}$. |
| 13 | D/C_L | Left Channel Output Amplifier Common. Bypass to ground with 10µF capacitor. |
| **Power Supply Connections** | | |
| 2 | DGND | Digital Ground. |
| 3 | $V_{DD}$ | Digital Power Supply (+5V). |
| 10 | AGND | Analog Ground. |
| 11 | $V_{CC}$ | Analog Power Supply (+3V). |



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# PCM1718E

www.burr-brown.com/databook/PCM1718.html

## SoundPLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER

## FEATURES

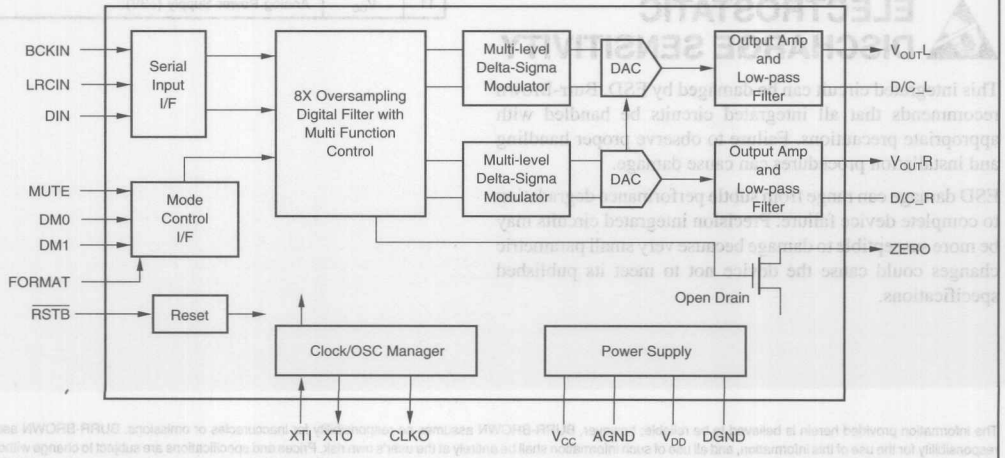
- **ACCEPTS 16- or 18-BIT I²S, OR 18-BIT NORMAL INPUT DATA**
- **COMPLETE STEREO DAC:**
  **8X Oversampling Digital Filter**
  **Multi-Level Delta-Sigma DAC**
  **Analog Low Pass Filter**
  **Output Amplifier**
- **HIGH PERFORMANCE:**
  **–90dB THD+N**
  **96dB Dynamic Range**
  **100dB SNR**
- **SYSTEM CLOCK: 256fs or 384fs**
- **WIDE POWER SUPPLY: +2.7V to +5.5V**
- **SELECTABLE FUNCTIONS:**
  **Soft Mute**
  **Digital De-emphasis**
- **SMALL 20-PIN SSOP PACKAGE**

## DESCRIPTION

The PCM1718 is a complete low cost stereo, audio digital-to-analog converter, including digital interpolation filter, 3rd-order delta-sigma DAC, and analog output amplifiers. PCM1718 is fabricated on a highly advanced 0.6µ CMOS process. PCM1718 accepts 18-bit normal input data format, or 16- or 18-bit I²S data format.

The digital filter performs an 8X interpolation function, as well as special functions such as soft mute and digital de-emphasis.

PCM1718 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required. Its low cost, small size, and single power supply make it ideal for BS tuners, keyboards, MPEG audio, PCMCIA audio cards (ZV port), MIDI applications, and set-top boxes.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

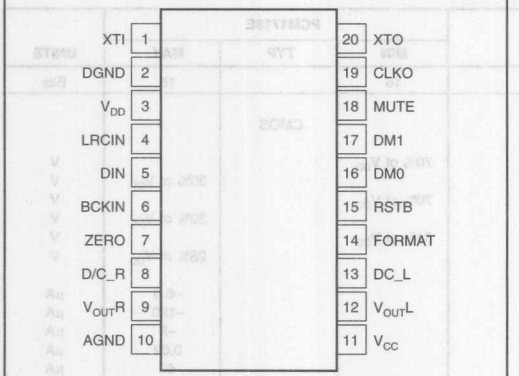
All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, fs = 44.1kHz, and 18-bit input data, SYSCLK = 384fs, unless otherwise noted. Measurement bandwidth is 20kHz.

| PARAMETER | CONDITIONS | PCM1718E MIN | PCM1718E TYP | PCM1718E MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | 16 | | 18 | Bits |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic Family | | | CMOS | | |
| Input Logic Level: | | | | | |
| $V_{IH}$(2) | | 70% of $V_{DD}$ | | | V |
| $V_{IL}$(2) | | | | 30% of $V_{DD}$ | V |
| $V_{IH}$(3) | | 70% of $V_{DD}$ | | | V |
| $V_{IL}$(3) | | | | 30% of $V_{DD}$ | V |
| $V_{IH}$(4) | | 64% of $V_{DD}$ | | | V |
| $V_{IL}$(4) | | | | 28% of $V_{DD}$ | V |
| Input Logic Current: | | | | | |
| $I_{IH}$(5) | | | | –6.0 | µA |
| $I_{IL}$(5) | | | | –120 | µA |
| $I_{IH}$(6) | | | | –2 | µA |
| $I_{IL}$(6) | | | | 0.02 | µA |
| $I_{IH}$(4) | $V_{IN}$ = 3.2V | | | 40 | µA |
| $I_{IL}$(4) | $V_{IN}$ = 1.4V | | | –40 | µA |
| Output Logic Level: ($+V_{DD}$ = +5V) | | | | | |
| $V_{OH}$(7) | $I_{OH}$ = –5mA | 3.8 | | | V |
| $V_{OL}$(7) | $I_{OL}$ = +5mA | | | 1.0 | V |
| $V_{OL}$(8) | $I_{OL}$ = +5mA | | | 1.0 | V |
| Interface Format | | | Selectable Normal, I²S | | |
| Data Format | | | 16/18 Bits MSB First Binary Two's Complement | | |
| Sampling Frequency | | 32 | 44.1 | 48 | kHz |
| System Clock Frequency | 256fs/384fs | 8.192/12.288 | 11.2896/16.9344 | 12.288/18.432 | MHz |
| **DC ACCURACY** | | | | | |
| Gain Error | | | ±1.0 | ±5.0 | % of FSR |
| Gain Mismatch Channel-to-Channel | | | ±1.0 | ±5.0 | % of FSR |
| Bipolar Zero Error | $V_O$ = 1/2 $V_{CC}$ at Bipolar Zero | | ±30 | | mV |
| **DYNAMIC PERFORMANCE**(1) | $V_{CC}$ = +5V, f = 991Hz | | | | |
| THD+N at FS (0dB) | | | –90 | –80 | dB |
| THD+N at –60dB | | | –34 | | dB |
| Dynamic Range | EIAJ, A-weighted | 90 | 96 | | dB |
| Signal-To-Noise Ratio | EIAJ, A-weighted | 92 | 100 | | dB |
| Channel Separation | | 90 | 97 | | dB |
| Level Linearity Error (–90dB) | | | ±0.5 | | dB |
| **DYNAMIC PERFORMANCE**(1) | $V_{CC}$ = +3V, f = 991Hz | | | | |
| THD+N at FS (0dB) | | | –86 | | dB |
| Dynamic Range | EIAJ, A-weighted | | 91 | | dB |
| Signal-To-Noise Ratio | EIAJ, A-weighted | | 94 | | dB |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Pass Band Ripple | | | | ±0.17 | dB |
| Stop Band Attenuation | | –35 | | | dB |
| Pass Band | | | | 0.445 | fs |
| Stop Band | | 0.555 | | | fs |
| De-emphasis Error | (fs = 32kHz ~ 48kHz) | –0.2 | | +0.55 | dB |
| Delay Time (Latency) | | | 11.125/fs | | sec |
| **ANALOG OUTPUT** | | | | | |
| Voltage Range | FS (0dB) OUT | | 62% of $V_{CC}$ | | Vp-p |
| Load Impedance | | 5 | | | kΩ |
| Center Voltage | | | 50% of $V_{CC}$ | | V |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range: | $+V_{CC}$ | +2.7 | | +5.5 | VDC |
| | $+V_{DD}$ | +2.7 | | +5.5 | VDC |
| Supply Current: $+I_{CC}$ $+I_{DD}$(9) | $+V_{CC}$ = $+V_{DD}$ = +5V | | 18.0 | 25.0 | mA |
| | $+V_{CC}$ = $+V_{DD}$ = +3V | | 9.0 | 15.0 | mA |
| Power Dissipation | $+V_{CC}$ = $+V_{DD}$ = +5V | | 90 | 125 | mW |
| | $+V_{CC}$ = $+V_{DD}$ = +3V | | 27 | 45 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Operation | | –25 | | +85 | °C |
| Storage | | –55 | | +100 | °C |

NOTES: (1) Tested with Shibasoku #725 THD. Meter 400Hz HPF, 30kHz LPF On, Average Mode with 20kHz bandwidth limiting. (2) Pins 4, 5, 6, 14: LRCIN, DIN, BCKIN, FORMAT. (3) Pins 15, 16, 17, 18: RSTB, DM0, DM1, MUTE (Schmitt trigger input). (4) Pin 1: XTI. (5) Pins 15, 16, 17, 18: RSTB, DM0, DM1, MUTE (if pull-up resistor is used). (6) Pins 4, 5, 6: LRCIN, DIN, BCKIN (if pull-up resistor is not used). (7) Pin 19: CLKO. (8) Pin 7: ZERO. (9) No load on pins 19 (CLKO) and 20 (XTO).

## PIN CONFIGURATION

TOP VIEW — SSOP




## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| PCM1718E | 20-Pin SSOP | 334-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | +6.5V |
| $+V_{CC}$ to $+V_{DD}$ Difference | ±0.1V |
| Input Logic Voltage | –0.3V to ($V_{DD}$ + 0.3V) |
| Power Dissipation | 200mW |
| Operating Temperature Range | –25°C to +85°C |
| Storge Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |
| Thermal Resistance, $\theta_{JA}$ | +70°C/W |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN ASSIGNMENTS

| PIN | NAME | FUNCTION |
|---|---|---|
| **Data Input Interface Pins** | | |
| 4 | LRCIN | Sample Rate Clock Input. Controls the update rate (fs). |
| 5 | DIN | Serial Data Input. MSB first, right justified (Sony format, 18 bits) or I²S (Philips format, 16 or 18 bits). |
| 6 | BCKIN | Bit Clock Input. Clocks in the data present on DIN input. |
| **Mode Control and Clock Signals** | | |
| 1 | XTI | Oscillator Input (External Clock Input). For an internal clock, tie XTI to one side of the crystal oscillator. For an external clock, tie XTI to the output of the chosen external clock. |
| 14(1) | FORMAT | A "HIGH" selects I²S input data format, and a "LOW" selects Normal (Sony) input data format. |
| 16(1) | DM0 | De-emphasis selection. |
| 17(1) | DM1 | De-emphasis selection. |
| 18(1) | MUTE | Soft Mute Control. When set "LOW", the outputs are muted. |
| 19 | CLKO | Buffered Output of Oscillator. Equivalent to XTI. |
| 20 | XTO | Oscillator Output. When using the internal clock, tie to the opposite side (from pin 1) of the crystal oscillator. When using an external clock, leave XTO open. |
| **Operational Controls and Flags** | | |
| 7 | ZERO | Infinite Zero Detection Flag, open drain output. When the input is continuously zero for 65,536 cycles of BCKIN, ZERO is "LOW". |
| 15(1) | RSTB | Resets DAC operation with an active "LOW" pulse. |
| **Analog Output Functions** | | |
| 8 | D/C_R | Right Channel Output Amplifier Common. Bypass to ground with 10µF capacitor. |
| 9 | $V_{OUT}R$ | Right Channel Analog Output. $V_{OUT}$ max = 0.62 x $V_{CC}$. |
| 12 | $V_{OUT}L$ | Left Channel Analog Output. $V_{OUT}$ max = 0.62 x $V_{CC}$. |
| 13 | D/C_L | Left Channel Output Amplifier Common. Bypass to ground with 10µF capacitor. |
| **Power Supply Connections** | | |
| 2 | DGND | Digital Ground. |
| 3 | $V_{DD}$ | Digital Power Supply (+5V or +3V). |
| 10 | AGND | Analog Ground. |
| 11 | $V_{CC}$ | Analog Power Supply (+5V or +3V). |

NOTE: (1) With internal pull-up.

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# PCM1719

www.burr-brown.com/databook/PCM1719.html

## SoundPLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER

## FEATURES

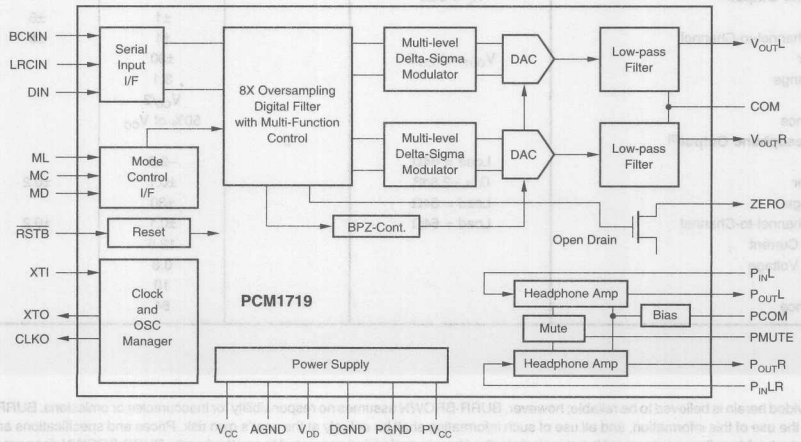
- ACCEPTS 16- OR 18-BIT INPUT DATA
- COMPLETE STEREO DAC:
  - 8X Oversampling Digital Filter
  - Multi-Level Delta-Sigma DAC
  - Analog Low Pass Filter
- ON-CHIP HEADPHONE AMPLIFIER
- HIGH PERFORMANCE:
  - –88dB THD+N
  - 96dB Dynamic Range
  - 100dB SNR
- SELECTABLE FUNCTIONS:
  - Digital De-emphasis
  - Digital Attenuation (256 Steps)
  - Soft Mute
  - Multiple Output Formats
- SYSTEM CLOCK: $256f_S$ or $384f_S$
- SINGLE +5V POWER SUPPLY
- SMALL 28-PIN SSOP PACKAGE

## DESCRIPTION

PCM1719 is a complete, low cost stereo audio digital-to-analog converter (DAC) including a digital interpolation filter, 3rd-order delta-sigma DAC, an analog low-pass filter and output amplifier. PCM1719 also has an on-chip stereo headphone amplifier.

PCM1719 can accept either 16-, or 18-bit input data. The audio data input format can be either MSB-first, right-justified or I²S. The system clock can be $256f_S$ or $384f_S$. PCM1719 is fabricated on a highly advanced 0.6µs CMOS process, which delivers high performance at very low power dissipation.

PCM1719 is ideal for applications which require headphone drivers such as CD-ROM drives, digital audio workstations, portable CD players, and digital musical instruments.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

All specifications at +25°C, $+V_{DD} = +V_{CC} = PV_{CC} = +5V$, $f_S = 44.1kHz$, SYSCLK = $384f_S$, 16-bit data, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1719E MIN | PCM1719E TYP | PCM1719E MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | 16 | | 18 | Bits |
| **DATA FORMAT** | | | | | |
| Audio Data Format | | | Normal/I²S Selectable | | |
| Data Bit Length | | | 16/18 Bits, Selectable | | |
| Sampling Frequency ($f_S$) | $256f_S/384f_S$ | 32 | 44.1 | 48 | kHz |
| System Clock Frequency | | 8.192/12.288 | 11.2896/16.9344 | 12.288/18.432 | MHz |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| **Logic Family** | | | TTL Compatible | | |
| Input Logic Level[2, 3] | | | | | |
| $V_{IH}$ | | 2 | | | VDC |
| $V_{IL}$ | | | | 0.8 | VDC |
| Input Logic Current | | | | | |
| $I_{IH}$ | | | | 0.8 | µA |
| $I_{IL}$ | | | | –0.8 | µA |
| $I_{IH}$ | $V_{IH}$ = 2.0V | | | –100 | µA |
| $I_{IL}$ | $V_{IL}$ = 0.0V | | | –120 | µA |
| $I_{IH}$ | $V_{IH}$ = 2.0V | | | 15 | µA |
| $I_{IL}$ | $V_{IL}$ = 0.0V | | | –15 | µA |
| $I_{IH}$ | $V_{IH}$ = 2.0V | | | –60 | µA |
| $I_{IL}$ | $V_{IL}$ = 0.0V | | | –100 | µA |
| Output Logic Level | | | | | |
| $V_{OH}$ | $I_{OH}$ = –5mA | 3.8 | | | VDC |
| $V_{OL}$ | $I_{OL}$ = 5mA | | | 1.0 | VDC |
| $V_{OL}$ | $I_{OL}$ = 5mA | | | 1.0 | VDC |
| **DYNAMIC PERFORMANCE[1]** | | | | | |
| **$V_{OUT}$L, $V_{OUT}$R: Line Output[5]** | | | | | |
| THD+N at $V_O$ = 0dB | $f_{OUT}$ = 991Hz | | –88 | –80 | dB |
| at $V_O$ = –60dB | $f_{OUT}$ = 991Hz | | –34 | | dB |
| Dynamic Range | EIAJ, A-weighted | 90 | 96 | | dB |
| Signal-to-Noise Ratio | EIAJ, A-weighted | 92 | 100 | | dB |
| Channel Separation | $f_{OUT}$ = 991Hz | 90 | 97 | | dB |
| Level Linearity Error | $f_{OUT}$ = 991Hz, –90dB | | ±0.5 | | dB |
| **$P_{OUT}$L, $P_{OUT}$R: Headphone Output[6]** | $R_L$ = 64Ω | | | | |
| THD+N at $V_O$ = 0dB | | | –68 | –60 | dB |
| Frequency Response | $f_{OUT}$ = 20Hz to 20kHz | | ±0.1 | ±0.2 | dB |
| Output Noise Level | EIAJ, A-weighted, $R_G$ = 0Ω | | 25 | 30 | µVrms |
| Channel Separation | | 87 | 90 | | dB |
| Analog Mute Attenuation Level | | 80 | 85 | | dB |
| **DC PERFORMANCE** | | | | | |
| **$V_{OUT}$L, $V_{OUT}$R: Line Output[5]** | $R_L$ = 64Ω | | | | |
| Gain Error | | | ±1 | ±5 | % of FSR |
| Gain Mismatch Channel-to-Channel | | | ±1 | ±5 | % of FSR |
| Bipolar Zero Error | $V_{OUT} = V_{CC}/2$ | | ±30 | | mV |
| Analog Output Range | | | 3.1 | | Vp-p |
| Center Voltage | | | $V_{CC}/2$ | | V |
| AC Load Impedance | | | 50% of $V_{CC}$ | | VDC |
| **$P_{OUT}$L, $P_{OUT}$R: Headphone Output[6]** | | 5 | | | kΩ |
| Voltage Gain | Load = 64Ω | | –2.8 | | dB |
| Voltage Gain Error | G = –2.8dB | | ±0.1 | ±0.2 | dB |
| Input Offset Voltage | Load = 64Ω | | ±30 | | mV |
| Gain Mismatch Channel-to-Channel | Load = 64Ω | | ±0.1 | ±0.2 | dB |
| Maximum Output Current | | | 12.5 | | mArms |
| Maximum Output Voltage | | | 0.8 | | Vrms |
| Output Power | | | 10 | | mW |
| AC Load Impedance | | | 64 | | Ω |

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## SPECIFICATIONS(CONT)

All specifications at +25°C, $+V_{DD}$ = $+V_{CC}$ = $PV_{CC}$ = +5V, $f_S$ = 44.1kHz, SYSCLK = 384$f_S$, 16-bit data, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1719E MIN | PCM1719E TYP | PCM1719E MAX | UNITS |
|---|---|---|---|---|---|
| **FILTER PERFORMANCE** | | | | | |
| **Digital Filter** | | | | | |
| Passband | | | | 0.445 | $f_S$ |
| Stopband | | 0.555 | | | $f_S$ |
| Passband Ripple | | | | ±0.17 | dB |
| Stopband Attenuation | | –35 | | | dB |
| De-emphasis Error | $f_S$ = 32kHz to 48kHz | –0.2 | | +0.55 | dB |
| Delay Time | | | 11.125/$f_S$ | | sec |
| **ANALOG FILTER: Line Outputs** | | | | | |
| Frequency Response | f = 20Hz to 20kHz | | –0.16 | | dB |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range | $V_{DD}$, $V_{CC}$, $PV_{CC}$ | +4.5 | 5.0 | +5.5 | VDC |
| Supply Current(7) | | | 18 | 25 | mA |
| $I_{CC}$ + $I_{DD}$ | $V_{DD}$ = $V_{CC}$ = 5.0V | | 18 | 25 | mA |
| $IP_{CC}$ (Full Scale Input) | $PV_{CC}$ = 5.0V | | 20 | 25 | mA |
| Power Dissipation | | | | | |
| $P_D$ | $V_{CC}$, $V_{DD}$ = 5.0 | | 90 | 125 | mW |
| $P_{PD}$ | $PV_{CC}$ = 5.0 | | 90 | 125 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Operation | | –25 | | +85 | °C |
| Storage | | –55 | | +100 | °C |

NOTES: (1) Dynamic performance specs are tested with external 20kHz low pass filter and THD-B specs are test with 30kHz LPF, 400Jz HPF, Average Mode, Shibasoku #725 THD Meter. (2) RSTB pin, MD pin, MC pin, and ML pin include an internal pull-up resistor. (3) RSTB pin, MD pin, MC pin, and ML pin include internal Schmitt trigger circuits. (4) ZERO pin is an open drain output. (5) Line output should be connected by a coupling capacitor. (6) Headphone output should be connected by a coupling capacitor. (7) Supply current and power dissipation are measured at CLKO pin = no load, XTO pin = no load.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | |
| $+V_{DD}$ | +6.5V |
| $+V_{CC}$ | +6.5V |
| $+PV_{CC}$ | +6.5V |
| $-V_{DD}$ to $+V_{CC}\Delta$ | 0.1V |
| $+V_{DD}$ to $+PV_{CC}\Delta$ | 0.1V |
| $+V_{DD}$ to $+PV_{CC}\Delta$ | 0.1V |
| Input Logic Voltage | –0.6V to ($V_{DD}$ + 06V) |
| Power Dissipation | 200mW |
| Operating Temperature Range | –25°C to +85°C |
| Storge Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |
| Junction Temperature, $\theta_{JA}$ | +130°C/W |

### PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| PCM1719E | 28-Pin SSOP | 324 |

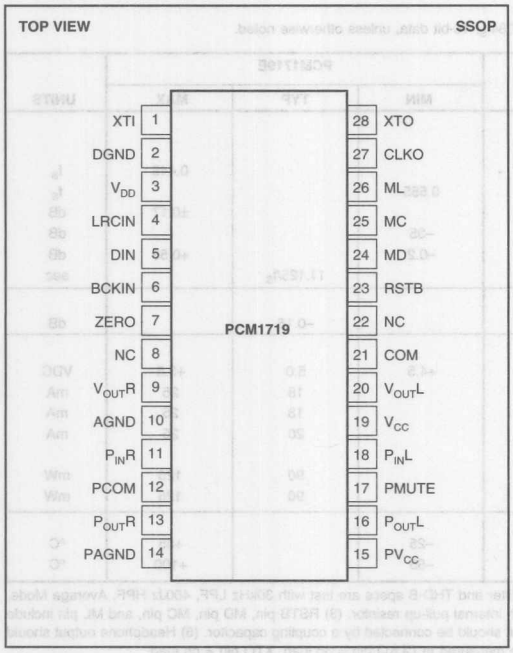
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN CONFIGURATION




## PIN ASSIGNMENTS

| PIN | NAME | TYPE | FUNCTION |
|---|---|---|---|
| 1 | XTI | IN | Crystal Oscillator Input. |
| 2 | DGND | PWR | Digital Ground. |
| 3 | $V_{DD}$ | PWR | +5V Digital Power Supply. |
| 4[1] | LRCIN | IN | Left/Right Word Clock. Frequency is equal to $f_S$. |
| 5 | DIN | IN | Serial Audio Data Input. |
| 6 | BCKIN | IN | Bit Clock for Loading in Audio Data. |
| 7 | ZERO | OUT | Zero Data Flag. This pin is "LOW" when the input data is continuously zero for 65, 536 periods of BCKIN. |
| 8 | NC | — | No Connection. |
| 9 | $V_{OUT}R$ | OUT | Right-Channel Analog Line Output. |
| 10 | AGND | PWR | Analog Ground. |
| 11 | $P_{IN}R$ | IN | Input for Headphone Amplifier, Right-Channel. |
| 12 | PCOM | PWR | Headphone Amplifier Common. Bypass with 100µF. |
| 13 | $P_{OUT}R$ | OUT | Right-Channel Headphone Amplifier Output. |
| 14 | PAGND | PWR | Headphone Amplifier Ground. |
| 15 | PVCC | PWR | +5V Headphone Amplifier Power Supply. |
| 16 | $P_{OUT}L$ | OUT | Left-Channel Headphone Amplifier Output. |
| 17[1] | PMUTE | IN | Mute Control for Headphone Amplifier. |
| 18 | $P_{IN}L$ | IN | Input for Headphone Amplifier, Left-Channel. |
| 19 | $V_{CC}$ | PWR | +5V Analog Power Supply. |
| 20 | $V_{OUT}L$ | OUT | Left-Channel Analog Line Output. |
| 21 | COM | PWR | Line Out Common. Bypass with 10µF. |
| 22 | NC | — | No Connection. |
| 23[1] | RSTB | IN | External Reset Control. |
| 24[1] | MD | IN | Data for Serial Control. |
| 25[1] | MC | IN | Clock for Serial Control. |
| 26[1] | ML | IN | Latch for Serial Control. |
| 27 | CLKO | OUT | System Clock ($256f_S$ or $384f_S$) Output. |
| 28 | XTO | OUT | Crystal Oscillator Output. |

NOTE: (1) With internal pull-up.

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# PCM1720

www.burr-brown.com/databook/PCM1720.html

## SoundPLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER MPEG2/AC-3 COMPATIBLE

## FEATURES

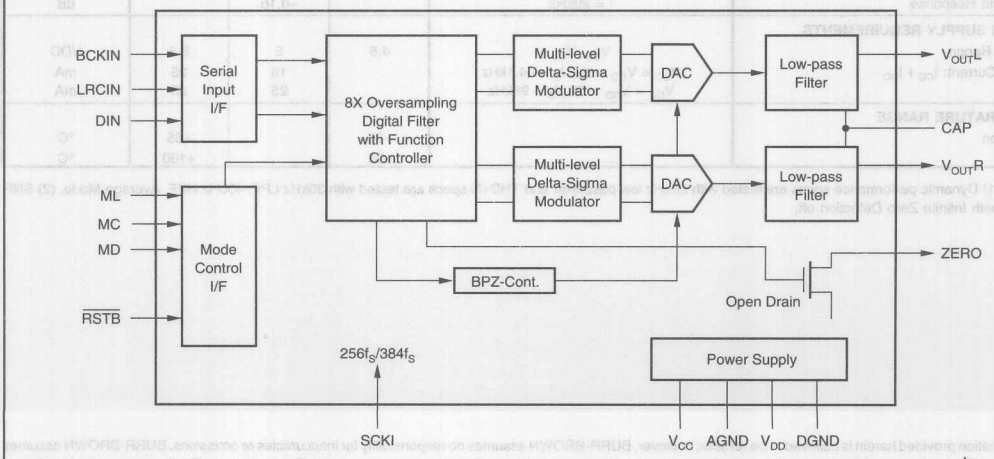
- ACCEPTS 16-, 20-, OR 24-BIT INPUT DATA
- COMPLETE STEREO DAC: Includes Digital Filter and Output Amp
- DYNAMIC RANGE: 96dB
- MULTIPLE SAMPLING FREQUENCIES: 16kHz to 96kHz
  8X Oversampling at All Sampling Frequencies
- SYSTEM CLOCK: $256f_S/384f_S$
- NORMAL OR I²S DATA INPUT FORMATS
- SELECTABLE FUNCTIONS:
  Soft Mute
  Digital Attenuator (256 Steps)
  Digital De-emphasis
- OUTPUT MODE: Left, Right, Mono, Mute

## DESCRIPTION

The PCM1720 is a complete low cost stereo audio digital-to-analog converter (DAC), operating off of a $256f_S$ or $384f_S$ system clock. The DAC contains a 3rd-order ΔΣ modulator, a digital interpolation filter, and an analog output amplifier. The PCM1720 can accept 16-, 20-, or 24-bit input data in either normal or I²S formats.

The digital filter performs an 8X interpolation function and includes selectable features such as soft mute, digital attenuation and digital de-emphasis. The PCM1720 can accept standard digital audio sampling frequencies as well as one-half and double sampling frequencies.

The PCM1720 is ideal for applications which combine compressed audio and video data such as DVD, DVD-ROM, set-top boxes and MPEG sound cards.



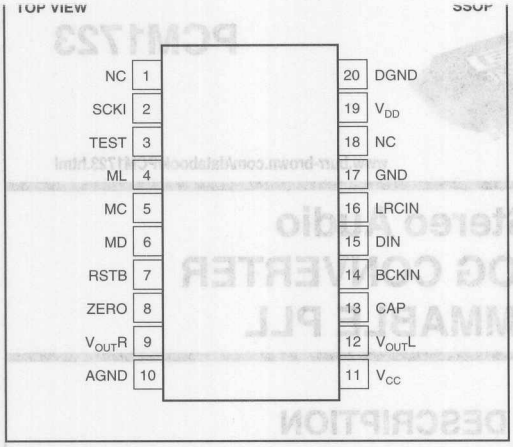

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All specifications at +25°C, $+V_{CC} = +V_{DD} = +5V$, $f_S = 44.1kHz$, and 16-bit input data, SYSCLK = $384f_S$, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1720 MIN | PCM1720 TYP | PCM1720 MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | 16 | | 24 | Bits |
| **DATA FORMAT** | | | | | |
| Audio Data Format | | | Standard/I²S | | |
| Data Bit Length | | | 16/20/24 | | |
| | | | Selectable | | |
| Sampling Frequency ($f_S$) | Standard $f_S$ | 32 | 44.1 | 48 | kHz |
| | One-half $f_S$ | 16 | 22.05 | 24 | kHz |
| | Double $f_S$ | 64 | 88.2 | 96 | kHz |
| Internal System Clock Frequency | | | $256f_S/384f_S$ | | |
| **DIGITAL INPUT/OUTPUT LOGIC LEVEL** | | | TTL | | |
| **DYNAMIC PERFORMANCE**(1) | | | | | |
| THD+N at $f_S$ (0dB) | $f_S$ = 44.1kHz | | –90 | –80 | dB |
| | $f_S$ = 96kHz | | –88 | | dB |
| THD+N at –60dB | $f_S$ = 44.1kHz | | –34 | | dB |
| | $f_S$ = 96kHz | | –31 | | dB |
| Dynamic Range | $f_S$ = 44.1kHz | 90 | 96 | | dB |
| | $f_S$ = 96kHz | | 93 | | dB |
| Signal-to-Noise Ratio(2) | $f_S$ = 44.1kHz | 92 | 100 | | dB |
| | $f_S$ = 96kHz | | 97 | | dB |
| Channel Separation | $f_S$ = 44.1kHz | 90 | 97 | | dB |
| **DC ACCURACY** | | | | | |
| Gain Error | | | ±1.0 | ±5.0 | % of FSR |
| Gain Mismatch, Channel-to-Channel | | | ±1.0 | ±5.0 | % of FSR |
| Bipolar Zero Error | $V_{OUT} = V_{CC}/2$ at BPZ | | ±30 | | mV |
| **ANALOG OUTPUT** | | | | | |
| Output Voltage | Full Scale (0dB) | | 0.62 x $V_{CC}$ | | Vp-p |
| Center Voltage | | | $V_{CC}/2$ | | VDC |
| Load Impedance | AC Load | 5 | | | kΩ |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Passband | | | | 0.445 | $f_S$ |
| Stopband | | 0.555 | | | $f_S$ |
| Passband Ripple | | | | ±0.17 | dB |
| Stopband Attenuation | | –35 | | | dB |
| Delay Time | | | $11.125/f_S$ | | sec |
| De-emphasis Error | | –0.2 | | +0.55 | dB |
| **INTERNAL ANALOG FILTER** | | | | | |
| –3dB Bandwidth | | | 100 | | kHz |
| Passband Response | f = 20kHz | | –0.16 | | dB |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range | $V_{DD}$, $V_{CC}$ | 4.5 | 5 | 5.5 | VDC |
| Supply Current: $I_{CC} + I_{DD}$ | $V_{CC} = V_{DD} = 5V$, $f_S = 44.1kHz$ | | 18 | 25 | mA |
| | $V_{CC} = V_{DD} = 5V$, $f_S = 96kHz$ | | 25 | 35 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Operation | | –25 | | +85 | °C |
| Storage | | –55 | | +100 | °C |

NOTES: (1) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode. (2) SNR is tested with Infinite Zero Detection off.

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| PIN | NAME | TYPE | FUNCTION |
|---|---|---|---|
| 1 | NC | — | No Connection. |
| 2 | SCKI | IN | System Clock Input: $256f_S$ or $384f_S$. |
| 3 | TEST | OUT | Reserved for Factory Use. |
| 4* | ML | IN | Latch Enable for Serial Control Data. |
| 5* | MC | IN | Clock for Serial Control Data. |
| 6* | MD | IN | Data Input for Serial Control. |
| 7* | RSTB | IN | Reset Input. When this pin is low, the digital filters and modulators are held in reset. |
| 8 | ZERO | OUT | Zero Data Flag. This pin is low when the data is continuously zero for more than 65,535 cycles of BCKIN. |
| 9 | $V_{OUT}R$ | OUT | Right Channel Analog Output. |
| 10 | AGND | PWR | Analog Ground. |
| 11 | $V_{CC}$ | PWR | Analog Power Supply (+5V). |
| 12 | $V_{OUT}L$ | OUT | Left Channel Analog Output. |
| 13 | CAP | — | Common Pin for Analog Output Amplifiers. |
| 14* | BCKIN | IN | Bit Clock for Clocking in the Audio Data. |
| 15* | DIN | IN | Serial Audio Data Input. |
| 16* | LRCIN | IN | Left/Right Word Clock. Frequency is equal to fs. |
| 17 | GND | PWR | Ground. |
| 18 | NC | — | No Connection. |
| 19 | $V_{DD}$ | PWR | Digital Power Supply (+5V). Recommended connection is to the analog power supply. |
| 20 | DGND | PWR | Digital Ground. Recommended connection is to the digital ground plane. |

* These pins include internal pull-up resistors.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| PCM1720 | 20-Pin SSOP | 334-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

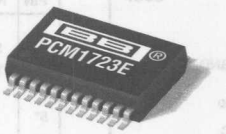
| | |
|---|---|
| Power Supply Voltage | +6.5V |
| $+V_{CC}$ to $+V_{DD}$ Difference | ±0.1V |
| Input Logic Voltage | –0.3V to ($V_{DD}$ + 0.3V) |
| Power Dissipation | 300mW |
| Operating Temperature Range | –25°C to +85°C |
| Storage Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |
| Thermal Resistance, $\theta_{JA}$ | +70°C/W |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®




# PCM1723

www.burr-brown.com/databook/PCM1723.html

## SoundPLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER WITH PROGRAMMABLE PLL

## FEATURES

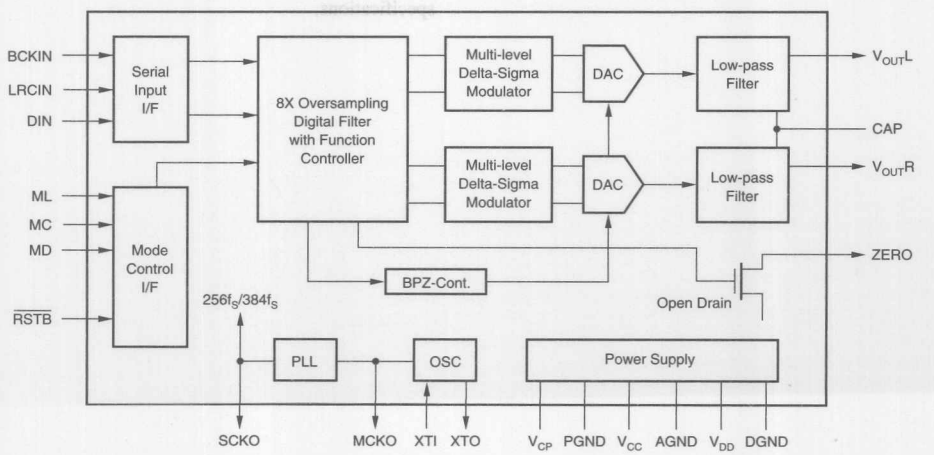
- ACCEPTS 16-, 20-, OR 24-BIT INPUT DATA
- COMPLETE STEREO DAC: Includes Digital Filter and Output Amp
- DYNAMIC RANGE: 94dB
- MULTIPLE SAMPLING FREQUENCIES:
  16kHz, 22.05kHz, 24kHz
  32kHz, 44.1kHz, 48kHz
  64kHz, 88.2kHz, 96kHz
- PROGRAMMABLE PLL CIRCUIT:
  $256f_S/384f_S$ from 27MHz Master Clock
- NORMAL OR $I^2S$ DATA INPUT FORMATS
- SELECTABLE FUNCTIONS:
  Soft Mute
  Digital Attenuator (256 Steps)
  Digital De-emphasis
- OUTPUT MODE: Left, Right, Mono, Mute

## DESCRIPTION

The PCM1723 is a complete low cost stereo audio digital-to-analog converter (DAC) with a phase-locked loop (PLL) circuit included. The PLL derives either $256f_S$ or $384f_S$ system clock from an external 27MHz reference frequency. The DAC contains a 3rd-order ΔΣ modulator, a digital interpolation filter, and an analog output amplifier. The PCM1723 can accept 16-, 20-, or 24-bit input data in either normal or $I^2S$ formats.

The digital filter performs an 8X interpolation function and includes selectable features such as soft mute, digital attenuation and digital de-emphasis. The PLL can be programmed for sampling at standard digital audio frequencies as well as one-half and double sampling frequencies.

The PCM1723 is ideal for applications which combine compressed audio and video data such as DVD, DVD-ROM, set-top boxes and MPEG sound cards.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

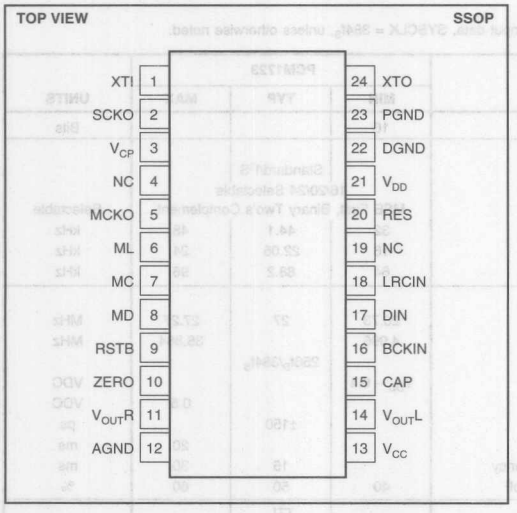
# SPECIFICATIONS

All specifications at +25°C, $+V_{CC} = +V_{DD} = +V_{CP} = +5V$, $f_S = 44.1kHz$, and 16-bit input data, SYSCLK = $384f_S$, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1723 MIN | PCM1723 TYP | PCM1723 MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | 16 | | | Bits |
| **DATA FORMAT** | | | | | |
| Audio Data Interface Format | | | Standard/I²S | | |
| Data Bit Length | | | 16/20/24 Selectable | | |
| Audio Data Format | | | MSB First, Binary Two's Complement | | |
| Sampling Frequency ($f_S$) | Standard $f_S$ | 32 | 44.1 | 48 | Selectable |
| | One-half $f_S$ | 16 | 22.05 | 24 | kHz |
| | Double $f_S$ | 64 | 88.2 | 96 | kHz |
| **PLL PERFORMANCE** | | | | | |
| Master Clock Input Frequency[4] | | 26.73 | 27 | 27.27 | MHz |
| Master Clock Output Frequency | | 4.096 | | 36.864 | MHz |
| Generated Sysclk Frequency | | | $256f_S/384f_S$ | | |
| Output Logic Level $V_{OH}$ | $I_{OH} = 2mA$ | $V_{DD} - 0.4$ | | | VDC |
| (MCKO, SCKO) $V_{OL}$ | $I_{OL} = 4mA$ | | | 0.5 | VDC |
| Generated Sysclk Jitter | Standard Dev | | ±150 | | ps |
| Generated Sysclk Transient[1] | $f_M = 27MHz$ | | | 20 | ns |
| Power-Up Time | To Programmed Frequency | | 15 | 30 | ms |
| Generated Sysclk Duty Cycle | $f_M = 27MHz$, $C_L = 15pF$ | 40 | 50 | 60 | % |
| **DIGITAL INPUT LOGIC LEVEL** | | | TTL | | |
| **DYNAMIC PERFORMANCE[2]** | | | | | |
| THD+N at $f_S$ (0dB) | fs = 44.1kHz | | –89 | –80 | dB |
| | fs = 96kHz | | –87 | | dB |
| THD+N at –60dB | fs = 44.1kHz | | –31 | | dB |
| | fs = 96kHz | | –29 | | dB |
| Dynamic Range (EIAJ Method) | fs = 44.1kHz | 90 | 94 | | dB |
| | fs = 96kHz | | 91 | | dB |
| Signal-to-Noise Ratio[3] (EIAJ Method) | fs = 44.1kHz | 90 | 96 | | dB |
| | fs = 96kHz | | 95 | | dB |
| Channel Separation | fs = 44.1kHz | 88 | 93 | | dB |
| **DC ACCURACY** | | | | | |
| Gain Error | | | ±1.0 | ±3.0 | % of FSR |
| Gain Mismatch, Channel-to-Channel | | | ±1.0 | ±2.0 | % of FSR |
| Bipolar Zero Error | $V_{OUT} = V_{CC}/2$ at BPZ | | ±30 | | mV |
| **ANALOG OUTPUT** | | | | | |
| Output Voltage | Full Scale (–0dB) | | 0.62 x $V_{CC}$ | | Vp-p |
| Center Voltage | | | $V_{CC}/2$ | | $V_{DC}$ |
| Load Impedance | AC Load | 5 | | | kΩ |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Passband | | | | 0.445 | $f_S$ |
| Stopband | | 0.555 | | | $f_S$ |
| Passband Ripple | | | | ±0.17 | dB |
| Stopband Attenuation | | –35 | | | dB |
| Delay Time | | | $11.125/f_S$ | | sec |
| De-emphasis Error | | –0.2 | | +0.55 | dB |
| **INTERNAL ANALOG FILTER** | | | | | |
| –3dB Bandwidth | | | 100 | | kHz |
| Passband Response | f = 20kHz | | –0.16 | | dB |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range | $V_{CC} = V_{DD} = V_{CP}$ | 4.5 | 5 | 5.5 | VDC |
| Supply Current: $I_{CC} + I_{DD} + I_{CP}$ | $f_S = 44.1kHz$ | | 20 | 24 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Operation | | –25 | | +85 | °C |
| Storage | | –55 | | +100 | °C |

NOTES: (1) Sysclk transient is the maximum frequency lock time when the PLL frequency is changed. (2) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode. (3) SNR is tested at Infinite Zero Detection off. (4) PLL evaluations tested with 1ns maximum jitter on the 27MHz input clock.

## PIN CONFIGURATION




## PIN ASSIGNMENTS

| PIN | NAME | TYPE | FUNCTION |
|---|---|---|---|
| 1 | XTI | IN | Master Clock Input. |
| 2 | SCKO | OUT | System Clock Out. This output is $256f_S$ or $384f_S$. system clock generated by the internal PLL. |
| 3 | $V_{CP}$ | PWR | PLL Power Supply (+5V). |
| 4 | NC | N/A | No connection. |
| 5 | MCKO | Out | Buffered clock output of crystal oscillator. |
| 6(1) | ML | IN | Latch for serial control data. |
| 7(1) | MC | IN | Clock for serial control data. |
| 8(1) | MD | IN | Data for serial control. |
| 9(1) | RSTB | IN | Reset Input. When this pin is low, the digital filters and modulators are held in reset. |
| 10 | ZERO | OUT | Zero Data Flag. This pin is low when the input data is continuously zero for more than 65, 535 cycles of BCKIN. |
| 11 | $V_{OUT}R$ | OUT | Right Channel Analog Output. |
| 12 | AGND | GND | Analog Ground. |
| 13 | $V_{CC}$ | PWR | Analog Power Supply (+5V). |
| 14 | $V_{OUT}L$ | OUT | Left Channel Analog Output. |
| 15 | CAP | | Common pin for analog output amplifiers. |
| 16(2) | BCKIN | IN | Bit clock for clocking in the audio data. |
| 17(2) | DIN | IN | Serial audio data input. |
| 18(2) | LRCIN | IN | Left/Right Word Clock. Frequency is equal to $f_S$. |
| 19 | NC | N/A | No connection. |
| 20 | RES | N/A | Reserved for factory use, do not connect. |
| 21 | $V_{DD}$ | PWR | Analog Power Supply (+5V). |
| 22 | DGND | GND | Digital Ground. |
| 23 | PGND | GND | PLL Ground. |
| 24 | XTO | Out | Crystal oscillator output. |

Note: (1) Schmitt triger input with internal pull-up resistors. (2) Schmitt triger input.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| PCM1723E | 24-Pin SSOP | 338 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | +6.5V |
| $+V_{CC}$ to $+V_{DD}$ Difference | ±0.1V |
| Input Logic Voltage | –0.3V to ($V_{DD}$ + 0.3V) |
| Input Current (except power supply) | ±10mA |
| Power Dissipation | 530mW |
| Operating Temperature Range | –25°C to +85°C |
| Storage Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |
| Thermal Resistance, $\theta_{JA}$ | +70°C/W |

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# PCM1725

www.burr-brown.com/databook/PCM1725.html

## SoundPLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER 16 Bits, 96kHz Sampling

## FEATURES

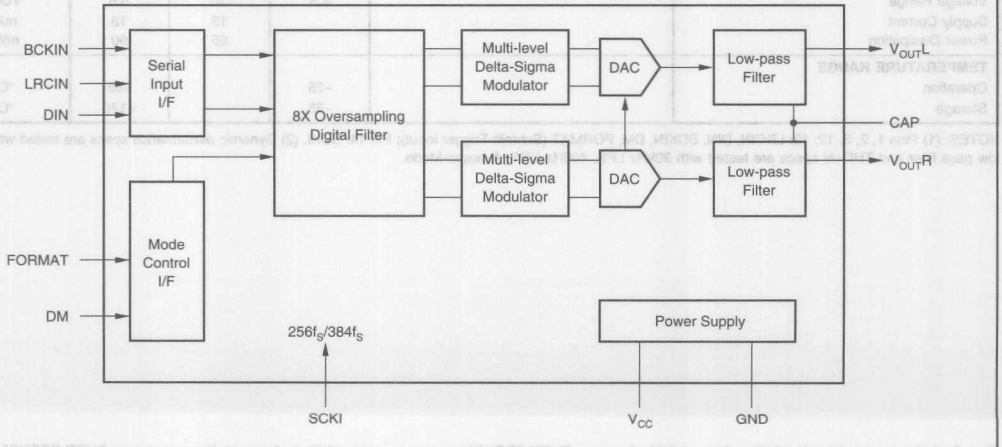
- COMPLETE STEREO DAC: Includes Digital Filter and Output Amp
- DYNAMIC RANGE: 95dB
- MULTIPLE SAMPLING FREQUENCIES: 16kHz to 96kHz
- 8X OVERSAMPLING DIGITAL FILTER
- SYSTEM CLOCK: $256f_S/384f_S$
- NORMAL OR I²S DATA INPUT FORMATS
- SMALL 14-PIN SOIC PACKAGE

## DESCRIPTION

The PCM1725 is a complete low cost stereo audio digital-to-analog converter (DAC), operating off of a $256f_S$ or $384f_S$ system clock. The DAC contains a 3rd-order ΔΣ modulator, a digital interpolation filter, and an analog output amplifier. The PCM1725 accepts 16-bit input data in either normal or I²S formats.

The digital filter performs an 8X interpolation function and includes de-emphasis at 44.1kHz. The PCM1725 can accept digital audio sampling frequencies from 16kHz to 96kHz, always at 8X oversampling.

The PCM1725 is ideal for low-cost, CD-quality consumer audio applications.






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# SPECIFICATIONS

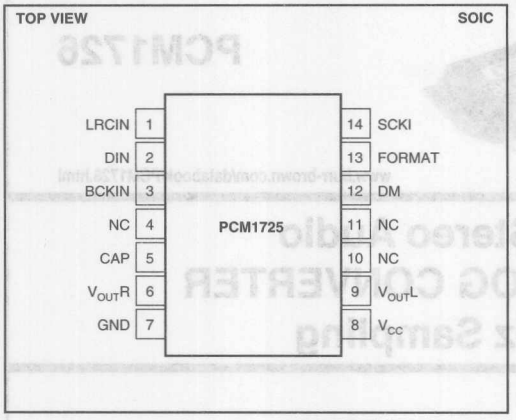
All specifications at +25°C, $+V_{CC}$ = +5V, $f_S$ = 44.1kHz, and 16-bit input data, SYSCLK = $384f_S$, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1725 MIN | PCM1725 TYP | PCM1725 MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | 16 | | Bits |
| **DATA FORMAT** | | | | | |
| Audio Data Interface Format | | | Standard/I²S | | |
| Audio Data Format | | | Binary Two's Complement | | |
| Sampling Frequency ($f_S$) | | 16 | | 96 | kHz |
| Internal System Clock Frequency | | | $256f_S$/$384f_S$ | | |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic Level | | | TTL | | |
| Input Logic Level | | | | | |
| $V_{IH}$(1) | | 2.0 | | | VDC |
| $V_{IL}$(1) | | | | 0.8 | VDC |
| Input Logic Current: $I_{IN}$(1) | | | | ±0.8 | µA |
| **DYNAMIC PERFORMANCE**(2) | f = 991kHz | | | | |
| THD+N at FS (0dB) | | | –83 | –78 | dB |
| THD+N at –60dB | | | –32 | | dB |
| Dynamic Range | A-weighted | 90 | 95 | | dB |
| Signal-to-Noise Ratio | A-weighted | 90 | 97 | | dB |
| Channel Separation | | 88 | 95 | | dB |
| **DC ACCURACY** | | | | | |
| Gain Error | | | ±1.0 | ±5.0 | % of FSR |
| Gain Mismatch, Channel-to-Channel | | | ±1.0 | ±5.0 | % of FSR |
| Bipolar Zero Error | $V_{OUT} = V_{CC}/2$ at BPZ | | ±20 | ±50 | mV |
| **ANALOG OUTPUT** | | | | | |
| Output Voltage | Full Scale (0dB) | | 0.62 x $V_{CC}$ | | Vp-p |
| Center Voltage | | | $V_{CC}/2$ | | VDC |
| Load Impedance | AC Load | 10 | | | kΩ |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Passband | | | | 0.445 | $f_S$ |
| Stopband | | 0.555 | | | $f_S$ |
| Passband Ripple | | | | ±0.17 | dB |
| Stopband Attenuation | | –35 | | | dB |
| Delay Time | | | 11.125/$f_S$ | | sec |
| **INTERNAL ANALOG FILTER** | | | | | |
| –3dB Bandwidth | | | 100 | | kHz |
| Passband Response | f = 20kHz | | –0.16 | | dB |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range | | 4.5 | 5 | 5.5 | VDC |
| Supply Current | | | 13 | 18 | mA |
| Power Dissipation | | | 65 | 90 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Operation | | –25 | | +85 | °C |
| Storage | | –55 | | +125 | °C |

NOTES: (1) Pins 1, 2, 3, 12, 13: LRCIN, DIN, BCKIN, DM, FORMAT (Schmitt Trigger Input); Pin 14: SCKI. (2) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN CONFIGURATION




## PIN ASSIGNMENTS

| PIN | NAME | I/O | FUNCTION |
|---|---|---|---|
| 1[1] | LRCIN | IN | Sample Rate Clock Input |
| 2[1] | DIN | IN | Audio Data Input |
| 3[1] | BCKIN | IN | Bit Clock Input for Audio Data. |
| 4 | NC | — | No Connection |
| 5 | CAP | — | Common Pin of Analog Output Amp |
| 6 | $V_{OUT}R$ | OUT | Right-Channel Analog Output |
| 7 | GND | — | Ground |
| 8 | $V_{CC}$ | — | Power Supply |
| 9 | $V_{OUT}L$ | OUT | Left-Channel Analog Output |
| 10 | NC | — | No Connection |
| 11 | NC | — | No Connection |
| 12[2] | DM | IN | De-emphasis Control<br>HIGH: De-emphasis ON<br>LOW: De-emphasis OFF |
| 13[2] | FORMAT | — | Audio Data Format Select<br>HIGH: I²S Data Format<br>LOW: Standard Data Format |
| 14 | SCKI | IN | System Clock Input ($256f_S$ or $384f_S$) |

NOTES: (1) Schmitt Trigger input. (2) Schmitt Trigger input with internal pull-up.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| PCM1725U | 14 Pin SOIC | 235 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | +6.5V |
| $+V_{CC}$ to $+V_{DD}$ Difference | ±0.1V |
| Input Logic Voltage | –0.3V to ($V_{DD}$ + 0.3V) |
| Power Dissipation | 290mW |
| Operating Temperature Range | –25°C to +85°C |
| Storage Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |
| Thermal Resistance, $\theta_{JA}$ | +90°C/W |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®




# PCM1726

www.burr-brown.com/databook/PCM1726.html

## SoundPLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER 16 Bits, 96kHz Sampling

## FEATURES

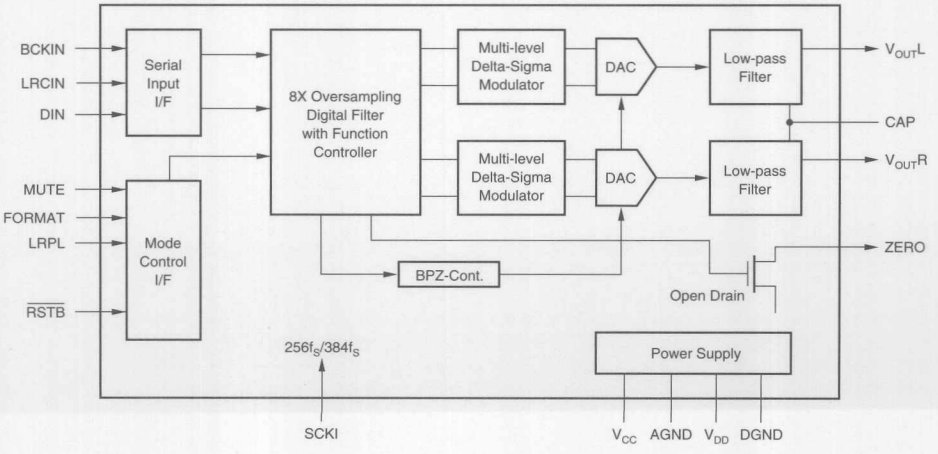
- COMPLETE STEREO DAC: Includes Digital Filter and Output Amp
- DYNAMIC RANGE: 96dB
- MULTIPLE SAMPLING FREQUENCIES: 16kHz to 96kHz 8X Oversampling at All Sampling Frequencies
- SYSTEM CLOCK: $256f_S/384f_S$
- NORMAL OR I²S DATA INPUT FORMATS
- SOFT MUTE

## DESCRIPTION

The PCM1726 is a complete low cost stereo audio digital-to-analog converter (DAC), operating off of a $256f_S$ or $384f_S$ system clock. The DAC contains a 3rd-order ΔΣ modulator, a digital interpolation filter, and an analog output amplifier. The PCM1726 accepts 16-bit input data in either normal or I²S formats.

The digital filter performs an 8X interpolation function and includes soft mute. The PCM1726 can accept standard digital audio sampling frequencies as well as one-half and double sampling frequencies.

The PCM1726 is ideal for applications which combine compressed audio and video data such as DVD, DVD-ROM, set-top boxes and MPEG sound cards.




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# SPECIFICATIONS

All specifications at +25°C, $+V_{CC} = +V_{DD} = +5V$, $f_S = 44.1kHz$, and 16-bit input data, SYSCLK = $384f_S$, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1726 MIN | PCM1726 TYP | PCM1726 MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | | 16 | Bits |
| **DATA FORMAT** | | | | | |
| Audio Data Format | | | Standard/I²S | | |
| Data Bit Length | | | 16 | | |
| Sampling Frequency ($f_S$) | | 16 | | 96 | kHz |
| Internal System Clock Frequency | | | $256f_S/384f_S$ | | |
| **DIGITAL INPUT/OUTPUT LOGIC LEVEL** | | | TTL | | |
| **DYNAMIC PERFORMANCE**[1] | | | | | |
| THD+N at $f_S$ (0dB) | $f_S$ = 44.1kHz | | –90 | –80 | dB |
| | $f_S$ = 96kHz | | –88 | | dB |
| THD+N at –60dB | $f_S$ = 44.1kHz | | –34 | | dB |
| | $f_S$ = 96kHz | | –31 | | dB |
| Dynamic Range | $f_S$ = 44.1kHz | 90 | 96 | | dB |
| | $f_S$ = 96kHz | | 93 | | dB |
| Signal-to-Noise Ratio[2] | $f_S$ = 44.1kHz | 92 | 100 | | dB |
| | $f_S$ = 96kHz | | 97 | | dB |
| Channel Separation | $f_S$ = 44.1kHz | 90 | 97 | | dB |
| **DC ACCURACY** | | | | | |
| Gain Error | | | ±1.0 | ±5.0 | % of FSR |
| Gain Mismatch, Channel-to-Channel | | | ±1.0 | ±5.0 | % of FSR |
| Bipolar Zero Error | $V_{OUT} = V_{CC}/2$ at BPZ | | ±30 | | mV |
| **ANALOG OUTPUT** | | | | | |
| Output Voltage | Full Scale (0dB) | | 0.62 x $V_{CC}$ | | Vp-p |
| Center Voltage | | | $V_{CC}/2$ | | VDC |
| Load Impedance | AC Load | 5 | | | kΩ |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Passband | | | | 0.445 | $f_S$ |
| Stopband | | 0.555 | | | $f_S$ |
| Passband Ripple | | | | ±0.17 | dB |
| Stopband Attenuation | | –35 | | | dB |
| Delay Time | | | $11.125/f_S$ | | sec |
| **INTERNAL ANALOG FILTER** | | | | | |
| –3dB Bandwidth | | | 100 | | kHz |
| Passband Response | f = 20kHz | | –0.16 | | dB |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range | $V_{DD}$, $V_{CC}$ | 4.5 | 5 | 5.5 | VDC |
| Supply Current: $I_{CC} + I_{DD}$ | $V_{CC} = V_{DD} = 5V$, $f_S$ = 44.1kHz | | 18 | 25 | mA |
| | $V_{CC} = V_{DD} = 5V$, $f_S$ = 96kHz | | 25 | 35 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Operation | | –25 | | +85 | °C |
| Storage | | –55 | | +100 | °C |

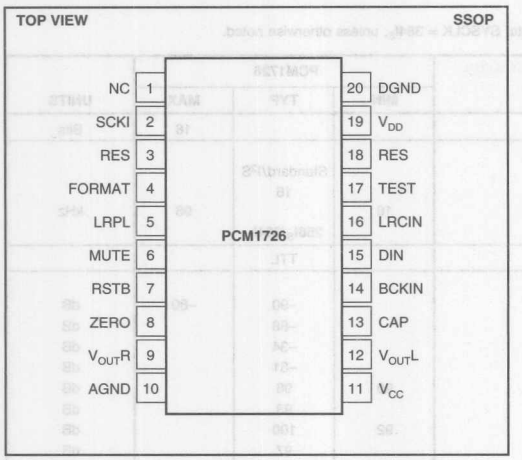
NOTES: (1) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode. (2) SNR is tested with Infinite Zero Detection off.



The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN CONFIGURATION

TOP VIEW — SSOP




## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| PCM1726E | 20-Pin SSOP | 334-1 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | +6.5V |
| $+V_{CC}$ to $+V_{DD}$ Difference | ±0.1V |
| Input Logic Voltage | –0.3V to ($V_{DD}$ + 0.3V) |
| Power Dissipation | 300mW |
| Operating Temperature Range | –25°C to +85°C |
| Storage Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |
| Thermal Resistance, $\theta_{JA}$ | +70°C/W |

## PIN ASSIGNMENTS

| PIN | NAME | TYPE | FUNCTION |
|---|---|---|---|
| 1 | NC | — | No Connection. |
| 2 | SCKI | IN | System Clock Input: $256f_S$ or $384f_S$. |
| 3 | RES | — | Reserved for Factory Use. Do not connect. |
| 4[1] | FORMAT | IN | Input Data Format Control. |
| 5[1] | LRPL | IN | Left/Right Polarity Control. |
| 6[1] | MUTE | IN | Soft Mute Control. |
| 7[1] | RSTB | IN | Reset Input. When this pin is low, the digital filters and modulators are held in reset. |
| 8 | ZERO | OUT | Zero Data Flag. This pin is low when the data is continuously zero for more than 65,535 cycles of BCKIN. |
| 9 | $V_{OUT}R$ | OUT | Right Channel Analog Output. |
| 10 | AGND | PWR | Analog Ground. |
| 11 | $V_{CC}$ | PWR | Analog Power Supply (+5V). |
| 12 | $V_{OUT}L$ | OUT | Left Channel Analog Output. |
| 13 | CAP | — | Common Pin for Analog Output Amplifiers. |
| 14[1] | BCKIN | IN | Bit Clock for Clocking in the Audio Data. |
| 15[1] | DIN | IN | Serial Audio Data Input. |
| 16[1] | LRCIN | IN | Left/Right Word Clock. Frequency is equal to $f_S$. |
| 17 | TEST | — | Must be Tied to Ground. |
| 18 | RES | — | Do Not Connect. |
| 19 | $V_{DD}$ | PWR | Digital Power Supply (+5V). Recommended connection is to the analog power supply. |
| 20 | DGND | PWR | Digital Ground. Recommended connection is to the digital ground plane. |

NOTE: (1) These pins include internal pull-up resistors.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®




# PCM1727

www.burr-brown.com/databook/PCM1727.html

## SoundPLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER WITH PROGRAMMABLE DUAL PLL

## FEATURES

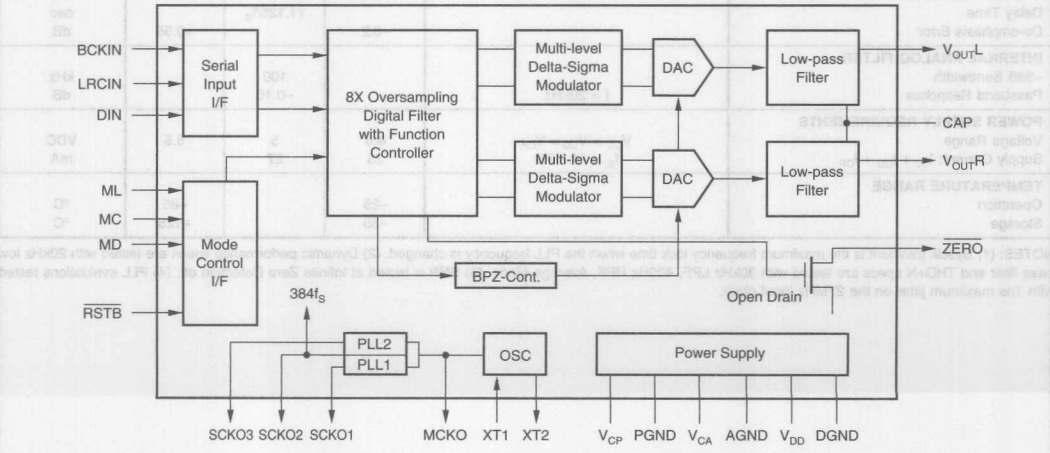
- ACCEPTS 16-, 20-, OR 24-BIT INPUT DATA
- COMPLETE STEREO DAC: Includes Digital Filter and Output Amp
- DYNAMIC RANGE: 92dB
- MULTIPLE SAMPLING FREQUENCIES: $f_S$ = 44.1kHz, 48kHz, 96kHz
- PROGRAMMABLE DUAL PLL CIRCUIT: 27MHz Master Clock Input
- GENERATED SYSTEM CLOCK
  SCKO1: 33.8688MHz
  SCK02: $384f_S$
  SCK03: $768f_S$ (44.1k/48kHz)
  $384f_S$ (96kHz)
- NORMAL OR I²S DATA INPUT FORMATS
- SELECTABLE FUNCTIONS:
  Soft Mute, Analog Output Mode
  Digital Attenuator (256 Steps)
  Digital De-emphasis
- +5V SINGLE POWER SUPPLY

## DESCRIPTION

The PCM1727 is a complete low cost stereo audio digital-to-analog converter (DAC) with a dual phase-locked loop (PLL) circuit included. PLL-1 derives a fixed 33.8688MHz ($768f_S$, $f_S$ = 44.1kHz) system clock (SCKO-1), and PLL-2 derives both the $384f_S$ ($f_S$ = 44.1k/48k/96kHz) system clock (SCKO-2), and the $768f_S$ ($f_S$ = 44.1k/48kHz)/$384f_S$ ($f_S$ = 96kHz) system clock (SCKO-3) from an external 27MHz reference frequency. The DAC contains a 3rd-order ΔΣ modulator, a digital interpolation filter, and an analog output amplifier. The PCM1727 can accept 16-, 20-, or 24-bit input data in either normal or I²S formats.

The digital filter performs an 8X interpolation function and includes selectable features such as soft mute, digital attenuation and digital de-emphasis.

The PCM1727 is ideal for applications which combine compressed audio and video data such as DVD, DVD Audio with CD-DA compatibility, karaoke DSP.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

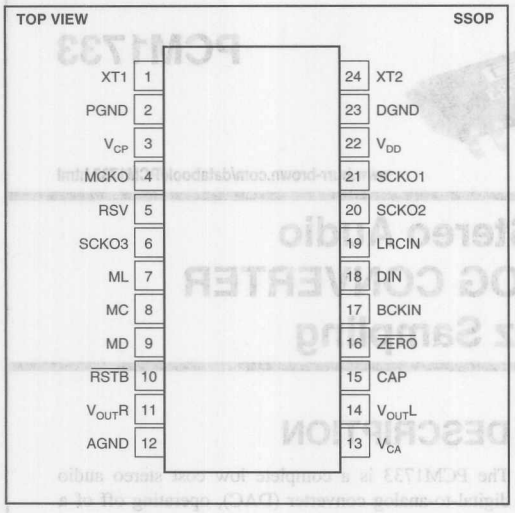
# SPECIFICATIONS

All specifications at +25°C, $+V_{CA} = +V_{DD} = +V_{CP} = +5V$, $f_S = 44.1kHz$, and 16-bit input data, SYSCLK = $384f_S$, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1727 MIN | PCM1727 TYP | PCM1727 MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | 16 | | | Bits |
| **DATA FORMAT** | | | | | |
| Audio Data Interface Format | | | Standard/I²S | | |
| Data Bit Length | | | 16/20/24 Selectable | | |
| Audio Data Format | | | MSB First, 2's Comp | | |
| Sampling Frequency ($f_S$) | | 44.1 | | 96 | Selectable kHz |
| **PLL PERFORMANCE** | | | | | |
| Master Clock Input Frequency[4] | | 26.73 | 27 | 27.27 | MHz |
| Generated System Clock | | | | | |
| SCKO-1 | $768f_S$ ($f_S$ = 44.1k) | | 33.8688 | | MHz |
| SCKO-2 | $384f_S$ | 16.9344 | | 36.8640 | MHz |
| SCKO-3 | $768f_S$ ($f_S$ = 44.1k/48k), $384f_S$ ($f_S$ = 96k) | 33.8688 | | 36.8640 | MHz |
| Output Logic Level $V_{OH}$ | $I_{OH}$ = 2mA | $V_{DD}$ – 0.4 | | | VDC |
| (MCKO, SCKO 1 ~ 3) $V_{OL}$ | $I_{OL}$ = 4mA | | | 0.5 | VDC |
| Generated Sysclk Jitter | Standard Dev | | ±150 | | ps |
| Generated Sysclk Transient[1] | $f_M$ = 27MHz | | | 20 | ms |
| Power-Up Time | To Programmed Frequency | | 15 | 30 | ms |
| Generated Sysclk Duty Cycle | $f_M$ = 27MHz, $C_L$ = 15pF | 40 | 50 | 60 | % |
| **DIGITAL INPUT LOGIC LEVEL** | | | TTL | | |
| **DYNAMIC PERFORMANCE[2]** | | | | | |
| THD+N at $f_S$ (0dB) | $f_S$ = 44.1kHz | | –89 | –80 | dB |
| | $f_S$ = 96kHz | | –87 | | dB |
| THD+N at –60dB | $f_S$ = 44.1kHz | | –31 | | dB |
| | $f_S$ = 96kHz | | –29 | | dB |
| Dynamic Range (EIAJ Method) | $f_S$ = 44.1kHz | 90 | 92 | | dB |
| | $f_S$ = 96kHz | | 90 | | dB |
| Signal-to-Noise Ratio[3] (EIAJ Method) | $f_S$ = 44.1kHz | 90 | 94 | | dB |
| | $f_S$ = 96kHz | | 90 | | dB |
| Channel Separation | $f_S$ = 44.1kHz | 88 | 93 | | dB |
| **DC ACCURACY** | | | | | |
| Gain Error | | | ±1.0 | ±3.0 | % of FSR |
| Gain Mismatch, Channel-to-Channel | | | ±1.0 | ±2.0 | % of FSR |
| Bipolar Zero Error | $V_{OUT} = V_{CC}/2$ at BPZ | | ±30 | | mV |
| **ANALOG OUTPUT** | | | | | |
| Output Voltage | Full Scale (–0dB) | | 0.62 x $V_{CA}$ | | Vp-p |
| Center Voltage | | | $V_{CA}/2$ | | $V_{DC}$ |
| Load Impedance | AC Load | 5 | | | kΩ |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Passband | | | | 0.445 | $f_S$ |
| Stopband | | 0.555 | | | $f_S$ |
| Passband Ripple | | | | ±0.17 | dB |
| Stopband Attenuation | | –35 | | | dB |
| Delay Time | | | 11.125/$f_S$ | | sec |
| De-emphasis Error | | –0.2 | | +0.55 | dB |
| **INTERNAL ANALOG FILTER** | | | | | |
| –3dB Bandwidth | | | 100 | | kHz |
| Passband Response | f = 20kHz | | –0.16 | | dB |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range | $V_{CC} = V_{DD} = V_{CP}$ | 4.5 | 5 | 5.5 | VDC |
| Supply Current: $I_{CC} + I_{DD} + I_{CP}$ | $f_S$ = 44.1kHz | 25 | 27 | | mA |
| **TEMPERATURE RANGE** | | | | | |
| Operation | | –25 | | +85 | °C |
| Storage | | –55 | | +125 | °C |

NOTES: (1) Sysclk transient is the maximum frequency lock time when the PLL frequency is changed. (2) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode. (3) SNR is tested at Infinite Zero Detection off. (4) PLL evaluations tested with 1ns maximum jitter on the 27MHz input clock.

## PIN CONFIGURATION




## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| PCM1727E | 24-Pin SSOP | 338 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | +6.5V |
| $+V_{CC}$ to $+V_{DD}$ Difference | ±0.1V |
| Input Logic Voltage | –0.3V to ($V_{DD}$ + 0.3V) |
| Input Current (except power supply) | ±10mA |
| Power Dissipation | 300mW |
| Operating Temperature Range | –25°C to +85°C |
| Storage Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |
| Thermal Resistance, $\theta_{JA}$ | +70°C/W |

## PIN ASSIGNMENTS

| PIN | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| 1 | XT1 | IN | 27MHz Crystal or External Clock Input |
| 2 | PGND | — | PLL Ground |
| 3 | $V_{CP}$ | — | PLL Power Supply (+5V) |
| 4 | MCKO | OUT | Buffered Clock Output of Crystal Oscillator |
| 5 | RSV | — | Reserve; This pin should be open. |
| 6 | SCKO3 | OUT | System Clock Out 3; This output is 768$f_S$ or 384$f_S$. |
| 7 | ML | IN | Latch Enable Input for Serial Interface Mode[2] |
| 8 | MC | IN | Bit Clock Input for Serial Interface Mode[2] |
| 9 | MD | IN | Serial Data Input for Serial Interface Mode[2] |
| 10 | $\overline{RSTB}$ | IN | Reset; When this pin is low, the DF and modulator are held in reset. |
| 11 | $V_{OUT}R$ | OUT | Right Channel, Analog Voltage Output of Audio Signal |
| 12 | AGND | — | Analog Ground |
| 13 | $V_{CA}$ | — | Analog Power Supply (+5V) |
| 14 | $V_{OUT}L$ | OUT | Left Channel, Analog Voltage Output of Audio Signal |
| 15 | CAP | — | Common Pin of Analog Output Amp |
| 16 | $\overline{ZERO}$ | OUT | Zero Data Flag; This pin is low when the input data is continuously zero for more than 65,535 cycles of BCKIN[1]. |
| 17 | BCKIN | IN | Bit Clock Input for Serial Audio Data[3] |
| 18 | DIN | IN | Serial Audio Data Input[3] |
| 19 | LRCIN | IN | Left and Right Clock (sampling rate–$f_S$)[3] |
| 20 | SCKO2 | OUT | System Clock Out 2; This output is 256$f_S$ or 384$f_S$ system clock. |
| 21 | SCKO1 | OUT | System Clock Out 1; This output is 33.8688MHz system clock. |
| 22 | $V_{DD}$ | — | Digital Power (+5V) |
| 23 | DGND | — | Digital Ground |
| 24 | XT2 | — | 27MHz Crystal. Connected to GND at external clock. |

Note: (1) Open Drain Output. (2) Schmitt triger input with internal pull-up resistors. (3) Schmitt triger input.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# PCM1733

www.burr-brown.com/databook/PCM1733.html

## SoundPLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER 18 Bits, 96kHz Sampling

## FEATURES

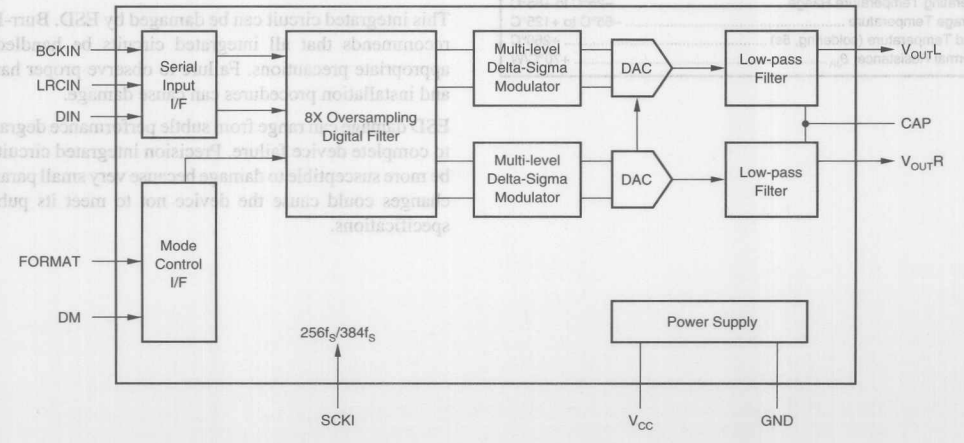
- COMPLETE STEREO DAC: Includes Digital Filter and Output Amp
- DYNAMIC RANGE: 95dB
- MULTIPLE SAMPLING FREQUENCIES: 16kHz to 96kHz
- 8X OVERSAMPLING DIGITAL FILTER
- SYSTEM CLOCK: $256f_S/384f_S$
- NORMAL OR I²S DATA INPUT FORMATS
- SMALL 14-PIN SOIC PACKAGE

## DESCRIPTION

The PCM1733 is a complete low cost stereo audio digital-to-analog converter (DAC), operating off of a $256f_S$ or $384f_S$ system clock. The DAC contains a 3rd-order ΔΣ modulator, a digital interpolation filter, and an analog output amplifier. The PCM1733 accepts 18-bit input data in either normal or I²S formats.

The digital filter performs an 8X interpolation function and includes de-emphasis at 44.1kHz. The PCM1733 can accept digital audio sampling frequencies from 16kHz to 96kHz, always at 8X oversampling.

The PCM1733 is ideal for low-cost, CD-quality consumer audio applications.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

All specifications at +25°C, $+V_{CC}$ = +5V, $f_S$ = 44.1kHz, and 18-bit input data, SYSCLK = $384f_S$, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1733 MIN | PCM1733 TYP | PCM1733 MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | 18 | | Bits |
| **DATA FORMAT** | | | | | |
| Audio Data Interface Format | | | Standard/I²S | | |
| Audio Data Format | | | Two's Binary Complement | | |
| Sampling Frequency ($f_S$) | | 16 | | 96 | kHz |
| Internal System Clock Frequency | | | $256f_S/384f_S$ | | |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic Level | | | TTL | | |
| Input Logic Level | | | | | |
| $V_{IH}$(1) | | 2.0 | | | VDC |
| $V_{IL}$(1) | | | | 0.8 | VDC |
| Input Logic Current: $I_{IN}$(1) | | | | ±0.8 | µA |
| **DYNAMIC PERFORMANCE**(2) | f = 991kHz | | | | |
| THD+N at FS (0dB) | | | –83 | –78 | dB |
| THD+N at –60dB | | | –32 | | dB |
| Dynamic Range | EIAJ, A-weighted | 90 | 95 | | dB |
| Signal-to-Noise Ratio | EIAJ, A-weighted | 90 | 97 | | dB |
| Channel Separation | | 88 | 95 | | dB |
| **DC ACCURACY** | | | | | |
| Gain Error | | | ±1.0 | ±5.0 | % of FSR |
| Gain Mismatch, Channel-to-Channel | | | ±1.0 | ±5.0 | % of FSR |
| Bipolar Zero Error | $V_{OUT} = V_{CC}/2$ at BPZ | | ±20 | ±50 | mV |
| **ANALOG OUTPUT** | | | | | |
| Output Voltage | Full Scale (0dB) | | 0.62 x $V_{CC}$ | | Vp-p |
| Center Voltage | | | $V_{CC}/2$ | | VDC |
| Load Impedance | AC Load | 10 | | | kΩ |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Passband | | | | 0.445 | $f_S$ |
| Stopband | | 0.555 | | | $f_S$ |
| Passband Ripple | | | | ±0.17 | dB |
| Stopband Attenuation | | –35 | | | dB |
| Delay Time | | | $11.125/f_S$ | | sec |
| **INTERNAL ANALOG FILTER** | | | | | |
| –3dB Bandwidth | | | 100 | | kHz |
| Passband Response | f = 20kHz | | –0.16 | | dB |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range | | 4.5 | 5 | 5.5 | VDC |
| Supply Current | | | 13 | 18 | mA |
| Power Dissipation | | | 65 | 90 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Operation | | –25 | | +85 | °C |
| Storage | | –55 | | +125 | °C |

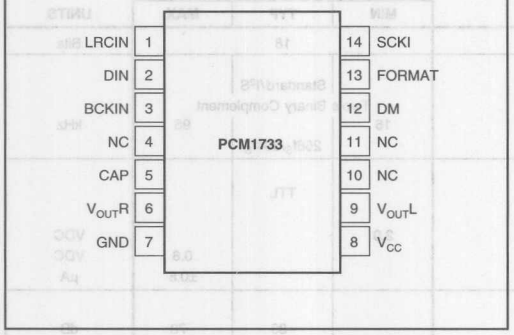
NOTES: (1) Pins 1, 2, 3, 12, 13, 14: LRCIN, DIN, BCKIN, DM, FORMAT, SCKI. (2) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode.



The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN CONFIGURATION

TOP VIEW — SOIC




## PIN ASSIGNMENTS

| PIN | NAME | I/O | FUNCTION |
|---|---|---|---|
| 1(1) | LRCIN | IN | Sample Rate Clock Input |
| 2(1) | DIN | IN | Audio Data Input |
| 3(1) | BCKIN | IN | Bit Clock Input for Audio Data. |
| 4 | NC | — | No Connection |
| 5 | CAP | — | Common Pin of Analog Output Amp |
| 6 | $V_{OUT}R$ | OUT | Right-Channel Analog Output |
| 7 | GND | — | Ground |
| 8 | $V_{CC}$ | — | Power Supply |
| 9 | $V_{OUT}L$ | OUT | Left-Channel Analog Output |
| 10 | NC | — | No Connection |
| 11 | NC | — | No Connection |
| 12(2) | DM | IN | De-emphasis Control<br>HIGH: De-emphasis ON<br>LOW: De-emphasis OFF |
| 13(2) | FORMAT | IN | Audio Data Format Select<br>HIGH: I²S Data Format<br>LOW: Standard Data Format |
| 14 | SCKI | IN | System Clock Input ($256f_S$ or $384f_S$) |

NOTES: (1) Schmitt Trigger input. (2) Schmitt Trigger input with internal pull-up.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| PCM1733U | 14 Pin SOIC | 235 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

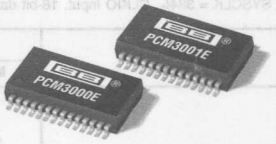
| | |
|---|---|
| Power Supply Voltage | +6.5V |
| $+V_{CC}$ to $+V_{DD}$ Difference | ±0.1V |
| Input Logic Voltage | –0.3V to ($V_{DD}$ + 0.3V) |
| Power Dissipation | 290mW |
| Operating Temperature Range | –25°C to +85°C |
| Storage Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |
| Thermal Resistance, $\theta_{JA}$ | +90°C/W |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR-BROWN®




# PCM3000
# PCM3001

www.burr-brown.com/databook/PCM3000.html

## Sound*plus*™ Stereo Audio CODEC
## 18-BITS, SERIAL INTERFACE

## FEATURES

- MONOLITHIC 18-BIT ΔΣ ADC AND DAC
- 16 OR 18-BIT INPUT/OUTPUT DATA
- STEREO ADC:
  - Single-ended Voltage Input
  - 64X Oversampling
  - High Performance:
    - –88dB THD+N
    - 94dB SNR
    - 94dB Dynamic Range
  - Digital High-Pass Filter
- STEREO DAC:
  - Single-ended Voltage Output
  - Analog Low Pass Filter
  - 8X Oversampling Digital Filter
  - High Performance:
    - –90dB THD+N
    - 98dB SNR
    - 97dB Dynamic Range
- SPECIAL FEATURES (PCM3000):
  - Digital De-emphasis
  - Digital Attenuation (256 Steps)
  - Soft Mute
  - Analog Loop Back
- SAMPLE RATE: 32kHz, 44.1kHz, 48kHz
- SYSTEM CLOCK: 256$f_S$, 384$f_S$, 512$f_S$
- SINGLE +5V POWER SUPPLY
- SMALL PACKAGE: 28-Pin SSOP

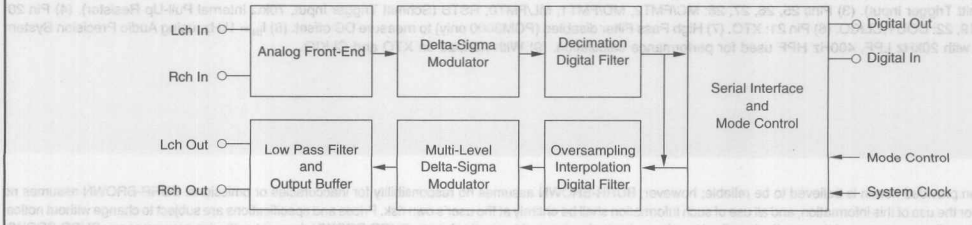
## DESCRIPTION

The PCM3000/3001 is a low cost single chip stereo audio CODEC (analog-to-digital and digital-to-analog converter) with single-ended analog voltage input and output.

Both ADCs and DACs employ delta-sigma modulation with 64X oversampling. The ADCs include a digital decimation filter and the DACs include an 8X oversampling digital interpolation filter. The DACs also include digital attenuation, de-emphasis, infinite zero detection and soft mute to form a complete subsystem. PCM3000/3001 operates with left-justified, right-justified, $I^2S$ or DSP data formats.

PCM3000 can be bit-mapped with a 3-wire serial interface for special features and data formats. PCM3001 can be pin-programmed for data formats.

Fabricated on a highly advanced 0.6µ CMOS process, PCM3000/3001 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required. Applications include sampling keyboards, digital mixers, mini-disc recorders, hard-disk recorders, karaoke systems, DSP-based car stereo, DAT recorders, and video conferencing.




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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

All specifications at +25°C, $V_{DD}$ = $V_{CC}$ = +5V, $f_S$ = 44.1kHz, SYSCLK = 384$f_S$, CLKIO Input, 18-bit data, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM3000E/3001E MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **DIGITAL INPUT/OUTPUT** | | | | | |
| **Input Logic** | | | | | |
| Input Logic Level: $V_{IH}$(1) | | 2.0 | | | VDC |
| $V_{IL}$(1) | | | | 0.8 | VDC |
| Input Logic Current: $I_{IN}$(2) | | | | ±1 | µA |
| Input Logic Current: $I_{IN}$(3) | | | | –120 | µA |
| Input Logic Level: $V_{IH}$(4) | | 0.64 x $V_{DD}$ | | | VDC |
| $V_{IL}$(4) | | | | 0.28 x $V_{DD}$ | VDC |
| Input Logic Current: $I_{IN}$(4) | | | | ±40 | µA |
| **Output Logic** | | | | | |
| Output Logic Level: $V_{OH}$(5) | $I_{OUT}$ = –1.6mA | 4.5 | | | VDC |
| $V_{OL}$(5) | $I_{OUT}$ = +3.2mA | | | 0.5 | VDC |
| Output Logic Level: $V_{OH}$(6) | $I_{OUT}$ = –3.2mA | 4.5 | | | VDC |
| $V_{OL}$(6) | $I_{OUT}$ = +3.2mA | | | 0.5 | VDC |
| **CLOCK FREQUENCY** | | | | | |
| Sampling Frequency ($f_S$) | | 32 | 44.1 | 48 | kHz |
| System Clock Frequency | 256$f_S$ | 8.1920 | 11.2896 | 12.2880 | MHz |
| | 384$f_S$ | 12.2880 | 16.9344 | 18.4320 | MHz |
| | 512$f_S$ | 16.3840 | 22.5792 | 24.5760 | MHz |
| **ADC CHARACTERISTICS** | | | | | |
| **RESOLUTION** | | 18 | | | Bits |
| **DC ACCURACY** | | | | | |
| Gain Mismatch Channel-to-Channel | | | ±1.0 | ±5.0 | % of FSR |
| Gain Error | | | ±2.0 | ±5.0 | % of FSR |
| Gain Drift | | | ±20 | | ppm of FSR/°C |
| Bipolar Zero Error | High-Pass Filter Off(7) | | ±1.7 | | %of FSR |
| Bipolar Zero Drift | High-Pass Filter Off(7) | | ±20 | | ppm of FSR/°C |
| **DYNAMIC PERFORMANCE**(8) | | | | | |
| THD+N: $V_{IN}$ = –0.5dB | f = 1kHz | | –88 | –80 | dB |
| $V_{IN}$ = –60dB | f = 1kHz | | –31 | | dB |
| Dynamic Range | f = 1kHz, A-Weighted | 90 | 94 | | dB |
| Signal-to-Noise Ratio | f = 1kHz, A-Weighted | 90 | 94 | | dB |
| Channel Separation | | 88 | 92 | | dB |
| **DIGITAL FILTER PERFORMANCE**(8) | | | | | |
| Passband | | | | 0.454$f_S$ | Hz |
| Stopband | | 0.583$f_S$ | | | Hz |
| Passband Ripple | | | | ±0.05 | dB |
| Stopband Attenuation | | –65 | | | dB |
| Delay Time (Latency) | | | 17.4/$f_S$ | | sec |
| **DIGITAL HIGH PASS FILTER RESPONSE** | | | | | |
| –3dB Frequency | | | 0.019$f_S$ | | mHz |
| **ANALOG INPUT** | | | | | |
| Voltage Range | 0dB (Full Scale) | | 2.9 | | Vp-p |
| Center Voltage | | | 2.1 | | V |
| Input Impedance | | | 15 | | kΩ |
| **ANTI-ALIASING FILTER** | | | | | |
| –3dB Frequency | $C_{EXT}$ = 470pF | | 170 | | kHz |

NOTES: (1) Pins 16, 17, 18, 22, 25, 26, 27, 28: LRCIN, BCKIN, DIN, CLKIO, MC/FMT2, MD/FMT1, ML/FMT0, RSTB. (2) Pins 16, 17, 18, 22: LRCIN, BCKIN, DIN, CLKIO (Schmitt Trigger Input). (3) Pins 25, 26, 27, 28: MC/FMT2, MD/FMT1, ML/FMT0, RSTB (Schmitt Trigger Input, 70kΩ Internal Pull-Up Resistor). (4) Pin 20: XTI. (5) Pins 19, 22: DOUT,CLKIO. (6) Pin 21: XTO. (7) High Pass Filter disabled (PCM3000 only) to measure DC offset. (8) $f_{IN}$ = 1kHz, using Audio Precision System II, rms mode with 20kHz LPF, 400Hz HPF used for performance calculation. (9) With no load on XTO and CLKIO.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## SPECIFICATIONS (CONT)

All specifications at +25°C, $V_{DD}$ = $V_{CC}$ = 5V, $f_S$ = 44.1kHz, SYSCLK = 384$f_S$, CLKIO Input, 18-bit data, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM3000E/3001E MIN | PCM3000E/3001E TYP | PCM3000E/3001E MAX | UNITS |
|---|---|---|---|---|---|
| **DAC CHARACTERISTICS** | | | | | |
| **RESOLUTION** | | 18 | | | Bits |
| **DC ACCURACY** | | | | | |
| Gain Mismatch Channel-to-Channel | | | ±1.0 | ±5.0 | % of FSR |
| Gain Error | | | ±1.0 | ±5.0 | % of FSR |
| Gain Drift | | | ±20 | | ppm of FSR/°C |
| Bipolar Zero Error | | | ±1.0 | | % of FSR |
| Bipolar Zero Drift | | | ±20 | | ppm of FSR/°C |
| **DYNAMIC PERFORMANCE**[8] | | | | | |
| THD+N: $V_{OUT}$ = 0dB (Full Scale) | | | –90 | –80 | dB |
| $V_{OUT}$ = –60dB | | | –34 | | dB |
| Dynamic Range | A-Weighted | 90 | 97 | | dB |
| Signal-to-Noise Ratio (Idle Channel) | A-Weighted | 92 | 98 | | dB |
| Channel Separation | | 90 | 95 | | dB |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Passband | | | | 0.445$f_S$ | Hz |
| Stopband | | 0.555$f_S$ | | | Hz |
| Passband Ripple | | | | ±0.17 | dB |
| Stopband Attenuation | | –35 | | | dB |
| Delay Time | | | 11.1/$f_S$ | | sec |
| **ANALOG OUTPUT** | | | | | |
| Voltage Range | | | 0.62 x $V_{CC}$ | | Vp-p |
| Center Voltage | | | 0.5 x $V_{CC}$ | | VDC |
| Load Impedance | AC Load | 5 | | | kΩ |
| **ANALOG LOW PASS FILTER** | | | | | |
| Frequency Response | f = 20kHz | | –0.16 | | dB |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range: $V_{CC}$ | | 4.5 | 5 | 5.5 | VDC |
| $V_{DD}$ | | 4.5 | 5 | 5.5 | VDC |
| Supply Current: +$I_{CC}$, +$I_{DD}$[9] | $V_{CC}$ = $V_{DD}$ = 5V | | 32 | 50 | mA |
| Power Dissipation | $V_{CC}$ = $V_{DD}$ = 5V | | 160 | 250 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Operation | | –25 | | +85 | °C |
| Storage | | –55 | | +125 | °C |

### PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| PCM3000E/3001E | 28-Pin SSOP | 324 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

### ELECTROSTATIC DISCHARGE SENSITIVITY

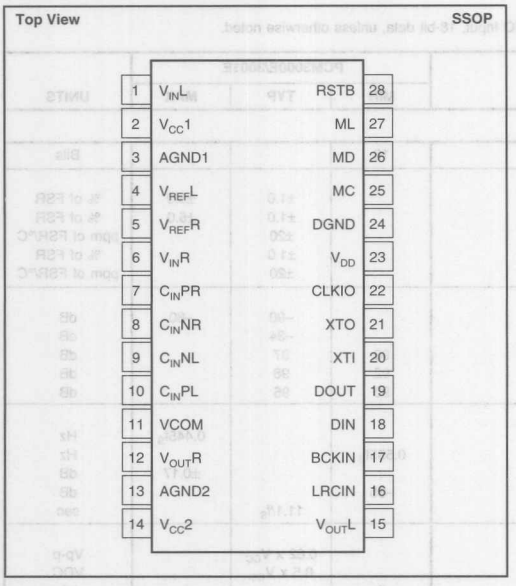
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

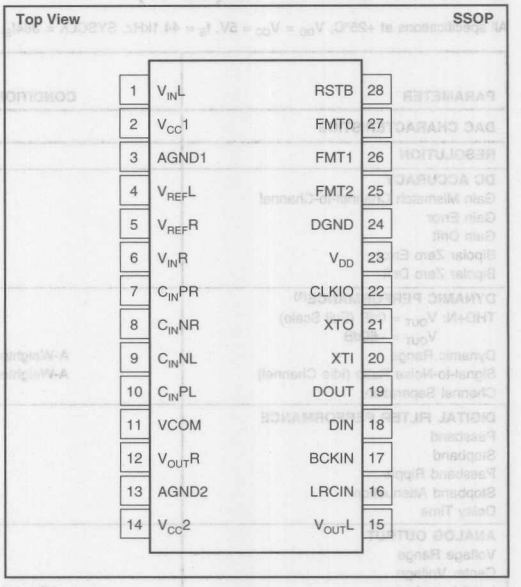
### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | |
| +$V_{DD}$, +$V_{CC}$1, +$V_{CC}$2 | +6.5V |
| Supply Voltage Differences | ±0.1V |
| GND Voltage Differences | ±0.1V |
| Digital Input Voltage | –0.3 to $V_{DD}$ + 0.3V |
| Analog Input Voltage | –0.3 to $V_{CC}$1, $V_{CC}$2 + 0.3V |
| Power Dissipation | 300mW |
| Input Current | ±10mA |
| Operating Temperature Range | –25°C to +85°C |
| Storage Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |
| (reflow, 10s) | +235°C |
| Thermal Resistance, $\theta_{JA}$ | 100°C/W |

## PIN CONFIGURATION—PCM3000




## PIN CONFIGURATION—PCM3001




## PIN ASSIGNMENTS PCM3000/3001

| PIN | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $V_{IN}L$ | IN | ADC Analog Input, Lch |
| 2 | $V_{CC}1$ | — | ADC Analog Power Supply |
| 3 | AGND1 | — | ADC Analog Ground |
| 4 | $V_{REF}L$ | — | ADC Input Reference, Lch |
| 5 | $V_{REF}R$ | — | ADC Input Reference, Rch |
| 6 | $V_{IN}R$ | IN | ADC Analog Input, Rch |
| 7 | $C_{IN}PR$ | — | ADC Anti-alias Filter Capacitor (+), Rch |
| 8 | $C_{IN}NR$ | — | ADC Anti-alias Filter Capacitor (–), Rch |
| 9 | $C_{IN}NL$ | — | ADC Anti-alias Filter Capacitor (–), Lch |
| 10 | $C_{IN}PL$ | — | ADC Anti-alias Filter Capacitor (+), Lch |
| 11 | VCOM | — | DAC Output Common |
| 12 | $V_{OUT}R$ | OUT | DAC Analog Output, Rch |
| 13 | AGND2 | — | DAC Analog Ground |
| 14 | $V_{CC}2$ | — | DAC Analog Power Supply |
| 15 | $V_{OUT}L$ | OUT | DAC Analog Output, Lch |
| 16 | LRCIN | IN | Sample Rate Clock Input ($f_S$)[2] |
| 17 | BCKIN | IN | Bit Clock Input |
| 18 | DIN | IN | Data Input |
| 19 | DOUT | OUT | Data Output |
| 20 | XTI | IN | Oscillator Input |
| 21 | XTO | OUT | Oscillator Output |
| 22 | CLKIO | I/O | Buffered Output of Oscillator or External Clock Input[2] |
| 23 | $V_{DD}$ | — | Digital Power Supply |
| 24 | DGND | — | Digital Ground |
| 25 | MC/FMT2 | IN | Serial Control Bit Clock (PCM3000)/Data Format Control 2 (PCM3001)[1, 2] |
| 26 | MD/FMT1 | IN | Serial Control Data (PCM3000)/Data Format Control 1 (PCM3001)[1, 2] |
| 27 | ML/FMT0 | IN | Serial Control Strobe Pulse/Data Format Control 0 (PCM3001)[1, 2] |
| 28 | RSTB | IN | Reset[1] |

NOTES: (1) With 70kΩ typical internal pull-up resistor. (2) Schmitt trigger input.

BURR-BROWN®




# PCM3002
# PCM3003

www.burr-brown.com/databook/PCM3002.html

# 16-/20-Bit Single-Ended Analog Input/Output SoundPLUS™ STEREO AUDIO CODECs

## FEATURES

- MONOLITHIC 20-BIT ΔΣ ADC AND DAC
- 16-/20-BIT INPUT/OUTPUT DATA
- SOFTWARE CONTROL: PCM3002
- HARDWARE CONTROL: PCM3003
- STEREO ADC:
  - Single-Ended Voltage Input
  - 64X Oversampling
  - High Performance
    - THD+N: –86dB
    - SNR: 90dB
    - Dynamic Range: 90dB
- STEREO DAC:
  - Single-Ended Voltage Output
  - Analog Low Pass Filter
  - 8X Oversampling Digital Filter
  - High Performance
    - THD+N: –86dB
    - SNR: 94dB
    - Dynamic Range: 94dB
- SPECIAL FEATURES
  - Digital De-emphasis
  - Digital Attenuation (256 Steps)
  - Soft Mute
  - Digital Loop Back
  - Power Down: ADC/DAC Independent
- SAMPLING RATE: 32kHz, 44.1kHz, 48kHz
- SYSTEM CLOCK: 256$f_S$, 384$f_S$, 512$f_S$
- SINGLE +3V POWER SUPPLY
- SMALL PACKAGE: 24-Lead SSOP

## DESCRIPTION

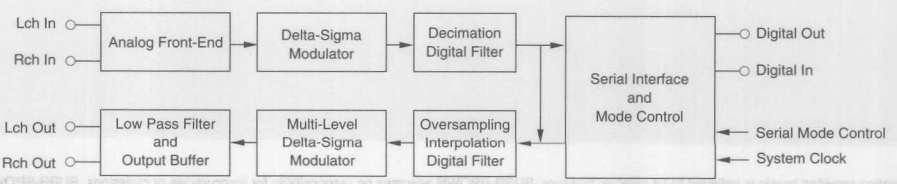
The PCM3002 and PCM3003 are low cost single chip stereo audio CODECs (analog-to-digital and digital-to-analog converters) with single-ended analog voltage input and output.

The ADCs and DACs employ delta-sigma modulation with 64X oversampling. The ADCs include a digital decimation filter, and the DACs include an 8X oversampling digital interpolation filter. The DACs also include digital attenuation, de-emphasis, infinite zero detection and soft mute to form a complete subsystem. PCM3002 and PCM3003 operate with left-justified, right-justified, or I²S data formats.

PCM3002 and PCM3003 provide a power-down mode that operates on the ADCs and DACs independently.

Fabricated on a highly advanced 0.6µs CMOS process, PCM3002 and PCM3003 are suitable for a wide variety of cost-sensitive consumer applications where good performance is required.

PCM3002's multi-functions are controlled by software and the PCM3003's functions include de-emphasis, power down, and audio data format selections, which are controlled by hardware.




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# SPECIFICATIONS

All specifications at +25°C, $V_{DD}$ = $V_{CC}$ = 3.0V, $f_S$ = 44.1kHz, SYSCLK = 384$f_S$, and 16-bit data, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM3002E/3003E MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **DIGITAL INPUT/OUTPUT** | | | | | |
| **Input Logic** | | | | | |
| Input Logic Level: $V_{IH}$[1, 2, 3] | | 0.7 x $V_{DD}$ | | | VDC |
| $V_{IL}$[1, 2, 3] | | | | 0.3 x $V_{DD}$ | VDC |
| Input Logic Current: $I_{IN}$[2] | | | | ±1 | µA |
| Input Logic Current: $I_{IN}$[1] | | | | 100 | µA |
| **Output Logic** | | | | | |
| Output Logic Level: $V_{OH}$[5] | $I_{OUT}$ = –1mA | $V_{DD}$ –0.3 | | | VDC |
| $V_{OL}$[5] | $I_{OUT}$ = +1mA | | | 0.3 | VDC |
| Output Logic Level: $V_{OL}$[4] | $I_{OUT}$ = +1mA | | | 0.3 | VDC |
| **CLOCK FREQUENCY** | | | | | |
| Sampling Frequency ($f_S$) | | 32 | 44.1 | 48 | kHz |
| System Clock Frequency | 256$f_S$ | 8.1920 | 11.2896 | 12.2880 | MHz |
| | 384$f_S$ | 12.2880 | 16.9344 | 18.4320 | MHz |
| | 512$f_S$ | 16.3840 | 22.5792 | 24.5760 | MHz |
| **ADC CHARACTERISTICS** | | | | | |
| **RESOLUTION** | | | 20 | | Bits |
| **DC ACCURACY** | | | | | |
| Gain Mismatch Channel-to-Channel | | | ±1.0 | ±3.0 | % of FSR |
| Gain Error | | | ±2.0 | ±5.0 | % of FSR |
| Gain Drift | | | ±20 | | ppm of FSR/°C |
| Bipolar Zero Error | High-Pass Filter Disabled[6] | | ±1.7 | | % of FSR |
| Bipolar Zero Drift | High-Pass Filter Disabled[6] | | ±20 | | ppm of FSR/°C |
| **DYNAMIC PERFORMANCE**[7] | | | | | |
| THD+N: $V_{IN}$ = –0.5dB | | | –86 | –80 | dB |
| $V_{IN}$ = –60dB | | | –28 | | dB |
| Dynamic Range | A-Weighted | 86 | 90 | | dB |
| Signal-to-Noise Ratio | A-Weighted | 86 | 90 | | dB |
| Channel Separation | | 84 | 88 | | dB |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Passband | | | | 0.454$f_S$ | Hz |
| Stopband | | 0.583$f_S$ | | | Hz |
| Passband Ripple | | | | ±0.05 | dB |
| Stopband Attenuation | | –65 | | | dB |
| Delay Time | | | 17.4/$f_S$ | | sec |
| HPF Frequency Response | –3dB | | 0.019$f_S$ | | mHz |
| **ANALOG INPUT** | | | | | |
| Voltage Range | | | 0.60 $V_{CC}$ | | Vp-p |
| Center Voltage | | | 0.50 $V_{CC}$ | | V |
| Input Impedance | | | 30 | | kΩ |
| Anti-Aliasing Filter Frequency Response | –3dB | | 150 | | kHz |

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# SPECIFICATIONS

All specifications at +25°C, $V_{DD}$ = $V_{CC}$ = 5V, $f_S$ = 44.1kHz, SYSCLK = 384$f_S$, CLKIO Input, 18-bit data, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM3002E/3003E MIN | PCM3002E/3003E TYP | PCM3002E/3003E MAX | UNITS |
|---|---|---|---|---|---|
| **DAC CHARACTERISTICS** | | | | | |
| **RESOLUTION** | | | 20 | | Bits |
| **DC ACCURACY** | | | | | |
| Gain Mismatch Channel-to-Channel | | | ±1.0 | ±3 | % of FSR |
| Gain Error | | | ±1.0 | ±5 | % of FSR |
| Gain Drift | | | ±20 | | ppm of FSR/°C |
| Bipolar Zero Error | | | ±1.0 | | % of FSR |
| Bipolar Zero Drift | | | ±20 | | ppm of FSR/°C |
| **DYNAMIC PERFORMANCE**[8] | | | | | |
| THD+N: $V_{OUT}$ = 0dB (Full Scale) | | | –86 | –80 | dB |
| $V_{OUT}$ = –60dB | | | –28 | | dB |
| Dynamic Range | EIAJ, A-Weighted | 88 | 94 | | dB |
| Signal-to-Noise Ratio | EIAJ, A-Weighted | 88 | 94 | | dB |
| Channel Separation | | 86 | 91 | | dB |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Passband | | | | 0.445$f_S$ | Hz |
| Stopband | | 0.555$f_S$ | | | Hz |
| Passband Ripple | | | | ±0.17 | dB |
| Stopband Attenuation | | –35 | | | dB |
| Delay Time | | | 11.1/$f_S$ | | sec |
| **ANALOG OUTPUT** | | | | | |
| Voltage Range | | | 0.60 x $V_{CC}$ | | Vp-p |
| Center Voltage | | | 0.5 x $V_{CC}$ | | VDC |
| Load Impedance | AC-Coupling | 10 | | | kΩ |
| LPF Frequency Response | f = 20kHz | | –0.16 | | dB |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range: $V_{CC}$, $V_{DD}$ | –25°C to +85°C | 2.7 | 3.0 | 3.6 | VDC |
| | 0° C to +70°C[9] | 2.4 | 3.0 | 3.6 | VDC |
| Supply Current: Operation | $V_{CC}$ = $V_{DD}$ = 3.0V | | 18 | 24 | mA |
| Power-Down | $V_{CC}$ = $V_{DD}$ = 3.0V | | 50 | | µA |
| Power Dissipation: Operation | $V_{CC}$ = $V_{DD}$ = 3.0V | | 54 | 72 | mW |
| Power-Down[10] | $V_{CC}$ = $V_{DD}$ = 3.0V | | 150 | | µW |
| **TEMPERATURE RANGE** | | | | | |
| Operation | | –25 | | +85 | °C |
| Storage | | –55 | | +125 | °C |
| Thermal Resistance, $\Theta_{JA}$ | | | 100 | | °C/W |

NOTES: (1) Pins 7, 8, 17 and 18: $\overline{RST}$, ML, MD, MC for the PCM3002; $\overline{PDAD}$, $\overline{PDDA}$, DEM1, DEM0 for PCM3003 (Schmitt-Trigger input with 100kΩ typical internal pull-down resistor). (2) Pins 9, 10, 11, 15: SYSCLK, LRCIN, BCKIN, DIN (Schmitt Trigger input). (3) Pin16: 20BIT for PCM3003 (Schmitt-Trigger input, 100kΩ typical internal pull-down resistor). (4) Pin 12: DOUT. (5) Pin 16: $\overline{ZFLG}$ (open drain output). (6) High Pass Filter for Offset Cancel. (7) $f_{IN}$ = 1kHz, using Audio Precision System II, rms mode with 20kHz LPF, 400Hz HPF used for performance calculation. (8) $f_{OUT}$ = 1kHz, using Audio Precision System II, rms mode with 20kHz LPF, 400Hz HPF used for performance calculation. (9) Applies for voltages between 2.4V to 2.7V for 0°C to +70°C and 256$f_S$/512$f_S$ operation (384$f_S$ not available). (10) SYSCLK, BCKIN, and LRCIN are stopped.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| PCM3002E/3003E | 24-Lead SSOP | 338 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | |
| $+V_{DD}$, $+V_{CC}1$, $+V_{CC}2$ | +6.5V |
| Supply Voltage Differences | ±0.1V |
| GND Voltage Differences | ±0.1V |
| Digital Input Voltage | –0.3 to $V_{DD}$ + 0.3V |
| Analog Input Voltage | –0.3 to $V_{CC}1$, $V_{CC}2$ + 0.3V |
| Power Dissipation | 300mW |
| Input Current | ±10mA |
| Operating Temperature Range | –25°C to +85°C |
| Storage Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |
| (reflow, 10s) | +235°C |

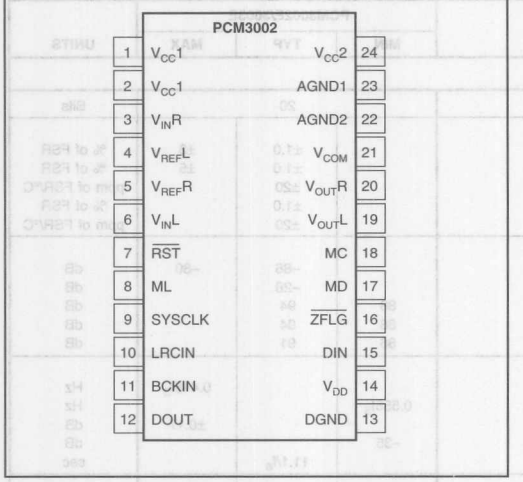
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

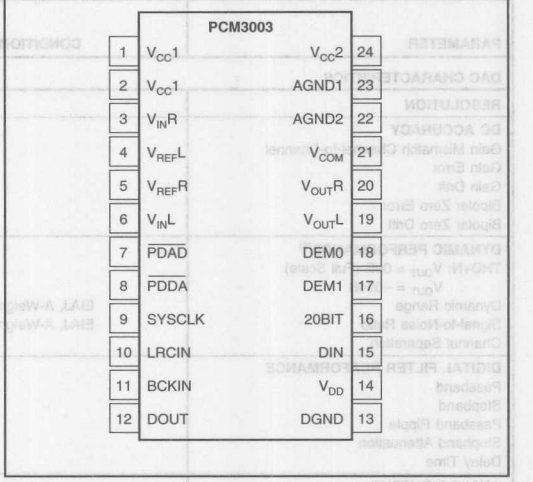
## PIN CONFIGURATION—PCM3002

Top View — SSOP




## PIN CONFIGURATION—PCM3003

Top View — SSOP




## PIN ASSIGNMENTS—PCM3002

| PIN | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $V_{CC}1$ | — | ADC Analog Power Supply |
| 2 | $V_{CC}1$ | — | ADC Analog Power Supply |
| 3 | $V_{IN}R$ | IN | ADC Analog Input, Rch |
| 4 | $V_{REF}L$ | — | ADC Reference, Lch |
| 5 | $V_{REF}R$ | — | ADC Reference, Rch |
| 6 | $V_{IN}L$ | IN | ADC Analog Input, Lch |
| 7 | $\overline{RST}$ | IN | Reset, Active LOW(1, 2) |
| 8 | ML | IN | Strobe Pulse for Mode Control(1, 2) |
| 9 | SYSCLK | IN | System Clock Input(2) |
| 10 | LRCIN | IN | Sample Rate Clock Input ($f_S$)(2) |
| 11 | BCKIN | IN | Bit Clock Input(2) |
| 12 | DOUT | OUT | Data Output |
| 13 | DGND | — | Digital Ground |
| 14 | $V_{DD}$ | — | Digital Power Supply |
| 15 | DIN | IN | Data Input(2) |
| 16 | $\overline{ZFLG}$ | OUT | Zero Flag Output, Active LOW(3) |
| 17 | MD | IN | Serial Data for Mode Control(1, 2) |
| 18 | MC | IN | Bit Clock for Mode Control(1, 2) |
| 19 | $V_{OUT}L$ | OUT | DAC Analog Output, Lch |
| 20 | $V_{OUT}R$ | OUT | DAC Analog Output, Rch |
| 21 | $V_{COM}$ | — | ADC/DAC Common |
| 22 | AGND2 | — | DAC Analog Ground |
| 23 | AGND1 | — | ADC Analog Ground |
| 24 | $V_{CC}2$ | — | DAC Analog Power Supply |

NOTES: (1) With 100kΩ typical internal pull-down resistor. (2) Schmitt-Trigger input. (3) Open drain output.

## PIN ASSIGNMENTS—PCM3003

| PIN | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $V_{CC}1$ | — | ADC Analog Power Supply |
| 2 | $V_{CC}1$ | — | ADC Analog Power Supply |
| 3 | $V_{IN}R$ | IN | ADC Analog Input, Rch |
| 4 | $V_{REF}L$ | — | ADC Reference, Lch |
| 5 | $V_{REF}R$ | — | ADC Reference, Rch |
| 6 | $V_{IN}L$ | IN | ADC Analog Input, Lch |
| 7 | $\overline{PDAD}$ | IN | ADC Power Down, Active LOW(1, 2) |
| 8 | $\overline{PDDA}$ | IN | DAC Power Down, Active LOW(1, 2) |
| 9 | SYSCLK | IN | System Clock Input(2) |
| 10 | LRCIN | IN | Sample Rate Clock Input ($f_S$)(2) |
| 11 | BCKIN | IN | Bit Clock Input(2) |
| 12 | DOUT | OUT | Data Output |
| 13 | DGND | — | Digital Ground |
| 14 | $V_{DD}$ | — | Digital Power Supply |
| 15 | DIN | IN | Data Input |
| 16 | 20BIT | IN | 20-Bit Format Select(1, 2) |
| 17 | DEM1 | IN | De-emphasis Control(1, 2) |
| 18 | DEM0 | IN | De-emphasis Control 0(1, 2) |
| 19 | $V_{OUT}L$ | OUT | DAC Analog Output, Lch |
| 20 | $V_{OUT}R$ | OUT | DAC Analog Output, Rch |
| 21 | $V_{COM}$ | — | ADC/DAC Common |
| 22 | AGND2 | — | DAC Analog Ground |
| 23 | AGND1 | — | ADC Analog Ground |
| 24 | $V_{CC}2$ | — | DAC Analog Power Supply |

NOTE: (1) With 100kΩ typical internal pull-down resistor. (2) Schmitt-Trigger input.

BURR - BROWN®




# PCM3006

www.burr-brown.com/databook/PCM3006.html

# 16-Bit, Single-Ended Analog Input/Output SoundPLUS™ STEREO AUDIO CODEC

## FEATURES

- MONOLITHIC 16-BIT ΔΣ ADC AND DAC
- STEREO ADC:
  - Single-Ended Voltage Input
  - 64X Oversampling
  - High Performance
    - THD+N: –84dB
    - SNR: 89dB
    - Dynamic Range: 89dB
  - Digital High Pass Filter
- STEREO DAC:
  - Single-Ended Voltage Output
  - Analog Low Pass Filter
  - 8X Oversampling Digital Filter
  - High Performance
    - THD+N: –85dB
    - SNR: 93dB
    - Dynamic Range: 93dB
- SPECIAL FEATURES
  - Digital De-emphasis
  - Power Down: ADC/DAC Independent
- SAMPLING RATE: Up to 48kHz
- SYSTEM CLOCK: 256$f_S$, 384$f_S$, 512$f_S$
- SINGLE +3V POWER SUPPLY
- SMALL PACKAGE: 24-Lead TSSOP

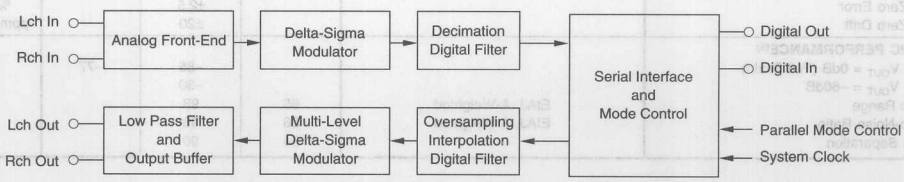
## DESCRIPTION

The PCM3006 is a low cost single chip stereo audio CODEC (analog-to-digital and digital-to-analog converters) with single-ended analog voltage input and output.

Both ADCs and DACs employ delta-sigma modulation with 64X oversampling. The ADCs include a digital decimation filter, and the DACs include an 8X oversampling digital interpolation filter. The DACs also include a de-emphasis function. PCM3006 operates with 16-bit, left-justified for ADC, right-justified for DAC data formats.

PCM3006 provides a Power-Down Mode that operates on the ADCs and DACs independently.

Fabricated on a highly advanced 0.6µs CMOS process, PCM3006 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required. Applications include sampling keyboards, digital mixers, effects processors, hard-disk recorders, data recorders and digital video cameras.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

All specifications at +25°C, $V_{DD} = V_{CC} = 3.0V$, $f_S = 44.1kHz$, SYSCLK = $384f_S$, and 16-bit data, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM3006T MIN | PCM3006T TYP | PCM3006T MAX | UNITS |
|---|---|---|---|---|---|
| **DIGITAL INPUT/OUTPUT** | | | | | |
| **Input Logic** | | | | | |
| Input Logic Level: $V_{IH}$[1] | | 0.7 x $V_{DD}$ | | | VDC |
| $V_{IL}$[1] | | | | 0.3 x $V_{DD}$ | VDC |
| Input Logic Current: $I_{IN}$[2] | | | | ±1 | µA |
| Input Logic Current: $I_{IN}$[3] | | | | 100 | µA |
| **Output Logic** | | | | | |
| Output Logic Level: $V_{OH}$[4] | $I_{OUT}$ = –1mA | $V_{DD}$ –0.3 | | | VDC |
| $V_{OL}$[4] | $I_{OUT}$ = +1mA | | | 0.3 | VDC |
| **CLOCK FREQUENCY** | | | | | |
| Sampling Frequency ($f_S$) | | 32 | 44.1 | 48 | kHz |
| System Clock Frequency | $256f_S$ | 8.1920 | 11.2896 | 12.2880 | MHz |
| | $384f_S$ | 12.2880 | 16.9344 | 18.4320 | MHz |
| | $512f_S$ | 16.3840 | 22.5792 | 24.5760 | MHz |
| **ADC CHARACTERISTICS** | | | | | |
| **RESOLUTION** | | | 16 | | Bits |
| **DC ACCURACY** | | | | | |
| Gain Mismatch Channel-to-Channel | | | ±1.0 | ±3.0 | % of FSR |
| Gain Error | | | ±2.0 | ±5.0 | % of FSR |
| Gain Drift | | | ±20 | | ppm of FSR/°C |
| Bipolar Zero Error | High-Pass Filter Disabled[6] | | ±1.7 | | % of FSR |
| Bipolar Zero Drift | High-Pass Filter Disabled[6] | | ±20 | | ppm of FSR/°C |
| **DYNAMIC PERFORMANCE**[5] | | | | | |
| THD+N: $V_{IN}$ = –0.5dB | | | –84 | –77 | dB |
| $V_{IN}$ = –60dB | | | –26 | | dB |
| Dynamic Range | A-Weighted | 84 | 89 | | dB |
| Signal-to-Noise Ratio | A-Weighted | 84 | 89 | | dB |
| Channel Separation | | 82 | 86 | | dB |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Passband | | | | $0.454f_S$ | Hz |
| Stopband | | $0.583f_S$ | | | Hz |
| Passband Ripple | | | | ±0.05 | dB |
| Stopband Attenuation | | –65 | | | dB |
| Delay Time | | | $17.4/f_S$ | | sec |
| HPF Frequency Response | –3dB | | $0.019f_S$ | | mHz |
| **ANALOG INPUT** | | | | | |
| Voltage Range | | | 0.60 $V_{CC}$ | | Vp-p |
| Center Voltage | | | 0.50 $V_{CC}$ | | V |
| Input Impedance | | | 30 | | kΩ |
| Anti-Aliasing Filter Frequency Response | –3dB | | 150 | | kHz |
| **DAC CHARACTERISTICS** | | | | | |
| **RESOLUTION** | | | 16 | | Bits |
| **DC ACCURACY** | | | | | |
| Gain Mismatch Channel-to-Channel | | | ±1.0 | ±3 | % of FSR |
| Gain Error | | | ±1.0 | ±5 | % of FSR |
| Gain Drift | | | ±20 | | ppm of FSR/°C |
| Bipolar Zero Error | | | ±2.5 | | % of FSR |
| Bipolar Zero Drift | | | ±20 | | ppm of FSR/°C |
| **DYNAMIC PERFORMANCE**[6] | | | | | |
| THD+N: $V_{OUT}$ = 0dB (Full Scale) | | | –85 | –77 | dB |
| $V_{OUT}$ = –60dB | | | –30 | | dB |
| Dynamic Range | EIAJ, A-Weighted | 86 | 93 | | dB |
| Signal-to-Noise Ratio | EIAJ, A-Weighted | 86 | 93 | | dB |
| Channel Separation | | 84 | 90 | | dB |

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## SPECIFICATIONS (CONT)

All specifications at +25°C, $V_{DD}$ = $V_{CC}$ = 3.0V, $f_S$ = 44.1kHz, SYSCLK = 384$f_S$, CLKIO Input, 16-bit data, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM3006T MIN | PCM3006T TYP | PCM3006T MAX | UNITS |
|---|---|---|---|---|---|
| **DAC CHARACTERISTICS (CONT)** | | | | | |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Passband | | | | 0.445$f_S$ | Hz |
| Stopband | | 0.555$f_S$ | | | Hz |
| Passband Ripple | | | | ±0.17 | dB |
| Stopband Attenuation | | –35 | | | dB |
| Delay Time | | | 11.1/$f_S$ | | sec |
| **ANALOG OUTPUT** | | | | | |
| Voltage Range | | | 0.6 x $V_{CC}$ | | Vp-p |
| Center Voltage | | | 0.5 x $V_{CC}$ | | VDC |
| Load Impedance | AC-Coupling | 10 | | | kΩ |
| LPF Frequency Response | f = 20kHz | | –0.16 | | dB |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range: $V_{CC}$, $V_{DD}$ | –25°C to +85°C | 2.7 | 3.0 | 3.6 | VDC |
| | 0° C to +70°C[7] | 2.4 | 3.0 | 3.6 | VDC |
| Supply Current: ADC/DAC Operation | $V_{CC}$ = $V_{DD}$ = 3.0V | | 18 | 24 | mA |
| ADC Operation | $V_{CC}$ = $V_{DD}$ = 3.0V | | 12 | 16 | mA |
| DAC Operation | $V_{CC}$ = $V_{DD}$ = 3.0V | | 7 | 10 | mA |
| ADC/DAC Power-Down[8] | $V_{CC}$ = $V_{DD}$ = 3.0V | | 50 | | µA |
| Power Dissipation: ADC/DAC Operation | $V_{CC}$ = $V_{DD}$ = 3.0V | | 54 | 72 | mW |
| ADC Operation | $V_{CC}$ = $V_{DD}$ = 3.0V | | 36 | 48 | mW |
| DAC Operation | $V_{CC}$ = $V_{DD}$ = 3.0V | | 21 | 30 | mW |
| ADC/DAC Power-Down[8] | $V_{CC}$ = $V_{DD}$ = 3.0V | | 150 | | µW |
| **TEMPERATURE RANGE** | | | | | |
| Operation | | –25 | | +85 | °C |
| Storage | | –55 | | +125 | °C |
| Thermal Resistance, $\Theta_{JA}$ | | | 100 | | °C/W |

NOTES: (1) Pins 7, 8, 9, 10, 11, 15, 17, 18: $\overline{PDAD}$, $\overline{PDDA}$, SYSCLK, LRCIN, BCKIN, DIN, DEM1, DEM0 (Schmitt-Trigger input with 100kΩ typical internal pull-down resistor). (2) Pins 9, 10, 11, 15: SYSCLK, LRCIN, BCKIN, DIN (Schmitt-Trigger input). (3) Pins 7, 8, 17, 18: $\overline{PDAD}$, $\overline{PDDA}$, DEM1, DEM0 (Schmitt-Trigger input, 100kΩ typical internal pull-down resistor). (4) Pin 12: DOUT. (5) $f_{IN}$ = 1kHz, using Audio Precision System II, rms mode with 20kHz LPF, 400Hz HPF used for performance calculation. (6) $f_{OUT}$ = 1kHz, using Audio Precision System II, rms mode with 20kHz LPF, 400Hz HPF used for performance calculation. (7) Applies for voltages between 2.4V to 2.7V for 0°C to +70°C and 256$f_S$/512$f_S$ operation (384$f_S$ not available). (8) SYSCLK, BCKIN, and LRCIN are stopped.

## PIN CONFIGURATION

Top View — TSSOP




NC = No Connection

## PIN ASSIGNMENTS

| PIN | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $V_{CC}1$ | — | ADC Analog Power Supply |
| 2 | $V_{CC}1$ | — | ADC Analog Power Supply |
| 3 | $V_{IN}R$ | IN | ADC Analog Input, Rch |
| 4 | $V_{REF}1$ | — | ADC Reference, 1 |
| 5 | $V_{REF}2$ | — | ADC Reference, 2 |
| 6 | $V_{IN}L$ | IN | ADC Analog Input, Lch |
| 7 | $\overline{PDAD}$ | IN | ADC Power Down, Active LOW(1, 2) |
| 8 | $\overline{PDDA}$ | IN | DAC Power Down, Active LOW(1, 2) |
| 9 | SYSCLK | IN | System Clock Input(2) |
| 10 | LRCIN | IN | Sample Rate Clock Input ($f_S$)(2) |
| 11 | BCKIN | IN | Bit Clock Input(2) |
| 12 | DOUT | OUT | Data Output |
| 13 | DGND | — | Digital Ground |
| 14 | $V_{DD}$ | — | Digital Power Supply |
| 15 | DIN | IN | Data Input |
| 16 | NC | IN | No Connection |
| 17 | DEM1 | IN | De-emphasis Control(1, 2) |
| 18 | DEM0 | IN | De-emphasis Control 0(1, 2) |
| 19 | $V_{OUT}L$ | OUT | DAC Analog Output, Lch |
| 20 | $V_{OUT}R$ | OUT | DAC Analog Output, Rch |
| 21 | $V_{COM}$ | — | ADC/DAC Common |
| 22 | AGND | — | Analog Ground |
| 23 | NC | — | No Connection |
| 24 | $V_{CC}2$ | — | DAC Analog Power Supply |

NOTES: (1) With 100kΩ typical internal pull-down resistor. (2) Schmitt-Trigger input.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | |
| $+V_{DD}$, $+V_{CC}1$, $+V_{CC}2$ | +6.5V |
| Supply Voltage Differences | ±0.1V |
| GND Voltage Differences | ±0.1V |
| Digital Input Voltage | –0.3 to $V_{DD}$ + 0.3V |
| Analog Input Voltage | –0.3 to $V_{CC}1$, $V_{CC}2$ + 0.3V |
| Power Dissipation | 300mW |
| Input Current | ±10mA |
| Operating Temperature Range | –25°C to +85°C |
| Storage Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |
| (reflow, 10s) | +235°C |

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| PCM3006T | 24-Lead TSSOP | 350 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# Appendix A

## Demonstration Boards

Burr-Brown offers a wide variety of demonstration boards to assist in the evaluation of its products. New demonstration boards are being added— availability information is available from our web site, your local salesperson or the factory technical assistance hot line. Descriptive data sheets for each demonstration board are available. The demonstration boards are arranged by applicable model number. In some cases there is more than one demonstration board for a unique part number.

| Applicable Model | Demo-Board Part Number | Device Included | Device Attach | Software Included | Cables | Support Card Supplied |
|---|---|---|---|---|---|---|
| ADS1210P | DEM-ADS1210/11 | N | Socket | Y | Y | |
| ADS1211P | DEM-ADS1210/11 | Y | Socket | Y | Y | |
| ADS1212P | DEM-ADS1210/11 | N | Socket | Y | Y | |
| ADS1213P | DEM-ADS1210/11 | Y | Socket | Y | Y | |
| ADS1214P | DEM-ADS1214/15 | N | Socket | Y | Y | |
| ADS1215P | DEM-ADS1214/15 | Y | Socket | Y | Y | |
| ADS1286P | DEM-ADS78DIP | N | Socket | | | |
| ADS7804P | DEM-ADS7804/05C | N | Socket | | | |
| ADS7805P | DEM-ADS7804/05C | Y | Socket | | | |
| ADS7810P | DEM-ADS7810/19 | N | Socket | | | |
| ADS7812P | DEM-ADS7812/13P | N | Socket | | | |
| ADS7813P | DEM-ADS7812/13P | Y | Socket | | | |
| ADS7815U | DEM-ADS7815U | Y | Socket | | | |
| ADS7816P | DEM-ADS78DIP | Y | Socket | | | |
| ADS7817P | DEM-ADS78DIP | Y | Socket | | | |
| ADS7818P | DEM-ADS78DIP | N | Socket | | | |
| ADS7819P | DEM-ADS7810/19 | N | Socket | | | |
| ADS7822P | DEM-ADS78DIP | Y | Socket | | | |
| ADS7833N | DEM-ADS7833-C | Y | Socket | | | |
| ADS7834P | DEM-ADS78DIP | N | Socket | | | |
| ADS7835P | DEM-ADS78DIP | N | Socket | | | |
| ADS800E | DEM-ADS8XXE | N | Solder | | | |
| ADS800U | DEM-ADS800U | Y | Solder | | | |
| ADS801E | DEM-ADS8XXE | N | Solder | | | |
| ADS801U | DEM-ADS801U | Y | Solder | | | |
| ADS802E | DEM-ADS8XXE | N | Solder | | | |
| ADS802U | DEM-ADS802U | Y | Solder | | | |
| ADS803U | DEM-ADS80XU | N | Solder | | | |
| ADS804U | DEM-ADS80XU | N | Solder | | | |
| ADS805U | DEM-ADS80XU | N | Solder | | | |
| ADS820E | DEM-ADS8XXE | N | Solder | | | |
| ADS820U | DEM-ADS820U | Y | Solder | | | |
| ADS821E | DEM-ADS8XXE | N | Solder | | | |

| Applicable Model | Demo-Board Part Number | Device Included | Device Attach | Software Included | Cables | Support Card Supplied |
|---|---|---|---|---|---|---|
| ADS821U | DEM-ADS821U | Y | Solder | | | |
| ADS900E | DEM-ADS9XXE | N | Solder | | | |
| ADS901E | DEM-ADS9XXE | N | Solder | | | |
| ADS930E | DEM-ADS9XXE | N | Solder | | | |
| ADS931E | DEM-ADS9XXE | N | Solder | | | |
| DDC101P | DEM-DDC101P-C | Y | Socket | Y | Y | |
| DDC112U | DEM-DDC112U | Y | Socket | Y | Y | |
| OPA2650E | DEM-OPA26XXE | N | Solder | | | |
| OPA2650P | DEM-OPA26XXP | N | Socket | | | |
| OPA2650U | DEM-OPA265XU | N | Solder | | | |
| OPA2658E | DEM-OPA26XXE | N | Solder | | | |
| OPA2650P | DEM-OPA26XXP | N | Solder | | | |
| OPA2658U | DEM-OPA265XU | N | Solder | | | |
| OPA4650P | DEM-OPA465XP | N | Socket | | | |
| OPA4650U | DEM-OPA465XU | N | Solder | | | |
| OPA4658P | DEM-OPA465XP | N | Socket | | | |
| OPA4658U | DEM-OPA465XU | N | Solder | | | |
| OPA640P | DEM-OPA64XP-N | N | Socket | | | |
| OPA640U | DEM-OPA64XU-N | N | Solder | | | |
| OPA642N | DEM-OPA6xxN | N | Solder | | | |
| OPA642P | DEM-OPA64XP-N | N | Socket | | | |
| OPA642U | DEM-OPA64XU-N | N | Solder | | | |
| OPA643N | DEM-OPA6xxN | N | Solder | | | |
| OPA643P | DEM-OPA64XP-N | N | Socket | | | |
| OPA643U | DEM-OPA64XU-N | N | Solder | | | |
| OPA644P | DEM-OPA64XP-N | N | Socket | | | |
| OPA644U | DEM-OPA64XU-N | N | Solder | | | |
| OPA646P | DEM-OPA64XP-N | N | Socket | | | |
| OPA646U | DEM-OPA64XU-N | N | Solder | | | |
| OPA650N | DEM-OPA6xxN | N | Solder | | | |
| OPA650P | DEM-OPA65XP | N | Socket | | | |
| OPA650U | DEM-OPA65XU | N | Solder | | | |
| OPA651N | DEM-OPA6xxN | N | Solder | | | |
| OPA651P | DEM-OPA65XP | N | Socket | | | |
| OPA651U | DEM-OPA65XU | N | Solder | | | |
| OPA655P | DEM-OPA65XP | N | Socket | | | |
| OPA655U | DEM-OPA65XU | N | Solder | | | |
| OPA658N | DEM-OPA6xxN | N | Solder | | | |
| OPA658P | DEM-OPA65XP | N | Socket | | | |
| OPA658U | DEM-OPA65XU | N | Solder | | | |
| SHC605AU | DEM-SHC605 | Y | Solder | | | |
| XTR501 | DEM-XTR501C | Y | Socket | | | |
| PCM1702 | DEM-PCM1702P | Y | Socket | | | |
| PCM1702 | EVM-1702 | Y | Socket | | | |
| PCM1710 | DEM-DAI1710 | Y | Socket | | | |

| Applicable Model | Demo-Board Part Number | Device Included | Device Attach | Software Included | Cables | Support Card Supplied |
|---|---|---|---|---|---|---|
| PCM1710 | DEM-PCM1710 | Y | Socket | | | |
| PCM1716 | DEM-DAI1716 | Y | Socket | | | DEM-DAI |
| PCM1716 | DEM-DAI1716-1 | Y | Socket | Y | Y | DEM-DAI |
| PCM1716 | DEM-PCM1716 | Y | Socket | | | |
| PCM1716 | DEM-PCM1716-1 | Y | Socket | Y | | |
| PCM1717 | DEM-DIA1717 | Y | Socket | Y | Y | |
| PCM1717 | DEM-PCM1717 | Y | Socket | | | |
| PCM1717 | DEM-PCM1717-1 | Y | Socket | Y | Y | |
| PCM1718 | DEM-DAI1718 | Y | Socket | | | DEM-DAI |
| PCM1718 | DEM-PCM1718 | Y | Socket | | | |
| PCM1719 | DEM-PCM1719 | Y | Socket | | | |
| PCM1719 | DEM-PCM1719-1 | Y | Socket | Y | Y | |
| PCM1720 | DEM-DAI1720 | Y | Socket | | | DEM-DAI |
| PCM1720 | DEM-DAI1720-1 | Y | Socket | Y | Y | DEM-DAI |
| PCM1720 | DEM-PCM1720 | Y | Socket | | | |
| PCM1720 | DEM-PCM1720-1 | Y | Socket | Y | Y | |
| PCM1723 | DEM-PCM1723 | Y | Socket | | | |
| PCM1723 | DEM-PCM1723-1 | Y | Socket | Y | | |
| PCM1725 | DEM-DAI1725 | Y | Socket | | | DEM-DAI |
| PCM1725 | DEM-PCM1725 | Y | Socket | | | |
| PCM1760 | DEM-PCM1760 | Y | Socket | | | |
| PCM1800 | DEM-DAI1800 | Y | Socket | Y | | DEM-DAI |
| PCM1800 | DEM-PCM1800 | Y | Socket | | | |
| PCM3000 | DEM-PCM3000 | Y | Socket | | | |
| PCM3000 | DEM-PCM3000-1 | Y | Socket | Y | Y | |
| PCM3001 | DEM-PCM3001 | Y | Socket | | | |
| PCM3002 | DEM-DAI3002 | Y | Socket | | | DEM-DAI |
| PCM3002 | DEM-DAI3002-1 | Y | Socket | Y | | DEM-DAI |
| PCM3002 | DEM-PCM3002 | Y | Socket | | | |
| PCM3002 | DEM-PCM3002-1 | Y | Socket | Y | | |
| PCM3003 | DEM-DAI3003 | Y | Socket | | | DEM-DAI |
| PCM3003 | DEM-DAI3003-1 | Y | Socket | Y | Y | DEM-DAI |
| PCM3003 | DEM-PCM3003 | Y | Socket | | | |

| Applicable Model | Demo-Board Part Number | Device Included | Device Attach | Software Included | Cables | Support Card Supplied |
|---|---|---|---|---|---|---|
| PCM1710 | DEM-PCM1710 | Y | Socket | | | |
| PCM1716 | DEM-DAI1716 | Y | Socket | | | DEM-DAI |
| PCM1716 | DEM-DAI1716-1 | Y | Socket | Y | Y | DEM-DAI |
| PCM1716 | DEM-PCM1716 | Y | Socket | | | |
| PCM1716 | DEM-PCM1716-1 | Y | Socket | Y | | |
| PCM1717 | DEM-DAI1717 | Y | Socket | Y | Y | |
| PCM1717 | DEM-PCM1717 | Y | Socket | | | |
| PCM1717 | DEM-PCM1717-1 | Y | Socket | Y | Y | |
| PCM1718 | DEM-DAI1718 | Y | Socket | | | DEM-DAI |
| PCM1718 | DEM-PCM1718 | Y | Socket | | | |
| PCM1719 | DEM-PCM1719 | Y | Socket | | | |
| PCM1719 | DEM-PCM1719-1 | Y | Socket | Y | Y | |
| PCM1720 | DEM-DAI1720 | Y | Socket | | | DEM-DAI |
| PCM1720 | DEM-DAI1720-1 | Y | Socket | Y | Y | DEM-DAI |
| PCM1720 | DEM-PCM1720 | Y | Socket | | | |
| PCM1720 | DEM-PCM1720-1 | Y | Socket | Y | Y | |
| PCM1723 | DEM-PCM1723 | Y | Socket | | | |
| PCM1723 | DEM-PCM1723-1 | Y | Socket | Y | | |
| PCM1725 | DEM-DAI1725 | Y | Socket | | | DEM-DAI |
| PCM1725 | DEM-PCM1725 | Y | Socket | | | |
| PCM1750 | DEM-PCM1750 | Y | Socket | | | |
| PCM1800 | DEM-DAI1800 | Y | Socket | Y | | DEM-DAI |
| PCM1800 | DEM-PCM1800 | Y | Socket | | | |
| PCM3000 | DEM-PCM3000 | Y | Socket | | | |
| PCM3003 | DEM-PCM3003-1 | Y | Socket | Y | Y | |
| PCM3001 | DEM-PCM3001 | Y | Socket | | | |
| PCM3002 | DEM-DAI3002 | Y | Socket | | | DEM-DAI |
| PCM3002 | DEM-DAI3002-1 | Y | Socket | Y | | DEM-DAI |
| PCM3002 | DEM-PCM3002 | Y | Socket | | | |
| PCM3002 | DEM-PCM3002-1 | Y | Socket | Y | | |
| PCM3008 | DEM-DAI3008 | Y | Socket | | | DEM-DAI |
| PCM3009 | DEM-DAI3009-1 | Y | Socket | Y | Y | DEM-DAI |
| PCM3003 | DEM-PCM3003 | Y | Socket | | | |

# Appendix B

## Tape and Reel Information

With the tremendous increase in the demand for surface-mount packages and the accompanying requirements for tape and reel, this year Burr-Brown has streamlined its model number system for the tape and reel option.

### TAPE AND REEL MODEL NUMBERING SYSTEM

Model numbers for products on tape and reel include the reel quantities as a suffix to the core model number separated by a slash, such as: OPA2237UA/2K5. The slash ("/") is the unique indicator for tape and reel.

To determine the complete model number for a given product, first note the package number that is given for each product in its respective product data sheet. Then look up that package number in Table I below to determine the quantity of devices per reel and the suffix.

To shorten tape and reel delivery times, all products will be stocked already taped and reeled. Therefore, no partial or odd size reels will be allowed. The quantity ordered must be equal to, or a multiple of, the suffix quantity.

Some Burr-Brown products (such as those in SOT-23 packages) are only available on tape and reel. In general, these products will also be available on the small 250-piece reel (/250) for pre-production purposes. If the product is available in rails, then only the larger full production reel size will be offered.

When entering an order for a part on tape and reel, please request the part number complete with the slash suffix along with the quantity of units desired. Thus, an order for 5000 pieces of OPA2237UA on tape and reel would be entered as:

| MATERIAL | QTY |
|---|---|
| OPA2237UA/2K5 | 5000 |

This would be supplied as two 2500-piece reels. It is always a good idea to confirm tape and reel model numbers with your nearest Burr-Brown Sales Office.

| PACKAGE NUMBER[1] | DESCRIPTION | TAPE WIDTH, W (mm) | PITCH, P (mm) | DEVICES PER REEL | REEL DIAMETER (mm) | SUFFIX |
|---|---|---|---|---|---|---|
| 178 | SO-24 | 24 | 16 | 1000 | 360 | /1K |
| 182 | SO-8 | 12 | 8 | 2500 | 360 | /2K5 |
| 211 | SOL-16 | 16 | 12 | 1000 | 360 | /1K |
| 217 | SO-28 | 24 | 12 | 1000 | 360 | /1K |
| 219 | SOL-18 | 24 | 16 | 1000 | 360 | /1K |
| 221 | SOL-20 | 24 | 12 | 1000 | 360 | /1K |
| 235 | SO-14 | 16 | 8 | 2500 | 360 | /2K5 |
| 239 | SOL-24 | 24 | 12 | 1000 | 360 | /1K |
| 248 | SO-20 | 24 | 12 | 1000 | 360 | /1K |
| 311 | SOT-23 | 12 | 8 | 2500 | 360 | /2K5 |
| 322 | SSOP-16 | 12 | 8 | 2500<br>250 | 360<br>178 | /2K5<br>/250 |
| 324 | SSOP-28 | 24 | 12 | 1000 | 360 | /1K |
| 325 | 5-Lead DD Pak | 24 | 16 | 1000 | 360 | /1K |
| 328 | 7-Lead DD Pak | 24 | 16 | 1000 | 360 | /1K |
| 331 | SOT23-5 | 8 | 4 | 3000<br>250 | 178<br>178 | /3K<br>/250 |
| 332 | SOT23-6 | 8 | 4 | 3000<br>250 | 178<br>178 | /3K<br>/250 |
| 333 | SSOP-48 | 32 | 16 | 1000 | 360 | /1K |
| 334 | SSOP-20 | 32 | 16 | 1000 | 360 | /1K |
| 337 | MSOP-8 | 12 | 8 | 2500<br>250 | 360<br>178 | /2K5<br>/250 |
| 338 | SSOP-24 | 16 | 12 | 360 | 1000 | /1K |
| 339 | 3-Lead DD Pak | 24 | 16 | 360 | 1000 | /1K |
| 340 | LQFP-48 | 16 | 12 | 360 | 1000 | /1K |
| 341 | SO-28 | 24 | 16 | 360 | 1000 | /1K |
| 346 | SSOP-56 | 32 | 16 | 360 | 1000 | /1K |
| 348 | SOT23-8 | 8 | 4 | 178<br>178 | 3000<br>250 | /3K<br>/250 |
| 349 | SSOP-20 (QSOP-20) | 16 | 8 | 360 | 1000 | /1K |
| 350 | TSSOP-24 | 16 | 12 | 360 | 1000 | /1K |

NOTE: (1) Package numbers can be found in individual product data sheets in the "Package Information" table. Package drawings are in Appendix C.

TABLE I.

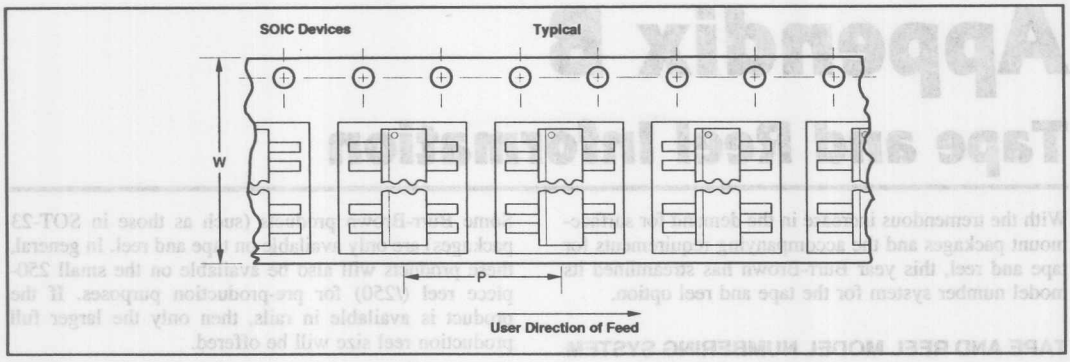



FIGURE 1.

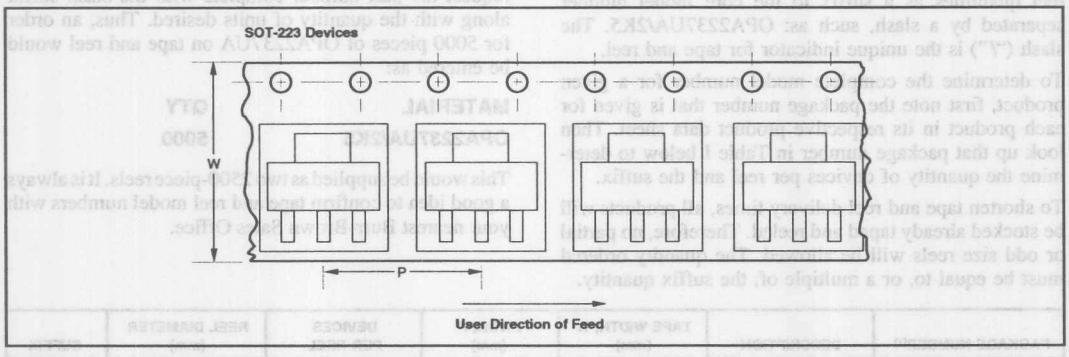



FIGURE 2.

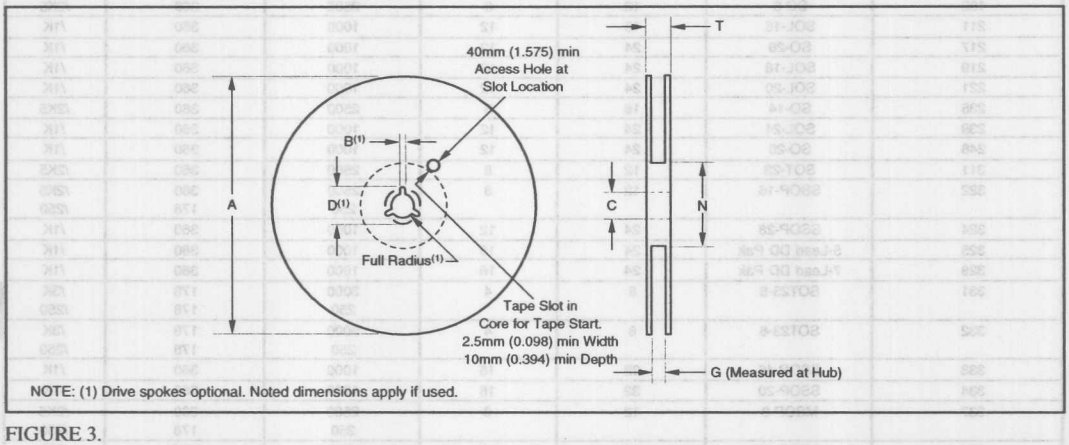


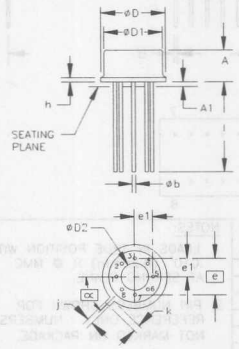

FIGURE 3.

| TAPE SIZE | A MAX | B MAX | C | D MIN | N MIN | G | T MAX |
|---|---|---|---|---|---|---|---|
| 8mm | 178mm | 1.91mm | 13.0 ±0.20mm | 20.2mm | 50mm | 8.4 + 1.5 | 11.4mm |
| 12mm | 330mm | 1.5mm | 13.0 ±0.20mm | 20.2mm | 50mm | 12.4 + 1.0 (–0.0mm) | 18.4mm |
| 16mm | 360mm | 1.5mm | 13.0 ±0.20mm | 20.2mm | 50mm | 16.4 + 1.0 (–0.08mm) | 22.4mm |
| 24mm | 360mm | 1.5mm | 13.0 ±0.20mm | 20.2mm | 50mm | 24.4 + 1.0 (–0.00mm) | 30.4mm |
| 32mm | 360mm | 1.5mm | 13.0 ±0.20mm | 20.2mm | 50mm | 32.4 + 1.0 | 38.4mm |

TABLE II.

# Appendix C
## Package Drawings (Mechanicals)

**Package Number 001 - 8-Lead TO-99**

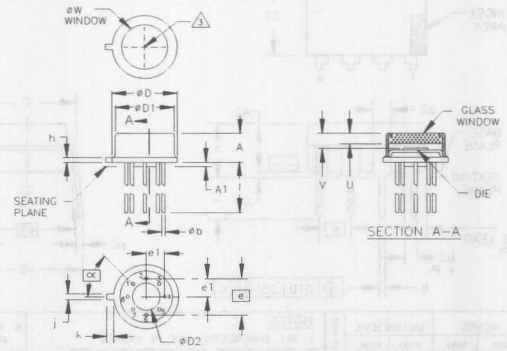



| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .165 | .185 | 4.19 | 4.70 | |
| A1 | .010 | .040 | 0.25 | 1.02 | |
| b | .016 | .021 | 0.41 | 0.53 | |
| D | .335 | .370 | 8.51 | 9.40 | |
| D1 | .305 | .335 | 7.75 | 8.51 | |
| D2 | .140 | .160 | 3.56 | 4.06 | |
| e | .200 BASIC | | 5.08 BASIC | | |
| e1 | .095 | .105 | 2.41 | 2.67 | |
| h | -- | .040 | -- | 1.02 | |
| j | .028 | .034 | 0.71 | 0.86 | |
| k | .029 | .045 | 0.74 | 1.14 | |
| l | .500 | -- | 12.70 | -- | |
| N | 8 | | 8 | | 3 |
| α | 45° BASIC | | 45° BASIC | | |

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. N IS THE NUMBER OF TERMINAL POSITIONS.

PACKAGE NUMBER: ZZ001 REV.: D
JEDEC NUMBER: TO-99

**Package Number 001-1 - 8-Lead TO-99 with Bulls-Eye Lid**

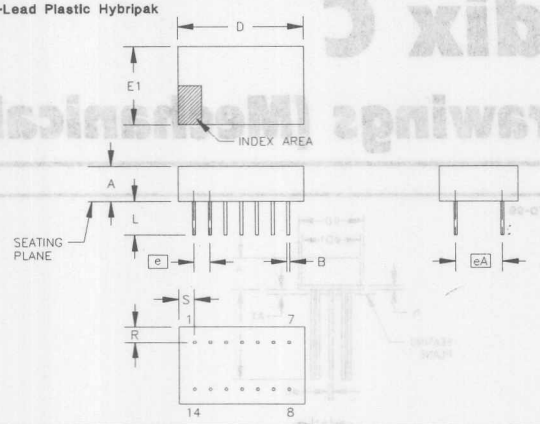



| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .149 | .165 | 3.79 | 4.19 | |
| A1 | .010 | .040 | 0.25 | 1.02 | |
| b | .016 | .021 | 0.41 | 0.53 | |
| D | .335 | .370 | 8.51 | 9.40 | |
| D1 | .305 | .335 | 7.75 | 8.51 | |
| D2 | .140 | .160 | 3.56 | 4.06 | |
| e | .200 BASIC | | 5.08 BASIC | | |
| e1 | .095 | .105 | 2.41 | 2.67 | |
| h | -- | .040 | -- | 1.02 | |
| j | .028 | .034 | 0.71 | 0.86 | |
| k | .029 | .045 | 0.74 | 1.14 | |
| l | .500 | -- | 12.70 | -- | |
| N | 8 | | 8 | | 4 |
| U | .040 | .050 | 1.02 | 1.27 | |
| V | .058 | .077 | 1.47 | 1.96 | |
| W | .246 | .254 | 6.25 | 6.45 | |
| α | 45° BASIC | | 45° BASIC | | |

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. DIE MAY BE ROTATED WITH RESPECT TO INDICATED AXIS.
4. N IS THE NUMBER OF TERMINAL POSITIONS.

PACKAGE NUMBER: ZZ001-1 REV.: D
JEDEC NUMBER: NONE

**Package Number 003 - 14-Lead Plastic Hybripak**

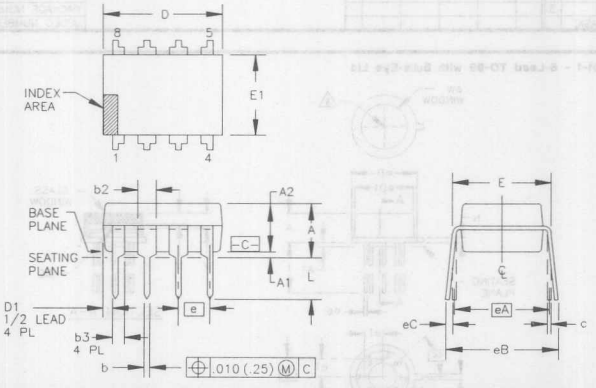



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .190 | .260 | 4.83 | 6.60 | |
| B | .018 | .021 | 0.46 | 0.53 | |
| D | .790 | .810 | 20.07 | 20.57 | |
| E1 | .490 | .510 | 12.45 | 12.95 | |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .300 | BASIC | 7.62 | BASIC | |
| L | .130 | .300 | 3.30 | 7.62 | |
| N | 14 | | 14 | | 3 |
| R | .080 | .115 | 2.03 | 2.92 | |
| S | .080 | .115 | 2.03 | 2.92 | |

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS ARE NOT MARKED ON PACKAGE.
3. N IS THE NUMBER OF TERMINAL POSITIONS.
4. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ003 REV.: B
JEDEC NUMBER: NONE

**Package Number 006 - 8-Pin Plastic, Single-Wide DIP**



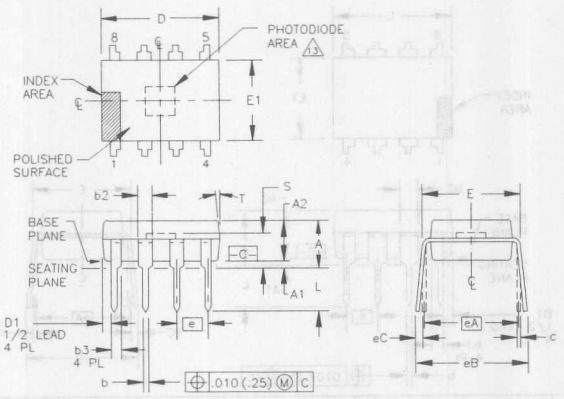

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .210 | -- | 5.33 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .115 | .195 | 2.92 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .045 | .070 | 1.14 | 1.78 | 9 |
| b3 | .030 | .045 | 0.76 | 1.14 | 9 |
| c | .008 | .014 | 0.20 | 0.36 | |
| D | .355 | .400 | 9.02 | 10.16 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .300 | .325 | 7.62 | 8.26 | 5 |
| E1 | .240 | .280 | 6.10 | 7.11 | 4 |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .300 | BASIC | 7.63 | BASIC | 5 |
| eB | -- | .430 | -- | 10.92 | 6 |

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| eC | .000 | .060 | 0.00 | 1.52 | 6 |
| L | .115 | .150 | 2.92 | 3.81 | 3 |
| N | 8 | | 8 | | 7 |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006 REV.: E
JEDEC NUMBER: MS-001-BA

**Package Number 006-1 - 8-Pin Transparent Plastic Single-Wide DIP**



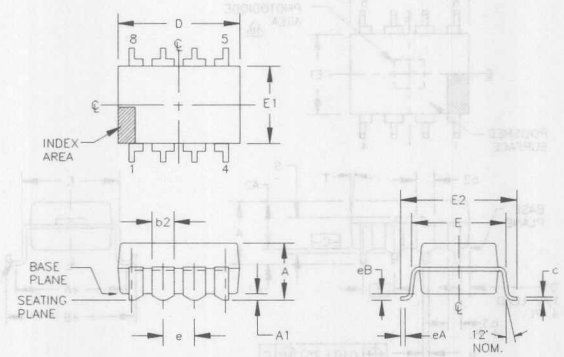

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .165 | -- | 4.19 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .120 | .135 | 3.05 | 3.43 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .045 | .070 | 1.14 | 1.78 | 9 |
| b3 | .030 | .045 | 0.762 | 1.143 | 9 |
| c | .008 | .015 | 0.20 | 0.38 | |
| D | .360 | .390 | 9.14 | 9.91 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .300 | .325 | 7.62 | 8.26 | 5 |
| E1 | .238 | .275 | 6.05 | 6.99 | 4 |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .300 BASIC | | 7.63 BASIC | | 5 |
| eB | -- | .430 | -- | 10.92 | 6 |

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| eC | .000 | .060 | 0.00 | 1.52 | 6 |
| L | .115 | .160 | 2.92 | 4.06 | 3 |
| N | 8 | | 8 | | 7 |
| S | .100 | .120 | 2.54 | 3.05 | |
| T | 5.5° | 8.5° | 5.5° | 8.5° | |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
13. CENTER OF PHOTODIODE MUST BE WITHIN .010 (0.25mm) OF CENTER OF PHOTODIODE AREA.

PACKAGE NUMBER: ZZ006-1 | REV.: E
JEDEC NUMBER: NONE

**Package Number 006-2 - 8-Pin Plastic, Single-Wide DIP With Gull Wing Leads**

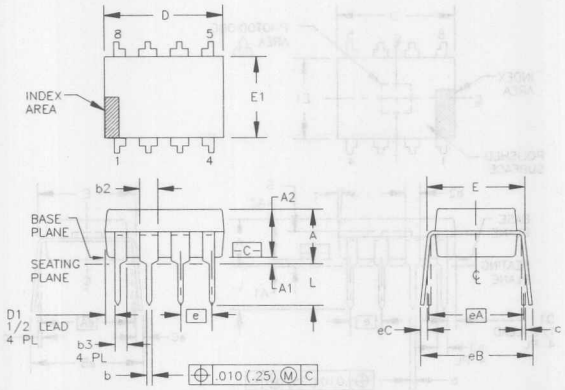



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .185 | -- | 4.70 | |
| A1 | .020 | -- | 0.51 | -- | |
| b2 | -- | .070 | -- | 1.78 | |
| c | .007 | .013 | 0.18 | 0.33 | |
| D | .370 | .390 | 9.40 | 9.91 | 3 |
| E | .290 | .310 | 7.37 | 7.87 | |
| E1 | .240 | .260 | 6.10 | 6.60 | 3 |
| E2 | .370 | .390 | 9.40 | 9.91 | |
| e | .090 | .110 | 2.29 | 2.79 | |
| eA | .015 | .035 | 0.38 | 0.89 | |
| eB | .015 | .025 | 0.38 | 0.64 | |
| N | 8 | | 8 | | 4 |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
4. N IS THE MAXIMUM OF TERMINAL POSITIONS.
5. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
6. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
7. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006-2 | REV.: C
JEDEC NUMBER: NONE

**Package Number 006-3 - 8-Pin Plastic, Single-Wide DIP**



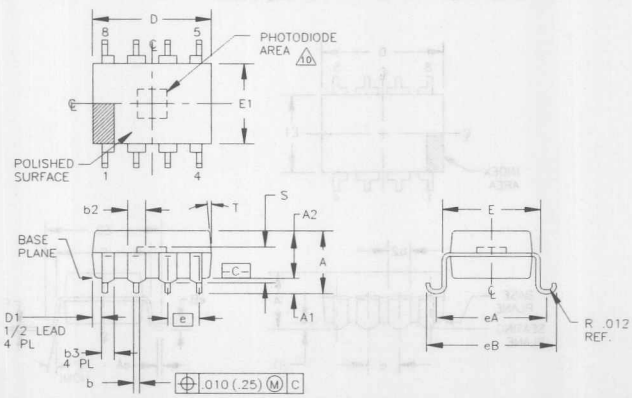

| DIM | INCHES | | MILLIMETERS | | NOTE | DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | | | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .210 | -- | 5.33 | 3 | eC | .000 | .060 | 0.00 | 1.52 | 6 |
| A1 | .015 | -- | 0.38 | -- | 3 | L | .115 | .150 | 2.92 | 3.81 | 3 |
| A2 | .115 | .195 | 2.92 | 4.95 | | N | 8 | | 8 | | 7 |
| b | .014 | .025 | 0.36 | .635 | | | | | | | |
| b2 | .045 | .070 | 1.14 | 1.78 | 9 | | | | | | |
| b3 | .030 | .045 | 0.76 | 1.14 | 9 | | | | | | |
| c | .008 | .014 | 0.20 | 0.36 | | | | | | | |
| D | .355 | .400 | 9.02 | 10.16 | 4 | | | | | | |
| D1 | .005 | -- | 0.13 | -- | 4 | | | | | | |
| E | .300 | .325 | 7.62 | 8.26 | 5 | | | | | | |
| E1 | .240 | .280 | 6.10 | 7.11 | 4 | | | | | | |
| e | .100 BASIC | | 2.54 BASIC | | | | | | | | |
| eA | .300 BASIC | | 7.63 BASIC | | 5 | | | | | | |
| eB | -- | .430 | -- | 10.92 | 6 | | | | | | |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006-3 | REV.: C

JEDEC NUMBER: MS-001-BA WITH THE EXCEPTION OF DIM. b

**Package Number 006-4 - Transparent J-Formed 8-Lead Surface-Mount DIP**




| DIM | INCHES | | MILLIMETERS | | NOTE | DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | | | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .255 | -- | 6.48 | | S | .100 | .120 | 2.54 | 3.05 | |
| A1 | .040 | .060 | 1.02 | 1.52 | | T | 5.5° | 8.5° | 5.5° | 8.5° | |
| A2 | .120 | .135 | 3.05 | 3.43 | | | | | | | |
| b | .014 | .022 | 0.36 | 0.56 | | | | | | | |
| b2 | .040 | .050 | 1.02 | 1.27 | 6 | | | | | | |
| b3 | .030 | .045 | 0.76 | 1.14 | 6 | | | | | | |
| D | .360 | .390 | 9.14 | 9.91 | 3 | | | | | | |
| D1 | .005 | -- | 0.13 | -- | 3 | | | | | | |
| E | .300 | .325 | 7.62 | 8.26 | 4 | | | | | | |
| E1 | .238 | .275 | 6.05 | 6.99 | 3 | | | | | | |
| e | .100 BASIC | | 2.54 BASIC | | | | | | | | |
| eA | .350 | .370 | 8.89 | 9.40 | 4 | | | | | | |
| eB | -- | .415 | -- | 10.54 | | | | | | | |
| N | 8 | | 8 | | 5 | | | | | | |

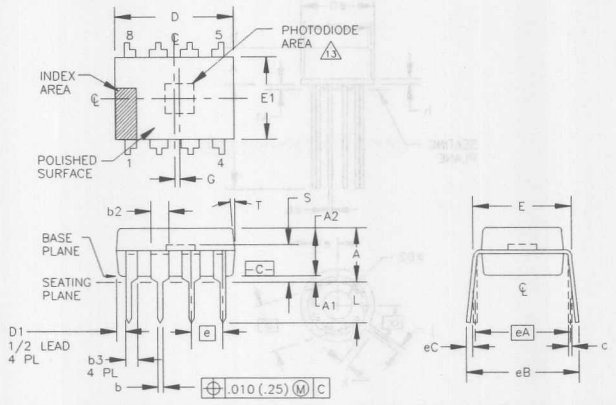
NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
4. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
5. N IS THE MAXIMUM OF TERMINAL POSITIONS.
6. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
7. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
9. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
10. CENTER OF PHOTODIODE MUST BE WITHIN .010 (0.25mm) OF CENTER OF PHOTODIODE AREA.

PACKAGE NUMBER: ZZ006-4 | REV.: C

JEDEC NUMBER: NONE

PACKAGE DRAWINGS (Mechanical)

**Package Number 006-5 - 8-Pin Transparent Plastic Single-Wide DIP**



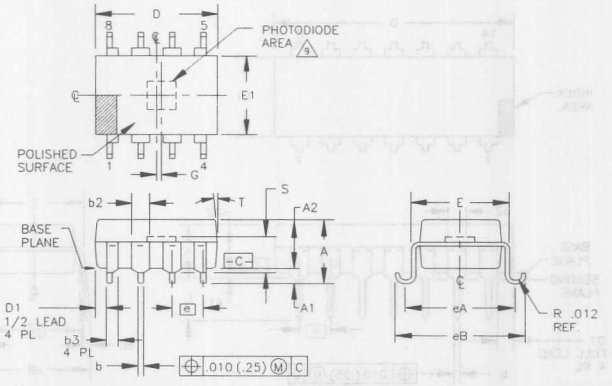

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .165 | -- | 4.19 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .120 | .135 | 3.05 | 3.43 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .040 | .050 | 1.02 | 1.27 | 9 |
| b3 | .030 | .045 | 0.76 | 1.14 | 9 |
| c | .008 | .014 | 0.20 | 0.36 | |
| D | .360 | .390 | 9.14 | 9.91 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .300 | .325 | 7.62 | 8.26 | 5 |
| E1 | .238 | .275 | 6.05 | 6.99 | 4 |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .300 BASIC | | 7.63 BASIC | | 5 |
| eB | -- | .430 | -- | 10.92 | 6 |

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| eC | .000 | .060 | 0.00 | 1.52 | 6 |
| G | .011 | .021 | 0.28 | 0.53 | |
| L | .115 | .150 | 2.92 | 3.81 | 3 |
| N | 8 | | 8 | | 7 |
| S | .100 | .120 | 2.54 | 3.05 | |
| T | 5.5° | 8.5° | 5.5° | 8.5° | |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
13. CENTER OF PHOTODIODE MUST BE WITHIN .010 (0.25mm) OF CENTER OF PHOTODIODE AREA.

PACKAGE NUMBER: ZZ006-5 | REV.: B
JEDEC NUMBER: NONE

**Package Number 006-6 - Transparent J-Formed 8-Lead Surface-Mount DIP**



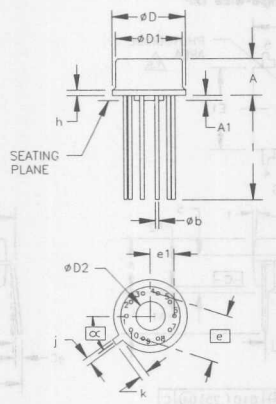

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .255 | -- | 6.48 | |
| A1 | .040 | .060 | 1.02 | 1.52 | |
| A2 | .120 | .135 | 3.05 | 3.43 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .040 | .050 | 1.02 | 1.27 | 5 |
| b3 | .030 | .045 | 0.76 | 1.14 | 5 |
| D | .360 | .390 | 9.14 | 9.91 | 3 |
| D1 | .005 | -- | 0.13 | -- | 3 |
| E | .300 | .325 | 7.62 | 8.26 | |
| E1 | .238 | .275 | 6.05 | 6.99 | 3 |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .350 | .370 | 8.89 | 9.40 | |
| eB | -- | .415 | -- | 10.54 | |
| G | .011 | .021 | 0.28 | 0.53 | |

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| N | 8 | | 8 | | 4 |
| S | .100 | .120 | 2.54 | 3.05 | |
| T | 5.5° | 8.5° | 5.5° | 8.5° | |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
4. N IS THE MAXIMUM OF TERMINAL POSITIONS.
5. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
6. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
7. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
8. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
9. CENTER OF PHOTODIODE MUST BE WITHIN .010 (0.25mm) OF CENTER OF PHOTODIODE AREA.

PACKAGE NUMBER: ZZ006-6 | REV.: B
JEDEC NUMBER: NONE

**Package Number 007 - 10-Lead TO-100**




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .165 | .185 | 4.19 | 4.70 | |
| A1 | .010 | .040 | 0.25 | 1.02 | |
| b | .016 | .021 | 0.41 | 0.53 | |
| D | .335 | .370 | 8.51 | 9.40 | |
| D1 | .305 | .335 | 7.75 | 8.51 | |
| D2 | .120 | .160 | 3.05 | 4.06 | |
| e | .230 | BASIC | 5.84 | BASIC | |
| e1 | .110 | .120 | 2.79 | 3.05 | |
| h | .010 | .040 | 0.25 | 1.02 | |
| j | .028 | .034 | 0.71 | 0.86 | |
| k | .029 | .045 | 0.74 | 1.14 | |
| l | .500 | -- | 12.70 | -- | |
| N | 10 | | 10 | | 3 |
| α | 36° | BASIC | 36° | BASIC | |

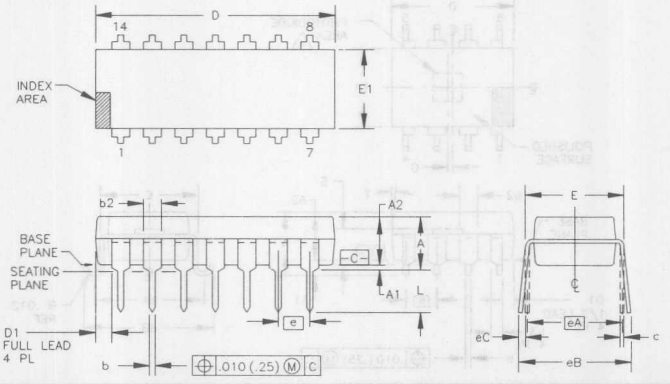
| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. N IS THE NUMBER OF TERMINAL POSITIONS.

PACKAGE NUMBER: ZZ007 | REV.: B
JEDEC NUMBER: TO-100

**Package Number 010 - 14-Pin Plastic, Single-Wide DIP**




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .210 | -- | 5.33 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .115 | .195 | 2.92 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .045 | .070 | 1.14 | 1.78 | 9 |
| c | .008 | .014 | 0.20 | 0.36 | |
| D | .735 | .775 | 18.67 | 19.69 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .300 | .325 | 7.62 | 8.26 | 5 |
| E1 | .240 | .280 | 6.10 | 7.11 | 4 |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .300 | BASIC | 7.63 | BASIC | 5 |
| eB | -- | .430 | -- | 10.92 | 6 |
| eC | .000 | .060 | 0.00 | 1.52 | 6 |

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| L | .115 | .150 | 2.92 | 3.81 | 3 |
| N | 14 | | 14 | | 7 |

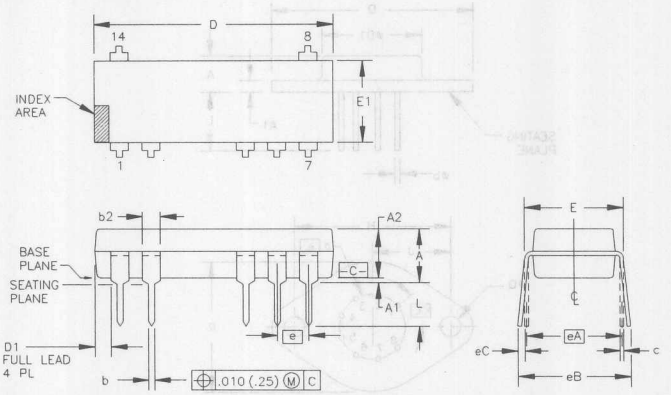
NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ010 | REV.: G
JEDEC NUMBER: MS-001-AA

PACKAGE DRAWINGS (Mechanical)

## Package Number 010-1 - 14-Pin Plastic, Single-Wide DIP

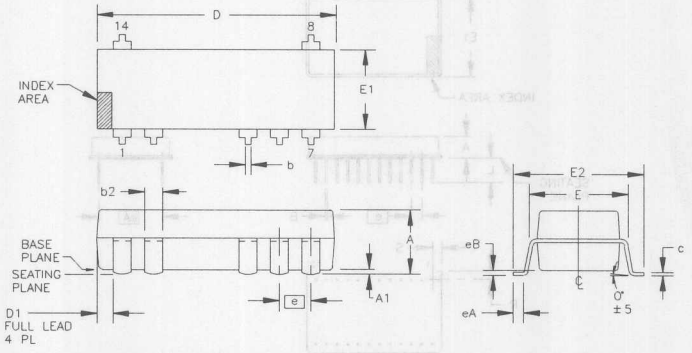



| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .210 | -- | 5.33 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .115 | .195 | 2.92 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .045 | .070 | 1.14 | 1.78 | 9 |
| c | .008 | .014 | 0.20 | 0.36 | |
| D | .735 | .775 | 18.67 | 19.69 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .300 | .325 | 7.62 | 8.26 | 5 |
| E1 | .240 | .280 | 6.10 | 7.11 | 4 |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .300 BASIC | | 7.63 BASIC | | 5 |
| eB | -- | .430 | -- | 10.92 | 6 |
| eC | .000 | .060 | 0.00 | 1.52 | 6 |
| L | .115 | .150 | 2.92 | 3.81 | 3 |
| N | 7 | | 7 | | 7 |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ010-1 | REV.: A
JEDEC NUMBER: MS-001-AA

## Package Number 010-2 - 14-Pin Plastic, Single-Wide DIP with Gull Wing Leads

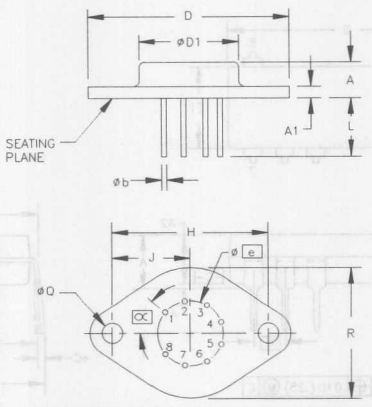



| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .210 | -- | 5.33 | |
| A1 | .015 | -- | 0.38 | -- | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .045 | .070 | 1.14 | 1.78 | 5 |
| c | .008 | .014 | 0.20 | 0.36 | |
| D | .735 | .775 | 18.67 | 19.69 | 3 |
| D1 | .005 | -- | 0.13 | -- | 3 |
| E | .300 | .325 | 7.62 | 8.26 | |
| E1 | .240 | .280 | 6.10 | 7.11 | 3 |
| E2 | .405 | .420 | 10.30 | 10.70 | |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .045 | .057 | 1.15 | 1.45 | |
| eB | .025 | .043 | 0.65 | 1.10 | |
| N | 7 | | 7 | | 4 |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
4. N IS THE MAXIMUM OF TERMINAL POSITIONS.
5. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
6. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
7. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
8. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ010-2 | REV.: B
JEDEC NUMBER: NONE

**Package Number 030 - 8-Lead TO-3**

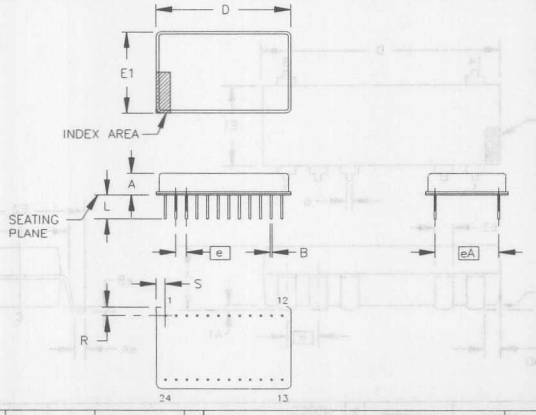



| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .260 | .300 | 6.60 | 7.62 | |
| A1 | .080 | .105 | 2.03 | 2.67 | |
| b | .038 | .042 | 0.97 | 1.07 | |
| D | 1.510 | 1.550 | 38.35 | 39.37 | |
| D1 | .745 | .770 | 18.92 | 19.56 | |
| e | .500 | BASIC | 12.70 | BASIC | |
| H | 1.182 | 1.192 | 30.02 | 30.28 | |
| J | .591 | .596 | 15.01 | 15.14 | |
| L | .400 | .500 | 10.16 | 12.70 | |
| N | 8 | | 8 | | 3 |
| Q | .151 | .161 | 3.84 | 4.09 | |
| R | .980 | 1.020 | 24.89 | 25.91 | |
| α | 40° | BASIC | 40° | BASIC | |

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. N IS THE NUMBER OF TERMINAL POSITIONS.

PACKAGE NUMBER: ZZ030 REV.: D
JEDEC NUMBER: NONE

**Package Number 037 - 24-Lead Metal Platform, .600 Wide**



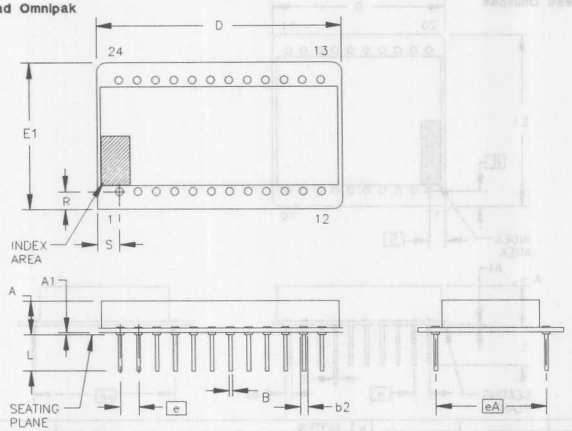

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .170 | .250 | 4.32 | 6.35 | |
| B | .016 | .021 | 0.41 | 0.53 | |
| D | 1.260 | 1.280 | 32.00 | 32.51 | |
| E1 | .760 | .800 | 19.30 | 20.32 | |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .600 | BASIC | 15.24 | BASIC | |
| L | .150 | .300 | 3.81 | 7.62 | |
| N | 24 | | 24 | | 3 |
| R | .070 | .100 | 1.78 | 2.54 | |
| S | .070 | .100 | 1.78 | 2.54 | |

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON THE PACKAGE.
3. N IS THE NUMBER OF TERMINAL POSITIONS.
4. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ037 REV.: D
JEDEC NUMBER: NONE

PACKAGE DRAWINGS (Mechanical)

## Package Number 075 - 24-Lead Omnipak

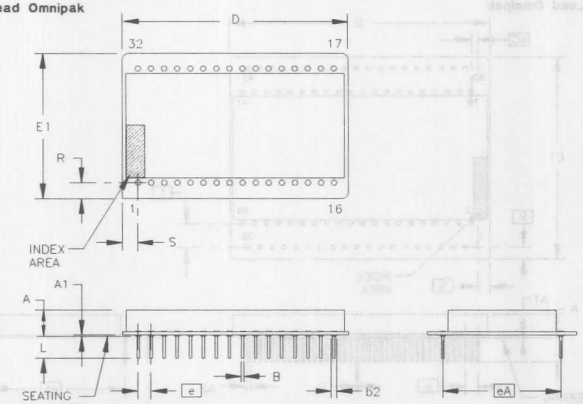



| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .150 | .210 | 3.81 | 5.33 | |
| A1 | .002 | .010 | 0.05 | 0.25 | |
| B | .018 | .021 | 0.46 | 0.53 | |
| b2 | .035 | .050 | 0.89 | 1.27 | |
| D | 1.310 | 1.360 | 33.27 | 34.54 | |
| E1 | .770 | .810 | 19.56 | 20.57 | |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .600 BASIC | | 15.24 BASIC | | |
| L | .150 | .250 | 3.81 | 6.35 | |
| N | 24 | | 24 | | 3 |
| R | .085 | .105 | 2.16 | 2.67 | |
| S | .110 | .130 | 2.79 | 3.30 | |

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. N IS THE NUMBER OF TERMINAL POSITIONS.
4. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ075 | REV.: B
JEDEC NUMBER: NONE

## Package Number 077 - 32-Lead Omnipak

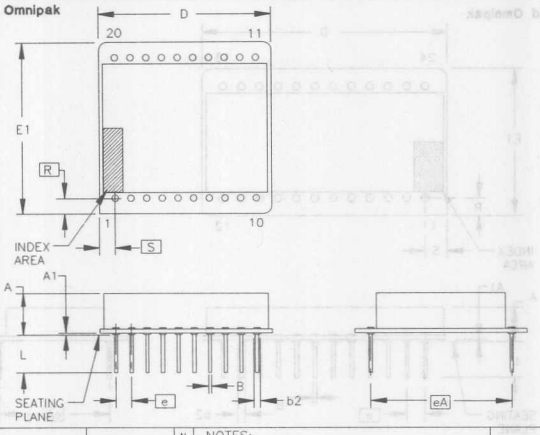



| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .170 | .230 | 4.32 | 5.84 | |
| A1 | .002 | .010 | 0.05 | 0.25 | |
| B | .018 | .021 | 0.46 | 0.53 | |
| b2 | .035 | .050 | 0.89 | 1.27 | |
| D | 1.700 | 1.760 | 43.18 | 44.70 | |
| E1 | 1.120 | 1.160 | 28.45 | 29.46 | |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .900 BASIC | | 22.86 BASIC | | |
| L | .160 | .180 | 4.06 | 4.57 | |
| N | 32 | | 32 | | 3 |
| R | .110 | .130 | 2.79 | 3.30 | |
| S | .110 | .130 | 2.79 | 3.30 | |

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. N IS THE NUMBER OF TERMINAL POSITIONS.
4. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ077 | REV.: C
JEDEC NUMBER: NONE

## Package Number 102 - 20-Lead Omnipak




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .235 | .285 | 5.97 | 7.24 | |
| A1 | .002 | .010 | 0.05 | 0.25 | |
| B | .018 | .021 | 0.46 | 0.53 | |
| b2 | .035 | .050 | 0.89 | 1.27 | |
| D | 1.080 | 1.120 | 27.43 | 28.45 | |
| E1 | 1.080 | 1.120 | 27.43 | 28.45 | |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .900 BASIC | | 22.86 BASIC | | |
| L | .150 | .350 | 3.81 | 8.89 | |
| N | 20 | | 20 | | 3 |
| R | .100 BASIC | | 2.54 BASIC | | |
| S | .100 BASIC | | 2.54 BASIC | | |

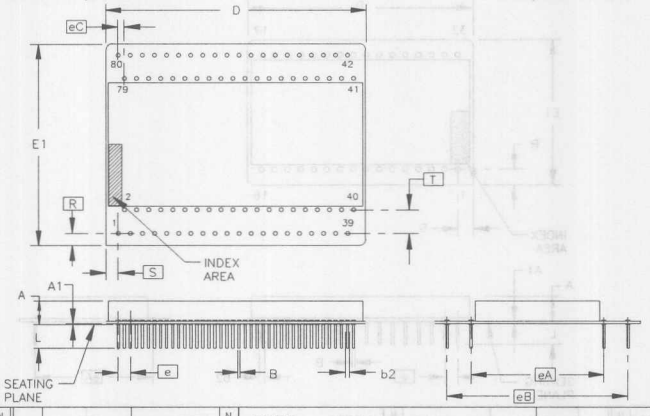
| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. N IS THE NUMBER OF TERMINAL POSITIONS.
4. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: ZZ102 | REV.: B |
|---|---|
| JEDEC NUMBER: NONE | |

## Package Number 103 - 80-Lead Omnipak




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .170 | .230 | 4.32 | 5.84 | |
| A1 | .002 | .010 | 0.05 | 0.25 | |
| B | .018 | .021 | 0.46 | 0.53 | |
| b2 | .035 | .050 | 0.89 | 1.27 | |
| D | 2.120 | 2.180 | 53.85 | 55.37 | |
| E1 | 1.670 | 1.720 | 42.42 | 43.69 | |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | 1.100 BASIC | | 27.94 BASIC | | |
| eB | 1.500 BASIC | | 38.10 BASIC | | |
| eC | .050 BASIC | | 1.27 BASIC | | |
| L | .150 | .250 | 3.81 | 6.35 | |
| N | 80 | | 80 | | 3 |
| R | .100 BASIC | | 2.54 BASIC | | |
| S | .100 BASIC | | 2.54 BASIC | | |

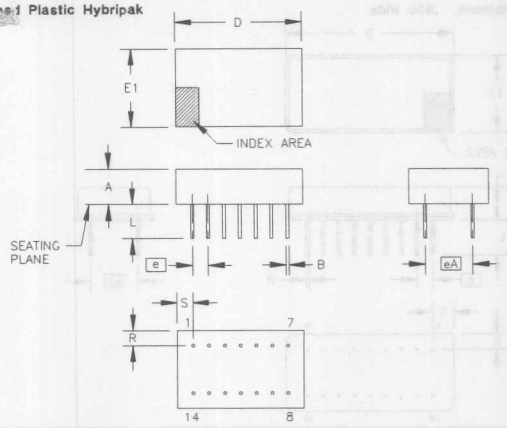
| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| T | .200 BASIC | | 5.08 BASIC | | |

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. N IS THE NUMBER OF TERMINAL POSITIONS.
4. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: ZZ103 | REV.: A |
|---|---|
| JEDEC NUMBER: NONE | |

**Package Number 105 - 14-Lead Plastic Hybripak**



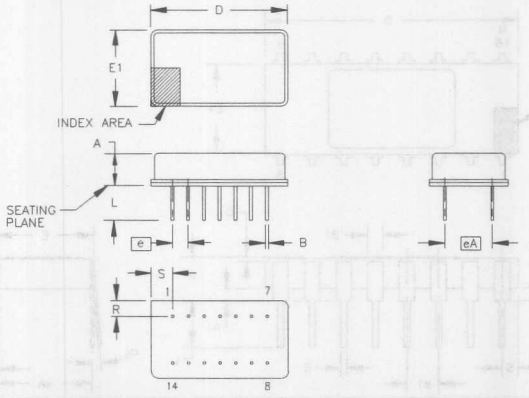

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .190 | .260 | 4.83 | 6.60 | |
| B | .018 | .021 | 0.46 | 0.53 | |
| D | .790 | .810 | 20.07 | 20.57 | |
| E1 | .490 | .510 | 12.45 | 12.95 | |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .300 BASIC | | 7.62 BASIC | | |
| L | .130 | .300 | 3.30 | 7.62 | |
| N | 14 | | 14 | | 3 |
| R | .080 | .115 | 2.03 | 2.92 | |
| S | .080 | .115 | 2.03 | 2.92 | |

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS ARE NOT MARKED ON PACKAGE.
3. N IS THE NUMBER OF TERMINAL POSITIONS.
4. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ105 | REV.: B
JEDEC NUMBER: NONE

**Package Number 107 - 14-Lead Metal Platform, .300 Wide**

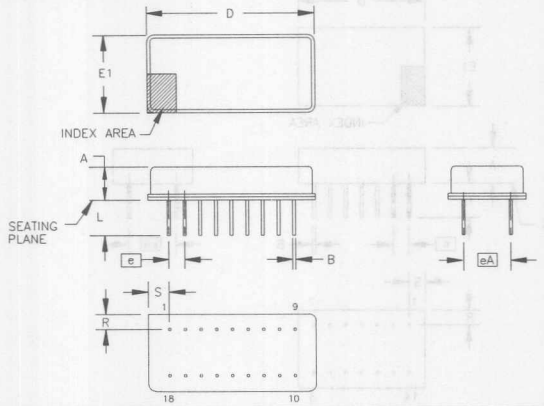



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .170 | .250 | 4.32 | 6.35 | |
| B | .016 | .021 | 0.41 | 0.53 | |
| D | .860 | .880 | 21.84 | 22.35 | |
| E1 | .490 | .510 | 12.45 | 12.95 | |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .300 BASIC | | 7.62 BASIC | | |
| L | .150 | .300 | 3.81 | 7.62 | |
| N | 14 | | 14 | | 3 |
| R | .080 | .120 | 2.03 | 3.05 | |
| S | .115 | .155 | 2.92 | 3.94 | |

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON THE PACKAGE.
3. N IS THE NUMBER OF TERMINAL POSITIONS.
4. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ107 | REV.: B
JEDEC NUMBER: NONE



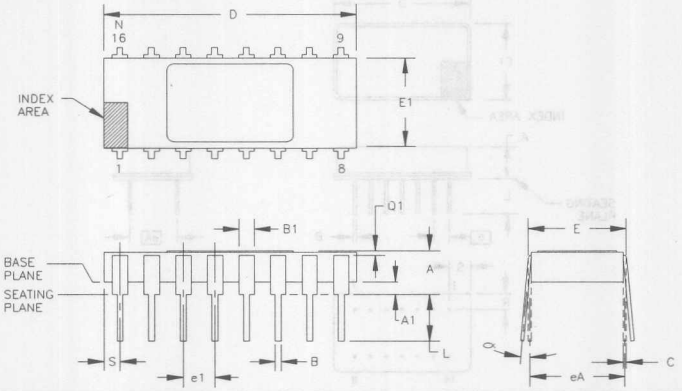

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .170 | .250 | 4.32 | 6.35 | |
| B | .016 | .021 | 0.41 | 0.53 | |
| D | 1.060 | 1.080 | 26.92 | 27.43 | |
| E1 | .490 | .510 | 12.45 | 12.95 | |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .300 | BASIC | 7.62 | BASIC | |
| L | .150 | .300 | 3.81 | 7.62 | |
| N | 18 | | 18 | | 3 |
| R | .080 | .120 | 2.03 | 3.05 | |
| S | .115 | .155 | 2.92 | 3.94 | |

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS ARE NOT MARKED ON PACKAGE.
3. N IS THE NUMBER OF TERMINAL POSITIONS.
4. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ108 | REV.: B
JEDEC NUMBER: NONE

**Package Number 109 - 16-Lead, Ceramic Side Braze DIP, .300 Wide**




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .105 | .175 | 2.67 | 4.45 | |
| A1 | .025 | .055 | 0.64 | 1.40 | |
| B | .015 | .021 | 0.38 | 0.53 | 5 |
| B1 | .038 | .060 | 0.97 | 1.52 | 5 |
| C | .008 | .012 | 0.20 | 0.30 | |
| D | .770 | .830 | 19.56 | 21.08 | |
| E | .290 | .325 | 7.37 | 8.26 | |
| E1 | .280 | .310 | 7.11 | 7.87 | 6 |
| e1 | .100 | TYP. | 2.54 | TYP. | 2 |
| eA | .300 | TYP. | 7.62 | TYP. | 2 |
| L | .125 | .175 | 3.18 | 4.45 | |
| N | 16 | | 16 | | 4 |
| Q1 | .010 | -- | 0.25 | -- | |
| S | .020 | .065 | 0.51 | 1.65 | |
| ∝ | 0° | 15° | 0° | 15° | 3 |

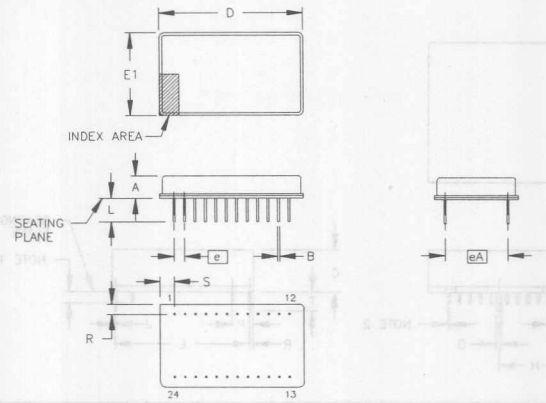
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ109 | REV.: D
JEDEC NUMBER: MO-36-AD

PACKAGE DRAWINGS (Mechanical)

**Package Number 113 - 24-Lead Metal Platform, .600 Wide**



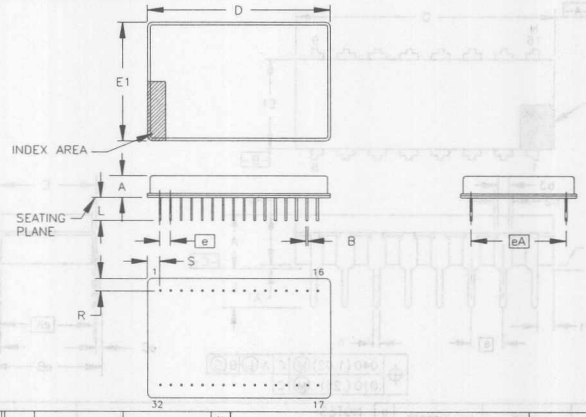

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .170 | .250 | 4.32 | 6.35 | |
| B | .016 | .021 | 0.41 | 0.53 | |
| D | 1.365 | 1.385 | 34.67 | 35.18 | |
| E1 | .790 | .810 | 20.07 | 20.57 | |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .600 | BASIC | 15.24 | BASIC | |
| L | .150 | .300 | 3.81 | 7.62 | |
| N | 24 | | 24 | | 3 |
| R | .080 | .110 | 2.03 | 2.79 | |
| S | .125 | .150 | 3.18 | 3.81 | |

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON THE PACKAGE.
3. N IS THE NUMBER OF TERMINAL POSITIONS.
4. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ113 | REV.: B
JEDEC NUMBER: NONE

**Package Number 116 - 32-Lead Metal Platform, .900 Wide**



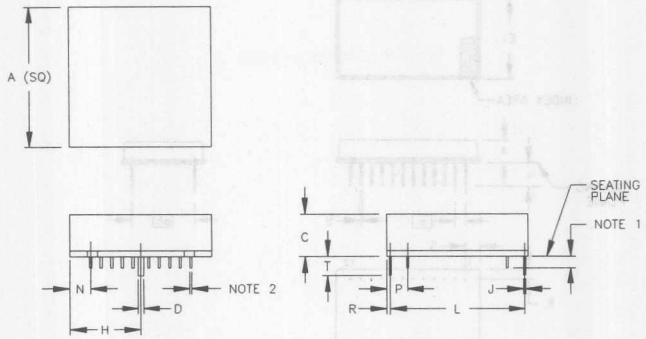

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .170 | .250 | 4.32 | 6.35 | |
| B | .016 | .021 | 0.41 | 0.53 | |
| D | 1.720 | 1.760 | 43.69 | 44.70 | |
| E1 | 1.120 | 1.160 | 28.45 | 29.46 | |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .900 | BASIC | 22.86 | BASIC | |
| L | .150 | .300 | 3.81 | 7.62 | |
| N | 32 | | 32 | | 3 |
| R | .100 | .140 | 2.54 | 3.56 | |
| S | .100 | .140 | 2.54 | 3.56 | |

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON THE PACKAGE.
3. N IS THE NUMBER OF TERMINAL POSITIONS.
4. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ116 | REV.: B
JEDEC NUMBER: NONE

## Package Number 124 - EMI Shield



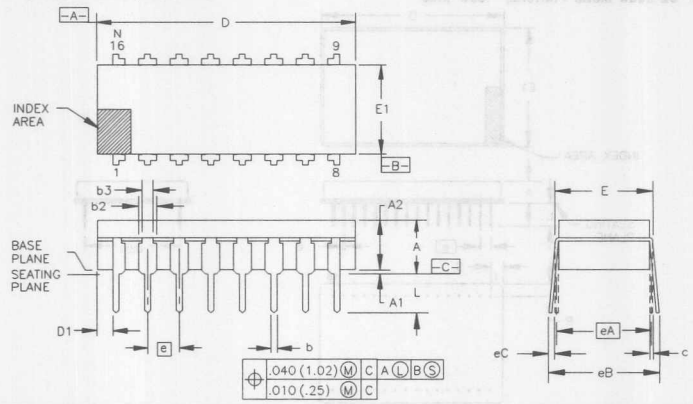

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | 1.320 | 1.380 | 33.53 | 35.05 | |
| C | .350 | .450 | 8.89 | 11.43 | |
| D | .040 | .060 | 1.02 | 1.52 | |
| H | .600 | .700 | 15.24 | 17.78 | |
| J | .015 | .025 | 0.38 | 0.64 | |
| L | 1.180 | 1.280 | 29.97 | 32.51 | |
| N | .150 | .250 | 3.81 | 6.35 | |
| P | .150 | .250 | 3.81 | 6.35 | |
| R | .015 | .055 | 0.38 | 1.40 | |
| T | .130 | .230 | 3.30 | 5.84 | |

NOTES:

1. ENCLOSED MODULE LEAD LENGTH MINUS .050" TO .100" (1.27mm TO 2.54mm).
2. PIN DIAMETER DETERMINED BY ENCLOSED MODULE.

PACKAGE NUMBER: ZZ124 | REV.: A
JEDEC NUMBER: NONE

## Package Number 129 - 16-Lead CERDIP, .300 Wide




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .230 | -- | 5.84 | |
| A1 | .015 | -- | 0.38 | -- | |
| A2 | .140 | .180 | 3.56 | 4.57 | |
| b | .015 | .023 | 0.38 | 0.58 | 9 |
| b2 | .045 | .070 | 1.14 | 1.78 | |
| b3 | .035 | TYP | 0.89 | TYP | |
| c | .008 | .015 | 0.20 | 0.38 | 9 |
| D | .753 | .885 | 19.13 | 22.48 | 3 |
| D1 | .005 | -- | 0.13 | -- | |
| E | .300 | .325 | 7.62 | 8.25 | 4 |
| E1 | .280 | .295 | 7.11 | 7.50 | 3 |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .300 | BASIC | 7.62 | BASIC | 4 |
| eB | -- | .450 | -- | 11.43 | 5 |

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| eC | .000 | -- | 0.00 | -- | 5 |
| L | .100 | -- | 2.54 | -- | |
| N | 16 | | 16 | | 6 |

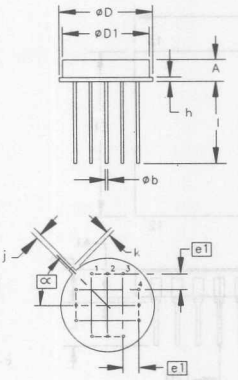
NOTES:

1. CONTROLLING DIMENSIONS: INCH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D AND E1 DIMENSIONS INCLUDE ALLOWANCE FOR GLASS OVERRUN AND MENISCUS, AND LID TO BASE MISMATCH.
4. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE C.
5. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
6. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
7. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
8. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
9. b AND c DIMENSIONS INCLUDE BOTH THE BASE MATERIAL AND THE COATING OR PLATING ON THE LEADS.
10. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ129 | REV.: D
JEDEC NUMBER: NONE

PACKAGE DRAWINGS (Mechanical)

**Package Number 138 - 12-Lead TO-8**

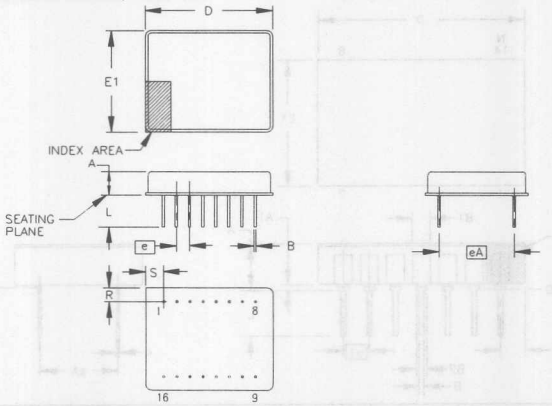



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .130 | .150 | 3.30 | 3.81 | |
| b | .016 | .019 | 0.41 | 0.48 | |
| D | .593 | .603 | 15.06 | 15.32 | |
| D1 | .547 | .553 | 13.79 | 14.05 | |
| e1 | .100 | BASIC | 2.54 | BASIC | |
| h | .010 | .040 | 0.25 | 1.02 | |
| l | .500 | .562 | 12.70 | 14.27 | |
| j | .026 | .036 | 0.66 | 0.91 | |
| k | .026 | .036 | 0.66 | 0.91 | |
| N | 12 | | 12 | | 3 |
| α | 45° | BASIC | 45° | BASIC | |

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. N IS THE NUMBER OF TERMINAL POSITIONS.

PACKAGE NUMBER: ZZ138 | REV.: A
JEDEC NUMBER: UNKNOWN

**Package Number 142 - 16-Lead Metal Platform, .600 Wide**

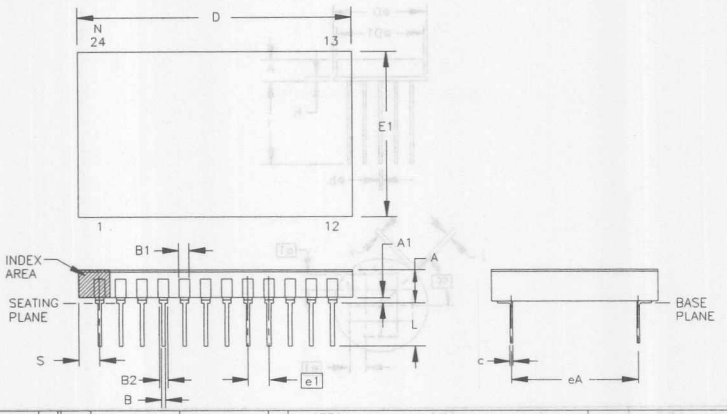



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .175 | .190 | 4.45 | 4.83 | |
| B | .014 | .022 | 0.36 | 0.56 | |
| D | .963 | .980 | 24.46 | 24.89 | |
| E1 | .760 | .805 | 19.30 | 20.45 | |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .600 | BASIC | 15.24 | BASIC | |
| L | .230 | .270 | 5.84 | 6.86 | |
| N | 16 | | 16 | | 3 |
| R | .095 | .115 | 2.41 | 2.92 | |
| S | .135 | .155 | 3.43 | 3.94 | |

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON THE PACKAGE.
3. N IS THE NUMBER OF TERMINAL POSITIONS.
4. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ142 | REV.: B
JEDEC NUMBER: NONE

## Package Number 143 - 24-Lead Bottom Braze DIP, .600 Wide



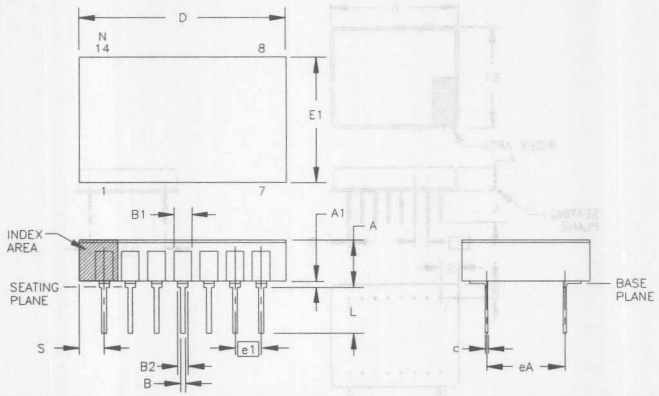

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .130 | .180 | 3.30 | 4.57 | |
| A1 | .015 | .035 | 0.38 | 0.89 | |
| B | .016 | .020 | 0.41 | 0.51 | |
| B1 | .045 | .055 | 1.14 | 1.40 | |
| B2 | .035 | .045 | 0.89 | 1.14 | |
| c | .009 | .012 | 0.23 | 0.30 | |
| D | 1.280 | 1.310 | 32.51 | 33.27 | |
| E1 | .780 | .800 | 19.81 | 20.32 | |
| e1 | .100 BASIC | | 2.54 BASIC | | |
| eA | .590 | .610 | 14.99 | 15.49 | |
| L | .200 | .210 | 5.08 | 5.33 | |
| N | 24 | | 24 | | |
| S | .088 | .108 | 2.24 | 2.74 | |

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ143 | REV.: C
JEDEC NUMBER: NONE

## Package Number 148 - 14-Lead Bottom Braze DIP, .300 Wide




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .155 | .215 | 3.94 | 5.46 | |
| A1 | .015 | .035 | 0.38 | 0.89 | |
| B | .016 | .020 | 0.41 | 0.51 | |
| B1 | .045 | .055 | 1.14 | 1.40 | |
| B2 | .035 | .045 | 0.89 | 1.14 | |
| c | .009 | .012 | 0.23 | 0.30 | |
| D | .770 | .810 | 19.56 | 20.57 | |
| E1 | .480 | .500 | 12.19 | 12.70 | |
| e1 | .100 BASIC | | 2.54 BASIC | | |
| eA | .290 | .310 | 7.37 | 7.87 | |
| L | .150 | .210 | 3.81 | 5.33 | |
| N | 14 | | 14 | | |
| S | .080 | .110 | 2.03 | 2.79 | |

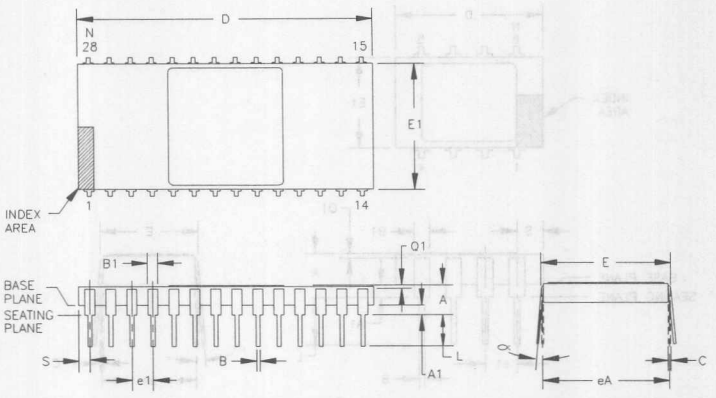
| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ148 | REV.: A
JEDEC NUMBER: NONE

PACKAGE DRAWINGS (Mechanical)

**Package Number 149 - 28-Lead Side Braze DIP, .600 Wide**




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .085 | .190 | 2.16 | 4.83 | |
| A1 | .020 | .070 | 0.51 | 1.78 | |
| B | .015 | .023 | 0.38 | 0.58 | 5 |
| B1 | .038 | .060 | 0.97 | 1.52 | 5 |
| C | .008 | .012 | 0.20 | 0.30 | |
| D | 1.380 | 1.430 | 35.05 | 36.32 | |
| E | .595 | .625 | 15.11 | 15.88 | |
| E1 | .580 | .610 | 14.73 | 15.49 | 6 |
| e1 | .100 TYP. | | 2.54 TYP. | | 2 |
| eA | .600 TYP. | | 15.24 TYP. | | 2 |
| L | .125 | .175 | 3.18 | 4.45 | |
| N | 28 | | 28 | | 4 |
| Q1 | .010 | -- | 0.25 | -- | |
| S | .030 | .065 | 0.76 | 1.65 | |

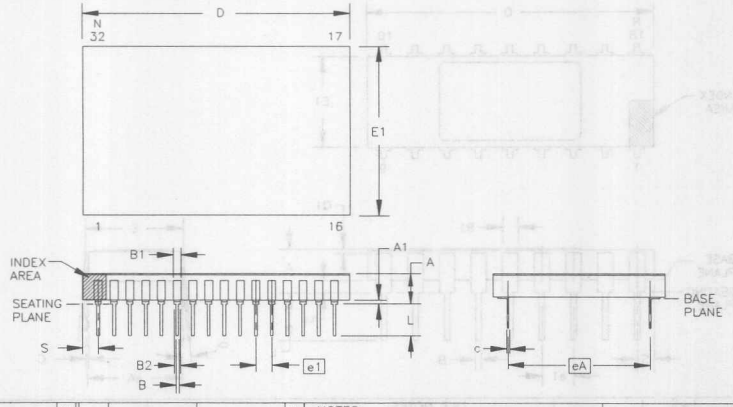
| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| ∝ | 0° | 15° | 0° | 15° | 3 |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0). TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: ZZ149 | REV.: C |
|---|---|
| JEDEC NUMBER: MO-038-AB | |

**Package Number 153 - 32-Lead Bottom Braze DIP, .900 Wide**



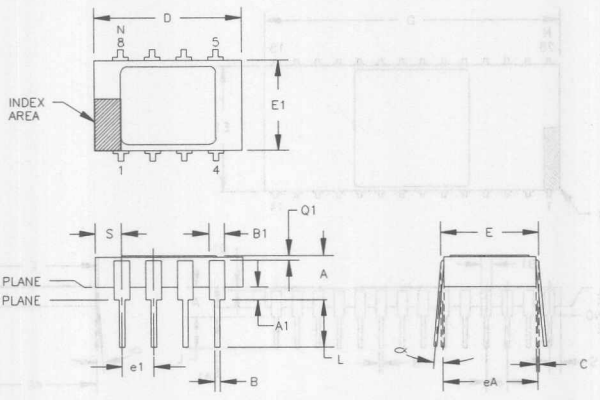

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .180 | .210 | 4.57 | 5.33 | |
| A1 | .015 | .035 | 0.38 | 0.89 | |
| B | .016 | .020 | 0.41 | 0.51 | |
| B1 | .045 | .055 | 1.14 | 1.40 | |
| B2 | .035 | .045 | 0.89 | 1.14 | |
| c | .009 | .012 | 0.23 | 0.30 | |
| D | 1.678 | 1.712 | 42.62 | 43.48 | |
| E1 | 1.079 | 1.101 | 27.41 | 27.97 | |
| e1 | .100 BASIC | | 2.54 BASIC | | |
| eA | .900 BASIC | | 22.86 BASIC | | |
| L | .200 | .210 | 5.08 | 5.33 | |
| N | 32 | | 32 | | |
| S | .089 | .106 | 2.26 | 2.69 | |

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: ZZ153 | REV.: A |
|---|---|
| JEDEC NUMBER: NONE | |

**Package Number 167 - 8-Lead, Ceramic Side Braze DIP, .300 Wide**




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .105 | .175 | 2.67 | 4.45 | |
| A1 | .025 | .055 | 0.64 | 1.40 | |
| B | .015 | .021 | 0.38 | 0.53 | 5 |
| B1 | .038 | .060 | 0.97 | 1.52 | 5 |
| C | .008 | .012 | 0.20 | 0.30 | |
| D | .380 | .550 | 9.65 | 13.97 | |
| E | .290 | .325 | 7.37 | 8.26 | |
| E1 | .280 | .310 | 7.11 | 7.87 | 6 |
| e1 | .100 TYP. | | 2.54 TYP. | | 2 |
| eA | .300 TYP. | | 7.62 TYP. | | 2 |
| L | .125 | .175 | 3.18 | 4.45 | |
| N | 8 | | 8 | | 4 |
| Q1 | .010 | -- | 2.54 | -- | |
| S | .030 | .120 | 0.76 | 3.05 | |

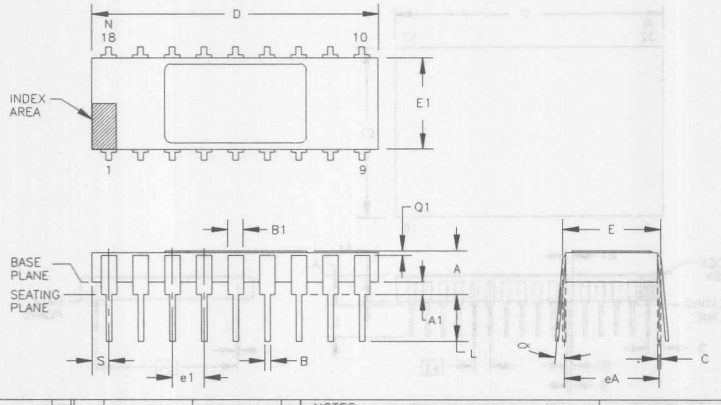
| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| ∝ | 0° | 15° | 0° | 15° | 3 |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: ZZ157 | REV.: C |
|---|---|
| JEDEC NUMBER: MO-36-AA | |

**Package Number 158 - 18-Lead, Ceramic Side Braze DIP, .300 Wide**




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .105 | .175 | 2.67 | 4.45 | |
| A1 | .025 | .055 | 0.64 | 1.40 | |
| B | .015 | .021 | 0.38 | 0.53 | 5 |
| B1 | .038 | .060 | 0.97 | 1.52 | 5 |
| C | .008 | .012 | 0.20 | 0.30 | |
| D | .880 | .930 | 22.35 | 23.62 | |
| E | .290 | .325 | 7.37 | 8.26 | |
| E1 | .280 | .310 | 7.11 | 7.87 | 6 |
| e1 | .100 TYP. | | 2.54 TYP. | | 2 |
| eA | .300 TYP. | | 7.62 TYP. | | 2 |
| L | .125 | .175 | 3.18 | 4.45 | |
| N | 18 | | 18 | | 4 |
| Q1 | .010 | -- | 0.25 | -- | |
| S | .030 | .065 | 0.76 | 1.65 | |

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| ∝ | 0° | 15° | 0° | 15° | 3 |

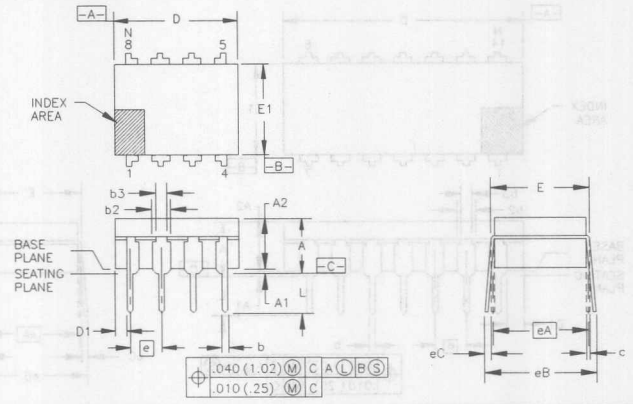
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: ZZ158 | REV.: C |
|---|---|
| JEDEC NUMBER: MO-36-AE | |

PACKAGE DRAWINGS (Mechanical)

**Package Number 161 - 8-Lead CERDIP, .300 Wide**



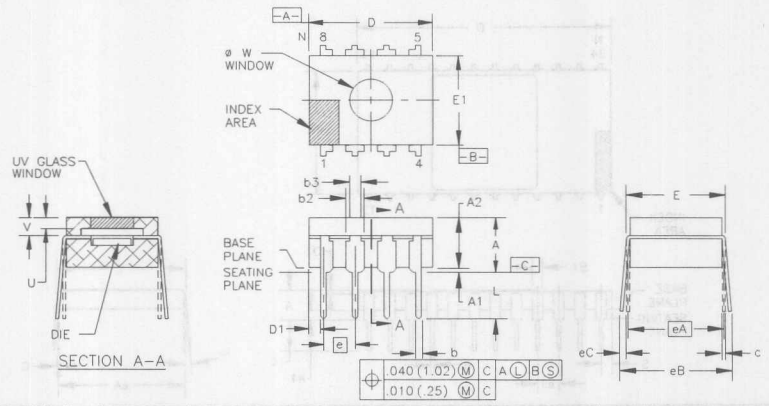

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .230 | -- | 5.84 | |
| A1 | .015 | -- | 0.38 | -- | |
| A2 | .140 | .180 | 3.56 | 4.57 | |
| b | .015 | .023 | 0.38 | 0.58 | 9 |
| b2 | .045 | .070 | 1.14 | 1.78 | |
| b3 | .035 | TYP | 0.89 | TYP | |
| c | .008 | .015 | 0.20 | 0.38 | 9 |
| D | .375 | .405 | 9.53 | 10.28 | 3 |
| D1 | .005 | -- | 0.13 | -- | |
| E | .300 | .325 | 7.62 | 8.25 | 4 |
| E1 | .280 | .295 | 7.11 | 7.50 | 3 |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .300 | BASIC | 7.62 | BASIC | 4 |
| eB | -- | .450 | -- | 11.43 | 5 |

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| eC | .000 | -- | 0.00 | -- | 5 |
| L | .100 | -- | 2.54 | -- | |
| N | 8 | | 8 | | 6 |

NOTES:
1. CONTROLLING DIMENSIONS: INCH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D AND E1 DIMENSIONS INCLUDE ALLOWANCE FOR GLASS OVERRUN AND MENISCUS, AND LID TO BASE MISMATCH.
4. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE C.
5. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
6. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
7. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
8. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
9. b AND c DIMENSIONS INCLUDE BOTH THE BASE MATERIAL AND THE COATING OR PLATING ON THE LEADS.
10. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: ZZ161 | REV.: C |
|---|---|
| JEDEC NUMBER: NONE | |

**Package Number 161-1 - 8-Lead CERDIP With Window, .300 Wide**



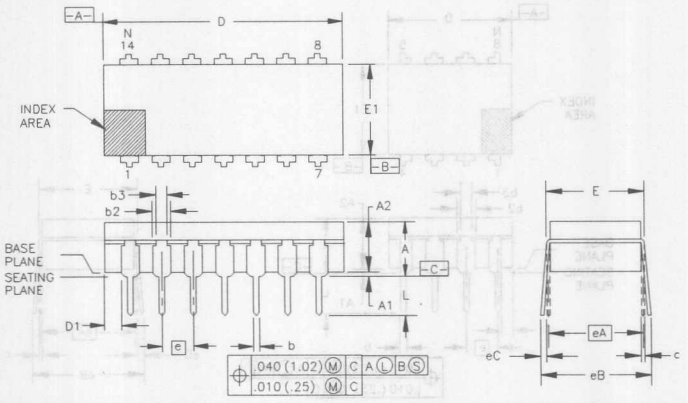

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .230 | -- | 5.84 | |
| A1 | .015 | -- | 0.38 | -- | |
| A2 | .140 | .180 | 3.56 | 4.57 | |
| b | .015 | .023 | 0.38 | 0.58 | 9 |
| b2 | .045 | .070 | 1.14 | 1.78 | |
| b3 | .035 | TYP | 0.89 | TYP | |
| c | .008 | .015 | 0.20 | 0.38 | 9 |
| D | .395 | .425 | 10.03 | 10.80 | 3 |
| D1 | .005 | -- | 0.13 | -- | |
| E | .300 | .325 | 7.62 | 8.25 | 4 |
| E1 | .280 | .295 | 7.11 | 7.50 | 3 |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .300 | BASIC | 7.62 | BASIC | 4 |
| eB | -- | .450 | -- | 11.43 | 5 |

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| eC | .000 | -- | 0.00 | -- | 5 |
| L | .100 | -- | 2.54 | -- | |
| N | 8 | | 8 | | 6 |
| U | .032 | .038 | 0.81 | 0.97 | |
| V | .058 | .064 | 1.47 | 1.63 | |
| W | .131 | .139 | 3.33 | 3.53 | |

NOTES:
1. CONTROLLING DIMENSIONS: INCH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D AND E1 DIMENSIONS INCLUDE ALLOWANCE FOR GLASS OVERRUN AND MENISCUS, AND LID TO BASE MISMATCH.
4. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE C.
5. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
6. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
7. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
8. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
9. b AND c DIMENSIONS INCLUDE BOTH THE BASE MATERIAL AND THE COATING OR PLATING ON THE LEADS.
10. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: ZZ161-1 | REV.: C |
|---|---|
| JEDEC NUMBER: NONE | |

## Package Number 163 - 14-Lead CERDIP, .300 Wide




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .230 | -- | 5.84 | |
| A1 | .015 | -- | 0.38 | -- | |
| A2 | .140 | .180 | 3.56 | 4.57 | |
| b | .015 | .023 | 0.38 | 0.58 | 9 |
| b2 | .045 | .070 | 1.14 | 1.78 | |
| b3 | .035 | TYP | 0.89 | TYP | |
| c | .008 | .015 | 0.20 | 0.38 | 9 |
| D | .753 | .767 | 19.13 | 19.48 | 3 |
| D1 | .005 | -- | 0.13 | -- | |
| E | .300 | .325 | 7.62 | 8.26 | 4 |
| E1 | .280 | .295 | 7.11 | 7.50 | 3 |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .300 | BASIC | 7.62 | BASIC | 4 |
| eB | -- | .450 | -- | 11.43 | 5 |

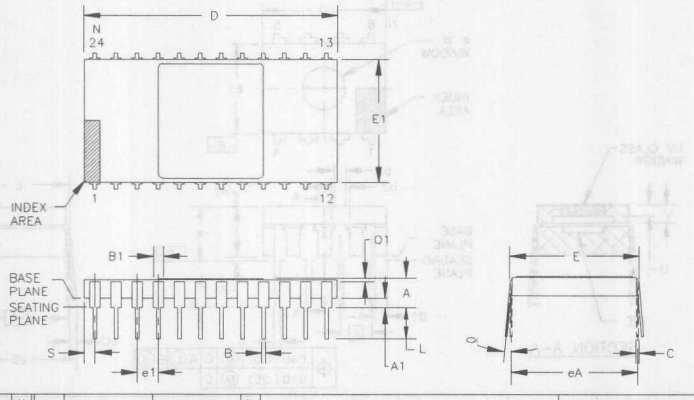
| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| eC | .000 | -- | 0.00 | -- | 5 |
| L | .100 | -- | 2.54 | -- | |
| N | 14 | | 14 | | 6 |

NOTES:

1. CONTROLLING DIMENSIONS: INCH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D AND E1 DIMENSIONS INCLUDE ALLOWANCE FOR GLASS OVERRUN AND MENISCUS, AND LID TO BASE MISMATCH.
4. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE C.
5. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
6. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
7. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
8. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
9. b AND c DIMENSIONS INCLUDE BOTH THE BASE MATERIAL AND THE COATING OR PLATING ON THE LEADS.
10. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: | ZZ163 | REV.: | C |
|---|---|---|---|
| JEDEC NUMBER: | NONE | | |

## Package Number 165 - 24-Lead Side Braze DIP, .600 Wide




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .085 | .190 | 2.16 | 4.83 | |
| A1 | .020 | .070 | 0.51 | 1.78 | |
| B | .015 | .023 | 0.38 | 0.58 | 5 |
| B1 | .038 | .060 | 0.97 | 1.52 | 5 |
| C | .008 | .012 | 0.20 | 0.30 | |
| D | 1.180 | 1.220 | 29.97 | 30.99 | |
| E | .595 | .625 | 15.11 | 15.88 | |
| E1 | .580 | .610 | 14.73 | 15.49 | 6 |
| e1 | .100 | TYP. | 2.54 | TYP. | 2 |
| eA | .600 | TYP. | 15.24 | TYP. | 2 |
| L | .125 | .175 | 3.18 | 4.45 | |
| N | 24 | | 24 | | 4 |
| Q1 | .010 | -- | 0.25 | -- | |
| S | .030 | .065 | 0.76 | 1.65 | |

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| α | 0° | 15° | 0° | 15° | 3 |

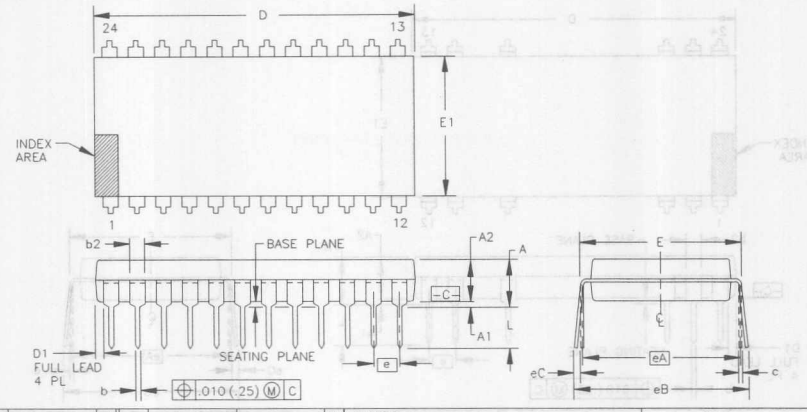
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. α APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0). TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: | ZZ165 | REV.: | C |
|---|---|---|---|
| JEDEC NUMBER: | MO-038-AA | | |

PACKAGE DRAWINGS (Mechanical)

**Package Number 167 - 24-Pin Plastic Double-Wide DIP**



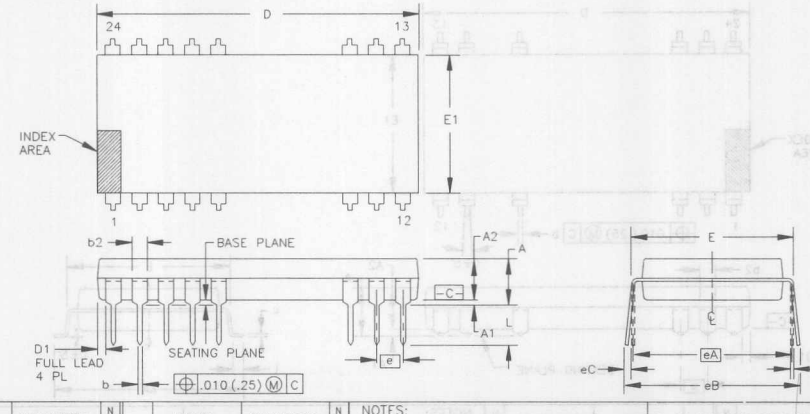

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .250 | -- | 6.35 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .125 | .195 | 3.18 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .030 | .070 | 0.76 | 1.78 | 9 |
| c | .008 | .015 | 0.20 | 0.38 | |
| D | 1.150 | 1.290 | 29.21 | 32.77 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .600 | .625 | 15.24 | 15.88 | 5 |
| E1 | .485 | .580 | 12.32 | 14.73 | 4 |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .600 | BASIC | 15.26 | BASIC | 5 |
| eB | -- | .700 | -- | 17.78 | 6 |
| eC | .000 | .060 | 0.00 | 1.52 | 6 |

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| L | .115 | .200 | 2.92 | 5.08 | 3 |
| N | 24 | | 24 | | 7 |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ167 | REV.: J
JEDEC NUMBER: MS-011-AA

**Package Number 167-1 - 24-Pin Plastic Double-Wide DIP**



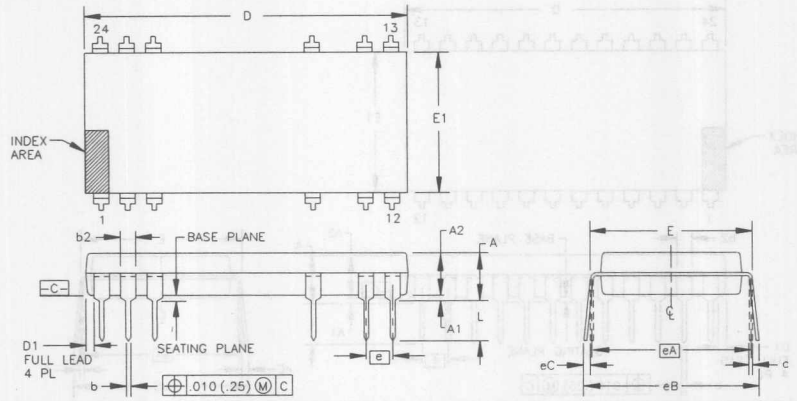

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .250 | -- | 6.35 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .125 | .195 | 3.18 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .030 | .070 | 0.76 | 1.78 | 9 |
| c | .008 | .015 | 0.20 | 0.38 | |
| D | 1.150 | 1.290 | 29.21 | 32.77 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .600 | .625 | 15.24 | 15.88 | 5 |
| E1 | .485 | .580 | 12.32 | 14.73 | 4 |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .600 | BASIC | 15.26 | BASIC | 5 |
| eB | -- | .700 | -- | 17.78 | 6 |
| eC | .000 | .060 | 0.00 | 1.52 | 6 |

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| L | .115 | .200 | 2.92 | 5.08 | 3 |
| N | 16 | | 16 | | 7 |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ167-1 | REV.: C
JEDEC NUMBER: MS-011-AA WITH THE EXCEPTION OF "N"

**Package Number 167-2 - 24-Pin Plastic Double-Wide DIP**



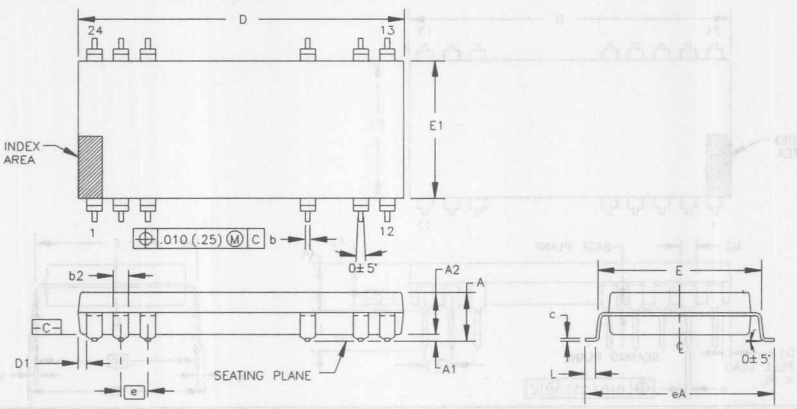

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .250 | -- | 6.35 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .125 | .195 | 3.18 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .030 | .070 | 0.76 | 1.78 | 9 |
| c | .008 | .015 | 0.20 | 0.38 | |
| D | 1.150 | 1.290 | 29.21 | 32.77 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .600 | .625 | 15.24 | 15.88 | 5 |
| E1 | .485 | .580 | 12.32 | 14.73 | 4 |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .600 BASIC | | 15.26 BASIC | | 5 |
| eB | -- | .700 | -- | 17.78 | 6 |
| eC | .000 | .060 | 0.00 | 1.52 | 6 |

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| L | .115 | .200 | 2.92 | 5.08 | 3 |
| N | 12 | | 12 | | 7 |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA ARE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE NUMBER OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ167-2 | REV.: A
JEDEC NUMBER: MS-011-AA WITH THE EXCEPTION OF "N".

**Package Number 167-3 - 24-Pin Plastic Double-Wide DIP With Gull Wing Leads**

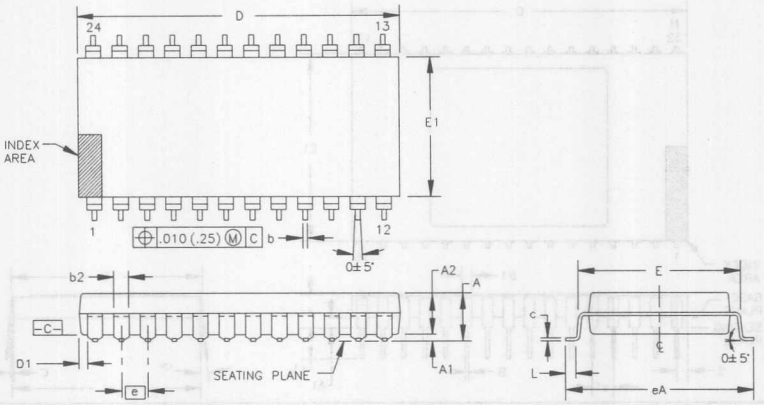



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .250 | -- | 6.35 | |
| A1 | .025 | -- | 0.635 | -- | |
| A2 | .125 | .195 | 3.18 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .030 | .070 | 0.76 | 1.78 | 5 |
| c | .008 | .015 | 0.20 | 0.38 | |
| D | 1.150 | 1.290 | 29.21 | 32.77 | 3 |
| D1 | .005 | -- | 0.13 | -- | 3 |
| E | .600 | .625 | 15.24 | 15.88 | |
| E1 | .485 | .580 | 12.32 | 14.73 | 3 |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .690 | .730 | 17.53 | 18.54 | |
| L | .045 | .057 | 1.15 | 1.45 | |
| N | 12 | | 12 | | 4 |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
6. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
7. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
8. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ167-3 | REV.: A
JEDEC NUMBER: NONE

**Package Number 167-4 - 24-Pin Plastic .600 Wide DIP With Gull Wing Leads**

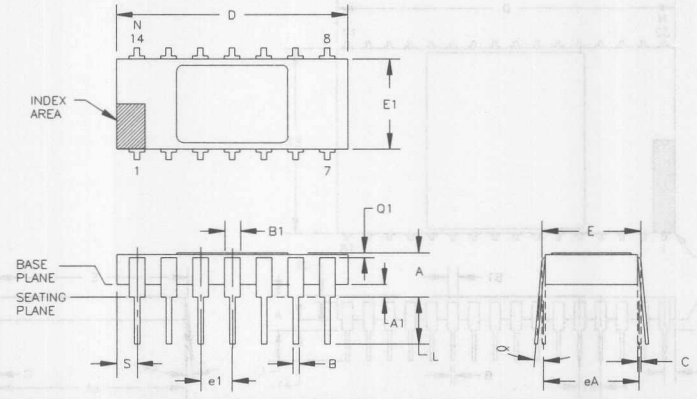



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .250 | -- | 6.35 | |
| A1 | .025 | -- | 0.635 | -- | |
| A2 | .125 | .195 | 3.18 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .030 | .070 | 0.76 | 1.78 | 5 |
| c | .008 | .015 | 0.20 | 0.38 | |
| D | 1.150 | 1.290 | 29.21 | 32.77 | 3 |
| D1 | .005 | -- | 0.13 | -- | 3 |
| E | .600 | .625 | 15.24 | 15.88 | |
| E1 | .485 | .580 | 12.32 | 14.73 | 3 |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .690 | .730 | 17.53 | 18.54 | |
| L | .045 | .057 | 1.15 | 1.45 | |
| N | 24 | | 24 | | 4 |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D, D1, AND E1 DIMENSIONS FOR PLASTIC PACKAGES DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
6. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
7. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
8. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ167-4 | REV.: A
JEDEC NUMBER: NONE

**Package Number 169 - 14-Lead, Ceramic Side Braze DIP, .300 Wide**

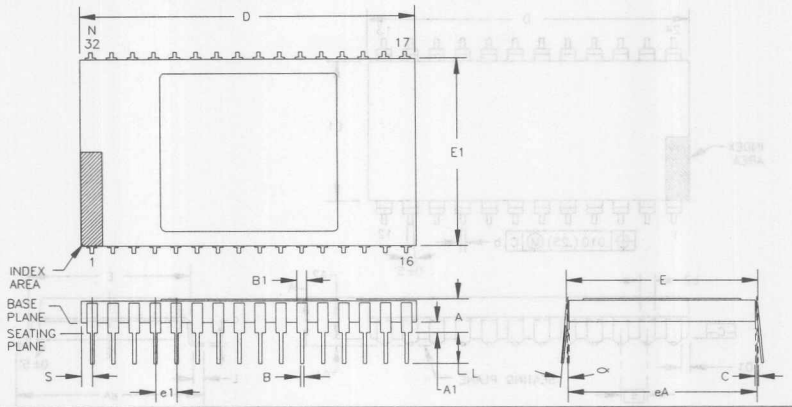



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .105 | .175 | 2.67 | 4.45 | |
| A1 | .025 | .055 | 0.64 | 1.40 | |
| B | .015 | .021 | 0.38 | 0.53 | 5 |
| B1 | .038 | .060 | 0.97 | 1.52 | 5 |
| C | .008 | .012 | 0.20 | 0.30 | |
| D | .690 | .770 | 17.53 | 19.56 | |
| E | .290 | .325 | 7.37 | 8.26 | |
| E1 | .280 | .310 | 7.11 | 7.87 | 6 |
| e1 | .100 TYP. | | 2.54 TYP. | | 2 |
| eA | .300 TYP. | | 7.62 TYP. | | 2 |
| L | .125 | .175 | 3.18 | 4.45 | |
| N | 14 | | 14 | | 4 |
| Q1 | .010 | -- | 0.25 | -- | |
| S | .030 | .095 | 0.76 | 2.41 | |
| ∝ | 0° | 15° | 0° | 15° | 3 |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0). TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ169 | REV.: F
JEDEC NUMBER: MO-36-AB

**Package Number 172 - 32-Lead Side Braze DIP, .900 Wide**



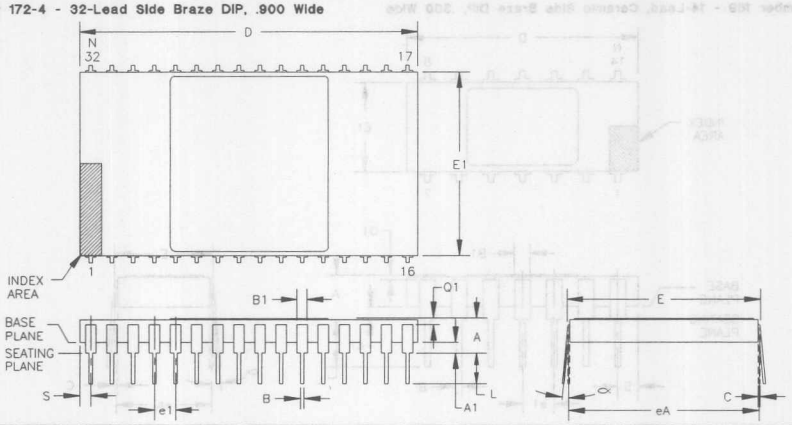

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .138 | .186 | 3.51 | 4.72 | |
| A1 | .040 | .060 | 1.02 | 1.52 | |
| B | .016 | .020 | 0.41 | 0.51 | 5 |
| B1 | .050 TYP. | | 1.27 TYP. | | 5 |
| C | .009 | .012 | 0.23 | 0.30 | |
| D | 1.580 | 1.620 | 40.13 | 41.15 | |
| E | .900 | .920 | 22.86 | 23.37 | |
| E1 | .885 | .905 | 22.48 | 22.99 | 6 |
| e1 | .100 TYP. | | 2.54 TYP. | | 2 |
| eA | .900 TYP. | | 22.86 TYP. | | 2 |
| L | .125 | .175 | 3.18 | 4.45 | |
| N | 32 | | 32 | | 4 |
| S | .030 | .065 | 0.76 | 1.65 | |
| ∝ | 0° | 15° | 0° | 15° | 3 |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0). TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ172 | REV.: B
JEDEC NUMBER: NONE

**Package Number 172-4 - 32-Lead Side Braze DIP, .900 Wide**




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .138 | .190 | 3.51 | 4.83 | |
| A1 | .040 | .060 | 1.02 | 1.52 | |
| B | .016 | .020 | 0.41 | 0.51 | 5 |
| B1 | .050 TYP. | | 1.27 TYP. | | 5 |
| C | .009 | .012 | 0.23 | 0.30 | |
| D | 1.580 | 1.620 | 40.13 | 41.15 | |
| E | .900 | .920 | 22.86 | 23.37 | |
| E1 | .885 | .905 | 22.48 | 22.99 | 6 |
| e1 | .100 TYP. | | 2.54 TYP. | | 2 |
| eA | .900 TYP. | | 22.86 TYP. | | 2 |
| L | .125 | .175 | 3.18 | 4.45 | |
| N | 32 | | 32 | | 4 |
| Q1 | .030 | -- | 0.76 | -- | |
| S | .030 | .065 | 0.76 | 1.65 | |
| ∝ | 0° | 15° | 0° | 15° | 3 |

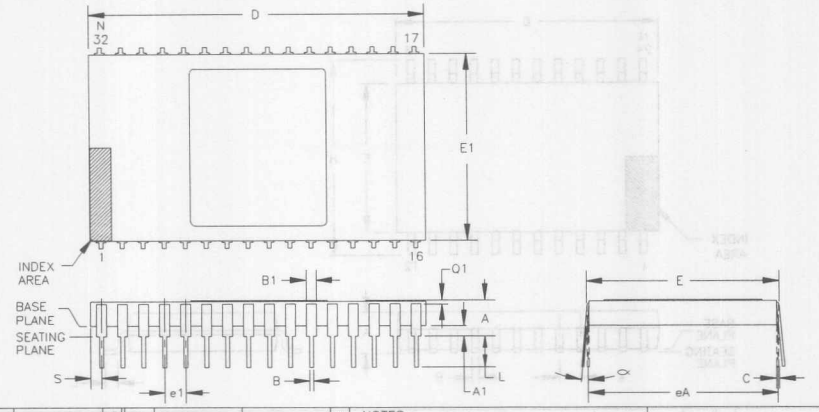
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0). TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ172-4 | REV.: B
JEDEC NUMBER: NONE

PACKAGE DRAWINGS (Mechanical)

**Package Number 172-5 - 32-Lead Side Braze DIP, .900 Wide**




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .145 | .195 | 3.68 | 4.95 | |
| A1 | .040 | .060 | 1.02 | 1.52 | |
| B | .016 | .020 | 0.41 | 0.51 | 5 |
| B1 | .050 TYP. | | 1.27 TYP. | | 5 |
| C | .009 | .012 | 0.23 | 0.30 | |
| D | 1.580 | 1.620 | 40.13 | 41.15 | |
| E | .900 | .920 | 22.86 | 23.37 | |
| E1 | .885 | .905 | 22.48 | 22.99 | 6 |
| e1 | .100 TYP. | | 2.54 TYP. | | 2 |
| eA | .900 TYP. | | 22.86 TYP. | | 2 |
| L | .125 | .175 | 3.18 | 4.45 | |
| N | 32 | | 32 | | 4 |
| Q1 | .010 | -- | 0.25 | -- | |
| S | .030 | .065 | 0.76 | 1.65 | |

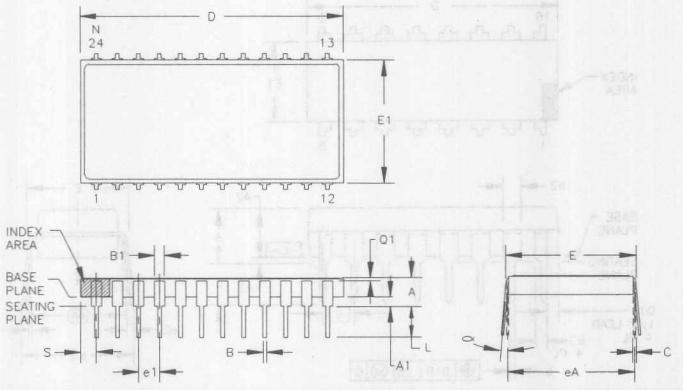
| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| ∝ | 0° | 15° | 0° | 15° | 3 |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: ZZ172-5 | REV.: B |
|---|---|
| JEDEC NUMBER: NONE | |

**Package Number 176 - 24-Lead Side Braze DIP, .600 Wide**




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .085 | .190 | 2.16 | 4.83 | |
| A1 | .020 | .070 | 0.51 | 1.78 | |
| B | .015 | .023 | 0.38 | 0.58 | 5 |
| B1 | .038 | .060 | 0.97 | 1.52 | 5 |
| C | .008 | .012 | 0.20 | 0.30 | |
| D | 1.238 | 1.262 | 31.45 | 32.05 | |
| E | .595 | .625 | 15.11 | 15.88 | |
| E1 | .580 | .610 | 14.73 | 15.49 | 6 |
| e1 | .100 TYP. | | 2.54 TYP. | | 2 |
| eA | .600 TYP. | | 15.24 TYP. | | 2 |
| L | .125 | .175 | 3.18 | 4.45 | |
| N | 24 | | 24 | | 4 |
| Q1 | .010 | -- | 0.25 | -- | |
| S | .060 | .090 | 1.52 | 2.29 | |

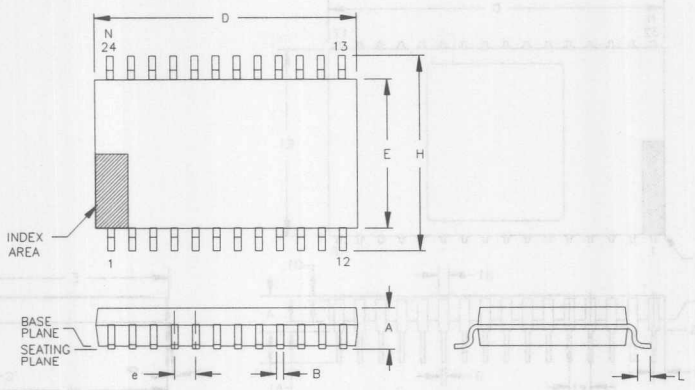
| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| ∝ | 0° | 15° | 0° | 15° | 3 |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: ZZ176 | REV.: D |
|---|---|
| JEDEC NUMBER: MO-038-AA WITH THE EXCEPTION OF DIM. D, S. | |

**Package Number 178 - 24-Lead SOIC, .450 Wide**



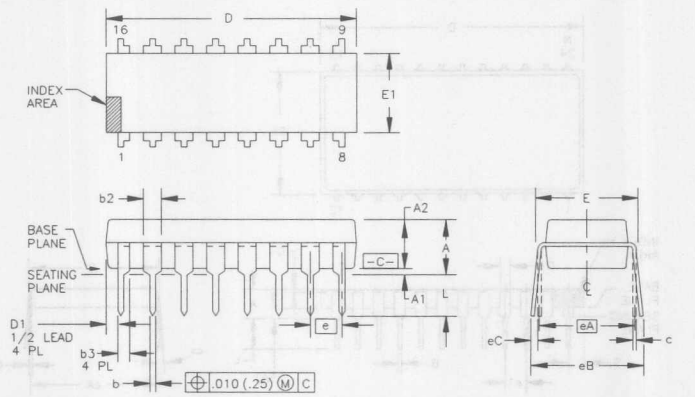

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .098 | -- | 2.50 | |
| B | .012 | .020 | 0.30 | 0.50 | |
| D | .614 | .630 | 15.60 | 16.00 | |
| E | .346 | .362 | 8.80 | 9.20 | |
| e | .046 | .054 | 1.17 | 1.37 | |
| H | .453 | .476 | 11.50 | 12.10 | |
| L | .031 | .047 | 0.80 | 1.20 | |
| N | 24 | | 24 | | 4 |

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
4. N IS THE NUMBER OF TERMINAL POSITIONS.

PACKAGE NUMBER: ZZ178 | REV.: B
JEDEC NUMBER: NONE

**Package Number 180 - 16-Pin Plastic, Single-Wide DIP**




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .210 | -- | 5.33 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .115 | .195 | 2.92 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .045 | .070 | 1.14 | 1.78 | 9 |
| b3 | .030 | .045 | 0.76 | 1.14 | 9 |
| c | .008 | .014 | 0.20 | 0.36 | |
| D | .735 | .775 | 18.67 | 21.34 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .300 | .325 | 7.62 | 8.26 | 5 |
| E1 | .240 | .280 | 6.10 | 7.11 | 4 |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .300 | BASIC | 7.63 | BASIC | 5 |
| eB | -- | .430 | -- | 10.92 | 6 |
| eC | .000 | .060 | 0.00 | 1.52 | 6 |
| L | .115 | .150 | 2.92 | 3.81 | 3 |
| N | 16 | | 16 | | 7 |

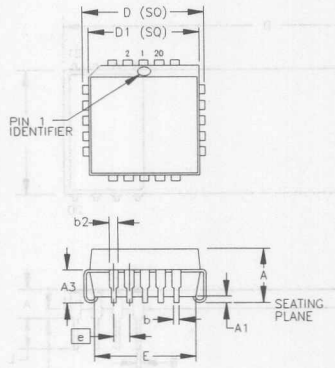
NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ180 | REV.: F
JEDEC NUMBER: MS-001-BB

PACKAGE DRAWINGS (Mechanical)

**Package Number 181 - 20-Pin PLCC**

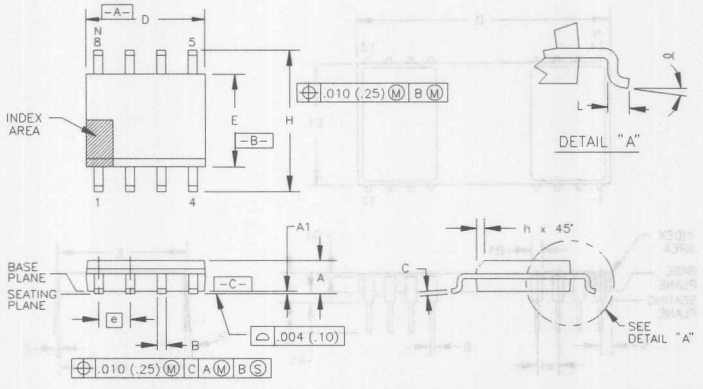



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .165 | .180 | 4.19 | 4.57 | |
| A1 | .020 | -- | 0.51 | -- | |
| A3 | .100 | .110 | 2.54 | 2.79 | |
| b | .013 | .021 | 0.33 | 0.53 | |
| b2 | .026 | .032 | 0.66 | 0.81 | |
| D | .385 | .395 | 9.78 | 10.03 | |
| D1 | .350 | .356 | 8.89 | 9.04 | |
| E | .305 | .325 | 7.75 | 9.26 | |
| e | .050 BASIC | | 1.27 BASIC | | |
| N | 20 | | 20 | | 3 |

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. N IS THE MAXIMUM OF TERMINAL POSITIONS.

PACKAGE NUMBER: ZZ181 | REV.: B
JEDEC NUMBER: UNKNOWN

**Package Number 182 - 8-Lead SOIC**

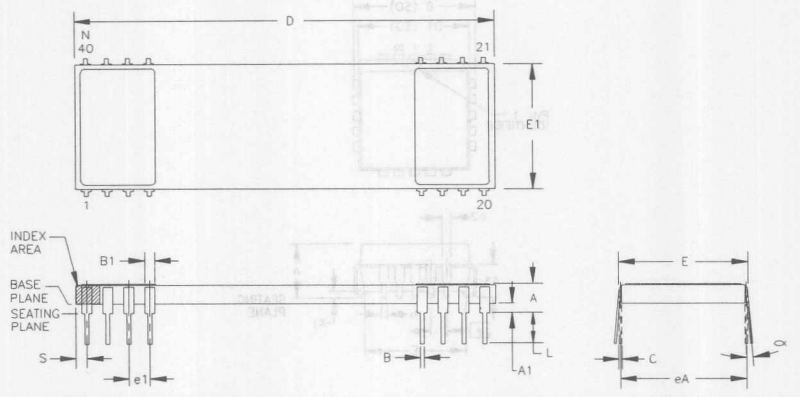



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .0532 | .0688 | 1.35 | 1.75 | |
| A1 | .004 | .0098 | 0.10 | 0.23 | |
| B | .013 | .020 | 0.33 | 0.51 | 7 |
| C | .0075 | .0098 | 0.20 | 0.25 | |
| D | .189 | .1968 | 4.80 | 4.98 | 2 |
| E | .1497 | .1574 | 3.80 | 4.00 | 3 |
| e | .050 BASIC | | 1.27 BASIC | | |
| H | .2284 | .244 | 5.80 | 6.20 | |
| h | .0099 | .0196 | 0.25 | 0.50 | 4 |
| L | .016 | .050 | 0.41 | 1.27 | 5 |
| N | 8 | | 8 | | 6 |
| ∝ | 0° | 8° | 0° | 8° | |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ182 | REV.: H
JEDEC NUMBER: MS-012-AA

**Package Number 206 - 40-Lead Side Braze DIP, .600 Wide, ISO Package**



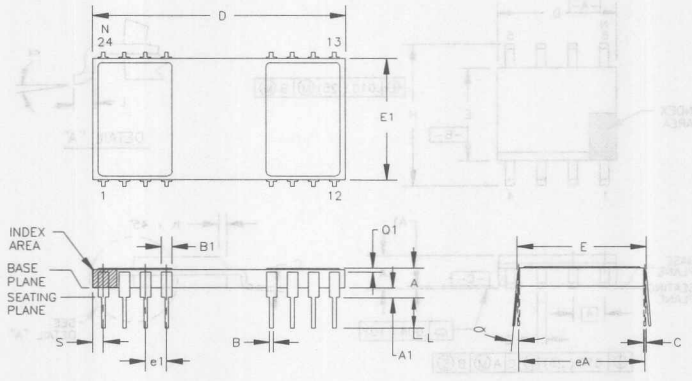

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .085 | .190 | 2.16 | 4.83 | |
| A1 | .020 | .070 | 0.51 | 1.78 | |
| B | .015 | .023 | 0.38 | 0.58 | 5 |
| B1 | .038 | .060 | 0.97 | 1.52 | 5 |
| C | .008 | .012 | 0.20 | 0.30 | |
| D | 1.980 | 2.030 | 50.29 | 51.56 | |
| E | .595 | .625 | 15.11 | 15.88 | |
| E1 | .580 | .610 | 14.73 | 15.49 | 6 |
| e1 | .100 TYP. | | 2.54 TYP. | | 2 |
| eA | .600 TYP. | | 15.24 TYP. | | 2 |
| L | .125 | .175 | 3.18 | 4.45 | |
| N | 16 | | 16 | | 4 |
| S | .030 | .065 | 0.76 | 1.65 | |
| α | 0° | 15° | 0° | 15° | 3 |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. α APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| | |
|---|---|
| PACKAGE NUMBER: ZZ206 | REV.: C |
| JEDEC NUMBER: MO-038-AC WITH THE EXCEPTION OF "N" | |

**Package Number 208 - 24-Lead Side Braze DIP, .600 Wide, ISO Package**




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .085 | .190 | 2.16 | 4.83 | |
| A1 | .020 | .070 | 0.51 | 1.78 | |
| B | .015 | .023 | 0.38 | 0.58 | 5 |
| B1 | .038 | .060 | 0.97 | 1.52 | 5 |
| C | .008 | .012 | 0.20 | 0.30 | |
| D | 1.180 | 1.220 | 29.97 | 30.99 | |
| E | .595 | .625 | 15.11 | 15.88 | |
| E1 | .580 | .610 | 14.73 | 15.49 | 6 |
| e1 | .100 TYP. | | 2.54 TYP. | | 2 |
| eA | .600 TYP. | | 15.24 TYP. | | 2 |
| L | .125 | .175 | 3.18 | 4.45 | |
| N | 16 | | 16 | | 4 |
| Q1 | .010 | -- | 0.25 | -- | |
| S | .030 | .065 | 0.76 | 1.65 | |

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| α | 0° | 15° | 0° | 15° | 3 |

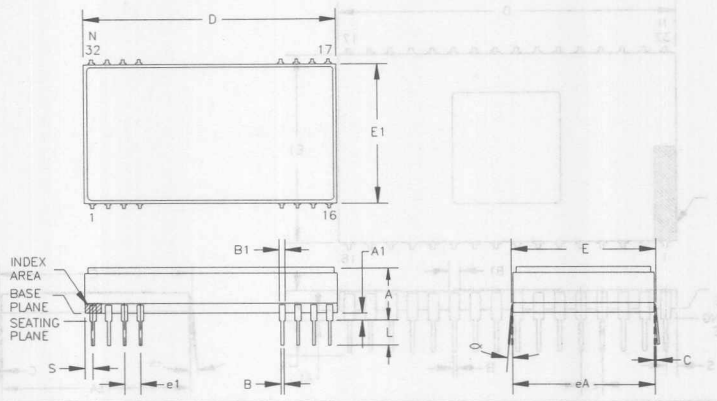
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. α APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| | |
|---|---|
| PACKAGE NUMBER: ZZ208 | REV.: C |
| JEDEC NUMBER: MO-038-AA WITH THE EXCEPTION OF "N" | |

PACKAGE DRAWINGS (Mechanical)

**Package Number 210 - 32-Lead Side Braze DIP, .900 Wide, ISO Package**

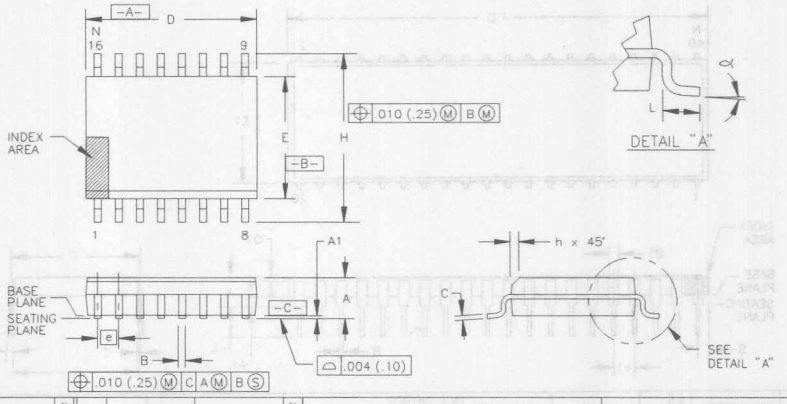



| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .310 | .370 | 7.87 | 9.40 | |
| A1 | .040 | .060 | 1.02 | 1.52 | |
| B | .016 | .020 | 0.41 | 0.51 | 5 |
| B1 | .040 | TYP. | 1.02 | TYP. | 5 |
| C | .009 | .012 | 0.23 | 0.30 | |
| D | 1.590 | 1.630 | 40.39 | 41.40 | |
| E | .895 | .925 | 22.73 | 23.49 | |
| E1 | .875 | .905 | 22.23 | 22.99 | 6 |
| e1 | .100 | TYP. | 2.54 | TYP. | 2 |
| eA | .900 | TYP. | 22.86 | TYP. | 2 |
| L | .125 | .180 | 3.18 | 4.57 | |
| N | 16 | | 16 | | 4 |
| S | .044 | .056 | 1.12 | 1.42 | |
| ∝ | 0° | 15° | 0° | 15° | 3 |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5–1982.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0). TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.

PACKAGE NUMBER: ZZ210 | REV.: G
JEDEC NUMBER: NONE

**Package Number 211 - 16-Lead SOIC, .300 Wide**

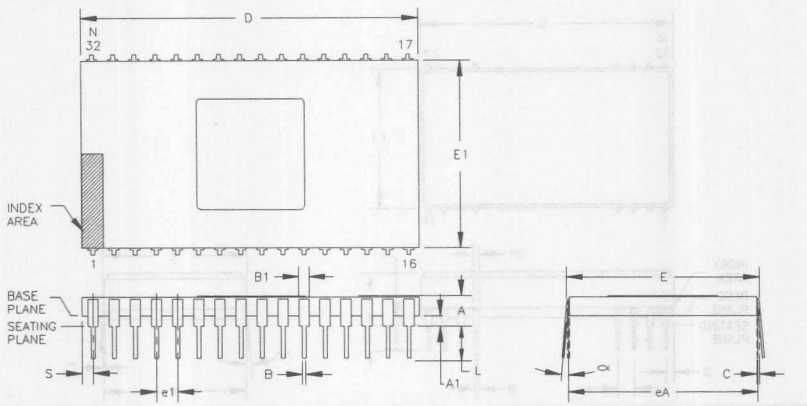



| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .0926 | .1043 | 2.35 | 2.65 | |
| A1 | .004 | .0118 | 0.10 | 0.30 | |
| B | .013 | .020 | 0.33 | 0.51 | 7 |
| C | .0091 | .0125 | 0.23 | 0.32 | |
| D | .3977 | .4133 | 10.10 | 10.50 | 2 |
| E | .2914 | .2992 | 7.40 | 7.60 | 3 |
| e | .050 | BASIC | 1.27 | BASIC | |
| H | .394 | .419 | 10.00 | 10.65 | |
| h | .010 | .029 | 0.25 | 0.75 | 4 |
| L | .016 | .050 | 0.40 | 1.27 | 5 |
| N | 16 | | 16 | | 6 |
| ∝ | 0° | 8° | 0° | 8° | |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ211 | REV.: F
JEDEC NUMBER: MS–013–AA

## Package Number 212 - 32-Lead Side Braze DIP, .900 Wide



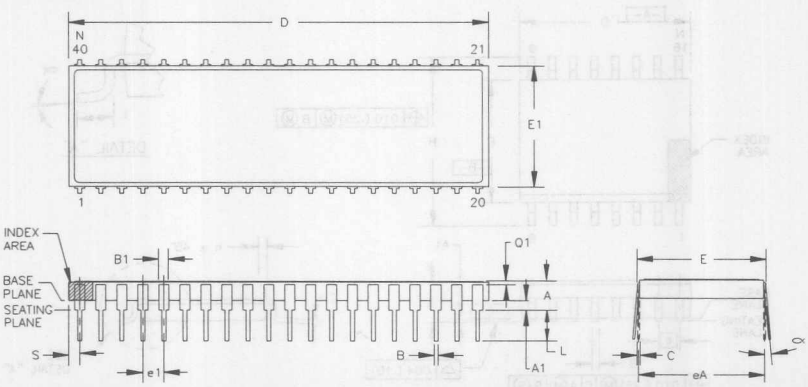

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .124 | .166 | 3.15 | 4.22 | |
| A1 | .040 | .060 | 1.02 | 1.52 | |
| B | .016 | .020 | 0.41 | 0.51 | 5 |
| B1 | .045 | .055 | 1.14 | 1.40 | 5 |
| C | .009 | .012 | 0.23 | 0.30 | |
| D | 1.584 | 1.616 | 40.23 | 41.05 | |
| E | .900 | .920 | 22.86 | 23.37 | |
| E1 | .885 | .905 | 22.48 | 22.99 | 6 |
| e1 | .100 TYP. | | 2.54 TYP. | | 2 |
| eA | .900 TYP. | | 22.86 TYP. | | 2 |
| L | .125 | .180 | 3.18 | 4.57 | |
| N | 32 | | 32 | | 4 |
| S | .030 | .065 | 0.76 | 1.65 | |
| ∝ | 0° | 15° | 0° | 15° | 3 |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5–1982.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ212 | REV.: C
JEDEC NUMBER: NONE

## Package Number 214 - 40-Lead Side Braze DIP, .600 Wide




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .085 | .190 | 2.16 | 4.83 | |
| A1 | .020 | .070 | 0.51 | 1.78 | |
| B | .015 | .023 | 0.38 | 0.58 | 5 |
| B1 | .038 | .060 | 0.97 | 1.52 | 5 |
| C | .008 | .012 | 0.20 | 0.30 | |
| D | 1.980 | 2.030 | 50.29 | 51.56 | |
| E | .595 | .625 | 15.11 | 15.88 | |
| E1 | .580 | .610 | 14.73 | 15.49 | 6 |
| e1 | .100 TYP. | | 2.54 TYP. | | 2 |
| eA | .600 TYP. | | 15.24 TYP. | | 2 |
| L | .125 | .175 | 3.18 | 4.45 | |
| N | 40 | | 40 | | 4 |
| Q1 | .010 | -- | 0.25 | -- | |
| S | .030 | .065 | 0.76 | 1.65 | |
| ∝ | 0° | 15° | 0° | 15° | 3 |

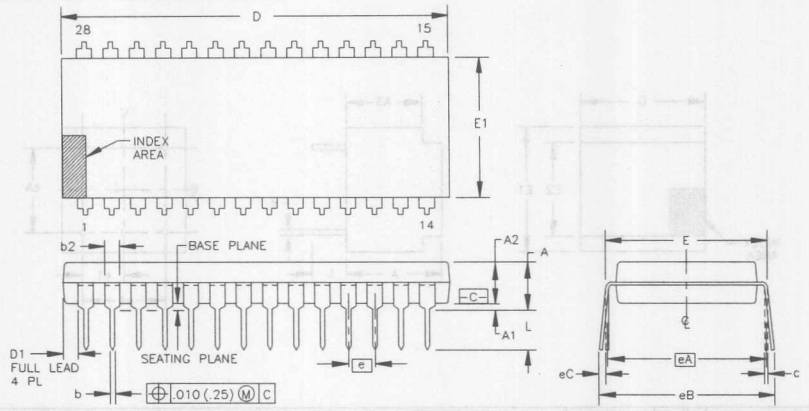
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5–1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ214 | REV.: C
JEDEC NUMBER: MO-038-AC

PACKAGE DRAWINGS (Mechanical)

**Package Number 215 - 28-Pin Plastic, Double-Wide DIP**



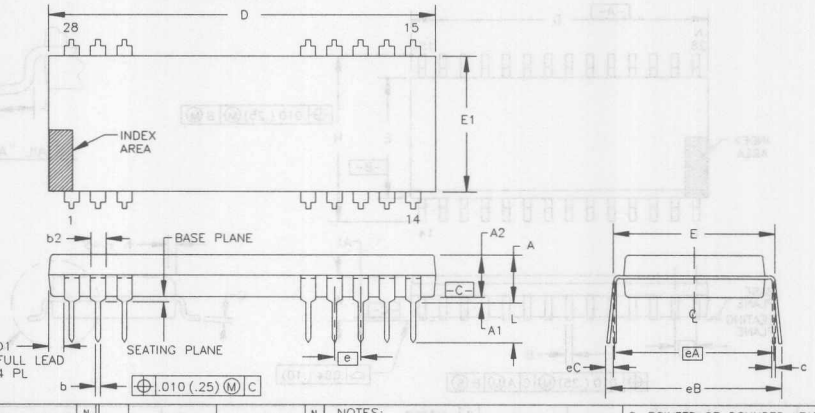

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .250 | -- | 6.35 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .125 | .195 | 3.18 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .030 | .070 | 0.76 | 1.78 | 9 |
| c | .008 | .015 | 0.20 | 0.38 | |
| D | 1.380 | 1.565 | 35.05 | 39.75 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .600 | .625 | 15.24 | 15.88 | 5 |
| E1 | .485 | .580 | 12.32 | 14.73 | 4 |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .600 BASIC | | 15.26 BASIC | | 5 |
| eB | -- | .700 | -- | 17.78 | 6 |
| eC | .000 | .060 | 0.00 | 1.52 | 6 |

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| L | .115 | .200 | 2.92 | 5.08 | 3 |
| N | 28 | | 28 | | 7 |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ215 | REV.: K
JEDEC NUMBER: MS-011-AB

**Package Number 215-1 - 28-Pin Plastic, Double-Wide DIP**



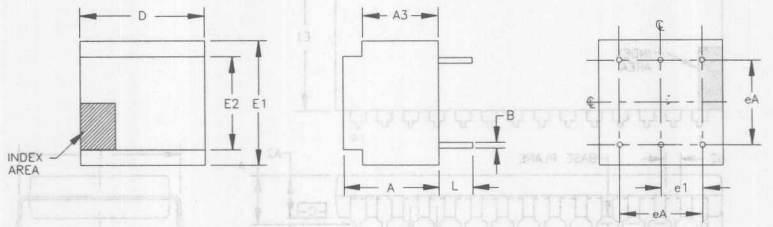

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .250 | -- | 6.35 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .125 | .195 | 3.18 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .030 | .070 | 0.76 | 1.78 | 9 |
| c | .008 | .015 | 0.20 | 0.38 | |
| D | 1.380 | 1.565 | 35.05 | 39.75 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .600 | .625 | 15.24 | 15.88 | 5 |
| E1 | .485 | .580 | 12.32 | 14.73 | 4 |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .600 BASIC | | 15.26 BASIC | | 5 |
| eB | -- | .700 | -- | 17.78 | 6 |
| eC | .000 | .060 | 0.00 | 1.52 | 6 |

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| L | .115 | .200 | 2.92 | 5.08 | 3 |
| N | 16 | | 16 | | 7 |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ215-1 | REV.: C
JEDEC NUMBER: MS-011-AB WITH THE EXCEPTION OF "N"

## Package Number 216 - 6-Pin Distributed Power Transformer

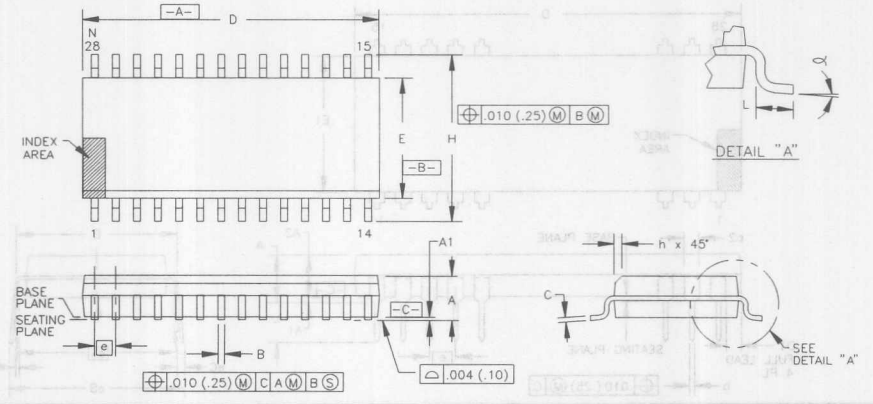



| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .390 | .520 | 9.91 | 13.21 | |
| A3 | .290 | .440 | 7.37 | 11.18 | |
| B | .020 | .030 | 0.50 | 0.76 | |
| D | .540 | .640 | 13.72 | 16.26 | |
| E1 | .540 | .640 | 13.72 | 16.26 | |
| E2 | .390 | .490 | 9.91 | 12.45 | |
| eA | .375 | .425 | 9.53 | 10.80 | |
| e1 | .177 | .217 | 4.50 | 5.12 | |
| L | .110 | .210 | 2.79 | 5.33 | |
| N | 6 | | 6 | | 2 |

NOTES:
1. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
2. N IS THE NUMBER OF TERMINAL POSITIONS.

PACKAGE NUMBER: ZZ216 REV.: F
JEDEC NUMBER: NONE

## Package Number 217 - 28-Lead SOIC



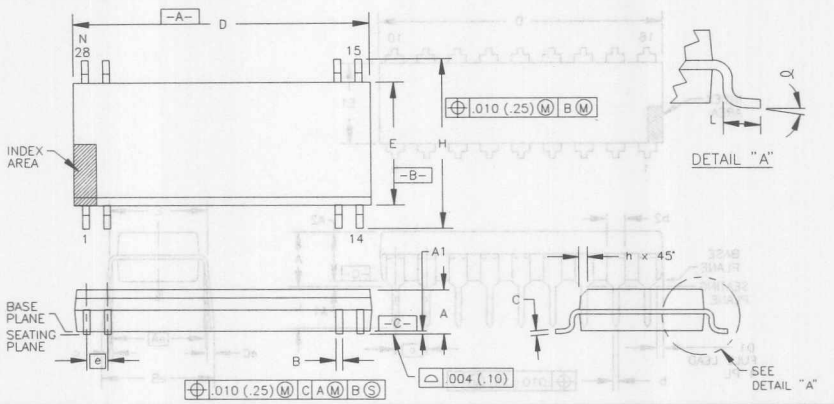

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .0926 | .1043 | 2.35 | 2.65 | |
| A1 | .004 | .0118 | 0.10 | 0.30 | |
| B | .013 | .020 | 0.33 | 0.51 | 7 |
| C | .0091 | .0125 | 0.23 | 0.32 | |
| D | .6969 | .7125 | 17.70 | 18.10 | 2 |
| E | .2914 | .2992 | 7.40 | 7.60 | 3 |
| e | .050 BASIC | | 1.27 BASIC | | |
| H | .398 | .419 | 10.11 | 10.65 | |
| h | .010 | .0295 | 0.25 | 0.75 | 4 |
| L | .020 | .040 | .508 | 1.02 | 5 |
| N | 28 | | 28 | | 6 |
| α | 0° | 8° | 0° | 8° | |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSSHATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ217 REV.: G
JEDEC NUMBER: MS-013-AE WITH THE EXCEPTION OF DIM. H, L

PACKAGE DRAWINGS (Mechanical)

**Package Number 217-1 - 28-Lead SOIC, ISO Package**



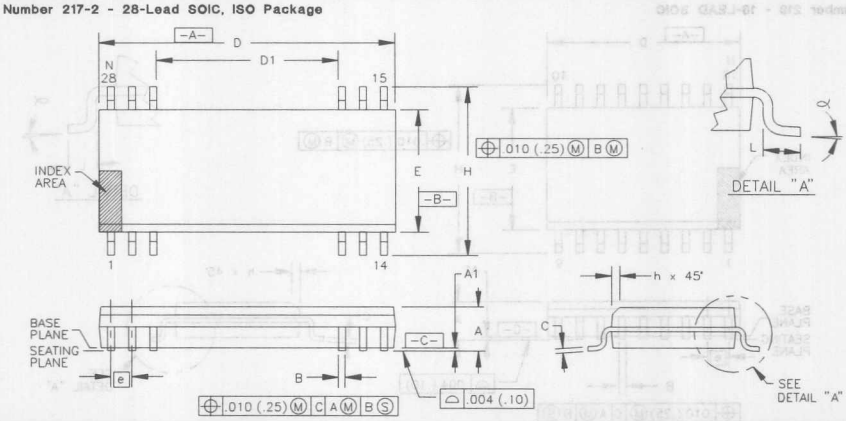

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .0926 | .1043 | 2.35 | 2.65 | |
| A1 | .004 | .0118 | 0.10 | 0.30 | |
| B | .013 | .020 | 0.33 | 0.51 | 7 |
| C | .0091 | .0125 | 0.23 | 0.32 | |
| D | .6969 | .7125 | 17.70 | 18.10 | 2 |
| E | .2914 | .2992 | 7.40 | 7.60 | 3 |
| e | .050 | BASIC | 1.27 | BASIC | |
| H | .394 | .419 | 10.01 | 10.65 | |
| h | .010 | .0295 | 0.25 | 0.75 | 4 |
| L | .016 | .050 | 0.40 | 1.27 | 5 |
| N | 8 | | 8 | | 6 |
| ∝ | 0° | 8° | 0° | 8° | |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

| PACKAGE NUMBER: | ZZ217–1 | REV.: | G |
|---|---|---|---|
| JEDEC NUMBER: | MS–013–AE WITH THE EXCEPTION OF "N". | | |

**Package Number 217-2 - 28-Lead SOIC, ISO Package**



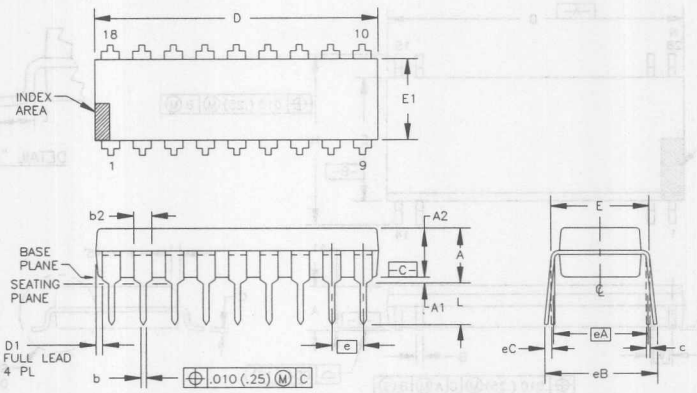

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .0926 | .1043 | 2.35 | 2.65 | |
| A1 | .004 | .0118 | 0.10 | 0.30 | |
| B | .013 | .020 | 0.33 | 0.51 | 7 |
| C | .0091 | .0125 | 0.23 | 0.32 | |
| D | .6969 | .7125 | 17.70 | 18.10 | 2 |
| D1 | .426 | .441 | 10.82 | 11.20 | |
| E | .2914 | .2992 | 7.42 | 7.60 | 3 |
| e | .050 | BASIC | 1.27 | BASIC | |
| H | .394 | .419 | 10.01 | 10.65 | |
| h | .010 | .0295 | 0.25 | 0.75 | 4 |
| L | .016 | .050 | 0.41 | 1.27 | 5 |
| N | 12 | | 12 | | 6 |
| ∝ | 0° | 8° | 0° | 8° | |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

| PACKAGE NUMBER: | ZZ217–2 | REV.: | D |
|---|---|---|---|
| JEDEC NUMBER: | MS–013–AE WITH THE EXCEPTION OF "N" | | |

**Package Number 218 - 18-Pin Plastic, Single-Wide DIP**



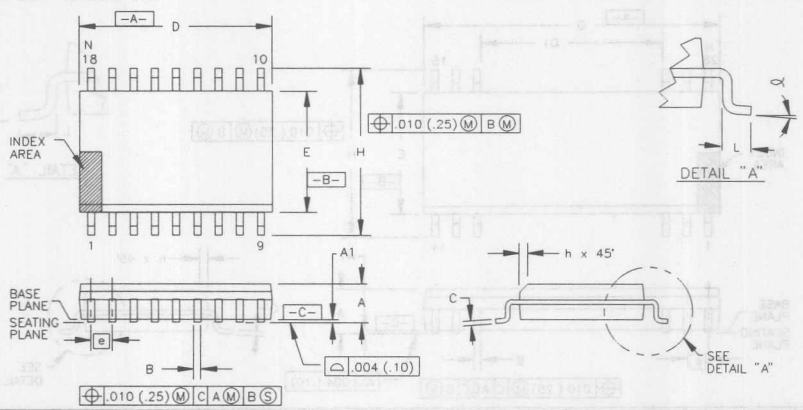

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .210 | -- | 5.33 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .115 | .195 | 2.92 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .045 | .070 | 1.14 | 1.78 | 9 |
| c | .008 | .014 | 0.20 | 0.36 | |
| D | .880 | .920 | 22.35 | 23.37 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .300 | .325 | 7.62 | 8.26 | 5 |
| E1 | .240 | .280 | 6.10 | 7.11 | 4 |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .300 BASIC | | 7.63 BASIC | | 5 |
| eB | -- | .430 | -- | 10.92 | 6 |
| eC | .000 | .060 | 0.00 | 1.52 | 6 |

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| L | .115 | .150 | 2.92 | 3.81 | 3 |
| N | 18 | | 18 | | 7 |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ218 | REV.: D
JEDEC NUMBER: MS-001-AC

**Package Number 219 - 18-LEAD SOIC**

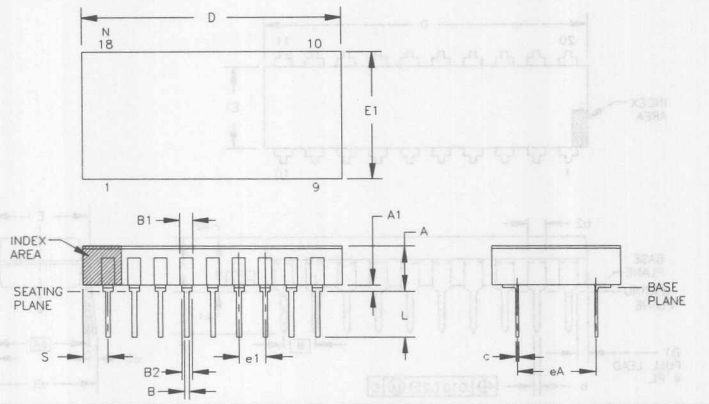



| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .0926 | .1043 | 2.35 | 2.65 | |
| A1 | .004 | .0118 | 0.10 | 0.30 | |
| B | .013 | .020 | 0.33 | 0.51 | 7 |
| C | .0091 | .0125 | 0.23 | 0.32 | |
| D | .4469 | .4625 | 11.35 | 11.75 | 2 |
| E | .2914 | .2992 | 7.40 | 7.60 | 3 |
| e | .050 BASIC | | 1.27 BASIC | | |
| H | .394 | .419 | 10.00 | 10.65 | |
| h | .010 | .029 | 0.25 | 0.75 | 4 |
| L | .016 | .050 | 0.40 | 1.27 | 5 |
| N | 18 | | 18 | | 6 |
| α | 0° | 8° | 0° | 8° | |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH, B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ219 | REV.: E
JEDEC NUMBER: MS-013-AB

**Package Number 220 - 18-Lead Bottom Braze DIP, .300 Wide**

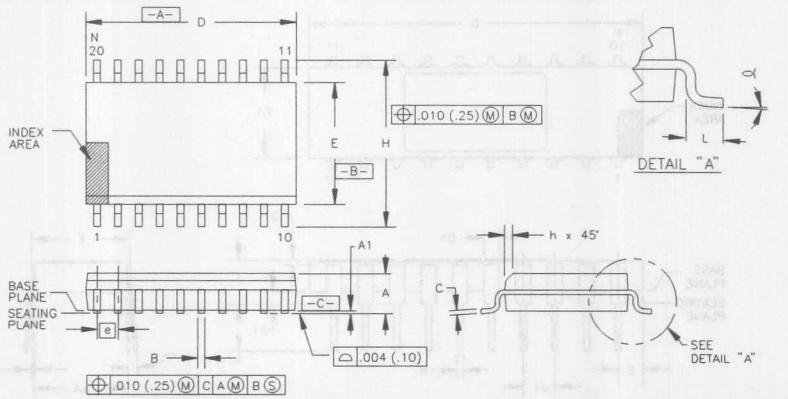



| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .148 | .197 | 3.76 | 5.00 | |
| A1 | .015 | .035 | 0.38 | 0.89 | |
| B | .016 | .020 | 0.41 | 0.51 | |
| B1 | .050 TYP. | | 1.27 TYP. | | |
| B2 | .040 TYP. | | 1.02 TYP. | | |
| c | .009 | .012 | 0.23 | 0.30 | |
| D | .982 | 1.002 | 24.94 | 25.45 | |
| E1 | .480 | .500 | 12.19 | 12.70 | |
| e1 | .095 | .105 | 2.41 | 2.67 | |
| eA | .290 | .310 | 7.37 | 7.87 | |
| L | .150 | .200 | 3.81 | 5.08 | |
| N | 18 | | 18 | | |
| S | .038 | .103 | 0.97 | 2.62 | |

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ220 | REV.: C
JEDEC NUMBER: NONE

**Package Number 221 - 20-LEAD SOIC**

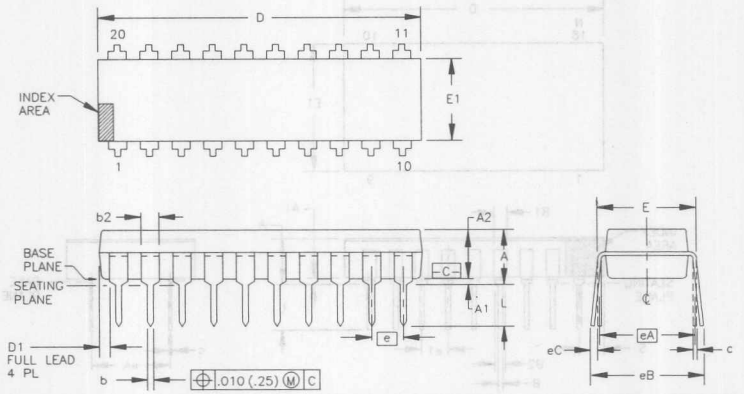



| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .0926 | .1043 | 2.35 | 2.65 | |
| A1 | .004 | .0118 | 0.10 | 0.30 | |
| B | .013 | .020 | 0.33 | 0.51 | 7 |
| C | .0091 | .0125 | 0.23 | 0.32 | |
| D | .4961 | .5118 | 12.60 | 13.00 | 2 |
| E | .2914 | .2992 | 7.40 | 7.60 | 3 |
| e | .050 BASIC | | 1.27 BASIC | | |
| H | .394 | .419 | 10.00 | 10.65 | |
| h | .010 | .029 | 0.25 | 0.75 | 4 |
| L | .016 | .050 | 0.40 | 1.27 | 5 |
| N | 20 | | 20 | | 6 |
| α | 0° | 8° | 0° | 8° | |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ221 | REV.: D
JEDEC NUMBER: MS-013-AC

## Package Number 222 - 20-Pin Plastic, Single-Wide DIP



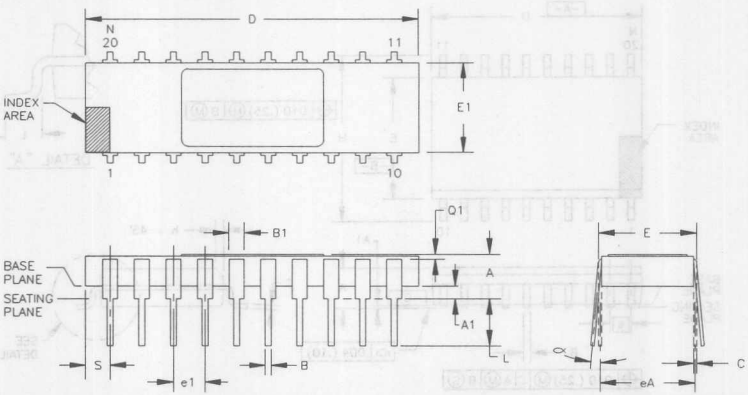

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .210 | -- | 5.33 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .115 | .195 | 2.92 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .045 | .070 | 1.14 | 1.78 | 9 |
| c | .008 | .014 | 0.20 | 0.36 | |
| D | .980 | 1.060 | 24.89 | 26.92 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .300 | .325 | 7.62 | 8.26 | 5 |
| E1 | .240 | .280 | 6.10 | 7.11 | 4 |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .300 BASIC | | 7.63 BASIC | | 5 |
| eB | -- | .430 | -- | 10.92 | 6 |
| eC | .000 | .060 | 0.00 | 1.52 | 6 |

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| L | .115 | .150 | 2.92 | 3.81 | 3 |
| N | 20 | | 20 | | 7 |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

| PACKAGE NUMBER: ZZ222 | REV.: C |
|---|---|
| JEDEC NUMBER: MS-001-AD | |

## Package Number 223 - 20-Lead, Ceramic Side Braze DIP, .300 Wide



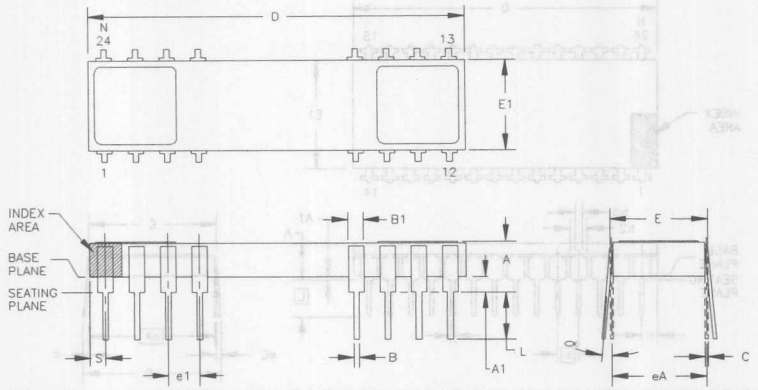

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .105 | .175 | 2.67 | 4.45 | |
| A1 | .025 | .055 | 0.64 | 1.40 | |
| B | .015 | .021 | 0.38 | 0.53 | 5 |
| B1 | .038 | .060 | 0.97 | 1.52 | 5 |
| C | .008 | .012 | 0.20 | 0.30 | |
| D | .990 | 1.120 | 25.15 | 28.45 | |
| E | .290 | .325 | 7.37 | 8.26 | |
| E1 | .280 | .310 | 7.11 | 7.87 | 6 |
| e1 | .100 TYP. | | 2.54 TYP. | | 2 |
| eA | .300 TYP. | | 7.62 TYP. | | 2 |
| L | .125 | .175 | 3.18 | 4.45 | |
| N | 20 | | 20 | | 4 |
| Q1 | .010 | -- | 0.25 | -- | |
| S | .030 | .065 | 0.76 | 1.65 | |

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| α | 0° | 15° | 0° | 15° | 3 |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. α APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: ZZ223 | REV.: D |
|---|---|
| JEDEC NUMBER: MO-36-AE WITH THE EXCEPTION OF DIM. D, N | |

**Package Number 225 - 24-Lead Side Braze DIP, .300 Wide, ISO Package**



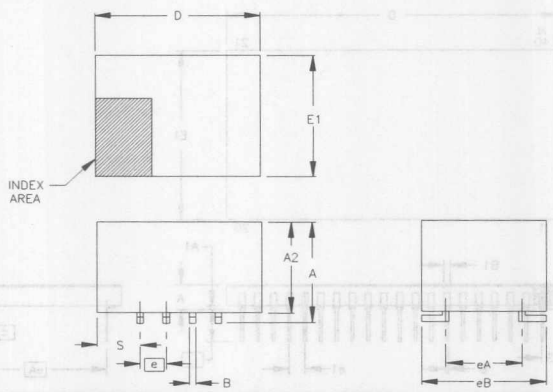

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .140 | .185 | 3.56 | 4.70 | |
| A1 | .040 | .060 | 1.02 | 1.52 | |
| B | .016 | .020 | 0.41 | 0.51 | 5 |
| B1 | .045 | .055 | 1.14 | 1.40 | 5 |
| C | .009 | .012 | 0.23 | 0.30 | |
| D | 1.188 | 1.212 | 30.18 | 30.78 | |
| E | .300 | .320 | 7.62 | 8.13 | |
| E1 | .280 | .300 | 7.11 | 7.62 | 6 |
| e1 | .100 TYP. | | 2.54 TYP. | | 2 |
| eA | .300 TYP. | | 7.62 TYP. | | 2 |
| L | .125 | .180 | 3.18 | 4.57 | |
| N | 16 | | 16 | | 4 |
| S | .035 | .065 | 0.89 | 1.65 | |
| ∝ | 0° | 15° | 0° | 15° | 3 |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: ZZ225 | REV.: E |
|---|---|
| JEDEC NUMBER: NONE | |

**Package Number 226 - Potted Transformer**



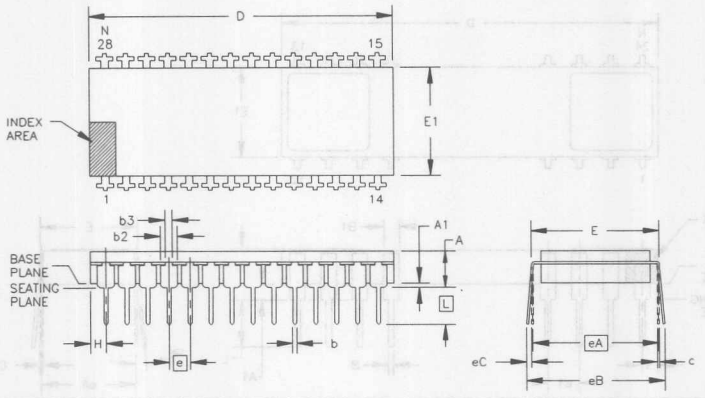

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .370 | .390 | 9.40 | 9.91 | |
| A2 | .350 | .370 | 8.89 | 9.40 | |
| B | .025 SQ. | | .635 SQ. | | |
| D | .620 | .640 | 15.78 | 16.26 | |
| E1 | .465 | .485 | 11.81 | 12.32 | |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .280 | .300 | 7.11 | 7.62 | |
| eB | .465 | .485 | 11.81 | 12.32 | |
| N | 8 | | 8 | | 2 |
| S | .165 | .185 | 4.19 | 4.70 | |

NOTES:

1. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
2. N IS THE NUMBER OF TERMINAL POSITIONS.

| PACKAGE NUMBER: ZZ226 | REV.: B |
|---|---|
| JEDEC NUMBER: NONE | |

**Package Number 228 - 28-Lead CERDIP, .600 Wide**




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .155 | .193 | 3.94 | 4.90 | |
| A1 | .018 | .022 | 0.46 | 0.56 | |
| b | .018 | TYP. | 0.46 | TYP. | 8 |
| b2 | .080 | TYP. | 2.03 | TYP. | |
| b3 | .035 | TYP. | 0.89 | TYP. | |
| c | .0098 | .0102 | 0.249 | 0.259 | 8 |
| D | 1.440 | 1.460 | 36.57 | 37.08 | 3 |
| E | .608 | .614 | 15.44 | 15.60 | |
| E1 | .514 | .526 | 13.06 | 13.36 | 3 |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .600 | BASIC | 15.24 | BASIC | |
| eB | .645 | .675 | 16.38 | 17.15 | 4 |
| eC | .000 | -- | 0.00 | -- | 4 |
| H | .070 | .080 | 1.78 | 2.03 | |

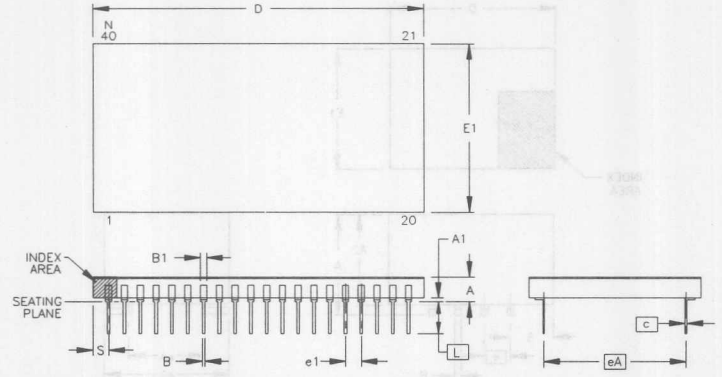
| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| L | .175 | BASIC | 4.45 | BASIC | |
| N | 28 | | 28 | | 5 |

NOTES:

1. CONTROLLING DIMENSIONS: INCH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D AND E1 DIMENSIONS INCLUDE ALLOWANCE FOR GLASS OVERRUN AND MENISCUS, AND LID TO BASE MISMATCH.
4. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
5. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
6. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
7. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
8. b AND c DIMENSIONS INCLUDE BOTH THE BASE MATERIAL AND THE COATING OR PLATING ON THE LEADS.
9. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: | ZZ228 | REV.: | B |
|---|---|---|---|
| JEDEC NUMBER: | NONE | | |

**Package Number 230 - 40-Lead Bottom Braze DIP, .900 Wide**




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .145 | .175 | 3.68 | 4.45 | |
| A1 | .015 | .035 | 0.38 | 0.89 | |
| B | .018 | TYP. | 0.46 | TYP. | |
| B1 | .040 | TYP. | 1.02 | TYP. | |
| c | .020 | BASIC | 0.51 | BASIC | |
| D | 2.075 | 2.115 | 52.71 | 53.72 | |
| E1 | 1.080 | 1.100 | 27.43 | 27.94 | |
| e1 | .100 | TYP. | 2.54 | TYP. | |
| eA | .900 | BASIC | 22.86 | BASIC | |
| L | .205 | BASIC | 5.21 | BASIC | |
| N | 40 | | 40 | | 4 |
| S | .093 | .103 | 2.36 | 2.62 | |

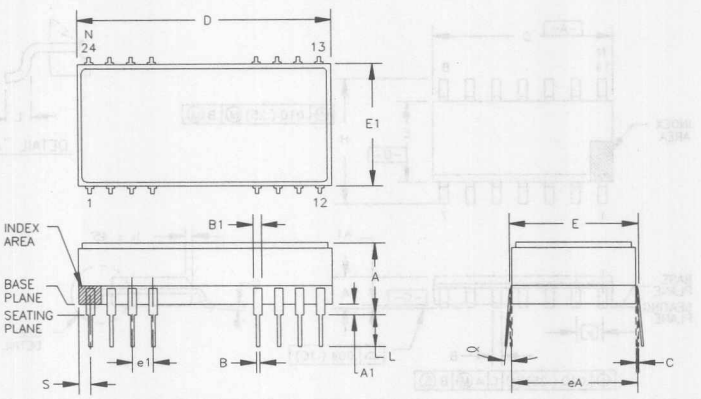
NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
4. N IS THE NUMBER OF TERMINAL POSITIONS.

| PACKAGE NUMBER: | ZZ230 | REV.: | B |
|---|---|---|---|
| JEDEC NUMBER: | NONE | | |

PACKAGE DRAWINGS (mechanical)

**Package Number 231 - 24-Lead Side Braze DIP, .600 Wide, ISO Package**



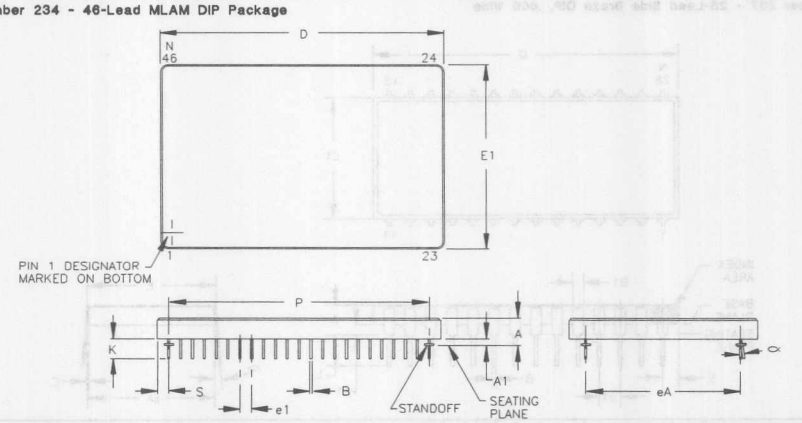

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .310 | .375 | 7.87 | 9.52 | |
| A1 | .040 | .060 | 1.02 | 1.52 | |
| B | .016 | .020 | 0.41 | 0.51 | 5 |
| B1 | .040 | TYP. | 1.02 | TYP. | 5 |
| C | .009 | .012 | 0.23 | 0.30 | |
| D | 1.180 | 1.265 | 29.97 | 32.13 | |
| E | .600 | .620 | 15.24 | 15.75 | |
| E1 | .570 | .610 | 14.48 | 15.49 | 6 |
| e1 | .100 | TYP. | 2.54 | TYP. | 2 |
| eA | .580 | .620 | 14.73 | 15.75 | 2 |
| L | .125 | .180 | 3.18 | 4.57 | |
| N | 16 | | 16 | | 4 |
| S | .044 | .056 | 1.12 | 1.42 | |
| ∝ | 0° | 15° | 0° | 15° | 3 |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: ZZ231 | REV.: E |
|---|---|
| JEDEC NUMBER: NONE | |

**Package Number 234 - 46-Lead MLAM DIP Package**



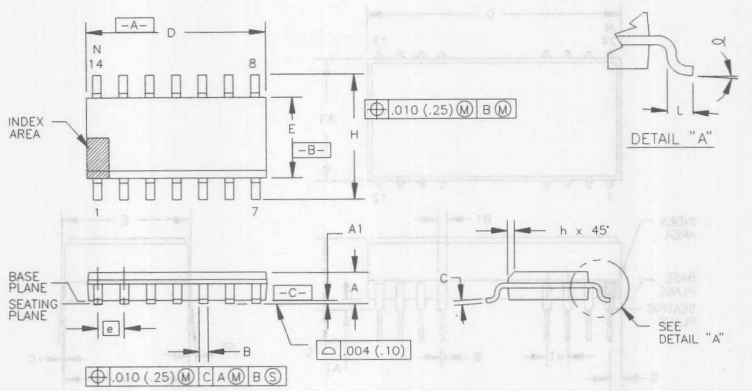

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .205 | .251 | 5.21 | 6.38 | |
| A1 | .045 | .055 | 1.14 | 1.40 | |
| B | .015 | .021 | 0.38 | 0.53 | |
| D | 2.370 | 2.420 | 60.20 | 61.47 | |
| E1 | 1.560 | 1.610 | 39.62 | 40.89 | |
| e1 | .095 | .105 | 2.41 | 2.67 | |
| eA | 1.290 | 1.310 | 32.77 | 33.27 | |
| K | .155 | .185 | 3.94 | 4.70 | |
| N | 46 | | 46 | | 3 |
| P | 2.190 | 2.210 | 55.63 | 56.13 | |
| S | .085 | .105 | 2.16 | 2.67 | |
| ∝ | -- | 10° | -- | 10° | |

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R AT MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. N IS THE NUMBER OF TERMINAL POSITIONS.

| PACKAGE NUMBER: ZZ234 | REV.: C |
|---|---|
| JEDEC NUMBER: NONE | |

## Package Number 235 - 14-Lead SOIC



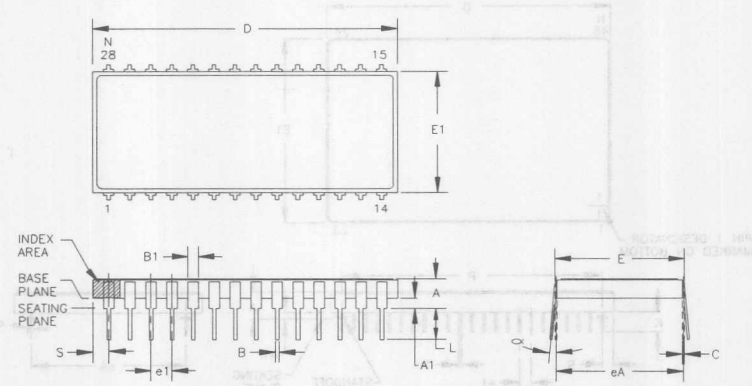

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .0532 | .0688 | 1.35 | 1.75 | |
| A1 | .004 | .0098 | 0.10 | 0.25 | |
| B | .013 | .020 | 0.33 | 0.51 | 7 |
| C | .0075 | .0098 | 0.19 | 0.25 | |
| D | .3367 | .3444 | 8.55 | 8.75 | 2 |
| E | .1497 | .1574 | 3.80 | 4.00 | 3 |
| e | .050 BASIC | | 1.27 BASIC | | |
| H | .2284 | .244 | 5.80 | 6.20 | |
| h | .0099 | .0196 | 0.25 | 0.50 | 4 |
| L | .016 | .050 | 0.40 | 1.27 | 5 |
| N | 14 | | 14 | | 6 |
| α | 0° | 8° | 0° | 8° | |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

| PACKAGE NUMBER: | ZZ235 | REV.: | E |
|---|---|---|---|
| JEDEC NUMBER: | MS–012–AB | | |

## Package Number 237 - 28-Lead Side Braze DIP, .600 Wide




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .085 | .190 | 2.16 | 4.83 | |
| A1 | .040 | .060 | 1.02 | 1.52 | |
| B | .016 | .020 | 0.41 | 0.51 | 5 |
| B1 | .045 | .055 | 1.14 | 1.40 | 5 |
| C | .009 | .012 | 0.23 | 0.30 | |
| D | 1.425 | 1.475 | 36.20 | 37.47 | |
| E | .600 | .620 | 15.24 | 15.75 | |
| E1 | .585 | .605 | 14.86 | 15.37 | 6 |
| e1 | .100 TYP. | | 2.54 TYP. | | 2 |
| eA | .590 | .610 | 14.99 | 15.49 | 2 |
| L | .125 | .180 | 3.18 | 4.57 | |
| N | 28 | | 28 | | 4 |
| S | .060 | .090 | 1.52 | 2.29 | |
| α | 0° | 15° | 0° | 15° | 3 |

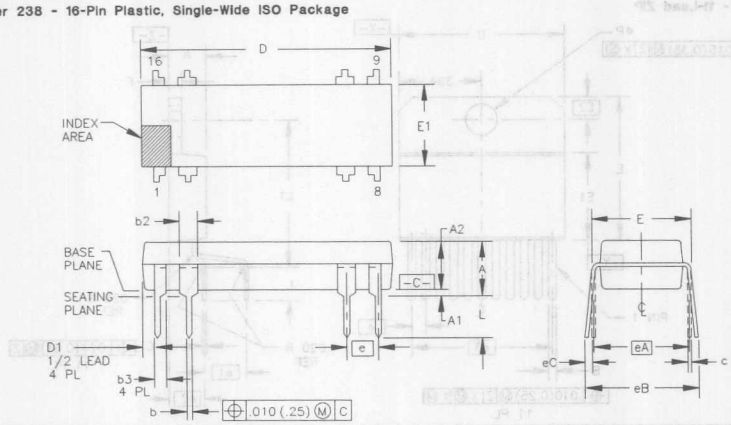
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5–1982.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. α APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.

| PACKAGE NUMBER: | ZZ237 | REV.: | C |
|---|---|---|---|
| JEDEC NUMBER: | NONE | | |

PACKAGE DRAWINGS (mechanical)

**Package Number 238 - 16-Pin Plastic, Single-Wide ISO Package**




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .210 | -- | 5.33 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .115 | .195 | 2.92 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .045 | .070 | 1.14 | 1.78 | 9 |
| b3 | .030 | .045 | 0.76 | 1.14 | 9 |
| c | .008 | .014 | 0.20 | 0.36 | |
| D | .735 | .775 | 18.67 | 21.34 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .300 | .325 | 7.62 | 8.26 | 5 |
| E1 | .240 | .280 | 6.10 | 7.11 | 4 |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .300 BASIC | | 7.63 BASIC | | 5 |
| eB | -- | .430 | -- | 10.92 | 6 |

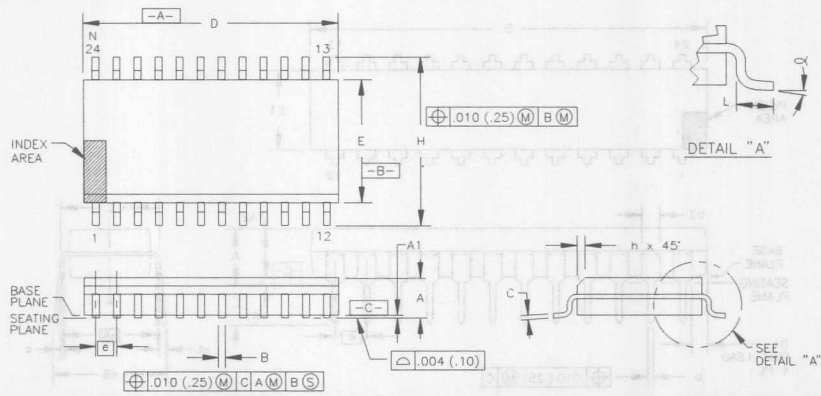
| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| eC | .000 | .060 | 0.00 | 1.52 | 6 |
| L | .115 | .150 | 2.92 | 3.81 | 3 |
| N | 8 | | 8 | | 7 |

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ238 | REV.: D
JEDEC NUMBER: MS-001-BB WITH THE EXCEPTION OF "N".

**Package Number 239 - 24-Lead SOIC**



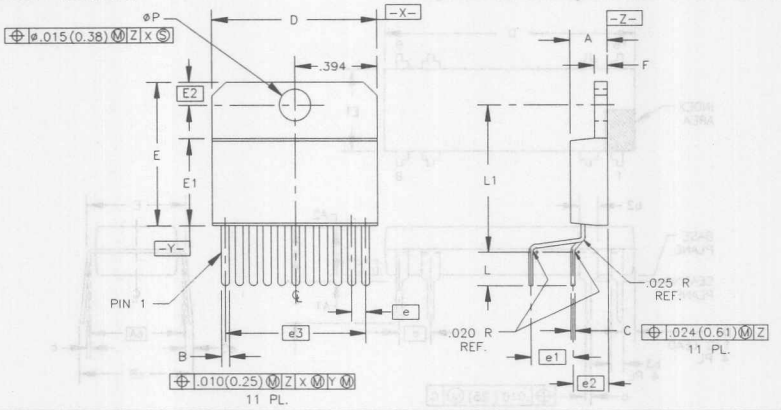

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .0926 | .1043 | 2.35 | 2.65 | |
| A1 | .004 | .0118 | 0.10 | 0.30 | |
| B | .013 | .020 | 0.33 | 0.51 | 7 |
| C | .0091 | .0125 | 0.23 | 0.32 | |
| D | .5985 | .6141 | 15.20 | 15.60 | 2 |
| E | .2914 | .2992 | 7.40 | 7.60 | 3 |
| e | .050 BASIC | | 1.27 BASIC | | |
| H | .394 | .419 | 10.00 | 10.65 | |
| h | .010 | .0295 | 0.25 | 0.75 | 4 |
| L | .016 | .050 | 0.40 | 1.27 | 5 |
| N | 24 | | 24 | | 6 |
| ∝ | 0° | 8° | 0° | 8° | |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM THE SEATING PLANE.

PACKAGE NUMBER: ZZ239 | REV.: E
JEDEC NUMBER: MS-013-AD

**Package Number 242 - 11-Lead ZIP**




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .172 | .182 | 4.37 | 4.62 | |
| B | .035 | .041 | 0.89 | 1.04 | |
| C | .014 | .024 | 0.36 | 0.61 | |
| D | .778 | .798 | 19.76 | 20.27 | |
| E | .671 | .694 | 17.04 | 17.63 | |
| E1 | .405 | .426 | 10.29 | 10.82 | |
| E2 | .110 | BASIC | .279 | BASIC | |
| e | .067 | BASIC | 1.70 | BASIC | |
| e1 | .200 | BASIC | 5.08 | BASIC | |
| e2 | .169 | BASIC | 4.29 | BASIC | |
| e3 | .670 | BASIC | 17.02 | BASIC | |
| F | .057 | .063 | 1.45 | 1.60 | |
| L | .150 | .176 | 3.81 | 4.47 | |
| L1 | .690 | .710 | 17.53 | 18.03 | |

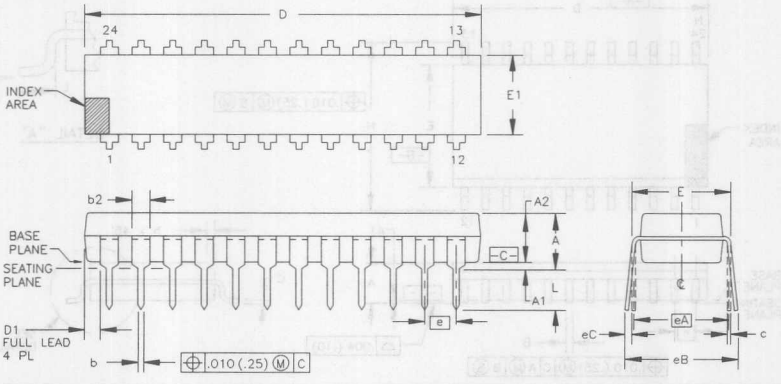
| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| N | 11 | | 11 | | 3 |
| P | .148 | .152 | 3.76 | 3.86 | |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. N IS THE NUMBER OF TERMINALS.

PACKAGE NUMBER: ZZ242 | REV.: D
JEDEC NUMBER: MO-48-AA

**Package Number 243 - 24-Pin Plastic, Single-Wide DIP**




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .210 | -- | 5.33 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .115 | .195 | 2.92 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .045 | .070 | 1.14 | 1.78 | 9 |
| c | .008 | .014 | 0.20 | 0.36 | |
| D | 1.230 | 1.280 | 31.24 | 32.51 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .300 | .325 | 7.62 | 8.26 | 5 |
| E1 | .240 | .280 | 6.10 | 7.11 | 4 |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .300 | BASIC | 7.62 | BASIC | 5 |
| eB | -- | .430 | -- | 10.92 | 6 |
| eC | .000 | .060 | 0.00 | 1.52 | 6 |

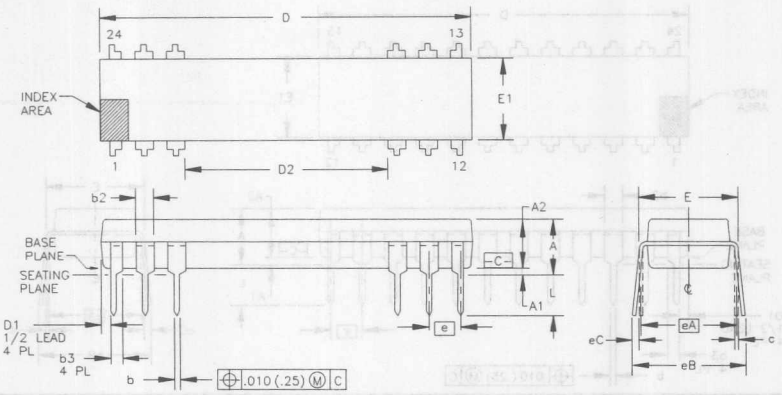
| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| L | .115 | .150 | 2.92 | 3.81 | 3 |
| N | 24 | | 24 | | 7 |

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ243 | REV.: D
JEDEC NUMBER: MS-001-AF

**Package Number 243-1 - 24-Pin Plastic, Single-Wide DIP, ISO Package**




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .210 | -- | 5.33 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .115 | .195 | 2.92 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .045 | .070 | 1.14 | 1.78 | 9 |
| b3 | .030 | .045 | 0.76 | 1.14 | 9 |
| c | .008 | .014 | 0.20 | 0.36 | |
| D | 1.160 | 1.195 | 29.46 | 30.35 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| D2 | .630 | .655 | 16.00 | 16.64 | |
| E | .300 | .325 | 7.62 | 8.26 | 5 |
| E1 | .240 | .280 | 6.10 | 7.11 | 4 |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .300 BASIC | | 7.62 BASIC | | 5 |

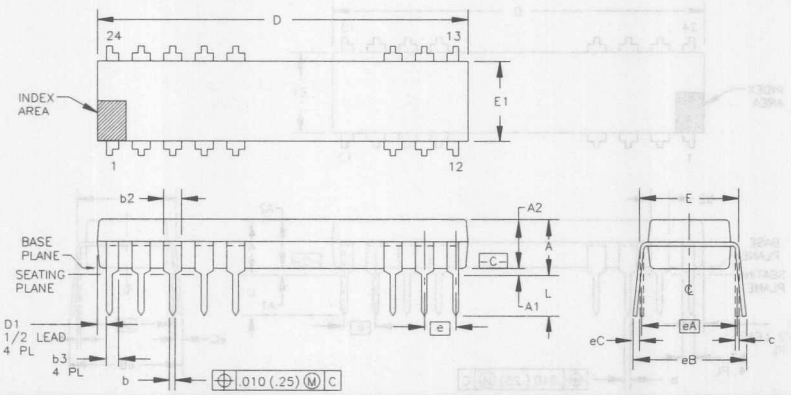
| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| eB | -- | .430 | -- | 10.92 | 6 |
| eC | .000 | .060 | 0.00 | 1.52 | 6 |
| L | .115 | .150 | 2.92 | 3.81 | 3 |
| N | 12 | | 12 | | 7 |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ243-1 | REV.: J

JEDEC NUMBER: MS-001-BE WITH THE EXCEPTION OF "N"

**Package Number 243-2 - 24-Pin Plastic, Single-Wide DIP**




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .210 | -- | 5.33 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .115 | .195 | 2.92 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .045 | .070 | 1.14 | 1.78 | 9 |
| b3 | .030 | .045 | 0.76 | 1.14 | 9 |
| c | .008 | .014 | 0.20 | 0.36 | |
| D | 1.160 | 1.195 | 29.46 | 30.35 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .300 | .325 | 7.62 | 8.26 | 5 |
| E1 | .240 | .280 | 6.10 | 7.11 | 4 |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .300 BASIC | | 7.62 BASIC | | 5 |
| eB | -- | .430 | -- | 10.92 | 6 |

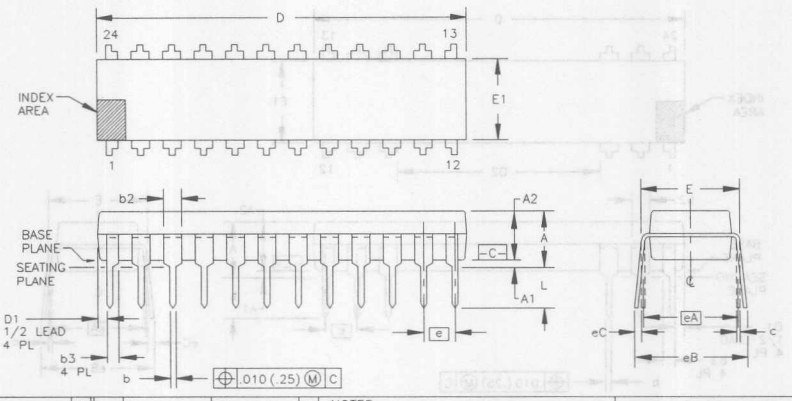
| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| eC | .000 | .060 | 0.00 | 1.52 | 6 |
| L | .115 | .150 | 2.92 | 3.81 | 3 |
| N | 16 | | 16 | | 7 |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ243-2 | REV.: C

JEDEC NUMBER: MS-001-BE WITH THE EXCEPTION OF "N"

**Package Number 243-3 - 24-Pin Plastic, Single-Wide DIP**



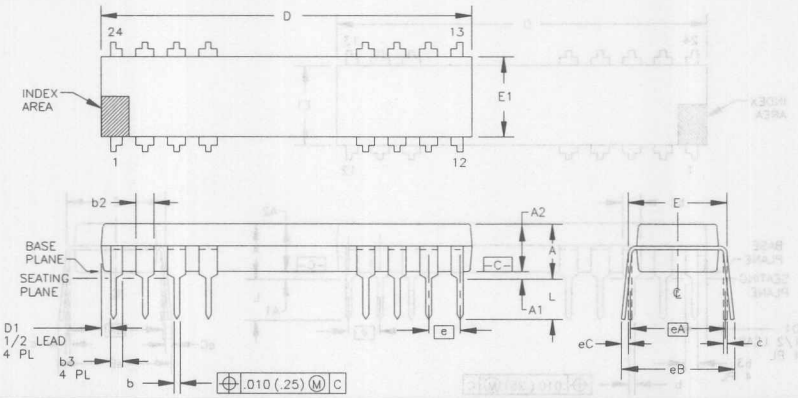

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .210 | -- | 5.33 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .115 | .195 | 2.92 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .045 | .070 | 1.14 | 1.78 | 9 |
| b3 | .030 | .045 | 0.76 | 1.14 | 9 |
| c | .008 | .014 | 0.20 | 0.36 | |
| D | 1.160 | 1.195 | 29.46 | 30.35 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .300 | .325 | 7.62 | 8.26 | 5 |
| E1 | .240 | .280 | 6.10 | 7.11 | 4 |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .300 | BASIC | 7.62 | BASIC | 5 |
| eB | -- | .430 | -- | 10.92 | 6 |

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| eC | .000 | .060 | 0.00 | 1.52 | 6 |
| L | .115 | .150 | 2.92 | 3.81 | 3 |
| N | 24 | | 24 | | 7 |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

| PACKAGE NUMBER: | ZZ243-3 | REV.: | A |
|---|---|---|---|
| JEDEC NUMBER: | MS-001-BE | | |

**Package Number 243-4 - 24-Pin Plastic, Single-Wide DIP, ISO Package**




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .210 | -- | 5.33 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .115 | .195 | 2.92 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .045 | .070 | 1.14 | 1.78 | 9 |
| b3 | .030 | .045 | 0.76 | 1.14 | 9 |
| c | .008 | .014 | 0.20 | 0.36 | |
| D | 1.160 | 1.195 | 29.46 | 30.35 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .300 | .325 | 7.62 | 8.26 | 5 |
| E1 | .240 | .280 | 6.10 | 7.11 | 4 |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .300 | BASIC | 7.62 | BASIC | 5 |
| eB | -- | .430 | -- | 10.92 | 6 |

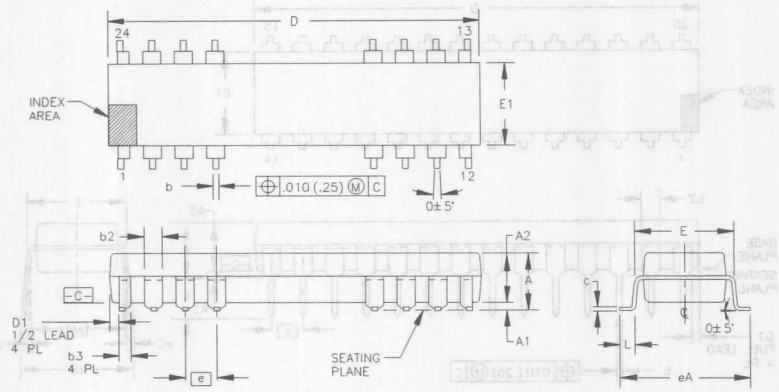
| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| eC | .000 | .060 | 0.00 | 1.52 | 6 |
| L | .115 | .150 | 2.92 | 3.81 | 3 |
| N | 16 | | 16 | | 7 |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

| PACKAGE NUMBER: | ZZ243-4 | REV.: | A |
|---|---|---|---|
| JEDEC NUMBER: | MS-001-BE WITH THE EXCEPTION OF "N" | | |

PACKAGE DRAWINGS (Mechanical)

**Package Number 243-5 - 24-Pin Plastic, Single-Wide DIP, ISO Package With Gull Wing Leads.**



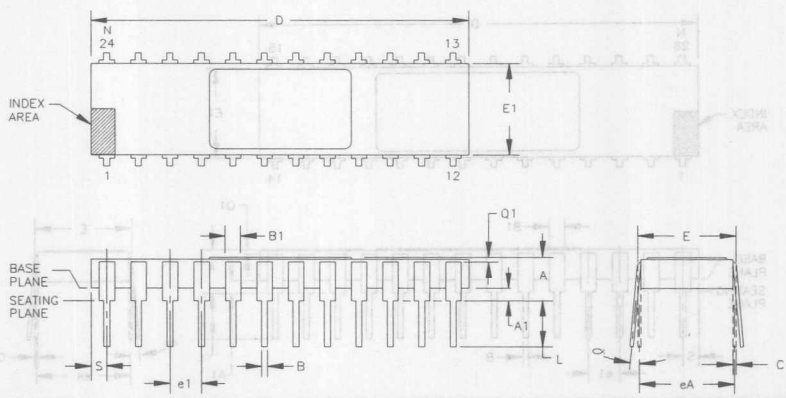

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .210 | -- | 5.33 | |
| A1 | .015 | -- | 0.38 | -- | |
| A2 | .115 | .195 | 2.92 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .045 | .070 | 1.14 | 1.78 | 5 |
| b3 | .030 | .045 | 0.76 | 1.14 | |
| c | .008 | .014 | 0.20 | 0.36 | |
| D | 1.160 | 1.195 | 29.46 | 30.35 | 3 |
| D1 | .005 | -- | 0.13 | -- | 3 |
| E | .300 | .325 | 7.62 | 8.26 | |
| E1 | .240 | .280 | 6.10 | 7.11 | 3 |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .390 | .430 | 9.91 | 10.92 | |
| L | .045 | .057 | 1.15 | 1.45 | |

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| N | 16 | | 16 | | 4 |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
6. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
7. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
8. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

| PACKAGE NUMBER: ZZ243-5 | REV.: A |
|---|---|
| JEDEC NUMBER: NONE | |

**Package Number 245 - 24-Lead, Ceramic Side Braze DIP, .300 Wide**



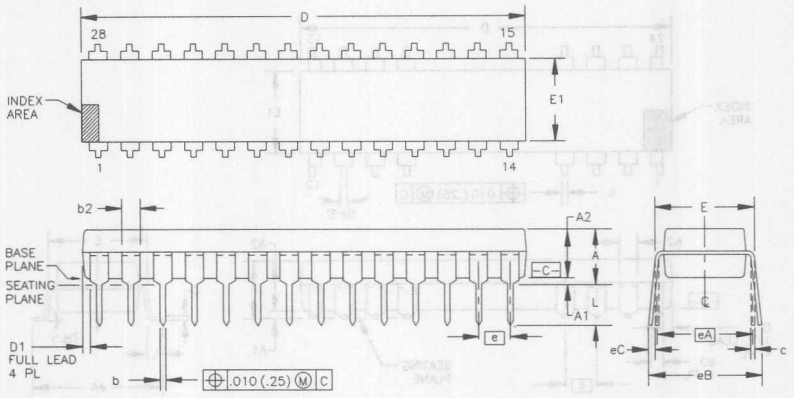

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .105 | .175 | 2.67 | 4.45 | |
| A1 | .025 | .055 | 0.64 | 1.40 | |
| B | .015 | .021 | 0.38 | 0.53 | 5 |
| B1 | .038 | .060 | 0.97 | 1.52 | 5 |
| C | .008 | .012 | 0.20 | 0.30 | |
| D | 1.188 | 1.212 | 30.18 | 30.78 | |
| E | .290 | .325 | 7.37 | 8.26 | |
| E1 | .280 | .310 | 7.11 | 7.87 | 6 |
| e1 | .100 TYP. | | 2.54 TYP. | | 2 |
| eA | .300 TYP. | | 7.62 TYP. | | 2 |
| L | .125 | .175 | 3.18 | 4.45 | |
| N | 24 | | 24 | | 4 |
| Q1 | .010 | -- | 0.25 | -- | |
| S | .030 | .065 | 0.76 | 1.65 | |

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| ∝ | 0° | 15° | 0° | 15° | 3 |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: ZZ245 | REV.: C |
|---|---|
| JEDEC NUMBER: MO-36-AE WITH THE EXCEPTION OF DIM. D, N | |

## Package Number 246 - 28-Pin Plastic, Single-Wide DIP




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .210 | -- | 5.33 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .115 | .195 | 2.92 | 4.95 | |
| b | .014 | .022 | 0.36 | 0.56 | |
| b2 | .045 | .070 | 1.14 | 1.78 | 9 |
| c | .008 | .014 | 0.20 | 0.36 | |
| D | 1.385 | 1.425 | 35.18 | 36.20 | 4 |
| D1 | .005 | -- | 0.13 | -- | 4 |
| E | .300 | .325 | 7.62 | 8.26 | 5 |
| E1 | .240 | .280 | 6.10 | 7.11 | 4 |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .300 BASIC | | 7.62 BASIC | | 5 |
| eB | -- | .430 | -- | 10.92 | 6 |
| eC | .000 | .060 | 0.00 | 1.52 | 6 |

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| L | .115 | .150 | 2.92 | 3.81 | 3 |
| N | 28 | | 28 | | 7 |

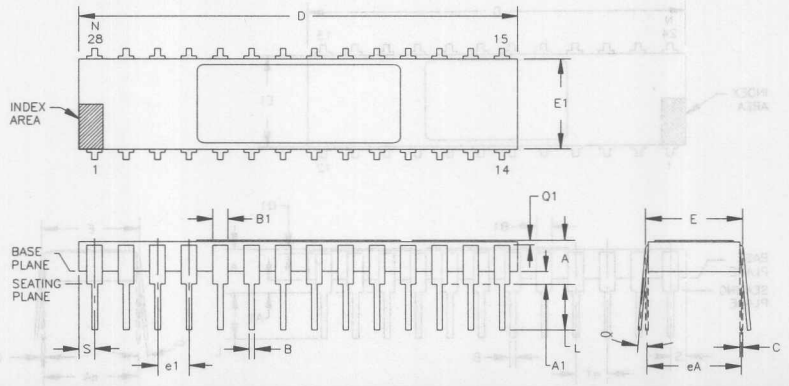
NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ246 | REV.: D

JEDEC NUMBER: MS-001-AG WITH THE EXCEPTION OF "N"

## Package Number 247 - 28-Lead, Ceramic Side Braze DIP, .300 Wide




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .105 | .175 | 2.67 | 4.45 | |
| A1 | .025 | .055 | 0.64 | 1.40 | |
| B | .015 | .021 | 0.38 | 0.53 | 5 |
| B1 | .038 | .060 | 0.97 | 1.52 | 5 |
| C | .008 | .012 | 0.20 | 0.30 | |
| D | 1.388 | 1.412 | 35.25 | 35.86 | |
| E | .290 | .325 | 7.37 | 8.26 | |
| E1 | .280 | .310 | 7.11 | 7.87 | 6 |
| e1 | .100 TYP. | | 2.54 TYP. | | 2 |
| eA | .300 TYP. | | 7.62 TYP. | | 2 |
| L | .125 | .175 | 3.18 | 4.45 | |
| N | 28 | | 28 | | 4 |
| Q1 | .010 | -- | 0.25 | -- | |
| S | .030 | .065 | 0.76 | 1.65 | |

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| α | 0° | 15° | 0° | 15° | 3 |

NOTES:

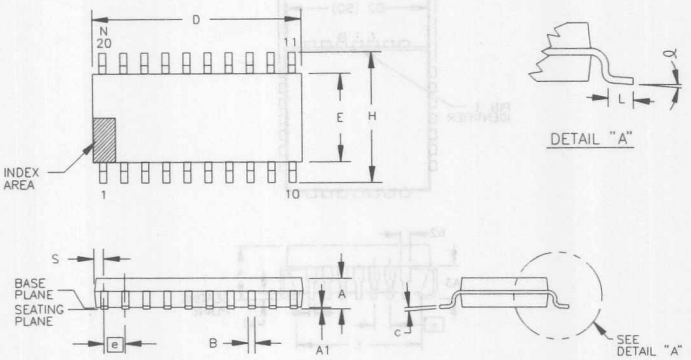
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. α APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0). TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ247 | REV.: D

JEDEC NUMBER: MO-036-AE WITH THE EXCEPTION OF DIM. D, N

PACKAGE DRAWINGS (Mechanical)

**Package Number 248 - 20-Lead SOIC, .300 Wide**



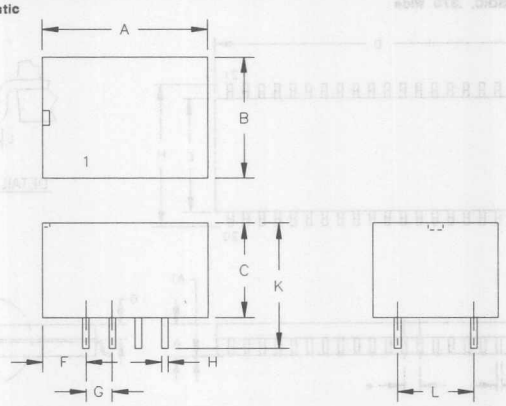

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .071 | .077 | 1.80 | 1.96 | |
| A1 | .002 | .006 | 0.05 | 0.15 | |
| B | .013 | .017 | 0.33 | 0.43 | |
| c | .0076 | .0082 | 0.19 | 0.21 | |
| D | .494 | .498 | 12.55 | 12.65 | |
| E | .206 | .210 | 5.23 | 5.33 | |
| e | .050 BASIC | | 1.27 BASIC | | |
| H | .303 | .311 | 7.70 | 7.90 | |
| L | .016 | .031 | 0.40 | 0.80 | |
| N | 20 | | 20 | | 4 |
| S | .021 | .025 | 0.53 | 0.64 | |
| α | 3° | 5° | 3° | 5° | |

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25 mm) @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
4. N IS THE NUMBER OF TERMINAL POSITIONS.

| PACKAGE NUMBER: | ZZ248 | REV.: | B |
|---|---|---|---|
| JEDEC NUMBER: | NONE | | |

**Package Number 250 - 8-Pin Plastic**

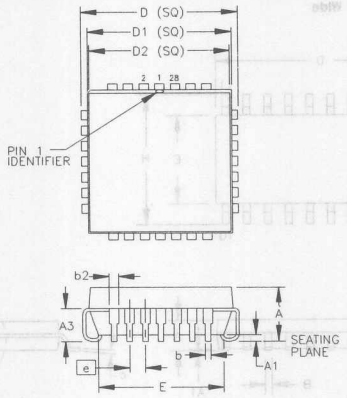



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .620 | .640 | 15.78 | 16.26 | |
| B | .465 | .485 | 11.81 | 12.32 | |
| C | .350 | .370 | 8.89 | 9.40 | |
| F | .165 | .185 | 4.19 | 4.70 | |
| G | .100 BASIC | | 2.54 BASIC | | |
| H | .025 SQ. | | .635 SQ. | | |
| K | .465 | .490 | 11.81 | 12.45 | |
| L | .280 | .300 | 7.11 | 7.62 | |

NOTES:

| PACKAGE NUMBER: | ZZ250 | REV.: | B |
|---|---|---|---|
| JEDEC NUMBER: | NONE | | |

## Package Number 251 - 28-Pin PLCC



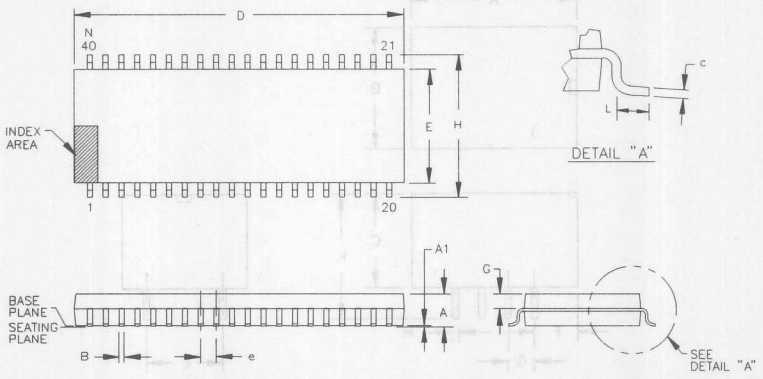

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .165 | .180 | 4.19 | 4.57 | |
| A1 | .015 | .025 | 0.38 | 0.64 | |
| A3 | .100 | .110 | 2.54 | 2.79 | |
| b | .013 | .023 | 0.33 | 0.58 | |
| b2 | .026 | .032 | 0.66 | 0.81 | |
| D | .485 | .495 | 12.32 | 12.57 | |
| D1 | .450 | .460 | 11.43 | 11.68 | |
| D2 | .450 | .460 | 11.43 | 11.68 | |
| E | .390 | .430 | 9.91 | 10.92 | |
| e | .050 BASIC | | 1.27 BASIC | | |
| N | 28 | | 28 | | 3 |

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. N IS THE MAXIMUM OF TERMINAL POSITIONS.

| PACKAGE NUMBER: | ZZ251 | REV.: | B |
|---|---|---|---|
| JEDEC NUMBER: | NONE | | |

## Package Number 252 - 40-Lead SOIC, .370 Wide




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .096 | .108 | 2.45 | 2.75 | |
| A1 | .002 TYP | | 0.05 TYP | | |
| B | .012 | .020 | 0.30 | 0.50 | |
| c | .004 | .012 | 0.10 | 0.30 | |
| D | 1.036 | 1.059 | 26.30 | 26.90 | |
| E | .362 | .378 | 9.20 | 9.60 | |
| e | .042 | .058 | 1.07 | 1.47 | |
| G | .043 | .051 | 1.10 | 1.30 | |
| H | .453 | .476 | 11.50 | 12.10 | |
| L | .009 | -- | 0.25 | -- | 4 |
| N | 40 | | 40 | | 5 |

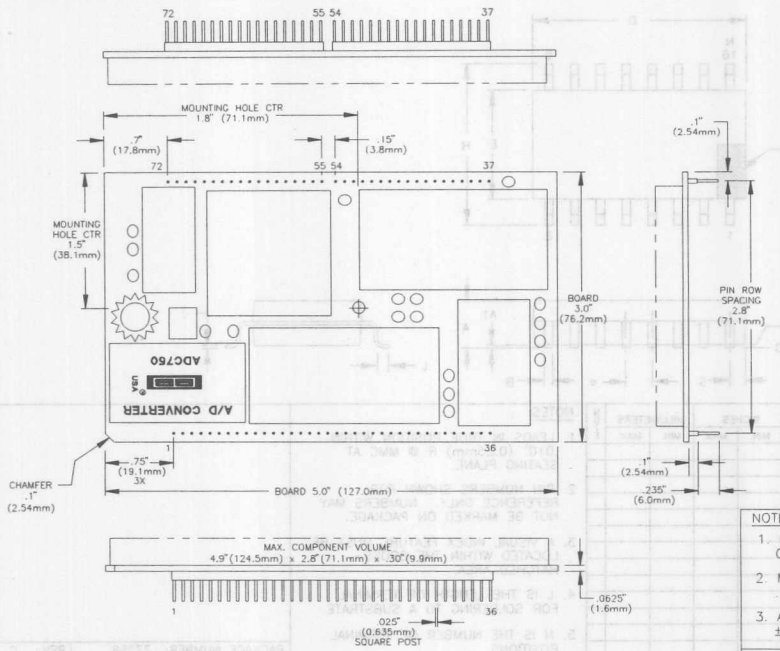
NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
4. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. N IS THE NUMBER OF TERMINAL POSITIONS.

| PACKAGE NUMBER: | ZZ252 | REV.: | B |
|---|---|---|---|
| JEDEC NUMBER: | NONE | | |

PACKAGE DRAWINGS (Mechanical)

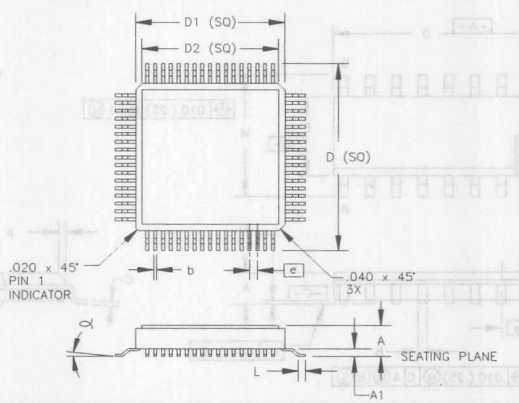
**Package Number 255 - Custom Module**




NOTES:
1. PIN SPACING .1" (2.54mm) UNLESS OTHERWISE NOTED.
2. MOUNTING HOLE DIAMETER .120" (3.05mm).
3. ALL DIMENSIONAL TOLERANCES ±.005" UNLESS OTHERWISE NOTED.

| PACKAGE NUMBER: | ZZ255 | REV.: | B |
|---|---|---|---|
| JEDEC NUMBER: | NONE | | |

**Package Number 256 - 68-Lead Quad. Pkg. With Gull Wing Leads**



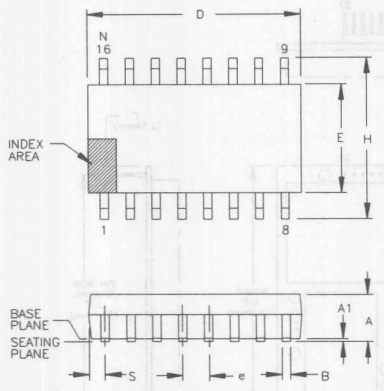

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .200 REF. | | 4.81 REF. | | |
| A1 | .045 | .055 | 1.14 | 1.40 | |
| b | .013 | .025 | 0.33 | 0.64 | |
| D | 1.200 | 1.220 | 30.48 | 30.99 | |
| D1 | .940 | .960 | 23.88 | 24.38 | |
| D2 | .865 | .875 | 21.97 | 22.23 | |
| e | .050 BASIC | | 1.27 BASIC | | |
| L | .045 REF. | | 1.14 REF. | | |
| N | 68 | | 68 | | 2 |
| α | 0° | 6° | 0° | 6° | |

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |

NOTES:
1. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004 MAX AT SEATING PLANE.
2. N IS THE MAXIMUM OF TERMINAL POSITIONS.

| PACKAGE NUMBER: | ZZ256 | REV.: | B |
|---|---|---|---|
| JEDEC NUMBER: | NONE | | |

**Package Number 258 - 16-Lead SOIC, .209 Wide**

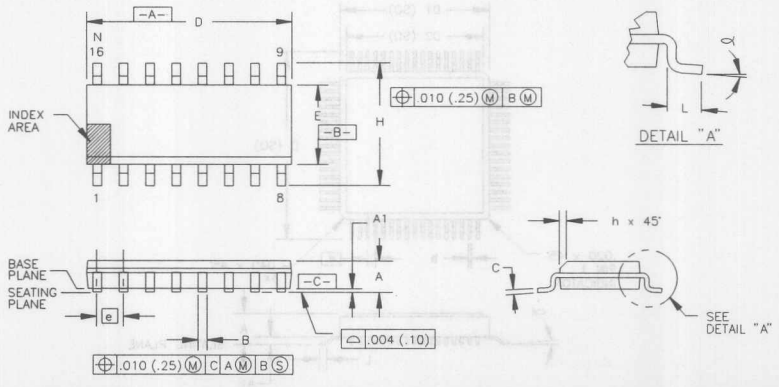



| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .090 | -- | 2.29 | |
| A1 | .004 | .008 | 0.10 | 0.20 | |
| B | .012 | .020 | 0.30 | 0.51 | |
| c | .005 | .008 | 0.13 | 0.20 | |
| D | .400 | .415 | 10.16 | 10.54 | |
| E | .205 | .214 | 5.21 | 5.44 | |
| e | .044 | .055 | 1.12 | 1.40 | |
| H | .300 | .324 | 7.62 | 8.23 | |
| L | .012 | .036 | 0.30 | 0.91 | |
| N | 16 | | 16 | | 5 |
| S | .020 | .031 | 0.51 | 0.79 | |

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
4. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. N IS THE NUMBER OF TERMINAL POSITIONS.

PACKAGE NUMBER: ZZ258 | REV.: C
JEDEC NUMBER: NONE

**Package Number 265 - 16-Lead SOIC, .150 Wide**



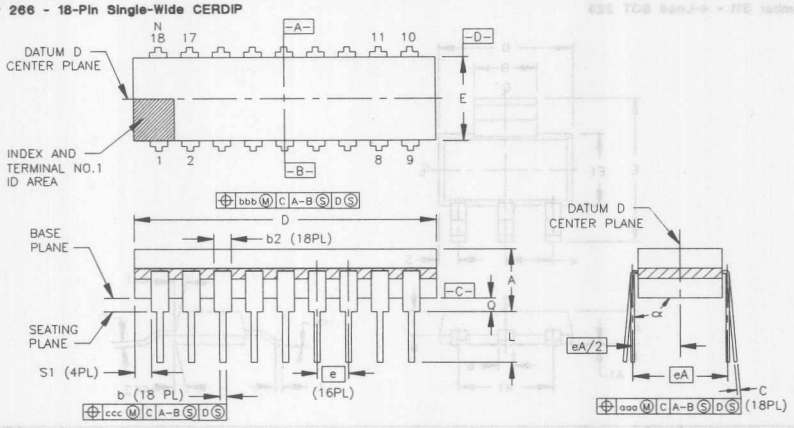

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .0532 | .0688 | 1.35 | 1.75 | |
| A1 | .004 | .0098 | 0.10 | 0.25 | |
| B | .013 | .020 | 0.33 | 0.51 | 7 |
| C | .0075 | .0098 | 0.19 | 0.25 | |
| D | .3859 | .3937 | 9.80 | 10.00 | 2 |
| E | .1497 | .1574 | 3.80 | 4.00 | 3 |
| e | .050 BASIC | | 1.27 BASIC | | |
| H | .2284 | .244 | 5.80 | 6.20 | |
| h | .0099 | .0196 | 0.25 | 0.50 | 4 |
| L | .016 | .050 | 0.40 | 1.27 | 5 |
| N | 16 | | 16 | | 6 |
| α | 0° | 8° | 0° | 8° | |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ265 | REV.: D
JEDEC NUMBER: MS-012-AC

PACKAGE DRAWINGS (Mechanical)

**Package Number 266 - 18-Pin Single-Wide CERDIP**




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .200 | -- | 5.08 | |
| b | .014 | .026 | 0.36 | 0.66 | |
| b2 | .045 | .065 | 1.14 | 1.65 | |
| C | .008 | .018 | 0.20 | 0.46 | |
| D | -- | .960 | -- | 24.38 | |
| E | .220 | .310 | 5.59 | 7.87 | |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .300 BASIC | | 7.62 BASIC | | |
| eA/2 | .150 BASIC | | 3.81 BASIC | | |
| L | .125 | .200 | 3.18 | 5.08 | |
| N | 18 | | 18 | | |
| Q | .015 | .070 | 0.38 | 1.78 | |
| S1 | .005 | -- | 0.13 | -- | |
| α | 90° | 105° | 90° | 105° | |

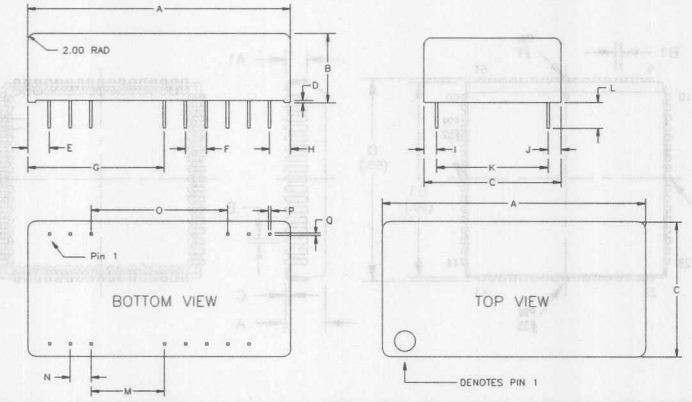
| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| aaa | -- | .015 | -- | 0.38 | |
| bbb | -- | .030 | -- | 0.76 | |
| ccc | -- | .010 | -- | 0.25 | |

NOTES:

1. DIMENSIONS ARE MIL-STD-1835 COMPLIANT. (REF GDIP-P188, D-6).

PACKAGE NUMBER: ZZ266 | REV.: B
JEDEC NUMBER: NONE

**Package Number 269 - 24-Pin Plastic**



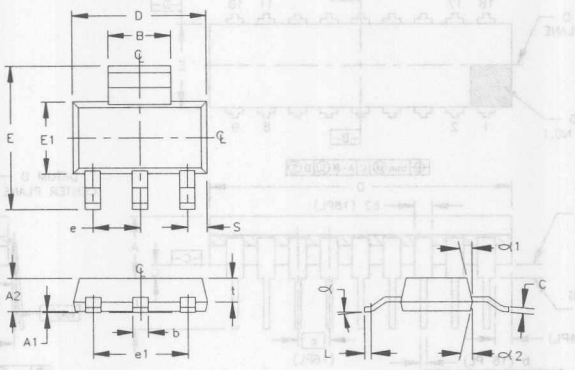

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | 2.504 | 2.505 | 63.61 | 63.63 | |
| B | 0.678 | 0.684 | 17.22 | 17.38 | |
| C | 1.305 | 1.306 | 33.15 | 33.17 | |
| D | 0.020 | 0.027 | 0.52 | 0.68 | |
| E | 0.199 | 0.206 | 5.06 | 5.22 | |
| F | 0.197 | 0.203 | 5.00 | 5.16 | |
| G | 1.299 | 1.306 | 33.00 | 33.16 | |
| H | 0.200 | 0.206 | 5.07 | 5.23 | |
| I | 0.151 | 0.154 | 3.845 | 3.915 | |
| J | 0.151 | 0.154 | 3.845 | 3.915 | |
| K | 0.997 | 1.003 | 25.32 | 25.48 | |
| L | 0.253 | 0.259 | 6.42 | 6.58 | |
| M | 0.697 | 0.703 | 17.70 | 17.86 | |
| N | 0.197 | 0.203 | 5.00 | 5.16 | |

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| O | 1.297 | 1.303 | 32.94 | 33.10 | |
| P | 0.024 | 0.026 | 0.61 | 0.67 | |
| Q | 0.024 | 0.026 | 0.61 | 0.67 | |

NOTES:

PACKAGE NUMBER: ZZ269 | REV.: A
JEDEC NUMBER: None

## Package Number 311 - 4-Lead SOT 223




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A1 | .0008 | .004 | 0.02 | 0.10 | |
| A2 | .060 | .067 | 1.50 | 1.70 | |
| B | .116 | .124 | 2.95 | 3.15 | |
| b | .026 | .033 | 0.66 | 0.73 | |
| C | .010 | .014 | 0.25 | 0.35 | |
| D | .248 | .264 | 6.30 | 6.70 | |
| E | .264 | .287 | 6.70 | 7.30 | |
| E1 | .130 | .146 | 3.30 | 3.70 | |
| e | .0905 | NOM. | 2.30 | NOM. | |
| e1 | .181 | NOM. | 4.60 | NOM. | |
| L | .012 | MIN. | 0.30 | MIN. | |
| N | 4 | | 4 | | 1 |
| S | .033 | .041 | 0.85 | 1.05 | |
| t | .043 | .051 | 1.10 | 1.30 | |

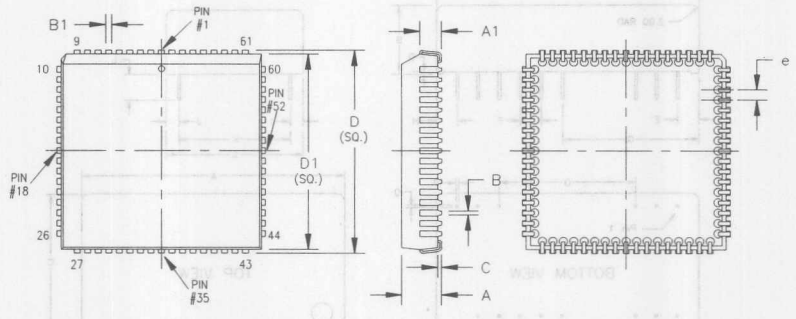
| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| α | 10° | MAX. | 10° | MAX. | |
| α1 | 10° | 16° | 10° | 16° | |
| α2 | 10° | 16° | 10° | 16° | |

NOTES:

1. N IS THE NUMBER OF TERMINAL POSITIONS.

PACKAGE NUMBER: ZZ311 REV: B
JEDEC NUMBER: NONE

## Package Number 312 - 68-Pin Plastic Quad




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .167 | .177 | 4.24 | 4.50 | |
| A1 | .100 | .110 | 2.54 | 2.79 | |
| B | .016 | .020 | 0.41 | 0.51 | |
| B1 | .026 | .032 | 0.66 | 0.81 | |
| C | .020 | .025 | 0.51 | 0.64 | |
| D | .985 | .995 | 25.02 | 25.27 | |
| D1 | .950 | .958 | 24.13 | 24.33 | 2 |
| e | .050 | BASIC | 1.27 | BASIC | |
| N | 68 | | 68 | | |

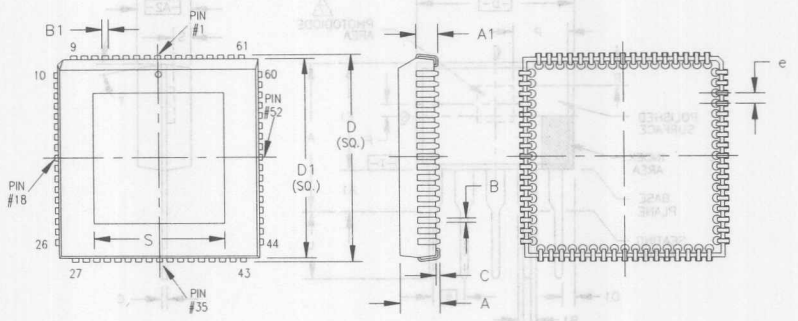
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. DIMENSION D1 DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .254mm/ .010 INCH.
3. CONTROLLING DIMENSION: INCH

PACKAGE NUMBER: ZZ312 REV: B
JEDEC NUMBER: NONE

PACKAGE DRAWINGS (Mechanical)

**Package Number 312-1 - 68-Pin Plastic Quad**



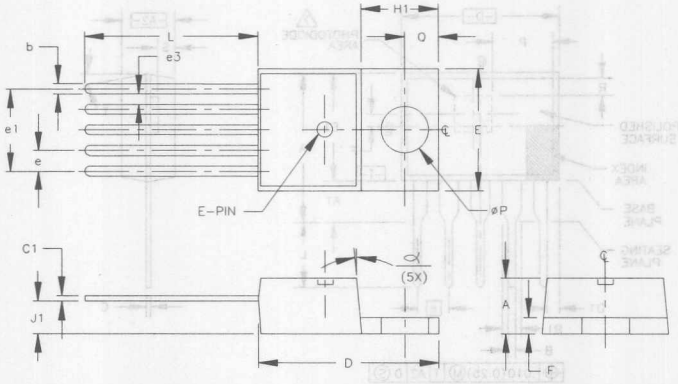

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .167 | .177 | 4.24 | 4.50 | |
| A1 | .100 | .110 | 2.54 | 2.79 | |
| B | .016 | .020 | 0.41 | 0.51 | |
| B1 | .026 | .032 | 0.66 | 0.81 | |
| C | .020 | .025 | 0.51 | 0.64 | |
| D | .985 | .995 | 25.02 | 25.27 | |
| D1 | .950 | .958 | 24.13 | 24.33 | 2 |
| e | .050 BASIC | | 1.27 BASIC | | |
| N | 68 | | 68 | | |
| S | .618 | .628 | 15.70 | 15.95 | |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D1 DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .254mm/ .010 INCH.
3. CONTROLLING DIMENSION: INCH

PACKAGE NUMBER: ZZ312-1 | REV.: B
JEDEC NUMBER: NONE

**Package Number 315 - TO-220, 5-Lead**

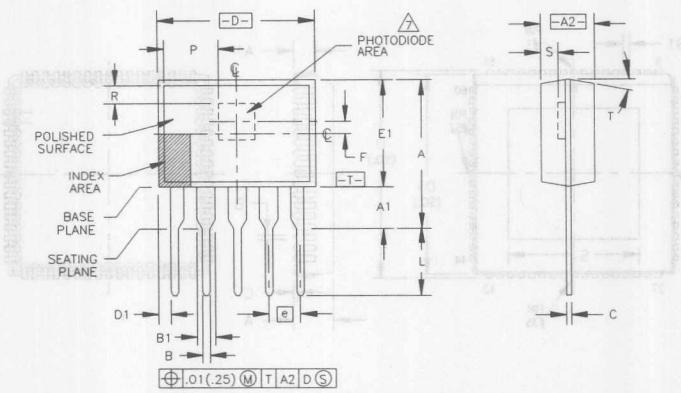



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .160 | .190 | 4.06 | 4.83 | |
| b | .025 | .040 | 0.63 | 1.02 | |
| C1 | .014 | .022 | 0.36 | 0.56 | |
| D | .560 | .590 | 14.22 | 14.99 | |
| E | .385 | .415 | 9.78 | 10.54 | |
| e | .062 | .072 | 1.57 | 1.83 | |
| e1 | .263 | .273 | 6.68 | 6.93 | |
| e3 | .030 | .040 | 0.76 | 1.02 | |
| F | .045 | .055 | 1.14 | 1.40 | |
| H1 | .234 | .258 | 5.94 | 6.55 | |
| J1 | .090 | .115 | 2.29 | 2.92 | |
| øP | .146 | .156 | 3.71 | 3.96 | |
| Q | .103 | .113 | 2.62 | 2.87 | |
| L | .540 | .560 | 13.72 | 14.22 | |
| α | 3° | 7° | 3° | 7° | |

NOTES:

PACKAGE NUMBER: ZZ315 | REV.: B
JEDEC NUMBER: NONE

**Package Number 321 - 5-Pin Transparent Plastic SIP**



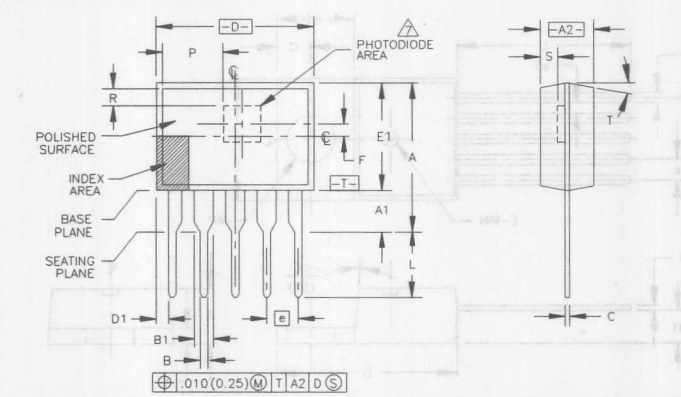

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .360 | -- | 9.14 | 3 |
| A1 | .070 | -- | 1.78 | -- | 3 |
| A2 | .120 | .135 | 3.05 | 3.43 | |
| B | .014 | .022 | 0.35 | 0.56 | |
| B1 | .040 | .050 | 1.02 | 1.27 | |
| C | .008 | .012 | 0.20 | 0.30 | |
| D | .360 | .390 | 9.14 | 9.91 | 4 |
| D1 | .005 | -- | 0.13 | -- | |
| E1 | .238 | .275 | 6.05 | 6.99 | 4 |
| e | .075 BASIC | | 1.91 BASIC | | |
| F | .015 | .035 | 0.38 | 0.89 | |
| L | .140 | .180 | 3.56 | 4.57 | 3 |
| N | 5 | | 5 | | 5 |
| P | .086 | .112 | 2.18 | 2.84 | |

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| R | .036 | .056 | 0.89 | 1.42 | |
| S | .036 | .043 | 0.91 | 1.09 | |
| T | 5.5° | 8.5° | 5.5° | 8.5° | |

NOTES:
1. CONTROLLING DIMENSION: INCH. IN CASE OF CONFLICT BETWEEN THE ENGLISH AND METRIC DIMENSIONS, THE INCH DIMENSIONS CONTROL.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D AND E1 DIMENSIONS FOR PLASTIC PACKAGES DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.25mm).
5. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
6. CENTER OF PHOTODIODE MUST BE WITHIN .01" OF CENTER OF PHOTODIODE AREA.
7. DIMENSIONS REFERENCED CORRELATE TO A PHOTODIODE SIZE .090 X .090 INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: | ZZ321 | REV.: | E |
|---|---|---|---|
| JEDEC NUMBER: | NONE | | |

**Package Number 321-1 - 5-Pin Transparent Plastic SIP**




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .360 | -- | 9.14 | 3 |
| A1 | .070 | -- | 1.78 | -- | 3 |
| A2 | .120 | .135 | 3.05 | 3.43 | |
| B | .014 | .022 | 0.35 | 0.56 | |
| B1 | .040 | .050 | 1.02 | 1.27 | |
| C | .008 | .012 | 0.20 | 0.30 | |
| D | .360 | .390 | 9.14 | 9.91 | 4 |
| D1 | .005 | -- | 0.13 | -- | |
| E1 | .238 | .275 | 6.05 | 6.99 | 4 |
| e | .075 BASIC | | 1.91 BASIC | | |
| F | .015 | .035 | 0.38 | 0.89 | |
| L | .140 | .180 | 3.56 | 4.57 | 3 |
| N | 5 | | 5 | | 5 |
| P | .102 | .128 | 2.59 | 3.25 | |

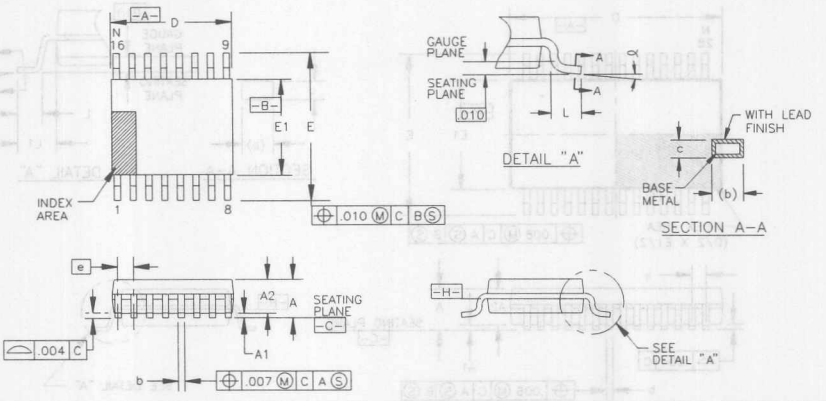
| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| R | .036 | .056 | 0.91 | 1.42 | |
| S | .036 | .043 | 0.91 | 1.09 | |
| T | 5.5° | 8.5° | 5.5° | 8.5° | |

NOTES:
1. CONTROLLING DIMENSION: INCH. IN CASE OF CONFLICT BETWEEN THE ENGLISH AND METRIC DIMENSIONS, THE INCH DIMENSIONS CONTROL.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D AND E1 DIMENSIONS FOR PLASTIC PACKAGES DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.25mm).
5. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
6. CENTER OF PHOTODIODE MUST BE WITHIN .010" OF CENTER OF PHOTODIODE AREA.
7. DIMENSIONS REFERENCED CORRELATE TO A PHOTODIODE SIZE .090 X .090 INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

| PACKAGE NUMBER: | ZZ321-1 | REV.: | B |
|---|---|---|---|
| JEDEC NUMBER: | NONE | | |

PACKAGE DRAWINGS (mechanical)

## Package Number 322 - 16-Lead SSOP, .150 Wide

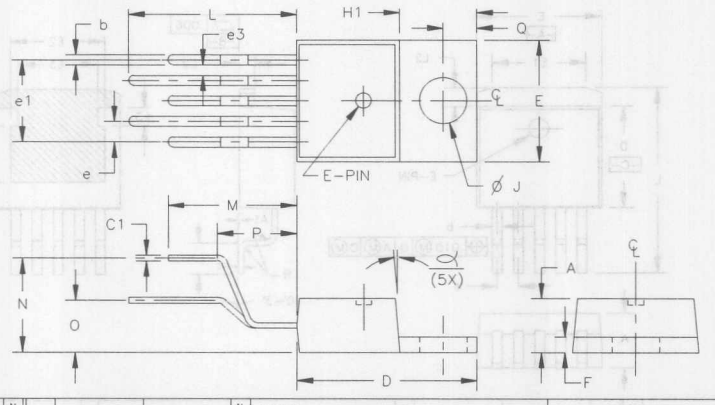



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .053 | .069 | 1.35 | 1.75 | |
| A1 | .004 | .010 | 0.10 | 0.25 | |
| A2 | .055 | .059 | 1.40 | 1.50 | |
| b | .008 | .012 | 0.20 | 0.30 | 3,7 |
| c | .007 | .010 | 0.19 | 0.25 | 7 |
| D | .188 | .197 | 4.78 | 5.00 | 2 |
| E | .228 | .244 | 5.80 | 6.20 | |
| E1 | .149 | .157 | 3.78 | 4.00 | 2 |
| e | .025 BASIC | | .635 BASIC | | |
| L | .016 | .050 | 0.40 | 1.27 | 4 |
| N | 16 | | 16 | | 5 |
| α | 0° | 8° | 0° | 8° | |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. D AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT DATUM PLANE -H- MOLD PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED .008 INCH (0.20mm) PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13mm) TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN .003 INCH (0.07mm) AT LEAST MATERIAL CONDITION.
4. DIMENSION L TO BE DETERMINED AT SEATING PLANE-DATUM "C".
5. "N" IS THE NUMBER OF TERMINAL POSITIONS.
6. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSSHATCHED AREA.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .004 AND .010 INCH FROM THE LEAD TIP.

PACKAGE NUMBER: ZZ322 | REV.: B
JEDEC NUMBER: MO-137-AB WITH THE EXCEPTION OF DIM. D, E1.

## Package Number 323 - TO220, 5-Lead ZIP



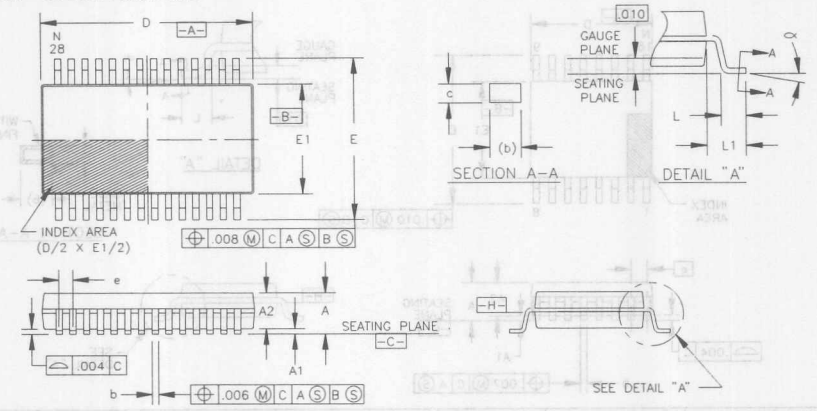

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .160 | .190 | 4.06 | 4.83 | |
| b | .025 | .040 | 0.63 | 1.02 | |
| C1 | .014 | .022 | 0.36 | 0.56 | |
| D | .560 | .590 | 14.22 | 14.99 | |
| E | .385 | 4.15 | 9.78 | 10.54 | |
| e | .057 | .077 | 1.57 | 1.83 | |
| e1 | .263 | .273 | 6.68 | 6.93 | |
| e3 | .030 | .040 | 0.76 | 1.02 | |
| F | .045 | .055 | 1.14 | 1.40 | |
| H1 | .234 | .258 | 5.94 | 6.55 | |
| ØJ | .146 | .156 | 3.71 | 3.96 | |
| Q | .103 | .113 | 2.62 | 2.87 | |
| L | .525 | .545 | 13.33 | 13.84 | |
| α | 3° | 7° | 3° | 7° | |

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| M | .400 | .420 | 10.16 | 10.67 | |
| N | .314 | .326 | 7.98 | 8.28 | |
| O | .160 | .170 | 4.06 | 4.32 | |
| P | .250 | .270 | 6.35 | 6.86 | |

NOTES:

PACKAGE NUMBER: ZZ323 | REV.: C
JEDEC NUMBER: NONE

**Package Number 324 - 28-Lead Plastic SSOP**



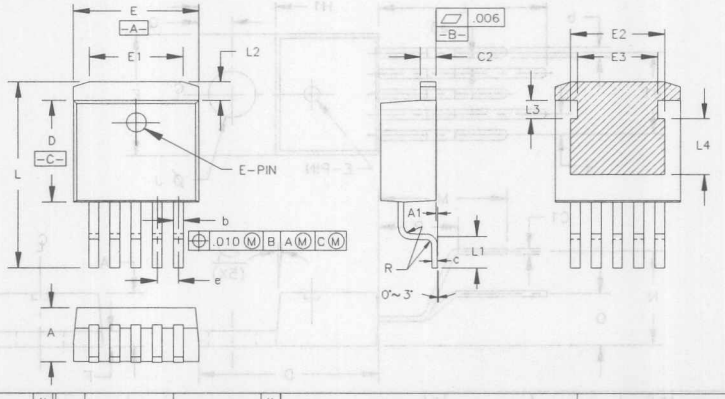

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .079 | -- | 2.00 | |
| A1 | .002 | -- | 0.05 | -- | |
| A2 | .065 | .073 | 1.65 | 1.85 | |
| b | .009 | .015 | 0.22 | 0.38 | 3,7 |
| c | .004 | .010 | 0.09 | 0.25 | 7 |
| D | .390 | .413 | 9.90 | 10.50 | 2 |
| E | .291 | .323 | 7.40 | 8.20 | |
| E1 | .196 | .220 | 5.00 | 5.60 | 2 |
| e | .0256 BASIC | | 0.65 BASIC | | |
| L | .022 | .037 | 0.55 | 0.95 | 4 |
| L1 | .049 | REF | 1.25 | REF | |
| N | 28 | | 28 | | 5 |
| θ | 0° | 8° | 0° | 8° | |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. D AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT DATUM PLANE -H- MOLD PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED .008 INCH PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN .003 INCH AT LEAST MATERIAL CONDITION.
4. DIMENSION L TO BE DETERMINED AT SEATING PLANE-DATUM C.
5. N IS THE NUMBER OF TERMINAL POSITIONS.
6. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
7. SECTION A-A DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .004 AND .010 INCH FROM THE LEAD TIP.

PACKAGE NUMBER: ZZ324 REV.: C
JEDEC NUMBER: MO-150

**Package Number 325 - 5-Lead DD PAK**




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .170 | .183 | 4.32 | 4.65 | |
| A1 | .000 | .004 | 0.00 | 0.10 | |
| b | .026 | .037 | 0.66 | 0.94 | 2,5 |
| C2 | .045 | .055 | 1.14 | 1.40 | |
| c | .014 | .026 | 0.36 | 0.66 | 2 |
| D | .310 | .350 | 7.87 | 8.89 | |
| E | .385 | .410 | 9.78 | 10.41 | |
| E1 | .297 | .303 | 7.54 | 7.70 | |
| E2 | .296 | .304 | 7.52 | 7.72 | |
| E3 | .252 | .300 | 6.40 | 7.62 | |
| e | .067 | REF | 1.70 | REF | |
| L | .595 | .605 | 15.11 | 15.37 | |
| L1 | .096 | .104 | 2.44 | 2.64 | |
| L2 | .0585 | .0625 | 1.485 | 1.587 | |
| L3 | .056 | .064 | 1.42 | 1.63 | |
| L4 | .179 | .187 | 4.55 | 4.75 | |
| N | 5 | | 5 | | 6 |
| R | .017 | .019 | 0.43 | 0.48 | |

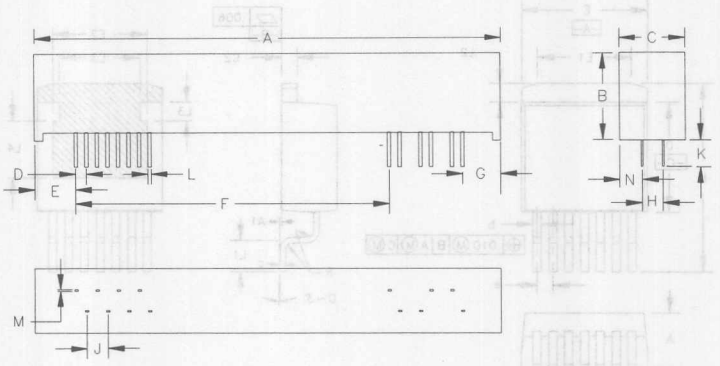
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14, 5M-1982.
2. DIMENSION b AND c APPLY TO THE PLATED LEAD.
3. LEADS ARE NOT ALLOWED ABOVE THE DATUM -B-.
4. STAND-OFF HEIGHT IS MEASURED FROM LEAD TIP WITH REFERENCE TO DATUM -B-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM "b" BY MORE THAN .003".
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. CROSSHATCH INDICATES EXPOSED METAL SURFACE.

PACKAGE NUMBER: ZZ325 REV.: D
JEDEC NUMBER: MO-169
WITH THE EXCEPTION OF DIM. D,L,L1,L2

PACKAGE DRAWINGS (Mechanical)

**Package Number 326 - 38-Lead Plastic ZIP**

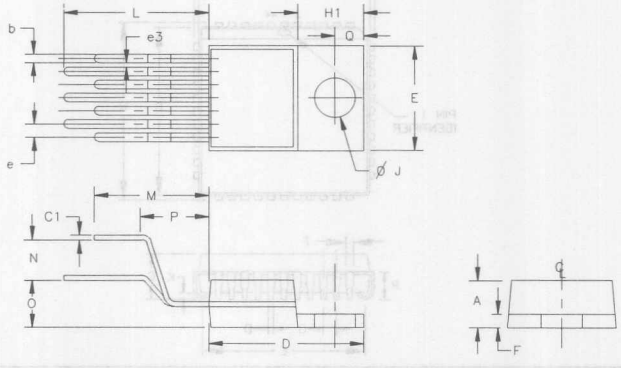



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | 2.220 | 2.246 | 56.39 | 57.05 | |
| B | 0.418 | 0.428 | 10.62 | 10.87 | |
| C | 0.295 | 0.325 | 7.49 | 8.26 | |
| D | 0.050 | TYPICAL | 1.27 | TYPICAL | |
| E | 0.190 | 0.200 | 4.83 | 5.08 | |
| F | 1.500 | TYPICAL | 38.10 | TYPICAL | |
| G | 0.183 | 0.193 | 4.65 | 4.90 | |
| H | 0.100 | TYPICAL | 2.54 | TYPICAL | |
| J | 0.100 | TYPICAL | 2.54 | TYPICAL | |
| K | 0.125 | TYPICAL | 3.18 | TYPICAL | |
| L | 0.016 | 0.020 | 0.41 | 0.51 | |
| M | 0.008 | 0.012 | 0.20 | 0.30 | |
| N | 0.080 | – | 2.03 | – | |

NOTES:

PACKAGE NUMBER: ZZ326 REV.: B
JEDEC NUMBER: NONE

**Package Number 327 - TO220, 7-Lead ZIP**

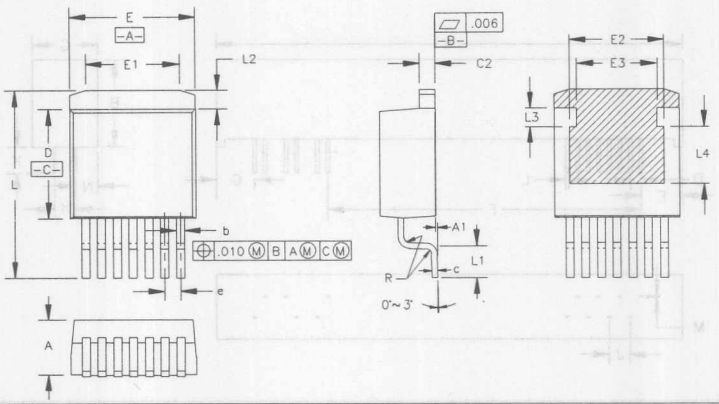



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .169 | .185 | 4.29 | 4.70 | |
| b | .026 | .036 | 0.66 | 0.91 | |
| C1 | .016 | .022 | 0.41 | 0.56 | |
| D | .560 | .590 | 14.22 | 14.99 | |
| E | .390 | .410 | 9.91 | 10.41 | |
| e | .045 | .055 | 1.14 | 1.40 | |
| e3 | .014 | .024 | 0.36 | 0.61 | |
| F | .045 | .055 | 1.14 | 1.40 | |
| H1 | .235 | .258 | 5.97 | 6.55 | |
| ØJ | .147 | .155 | 3.73 | 3.94 | |
| Q | .103 | .113 | 2.62 | 2.87 | |
| L | .503 | .571 | 12.78 | 14.50 | |
| M | .395 | .453 | 10.03 | 11.51 | |
| N | .135 | .165 | 3.43 | 4.19 | |
| O | .155 | .195 | 3.94 | 4.95 | |
| P | .243 | .251 | 6.17 | 6.38 | |

NOTES:

PACKAGE NUMBER: ZZ327 REV.: A
JEDEC NUMBER: NONE

## Package Number 328 - 7-Lead DD PAK




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .170 | .183 | 4.32 | 4.65 | |
| A1 | .000 | .012 | 0.00 | .305 | |
| b | .022 | .034 | 0.57 | 0.86 | 2,5 |
| C2 | .045 | .055 | 1.14 | 1.40 | |
| c | .014 | .026 | 0.36 | 0.66 | 2 |
| D | .330 | .370 | 8.38 | 9.40 | |
| E | .385 | .410 | 9.78 | 10.41 | |
| E1 | .297 | .303 | 7.54 | 7.70 | |
| E2 | .296 | .304 | 7.52 | 7.72 | |
| E3 | .252 | .300 | 6.40 | 7.62 | |
| e | .050 REF | | 1.27 REF | | |
| L | .595 | .605 | 15.11 | 15.37 | |
| L1 | .096 | .104 | 2.44 | 2.64 | |
| L2 | .0585 | .0625 | 1.485 | 1.587 | |

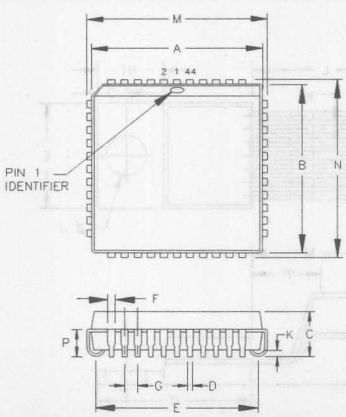
| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| L3 | .056 | .064 | 1.42 | 1.63 | |
| L4 | .179 | .187 | 4.55 | 4.75 | |
| N | 7 | | 7 | | 6 |
| R | .017 | .019 | 0.43 | 0.48 | |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. DIMENSION b AND c APPLY TO THE PLATED LEAD.
3. LEADS ARE NOT ALLOWED ABOVE THE DATUM –B–.
4. STAND–OFF HEIGHT IS MEASURED FROM LEAD TIP WITH REFERENCE TO DATUM –B–.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM "b" BY MORE THAN .003".
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. CROSSHATCH INDICATES EXPOSED METAL SURFACE.

PACKAGE NUMBER: ZZ328 | REV.: B
JEDEC NUMBER: MO–169 WITH THE EXCEPTION OF DIM. L, L1, L2

## Package Number 329 - 44-Pin PLCC




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .650 | .656 | 16.51 | 16.66 | |
| B | .650 | .656 | 16.51 | 16.66 | |
| C | -- | .180 | -- | 4.57 | |
| D | .014 | .022 | 0.36 | 0.56 | |
| E | .600 | .620 | 15.24 | 15.75 | |
| F | .024 | .032 | 0.61 | 0.81 | |
| G | .050 BASIC | | 1.27 BASIC | | |
| K | .020 | -- | 0.51 | -- | |
| M | .685 | .695 | 17.40 | 17.65 | |
| N | .685 | .695 | 17.40 | 17.65 | |
| P | .100 | .110 | 2.54 | 2.79 | |

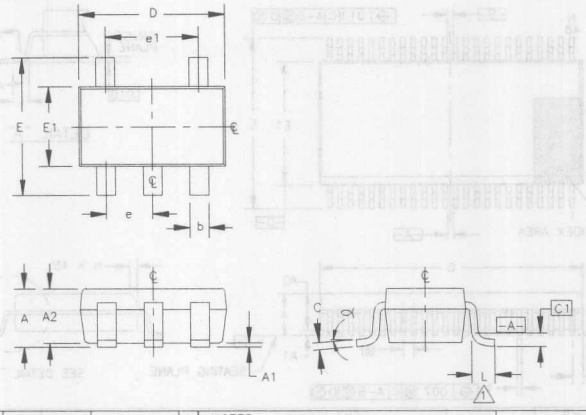
NOTES:

1. LEADS IN TRUE POSITION WITHIN 0.01" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.

PACKAGE NUMBER: ZZ329 | REV.: A
JEDEC NUMBER: NONE

PACKAGE DRAWINGS (mechanical)

**Package Number 331 - 5-Lead SOT-23**



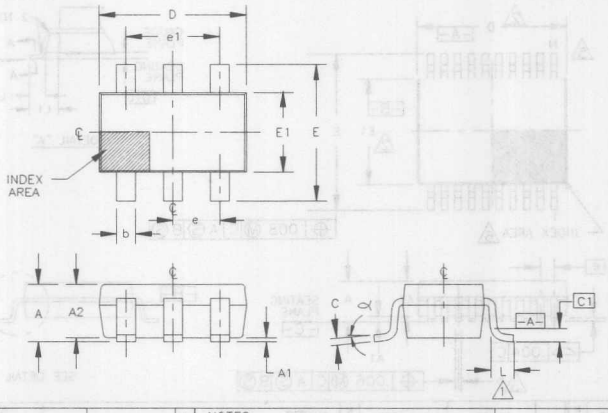

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .035 | .057 | 0.90 | 1.45 | |
| A1 | .000 | .006 | 0.00 | 0.15 | |
| A2 | .035 | .051 | 0.90 | 1.30 | |
| b | .010 | .020 | 0.25 | 0.50 | |
| C | .003 | .008 | 0.08 | 0.20 | |
| C1 | .007 | BASIC | 0.20 | BASIC | |
| D | .110 | .118 | 2.80 | 3.00 | |
| E | .102 | .118 | 2.60 | 3.00 | |
| E1 | .059 | .069 | 1.50 | 1.75 | |
| e | .037 | REF | 0.95 | REF | |
| e1 | .075 | REF | 1.90 | REF | |
| L | .014 | .022 | 0.35 | 0.55 | 1 |
| N | 5 | | 5 | | 4 |
| ∝ | 0° | 10° | 0° | 10° | |

NOTES:

1. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A AND LEAD SURFACE.
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH AND METAL BURR.
3. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
4. N IS THE MAXIMUM QUANTITY OF LEAD POSITIONS.

PACKAGE NUMBER: ZZ331 REV.: C
JEDEC NUMBER: NONE

**Package Number 332 - 6-Lead SOT-23**



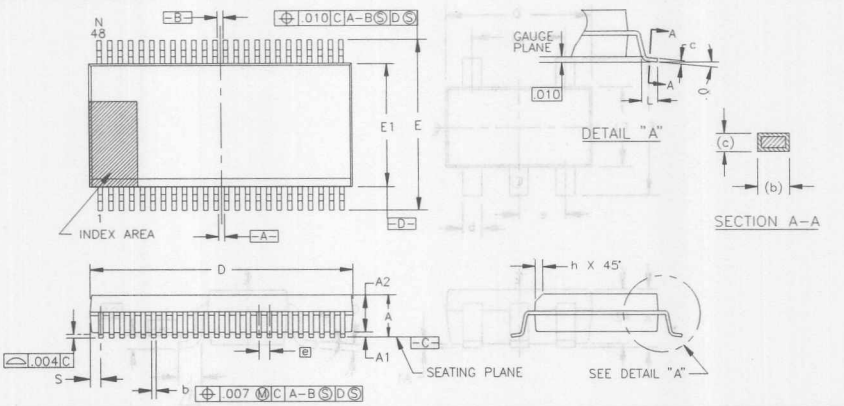

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .035 | .057 | 0.90 | 1.45 | |
| A1 | .000 | .006 | 0.00 | 0.15 | |
| A2 | .035 | .051 | 0.90 | 1.30 | |
| b | .010 | .020 | 0.25 | 0.50 | |
| C | .003 | .008 | 0.08 | 0.20 | |
| C1 | .007 | BASIC | 0.20 | BASIC | |
| D | .110 | .118 | 2.80 | 3.00 | |
| E | .102 | .118 | 2.60 | 3.00 | |
| E1 | .059 | .069 | 1.50 | 1.75 | |
| e | .037 | REF | 0.95 | REF | |
| e1 | .075 | REF | 1.90 | REF | |
| L | .014 | .022 | 0.35 | 0.55 | 1 |
| N | 6 | | 6 | | 5 |
| ∝ | 0° | 10° | 0° | 10° | |

NOTES:

1. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A AND LEAD SURFACE.
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH AND METAL BURR.
3. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
4. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. N IS THE MAXIMUM QUANTITY OF LEAD POSITIONS.

PACKAGE NUMBER: ZZ332 REV.: C
JEDEC NUMBER: NONE

## Package Number 333 - 48-Lead SSOP

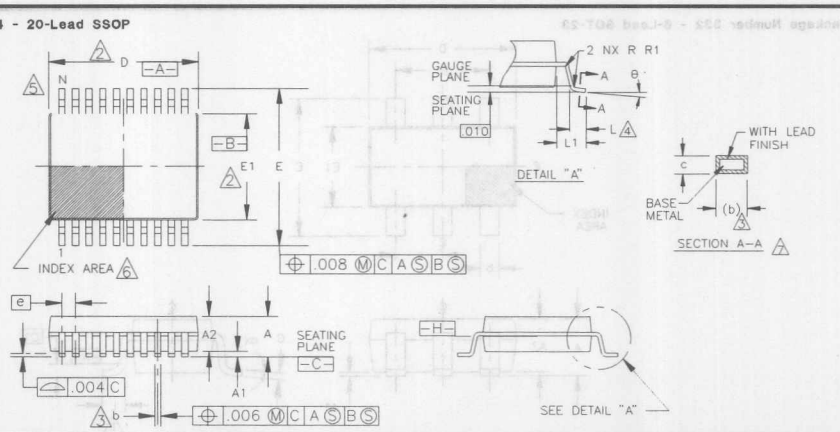



| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .095 | .110 | 2.41 | 2.79 | |
| A1 | .008 | .016 | 0.20 | 0.41 | |
| A2 | .088 | .092 | 2.24 | 2.34 | |
| b | .008 | .0135 | 0.20 | 0.34 | 8 |
| c | .005 | .010 | 0.13 | 0.25 | 8 |
| D | .620 | .630 | 15.75 | 16.00 | 2 |
| E | .395 | .420 | 10.03 | 10.67 | |
| E1 | .291 | .299 | 7.39 | 7.59 | 3 |
| e | .025 | BASIC | 0.635 | BASIC | |
| L | .020 | .040 | 0.51 | 1.02 | 5 |
| h | .015 | .025 | 0.38 | 0.64 | 4 |
| N | 48 | | 48 | | 6,7 |
| S | .023 | .027 | 0.58 | 0.69 | |
| α | 0° | 8° | 0° | 8° | |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .006 INCH (0.15mm) PER SIDE.
3. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED .015 INCH (0.38mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF THE TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
7. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
8. SECTION A–A DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005" AND .010" FROM LEAD TIP.

PACKAGE NUMBER: ZZ333 | REV.: B
JEDEC NUMBER: MO-118-AA WITH THE EXCEPTION OF DIM. S & A2.

## Package Number 334 - 20-Lead SSOP



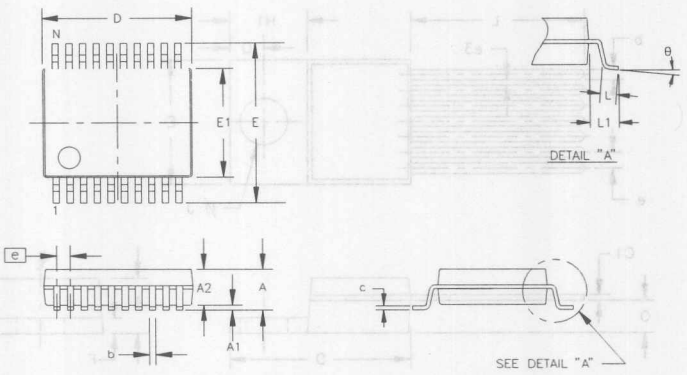

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .079 | -- | 2.00 | |
| A1 | .002 | -- | 0.05 | -- | |
| A2 | .065 | .073 | 1.65 | 1.85 | |
| b | .009 | .015 | 0.22 | 0.38 | 3,7 |
| c | .004 | .010 | 0.09 | 0.25 | 7 |
| D | .272 | .295 | 6.90 | 7.50 | 2 |
| E | .291 | .323 | 7.40 | 8.20 | |
| E1 | .197 | .220 | 5.00 | 5.60 | 2 |
| e | .0256 | BASIC | 0.65 | BASIC | |
| L | .022 | .037 | 0.55 | 0.95 | 4 |
| L1 | .049 | REF | 1.25 | REF | |
| N | 20 | | 20 | | 5 |
| θ | 0° | 8° | 0° | 8° | |
| R1 | .004 | -- | 0.09 | -- | |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. "D" AND "E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT DATUM PLANE -H- MOLD PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED .008 INCH (0.20mm) PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13mm) TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN .003 INCH (0.07mm) AT LEAST MATERIAL CONDITION.
4. TO BE DETERMINED AT SEATING PLANE–DATUM "C".
5. "N" IS THE NUMBER OF TERMINAL POSITIONS.
6. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSSHATCHED AREA.
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .004 AND .010 INCH FROM THE LEAD TIP.

PACKAGE NUMBER: ZZ334 | REV.: A
JEDEC NUMBER: MO-150 AE

PACKAGE DRAWINGS (Mechanical)

**Package Number 334-1 - 20-Lead SSOP**



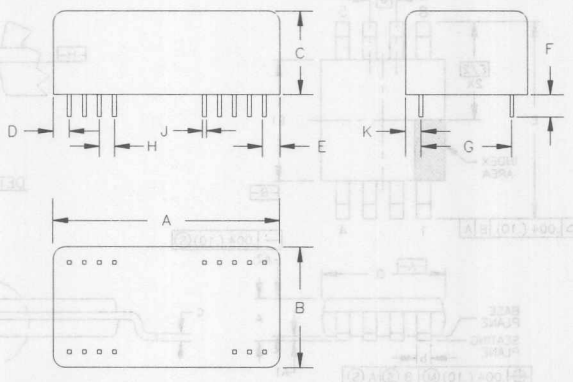

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .079 | -- | 2.00 | |
| A1 | .002 | -- | 0.05 | -- | |
| A2 | .065 | .073 | 1.65 | 1.85 | |
| b | .009 | .015 | 0.22 | 0.38 | |
| c | .004 | .010 | 0.09 | 0.25 | |
| D | .272 | .295 | 6.90 | 7.50 | |
| E | .291 | .323 | 7.40 | 8.20 | |
| E1 | .196 | .220 | 5.00 | 5.60 | |
| e | .0256 | BASIC | 0.65 | BASIC | |
| L | .018 | .037 | 0.45 | 0.95 | |
| L1 | .047 | .055 | 1.20 | 1.40 | |
| N | 20 | | 20 | | |
| θ | 0° | 8° | 0° | 8° | |

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| | | | | | |

NOTES:

| | |
|---|---|
| PACKAGE NUMBER: | ZZ334-1 REV.: A |
| JEDEC NUMBER: | NONE |

**Package Number 335 - Custom Module**



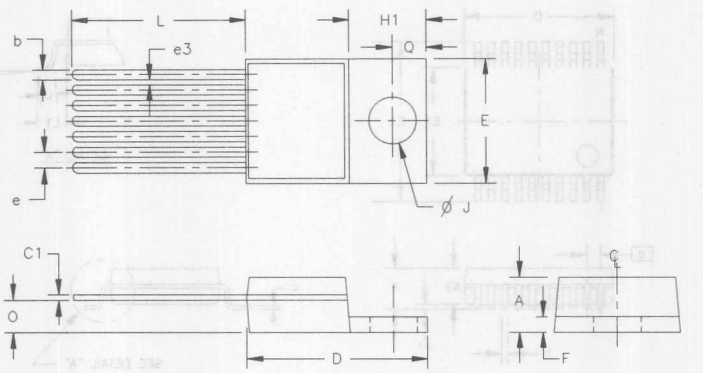

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | 1.506 | 1.512 | 38.24 | 38.40 | |
| B | 0.806 | 0.812 | 20.46 | 20.62 | |
| C | 0.568 | 0.574 | 14.42 | 14.58 | |
| D | 0.103 | 0.109 | 2.62 | 2.78 | |
| E | 0.103 | 0.109 | 2.62 | 2.78 | |
| F | 0.132 | 0.171 | 3.35 | 4.35 | |
| G | 0.6 | BASIC | 15.24 | BASIC | |
| H | 0.1 | BASIC | 2.54 | BASIC | |
| J | 0.025 | TYP. | 0.64 | TYP. | |
| K | 0.101 | 0.107 | 2.57 | 2.73 | |

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| | | | | | |

NOTES:

| | |
|---|---|
| PACKAGE NUMBER: | ZZ335 REV.: A |
| JEDEC NUMBER: | NONE |

## Package Number 336 - TO220, 7-Lead

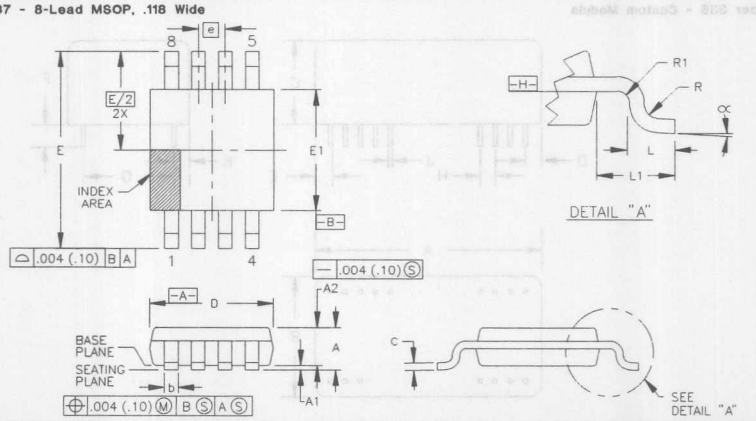



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .169 | .185 | 4.29 | 4.70 | |
| b | .026 | .036 | 0.66 | 0.91 | |
| C1 | .016 | .022 | 0.41 | 0.56 | |
| D | .560 | .590 | 14.22 | 14.99 | |
| E | .390 | .410 | 9.91 | 10.41 | |
| e | .045 | .055 | 1.14 | 1.40 | |
| e3 | .014 | .024 | 0.36 | 0.61 | |
| F | .045 | .055 | 1.14 | 1.40 | |
| H1 | .235 | .258 | 5.97 | 6.55 | |
| ØJ | .147 | .155 | 3.73 | 3.94 | |
| Q | .103 | .113 | 2.62 | 2.87 | |
| L | .540 | .560 | 13.72 | 14.22 | |
| Q | .090 | .115 | 2.29 | 2.92 | |

NOTES:

PACKAGE NUMBER: ZZ336 REV.: A
JEDEC NUMBER: NONE

## Package Number 337 - 8-Lead MSOP, .118 Wide

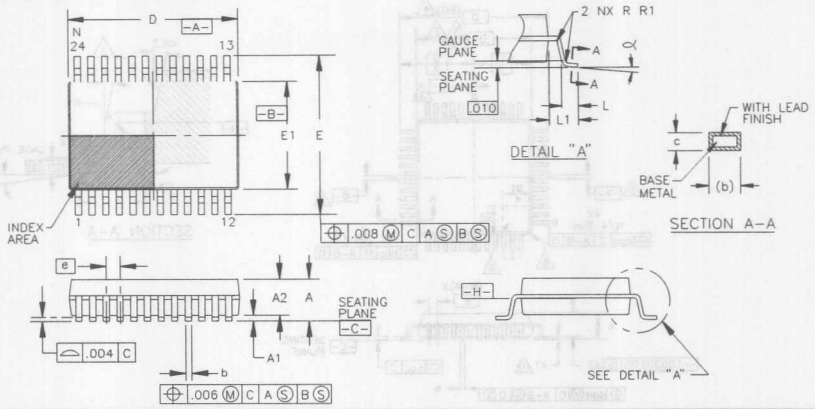



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .032 | .043 | 0.81 | 1.10 | |
| A1 | .002 | .006 | 0.05 | 0.15 | |
| A2 | .030 | .038 | 0.76 | 0.97 | |
| b | .011 | .015 | 0.28 | 0.38 | 4 |
| c | .005 | .009 | 0.13 | 0.23 | |
| D | .114 | .122 | 2.90 | 3.10 | 2,8 |
| E | .193 REF | | 4.90 REF | | |
| E1 | .114 | .122 | 2.90 | 3.10 | 3,8 |
| e | .0256 BASIC | | 0.65 BASIC | | |
| L | .0175 | .0255 | 0.45 | 0.65 | |
| L1 | .037 REF | | 0.94 REF | | |
| N | 8 | | 8 | | 6 |
| R | .003 | .009 | 0.08 | 0.23 | |
| R1 | .003 | .009 | 0.08 | 0.23 | |
| ∝ | 0° | 6° | 0° | 6° | |

NOTES:
1. ALL DIMENSIONS ARE IN INCHES (ANGLES IN DEGREES), UNLESS OTHERWISE SPECIFIED.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .004 IN. (0.10 mm) TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. NO INTRUSION IS ALLOWED. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
8. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-.
9. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ337 REV.: D
JEDEC NUMBER: NONE

## Package Number 338 - 24-Lead SSOP, .209 Wide



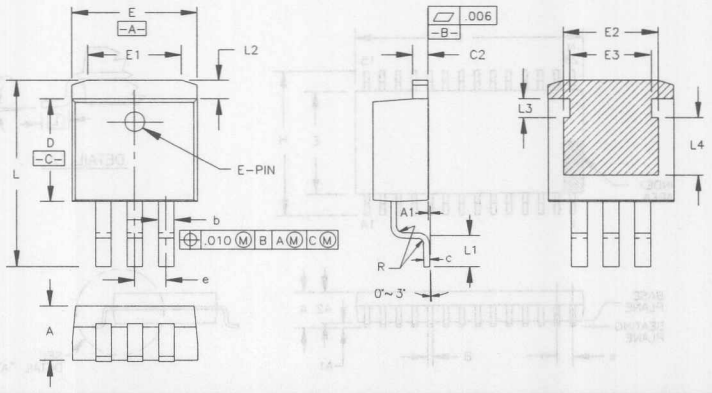

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .079 | -- | 2.00 | |
| A1 | .002 | -- | 0.05 | -- | |
| A2 | .065 | .073 | 1.65 | 1.85 | |
| b | .009 | .015 | 0.22 | 0.38 | 3,7 |
| c | .004 | .010 | 0.09 | 0.25 | 7 |
| D | .311 | .335 | 7.90 | 8.50 | 2 |
| E | .291 | .323 | 7.40 | 8.20 | |
| E1 | .197 | .220 | 5.00 | 5.60 | 2 |
| e | .0256 | BASIC | 0.65 | BASIC | |
| L | .022 | .037 | 0.55 | 0.95 | 4 |
| L1 | .049 | REF | 1.25 | REF | |
| N | 24 | | 24 | | 5 |
| α | 0° | 8° | 0° | 8° | |
| R1 | .004 | -- | 0.09 | -- | |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. D AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT DATUM PLANE -H- MOLD PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED .008 INCH (0.20mm) PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13mm) TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN .003 INCH (0.07mm) AT LEAST MATERIAL CONDITION.
4. DIMENSION L TO BE DETERMINED AT SEATING PLANE-DATUM "C".
5. N IS THE NUMBER OF TERMINAL POSITIONS.
6. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSSHATCHED AREA.
7. SECTION A-A DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .004 AND .010 INCH FROM THE LEAD TIP.

PACKAGE NUMBER: ZZ338 | REV.: A
JEDEC NUMBER: MO-150-AG

## Package Number 339 - 3-Lead DD PAK



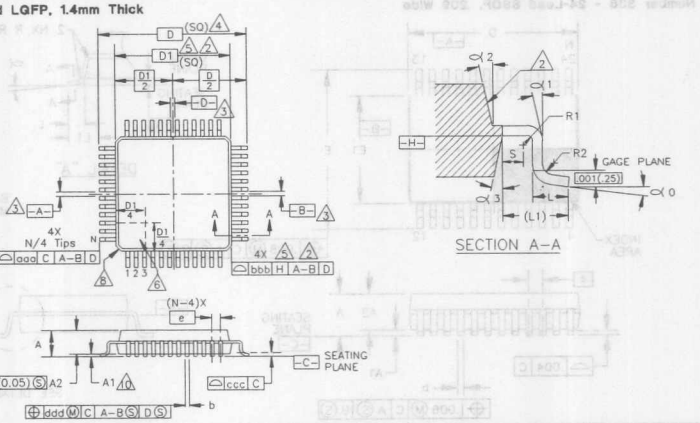

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .170 | .183 | 4.32 | 4.65 | |
| A1 | .000 | .004 | 0.00 | 0.10 | |
| b | .049 | .051 | 1.25 | 1.30 | 2,5 |
| C2 | .045 | .055 | 1.14 | 1.40 | |
| c | .014 | .026 | 0.36 | 0.66 | 2 |
| D | .329 | .333 | 8.36 | 8.46 | |
| E | .385 | .410 | 9.78 | 10.41 | |
| E1 | .297 | .303 | 7.54 | 7.70 | |
| E2 | .296 | .304 | 7.52 | 7.72 | |
| E3 | .252 | .300 | 6.40 | 7.62 | |
| e | .100 | REF | 2.54 | REF | |
| L | .595 | .605 | 15.11 | 15.37 | |
| L1 | .096 | .104 | 2.44 | 2.64 | |
| L2 | .0585 | .0625 | 1.485 | 1.587 | |
| L3 | .056 | .064 | 1.42 | 1.63 | |
| L4 | .179 | .187 | 4.55 | 4.75 | |
| N | 3 | | 3 | | 6 |
| R | .017 | .019 | 0.43 | 0.48 | |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION b AND c APPLY TO THE PLATED LEAD.
3. LEADS ARE NOT ALLOWED ABOVE THE DATUM -B-.
4. STAND-OFF HEIGHT IS MEASURED FROM LEAD TIP WITH REFERENCE TO DATUM -B-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM "b" BY MORE THAN .003".
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. CROSSHATCH INDICATES EXPOSED METAL SURFACE.

PACKAGE NUMBER: ZZ339 | REV.: B
JEDEC NUMBER: MO-169 WITH THE EXCEPTION OF DIM. b,D,L,L1,L2

**Package Number 340 - 48-Lead LQFP, 1.4mm Thick**




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .063 | -- | 1.60 | |
| A1 | .002 | .006 | 0.05 | 0.15 | 10 |
| A2 | .053 | .057 | 1.35 | 1.45 | |
| b | .007 | .011 | 0.17 | 0.27 | 7,9 |
| C | .004 | .008 | 0.09 | 0.20 | 9 |
| D | .354 | BASIC | 9.00 | BASIC | 4 |
| D1 | .276 | BASIC | 7.00 | BASIC | 2,5 |
| e | .020 | BASIC | 0.50 | BASIC | |
| L | .018 | .030 | 0.45 | 0.75 | |
| L1 | .039 | REF | 1.00 | REF | |
| N | 48 | | 48 | | |
| R1 | .003 | -- | 0.08 | -- | |
| R2 | .003 | .008 | 0.08 | 0.20 | |
| S | .008 | -- | 0.20 | -- | |

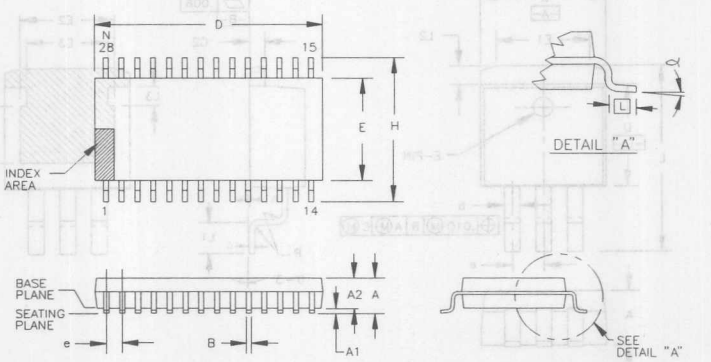
| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| aaa | .008 | NOM. | 0.20 | NOM. | |
| bbb | .008 | NOM. | 0.20 | NOM. | |
| ccc | .003 | NOM. | 0.08 | NOM. | |
| ddd | .003 | NOM. | 0.08 | NOM. | |
| ∝0 | 0° | 7° | 0° | 7° | |
| ∝1 | 0° | -- | 0° | -- | |
| ∝2 | 11° | 13° | 11° | 13° | |
| ∝3 | 11° | 13° | 11° | 13° | |

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M–1982.
2. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE BY AS MUCH AS .006 in.(0.15mm).
3. DATUMS A–B AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
4. TO BE DETERMINED AT SEATING PLANE –C–
5. DIMENSION D1 DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .001 in.(0.25mm) PER SIDE. D1 IS THE MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIM. BY MORE THAN .003 in.(0.08mm). DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS .003 in.(0.07mm) FOR .016 in.(0.4mm) AND .020 in.(0.5mm) PITCH PACKAGES.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
9. DIMENSION b AND C APPLY TO THE FLAT SECTION OF LEAD BETWEEN .004 in.(0.10mm) AND .002 in.(0.25mm) FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
11. CONTROLLING DIMENSION IS MILLIMETER.

| PACKAGE NUMBER: | ZZ340 | REV.: | B |
|---|---|---|---|
| JEDEC NUMBER: | MS–026–BBC | | |

**Package Number 341 - 28-Lead SOIC, .330 Wide**




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .118 | -- | 3.00 | |
| A1 | .000 | .008 | 0.00 | 0.20 | |
| A2 | .096 | .108 | 2.45 | 2.75 | |
| B | .012 | .020 | 0.30 | 0.50 | |
| D | .709 | .732 | 18.00 | 18.60 | |
| E | .323 | .339 | 8.20 | 8.60 | |
| e | .050 | TYPICAL | 1.27 | TYPICAL | |
| H | .449 | .480 | 11.40 | 12.20 | |
| L | .039 | BASIC | 1.00 | BASIC | |
| N | 28 | | 28 | | 4 |
| ∝ | 0° | 10° | 0° | 10° | |

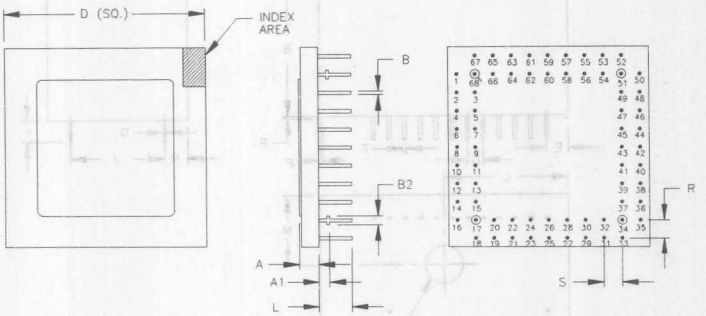
NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25 mm) @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.
4. N IS THE NUMBER OF TERMINAL POSITIONS.

| PACKAGE NUMBER: | ZZ341 | REV.: | A |
|---|---|---|---|
| JEDEC NUMBER: | NONE | | |

PACKAGE DRAWINGS (Mechanical)

**Package Number 342 - 68-Lead Ceramic PGA**

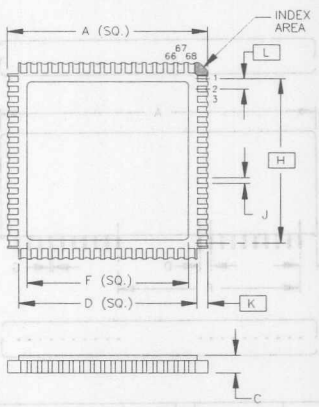



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .095 | .120 | 2.413 | 3.048 | |
| A1 | .045 | .055 | 1.143 | 1.397 | |
| B | .016 | .020 | .406 | .508 | |
| B2 | .045 | .055 | 1.143 | 1.397 | |
| D | 1.087 | 1.109 | 27.610 | 28.169 | |
| L | .162 | .198 | 4.115 | 5.029 | |
| N | 68 | | 68 | | 4 |
| R | .100 BASIC | | 2.540 BASIC | | |
| S | .100 BASIC | | 2.540 BASIC | | |

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (0.25 mm) @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
4. N IS THE NUMBER OF TERMINAL POSITIONS.

PACKAGE NUMBER: ZZ342 | REV.: A
JEDEC NUMBER: UNKNOWN

**Package Number 343 - 68-Lead LCC**

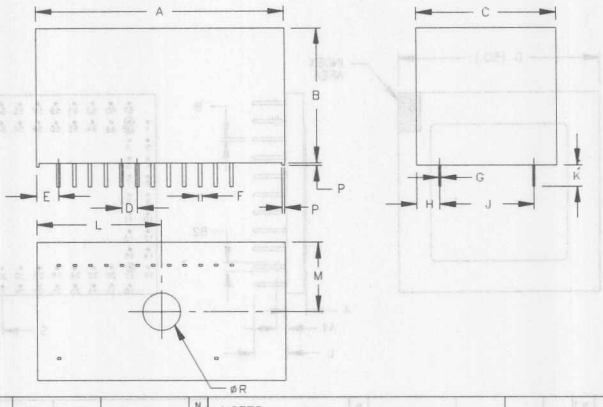



| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .945 | .965 | 24.003 | 24.511 | |
| C | .076 | .094 | 1.934 | 2.388 | |
| D | .841 | .859 | 21.361 | 21.819 | |
| F | .755 | .785 | 19.177 | 19.939 | |
| H | .800 BASIC | | 20.320 BASIC | | |
| J | .027 | .033 | .686 | .838 | |
| K | .045 BASIC | | 1.143 BASIC | | |
| L | .050 BASIC | | 1.270 BASIC | | |
| N | 68 | | 68 | | 3 |

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R AT MMC AT SEATING PLANE.
2. PIN NUMBER SHOWN FOR REFERENCE ONLY.
3. N IS THE NUMBER OF TERMINAL POSITIONS.
4. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ343 | REV.: A
JEDEC NUMBER: UNKNOWN

**Package Number 344 - 14-Lead Custom Module**



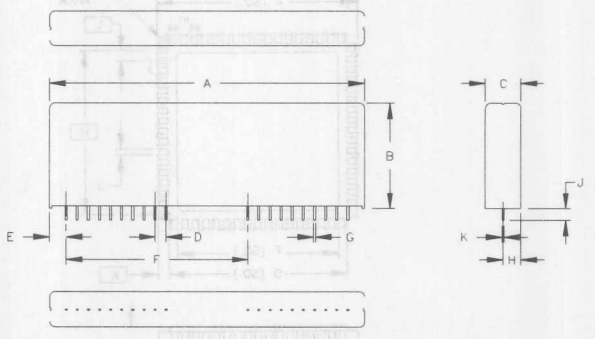

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | 1.58 | | 40.00 | | |
| B | .87 | | 22.00 | | |
| C | .89 | | 22.60 | | |
| D | .10 | | 2.54 | | |
| E | .14 | | 3.49 | | |
| F | .023 | | 0.58 | | |
| G | .011 | | 0.25 | | |
| H | .13 | | 3.38 | | |
| J | .60 | | 15.24 | | |
| K | .15 | | 3.81 | | |
| L | .79 | | 20.00 | | |
| M | .44 | | 11.30 | | |
| N | 14 | | 14 | | 2 |
| P | .024 | | 0.60 | | |

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| R | .24 | | 6.00 | | |

NOTES:
1. ALL DIMENSIONS ARE TYPICAL.
2. N IS THE NUMBER OF TERMINAL POSITIONS.

| | | |
|---|---|---|
| PACKAGE NUMBER: | ZZ344 | REV.: A |
| JEDEC NUMBER: | NONE | |

**Package Number 345 - 20-Lead Custom Module**




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | 2.998 | 3.010 | 76.15 | 76.45 | |
| B | .994 | 1.006 | 25.25 | 25.55 | |
| C | .327 | .350 | 8.30 | 8.90 | |
| D | .093 | .106 | 2.35 | 2.70 | |
| E | .146 | .158 | 3.71 | 4.01 | |
| F | 1.693 | 1.707 | 43.00 | 43.35 | |
| G | .019 | .021 | 0.48 | 0.53 | |
| H | .163 | .175 | 4.15 | 4.45 | |
| J | .120 | .160 | 3.05 | 4.06 | |
| K | .009 | .011 | 0.23 | 0.28 | |
| L | .014 | .026 | 0.35 | 0.65 | |
| N | 20 | | 20 | | 1 |

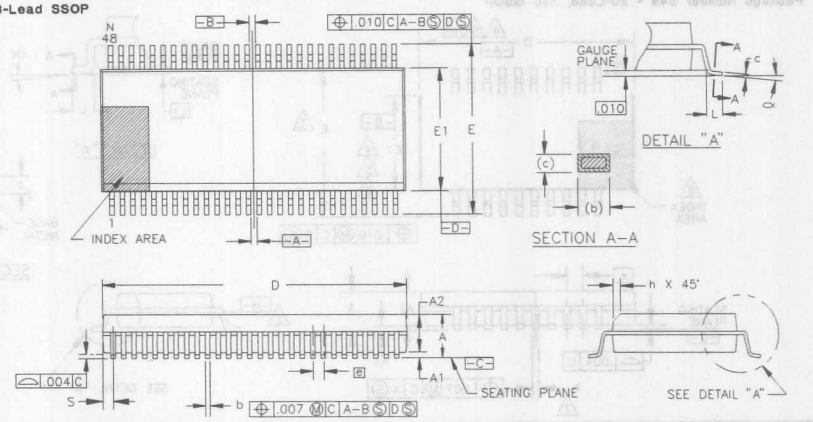
| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|

NOTES:
1. N IS THE NUMBER OF TERMINAL POSITIONS.

| | | |
|---|---|---|
| PACKAGE NUMBER: | ZZ345 | REV.: A |
| JEDEC NUMBER: | NONE | |

PACKAGE DRAWINGS (Mechanical)

**Package Number 346 - 56-Lead SSOP**



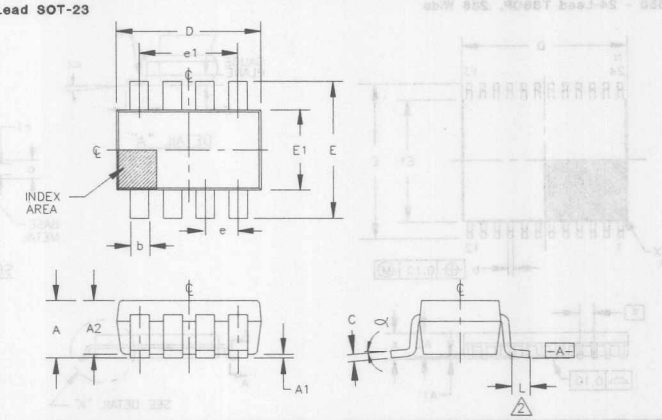

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .095 | .110 | 2.41 | 2.79 | |
| A1 | .008 | .016 | 0.20 | 0.41 | |
| A2 | .088 | .092 | 2.24 | 2.34 | |
| b | .008 | .0135 | 0.20 | 0.34 | 8 |
| c | .005 | .010 | 0.13 | 0.25 | 8 |
| D | .720 | .730 | 18.29 | 18.54 | 2 |
| E | .395 | .420 | 10.03 | 10.67 | |
| E1 | .291 | .299 | 7.39 | 7.59 | 3 |
| e | .025 BASIC | | 0.635 BASIC | | |
| L | .020 | .040 | 0.51 | 1.02 | 5 |
| h | .015 | .025 | 0.38 | 0.64 | 4 |
| N | 56 | | 56 | | 6,7 |
| S | .023 | .027 | 0.58 | 0.69 | |
| α | 0° | 8° | 0° | 8° | |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .006 INCH (0.15mm) PER SIDE.
3. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED .015 INCH (0.38mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF THE TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
7. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
8. SECTION A-A DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005" AND .010" FROM LEAD TIP.

PACKAGE NUMBER: ZZ346 | REV.: A

JEDEC NUMBER: MO-118-AB

**Package Number 348 - 8-Lead SOT-23**




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .035 | .057 | 0.90 | 1.45 | |
| A1 | .000 | .006 | 0.00 | 0.15 | |
| A2 | .035 | .051 | 0.90 | 1.30 | |
| b | .011 | .018 | 0.28 | 0.45 | |
| C | .004 | .008 | 0.09 | 0.20 | |
| D | .110 | .118 | 2.80 | 3.00 | |
| E | .102 | .118 | 2.60 | 3.00 | |
| E1 | .059 | .069 | 1.50 | 1.75 | |
| e | .0256 REF | | 0.65 REF | | |
| e1 | .077 REF | | 1.95 REF | | |
| L | .004 | .024 | 0.10 | 0.60 | 2 |
| N | 8 | | 8 | | 5 |
| α | 0° | 10° | 0° | 10° | |

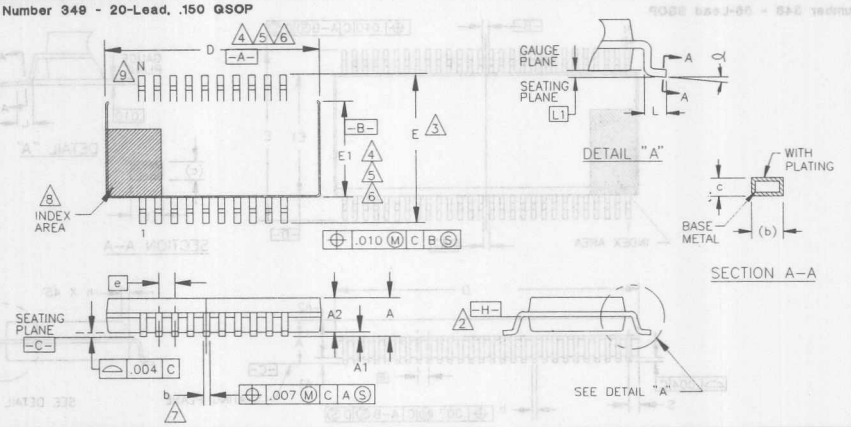
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED REFERENCE TO FLAT FOOT SURFACE PARALLEL TO DATUM -A-
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH, METAL BURR & DAMBAR PROTRUSION/INTRUSION.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. N IS THE MAXIMUM QUANTITY OF LEAD POSITIONS.
6. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ348 | REV.: B

JEDEC NUMBER: NONE

EIAJ REF.NUMBER: SC-74 (6-LEAD VERSION)

## Package Number 349 - 20-Lead, .150 GSOP



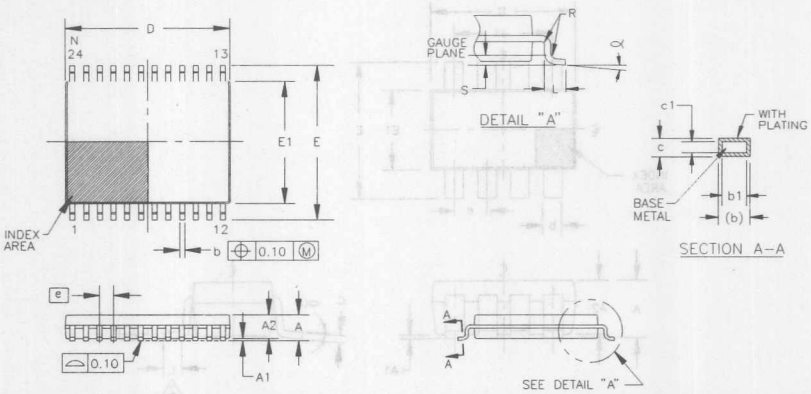

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .053 | .069 | 1.35 | 1.75 | |
| A1 | .004 | .010 | 0.10 | 0.25 | |
| A2 | -- | .059 | -- | 1.50 | |
| b | .008 | .012 | 0.20 | 0.31 | 7 |
| c | .006 | .010 | 0.15 | 0.25 | |
| D | .337 | .344 | 8.56 | 8.74 | 5,6 |
| E | .228 | .244 | 5.79 | 6.20 | 3 |
| E1 | .150 | .157 | 3.81 | 3.99 | 5,6 |
| e | .025 BASIC | | 0.64 BASIC | | |
| L | .016 | .050 | 0.41 | 1.27 | |
| L1 | .010 BASIC | | 0.25 BASIC | | |
| N | 20 | | 20 | | 9 |
| ∝ | 0° | 8° | 0° | 8° | |

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |

NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982.
2. DATUM PLANE -H- COINCIDENT WITH BOTTOM OF LEAD, WHERE LEAD EXITS BODY.
3. TO BE DETERMINED AT SEATING PLANE -C-.
4. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM -H-.
5. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS. MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006" (0.15mm) PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS. INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED .010" (0.25mm) PER SIDE.
6. TO BE DETERMINED AT PLANE -H-
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .004" (0.10mm) TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN .002 "" (0.05mm) AT LEAST MATERIAL CONDITION.
8. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
9. N IS THE MAXIMUM NUMBER OF LEADS.

PACKAGE NUMBER: ZZ349 | REV.: A
JEDEC NUMBER: MO-137-AD

## Package Number 350 - 24-Lead TSSOP, .236 Wide




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .041 | .057 | 1.05 | 1.45 | |
| A1 | .002 | .006 | 0.05 | 0.15 | |
| A2 | .045 TYP. | | 1.15 TYP. | | |
| b | .007 | .012 | 0.19 | 0.30 | 3,4 |
| b1 | .007 | .010 | 0.19 | 0.25 | 4 |
| c | .004 | .008 | 0.09 | 0.20 | 4 |
| c1 | .004 | .006 | 0.09 | 0.16 | 4 |
| D | .303 | .323 | 7.70 | 8.20 | 2 |
| E | .291 | .307 | 7.40 | 7.80 | |
| E1 | -- | .236 | -- | 6.00 | 2 |
| e | .026 BASIC | | 0.65 BASIC | | |
| L | .012 | .028 | 0.30 | 0.70 | |
| N | 24 | | 24 | | 5 |
| R | .004 | -- | 0.09 | -- | |

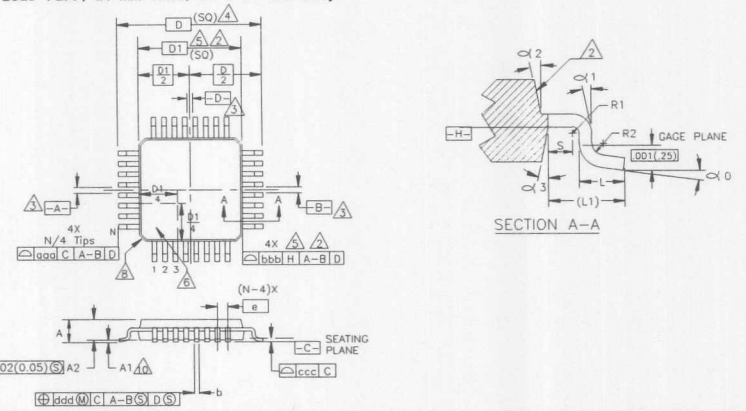
| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| S | .010 REF. | | 0.25 REF. | | |
| ∝ | 0° | 10° | 0° | 10° | |

NOTES:
1. MILLIMETERS SHALL BE CONTROLLING UNITS.
2. D AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT DATUM PLANE, MOLD PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.20mm (.008 INCH) PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13mm (.005 INCH) TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.07mm (.003 INCH) AT LEAST MATERIAL CONDITION.
4. b, b1, c, AND c1 DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.004 INCH) AND 0.25mm (.010 INCH) FROM THE LEAD TIPS.
5. N IS THE NUMBER OF LEADS.
6. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSSHATCHED AREA.

PACKAGE NUMBER: ZZ350 | REV.: A
JEDEC NUMBER: NONE

PACKAGE DRAWINGS (Mechanical)

## Package Number 351 - 32-Lead TQFP, 1.4 mm Thick, 5.0 x 5.0 mm Body



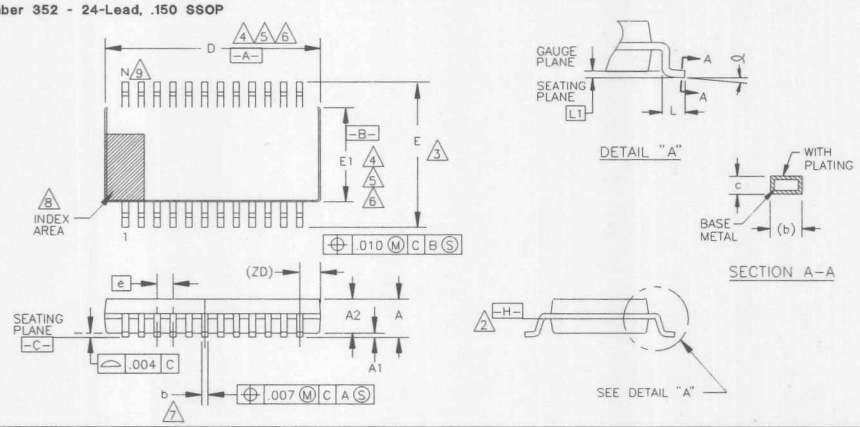

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .047 | -- | 1.20 | |
| A1 | .002 | .006 | 0.05 | 0.15 | 10 |
| A2 | .037 | .041 | 0.95 | 1.05 | |
| b | .007 | .011 | 0.17 | 0.27 | 7,9 |
| c | .004 | .008 | 0.09 | 0.20 | 9 |
| D | .276 | BASIC | 7.00 | BASIC | 4 |
| D1 | .197 | BASIC | 5.00 | BASIC | 2,5 |
| e | .020 | BASIC | 0.50 | BASIC | |
| L | .018 | .030 | 0.45 | 0.75 | |
| L1 | .039 | REF | 1.00 | REF | |
| N | 32 | | 32 | | 12 |
| R1 | .003 | -- | 0.08 | -- | |
| R2 | .003 | .008 | 0.08 | 0.20 | |
| S | .008 | -- | 0.20 | -- | |

| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| aaa | .008 | NOM. | 0.20 | NOM. | |
| bbb | .008 | NOM. | 0.20 | NOM. | |
| ccc | .003 | NOM. | 0.08 | NOM. | |
| ddd | .003 | NOM. | 0.08 | NOM. | |
| ∝0 | 0° | 7° | 0° | 7° | |
| ∝1 | 0° | -- | 0° | -- | |
| ∝2 | 11° | 13° | 11° | 13° | |
| ∝3 | 11° | 13° | 11° | 13° | |

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M–1982.
2. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE BY AS MUCH AS .006 in.(0.15mm).
3. DATUMS [A–B] AND [–D–] TO BE DETERMINED AT DATUM PLANE [–H–].
4. TO BE DETERMINED AT SEATING PLANE [–C–].
5. DIMENSION D1 DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .001 in.(0.25mm) PER SIDE. D1 IS THE MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIM. BY MORE THAN .003 in.(0.08mm). DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS .003 in.(0.07mm) FOR .016 in.(0.4mm) AND .020 in.(0.5mm) PITCH PACKAGES.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
9. DIMENSION b AND C APPLY TO THE FLAT SECTION OF LEAD BETWEEN .004 in.(0.10mm) AND .002 in.(0.25mm) FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
11. CONTROLLING DIMENSION IS MILLIMETER.
12. N IS THE NUMBER OF LEADS.

| PACKAGE NUMBER: ZZ351 | REV.: A |
|---|---|
| JEDEC NUMBER: MS–026–AAA | |

## Package Number 352 - 24-Lead, .150 SSOP




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .053 | .069 | 1.35 | 1.75 | |
| A1 | .004 | .010 | 0.10 | 0.25 | |
| A2 | -- | .059 | -- | 1.50 | |
| b | .008 | .012 | 0.20 | 0.31 | 7 |
| c | .006 | .010 | 0.15 | 0.25 | |
| D | .337 | .344 | 8.56 | 8.74 | 5,6 |
| E | .228 | .244 | 5.79 | 6.20 | 3 |
| E1 | .150 | .157 | 3.81 | 3.99 | 5,6 |
| e | .025 | BASIC | 0.64 | BASIC | |
| L | .016 | .050 | 0.41 | 1.27 | |
| L1 | .010 | BASIC | 0.25 | BASIC | |
| N | 24 | | 24 | | 9 |
| ZD | .033 | REF. | 0.84 | REF. | |
| ∝ | 0° | 8° | 0° | 8° | |

NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982.
2. DATUM PLANE [–H–] COINCIDENT WITH BOTTOM OF LEAD, WHERE LEAD EXITS BODY.
3. TO BE DETERMINED AT SEATING PLANE [–C–].
4. DATUMS [–A–] AND [–B–] TO BE DETERMINED AT DATUM [–H–].
5. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS. MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006" (0.15mm) PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS. INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED .010" (0.25mm) PER SIDE.
6. TO BE DETERMINED AT PLANE [–H–].
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .004" (0.10mm) TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN .002 " (0.05mm) AT LEAST MATERIAL CONDITION.
8. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
9. N IS THE MAXIMUM NUMBER OF LEADS.

| PACKAGE NUMBER: ZZ352 | REV.: A |
|---|---|
| JEDEC NUMBER: MO–137–AE WITH THE EXCEPTION OF DIM. "c" | |

